

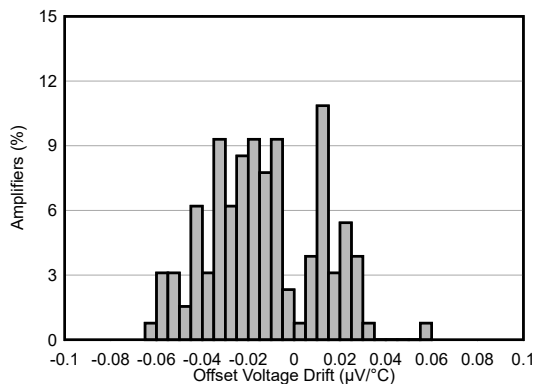
OPA2205 2 μ V、0.04 μ V/°C 低功耗超 β 双极 e-trim™ 运算放大器

1 特性

- e-trim™ 运算放大器性能
 - 低失调电压：15 μ V (最大值)
 - 低失调电压漂移： $\pm 0.2\mu$ V/°C (最大值)
- 超 β 输入
 - 输入偏置电流：0.4nA (最大值)
 - 输入电流噪声：110fA/ $\sqrt{\text{Hz}}$
- 低噪声
 - 0.1 至 10Hz：0.2 μ V_{PP}
 - 电压噪声：7.2nV/ $\sqrt{\text{Hz}}$
- A_{OL}、CMRR 和 PSRR：> 126dB (全温度范围)
- 增益带宽积：3.6MHz
- 低静态电流：240 μ A (最大值)
- 压摆率：4V/ μ s
- 过载功率限制器
- 轨到轨输出
- 输入已滤除 EMI 和 RFI
- 宽电源电压：4.5V 至 36V
- 温度范围：-40°C 至 +125°C
- 提供高等级 (OPA2205) 和标准等级 (OPA2205A)

2 应用

- 流量变送器
- 串式逆变器
- 数据采集 (DAQ)
- 源测量单元 (SMU)
- 实验室和现场仪表
- 电池测试
- 模拟输入模块
- 压力变送器



OPA2205 失调电压漂移

3 说明

OPA2205 是业界通用 OPAx277 系列的新一代版本。该器件是一款具有超 β 输入的精密双极 e-trim™ 运算放大器。该器件使用 TI 的专有微调技术来实现 $\pm 2\mu$ V (典型值) 的输入失调电压和 $\pm 0.04\mu$ V (典型值) 的输入失调电压漂移。

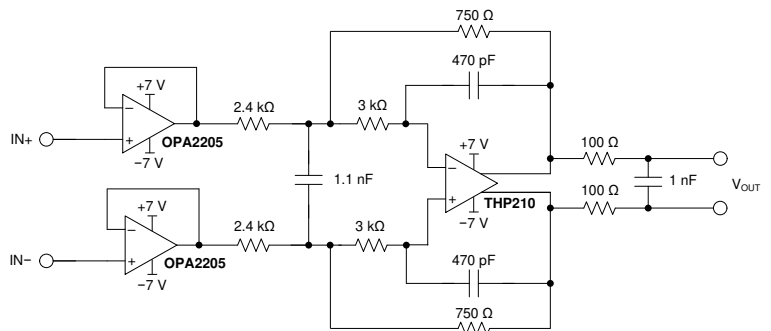
OPA2205 采用双极工艺设计，可针对仅 220 μ A 的静态电流提供 3.6MHz 增益带宽。该器件还可在 1kHz 下实现仅 7.2nV/ $\sqrt{\text{Hz}}$ 的低电压噪声密度。得益于超 β 输入，OPA2205 具有 100pA (典型值) 的超低输入偏置电流和 110fA/ $\sqrt{\text{Hz}}$ 的电流噪声密度。

OPA2205 的高性能使该器件成为了高精度和低功耗系统的理想选择，例如流量和压力变送器、便携式数据采集 (DAQ) 系统和高密度源测量单元 (SMU)。OPA2206 是一款使用相同运算放大器内核，但额外具有输入过压保护特性的相关产品。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
OPA2205	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



OPA2205 典型应用



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4 Revision History

Changes from Revision A (May 2021) to Revision B (August 2021)	Page
Changed Figure 6-22, <i>Voltage Noise Density vs Frequency</i>, to show voltage noise density instead of current noise density.....	9
Changes from Revision * (April 2020) to Revision A (May 2021)	Page
- 更新了整个文档中的表格、图和交叉参考的编号格式..... - 将 OPA2205 从“预告信息 (预发布)”更改为“量产数据 (正在供货)” - Changed both <i>Electrical Characteristics</i> tables to show differentiated performance between OPA2205 (high grade) and OPA2205A (standard grade).....	1 1 5

5 Pin Configuration and Functions

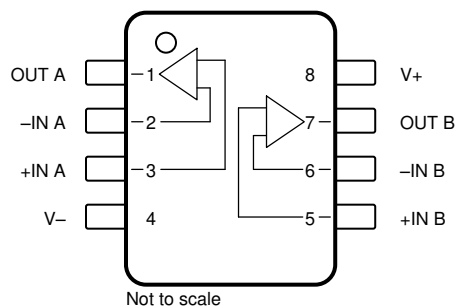


图 5-1. DGK (8-Pin VSSOP) Package, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
- IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
- IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V -	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V ⁺) – (V [–])	Single supply		40	V
		Dual supply		±20	
	Signal input pin voltage	Common-mode	(V [–]) – 0.5	(V ⁺) + 0.5	V
		Differential		±0.5	
	Signal input pin current			±10	mA
	Output short-circuit ⁽²⁾		Continuous		
T _A	Operating temperature		– 40	150	°C
T _J	Junction temperature			150	°C
T _{STG}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V ⁺) – (V [–])	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T _A	Operating temperature		– 40		125	°C

6.4 Thermal Information: OPA2205

THERMAL METRIC ⁽¹⁾		OPA2205	UNIT
		DGK (VSSOP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	175.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	63.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	97.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	95.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics: $V_S = \pm 5\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	OPA2205		±2		±15	μ V
			T _A = - 40°C to +125°C			±25	
		OPA2205A		±8		±50	
			T _A = - 40°C to +125°C			±80	
dV _{OS} /dT	Input offset voltage drift	OPA2205, T _A = - 40°C to +125°C		±0.04		±0.2	μ V/°C
		OPA2205A, T _A = - 40°C to +125°C		±0.08		±0.5	
PSRR	Power supply rejection ratio	OPA2205, V _S = ±2.25 V to ±18 V		±0.05		±0.25	μ V/V
			T _A = - 40°C to +125°C			±0.5	
		OPA2205A, V _S = ±2.25 V to ±18 V		±0.05		±0.5	
			T _A = - 40°C to +125°C			±1	
	Channel separation, (dual, quad)	f = DC		130		dB	
		f = 100 kHz		110			
INPUT BIAS CURRENT							
I _B	Input bias current	OPA2205		±0.1		±0.4	nA
			T _A = 0°C to 85°C			±0.6	
			T _A = - 40°C to +125°C			±0.9	
		OPA2205A		±0.1		±0.5	
			T _A = 0°C to 85°C			±0.75	
			T _A = - 40°C to +125°C			±1	
I _{OS}	Input offset current			±0.1		±0.4	nA
		T _A = 0°C to 85°C				±0.5	
		T _A = - 40°C to +125°C				±0.6	
NOISE							
e _{n p-p}	Input voltage noise	f = 0.1 Hz to 10 Hz		0.2			μ V _{pp}
e _n	Input voltage noise density	f = 10 Hz		7.4		nV/ √ Hz	
		f = 100 Hz		7.2			
		f = 1 kHz		7.2			
i _n	Input current noise	f = 1 kHz		110			fA/ √ Hz
INPUT VOLTAGE							
V _{CM}	Common-mode voltage			(V -) + 1	(V+) - 1.4	V	
CMRR	Common-mode rejection ratio	OPA2205, (V -) + 1 V < V _{CM} < (V+) - 1.4 V, T _A = - 40°C to +125°C		124	140	dB	
		OPA2205A, (V -) + 1 V < V _{CM} < (V+) - 1.4 V, T _A = - 40°C to +125°C		124	140		
INPUT IMPEDANCE							
Z _{ID}	Differential			9 4.4		M Ω pF	
Z _{ICM}	Common-mode			300 4.4		G Ω pF	

6.5 Electrical Characteristics: $V_S = \pm 5\text{ V}$ (continued)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	OPA2205, T _A = - 40°C to +125°C, (V -) + 200 mV < V _O < (V+) - 200 mV	R _L = 10 kΩ	126	132	dB	
			R _L = 2 kΩ	126	130		
		OPA2205A, T _A = - 40°C to +125°C, (V -) + 200 mV < V _O < (V+) - 200 mV	R _L = 10 kΩ	126	132		
			R _L = 2 kΩ	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product			3.6		MHz	
SR	Slew rate	4-V step, G = - 1		3.2		V/ μ s	
	Phase margin	R _L = 10 kΩ, C _L = 25 pF		67		degrees	
t _s	Settling time	To 0.024% (12-bit), 4-V step, Gain = 1, C _L = 30 pF	Falling	2.2		μ s	
			Rising	2.8			
	Overload recovery time	G = - 10		0.3		μ s	
THD+N	Total harmonic distortion + noise	V _O = 5 V _{PP} , G = +1, f = 1 kHz, R _L = 2 kΩ		0.0004		%	
OUTPUT							
	Voltage output swing from rail	A _{OL} > 126 dB	R _L = 10 kΩ	(V -) + 0.2	(V+) - 0.2	V	
			R _L = 2 kΩ	(V -) + 0.2	(V+) - 0.2		
		T _A = - 40°C to +125°C, R _L = 10 kΩ		(V -) + 0.2	(V+) - 0.2		
I _{SC}	Short-circuit current			±25		mA	
C _{LOAD}	Capacitive load drive			See Typical Characteristics			
R _O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I _Q	Quiescent current per amplifier	I _O = 0 mA		220	240	μ A	
		I _O = 0 mA, T _A = - 40°C to +125°C			310		

6.6 Electrical Characteristics: $V_S = \pm 15\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{O\text{ UT}} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	OPA2205			±2	±15	μ V
			T _A = - 40°C to +125°C			±25	
		OPA2205A			±8	±50	
			T _A = - 40°C to +125°C			±80	
dV _{OS} /dT	Input offset voltage drift	OPA2205, T _A = - 40°C to +125°C			±0.04	±0.2	μ V/°C
		OPA2205A, T _A = - 40°C to +125°C			±0.08	±0.5	
PSRR	Power supply rejection ratio	OPA2205, V _S = ±2.25 V to ±18 V			±0.05	±0.25	μ V/V
			T _A = - 40°C to +125°C			±0.5	
		OPA2205A, V _S = ±2.25 V to ±18 V			±0.05	±0.5	
			T _A = - 40°C to +125°C			±1	
	Channel separation, (dual, quad)	f = DC			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I _B	Input bias current	OPA2205			±0.1	±0.4	nA
			T _A = 0°C to 85°C			±0.6	
			T _A = - 40°C to +125°C			±0.9	
		OPA2205A			±0.1	±0.5	
			T _A = 0°C to 85°C			±1	
			T _A = - 40°C to +125°C			±1.2	
I _{OS}	Input offset current				±0.1	±0.4	nA
		T _A = 0°C to 85°C				±0.8	
		T _A = - 40°C to +125°C				±0.9	
NOISE							
e _{n p-p}	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		μ V _{PP}
e _n	Input voltage noise density	f = 10 Hz			7.4		nV/ √ Hz
		f = 100 Hz			7.2		
		f = 1 kHz			7.2		
i _n	Input current noise	f = 1 kHz			110		fA/ √ Hz
INPUT VOLTAGE							
V _{CM}	Common-mode voltage				(V -) + 1	(V+) - 1.4	V
CMRR	Common-mode rejection ratio	OPA2205, (V -) + 1 V < V _{CM} < (V+) - 1.4 V		126	140	dB	
			T _A = - 40°C to +125°C	124	140		
		OPA2205A, (V -) + 1 V < V _{CM} < (V+) - 1.4 V		126	140		
			T _A = - 40°C to +125°C	124	140		
INPUT IMPEDANCE							
Z _{ID}	Differential				9 4.4		M Ω pF
Z _{ICM}	Common-mode				300 4.3		G Ω pF

6.6 Electrical Characteristics: $V_S = \pm 15\text{ V}$ (continued)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{O\ UT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	OPA2205, T _A = - 40°C to +125°C	R _L = 10 kΩ, (V ₋) + 200 mV < V _O < (V ₊) - 200 mV	132	135	dB	
			R _L = 2 kΩ, (V ₋) + 350 mV < V _O < (V ₊) - 350 mV	132	135		
		OPA2205A, T _A = - 40°C to +125°C	R _L = 10 kΩ, (V ₋) + 200 mV < V _O < (V ₊) - 200 mV	126	132		
			R _L = 2 kΩ, (V ₋) + 350 mV < V _O < (V ₊) - 350 mV	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C _L = 30 pF		3.6		MHz	
SR	Slew rate	10-V step, G = - 1		4		V/ μ s	
	Phase margin	R _L = 10 kΩ, C _L = 25 pF		58		degrees	
t _S	Settling time	To 0.024% (12-bit), 10-V step , Gain = 1, C _L = 30 pF	Falling	2.8		μ s	
			Rising	4.5			
	Overload recovery time	G = - 10		0.2		μ s	
THD+N	Total harmonic distortion + noise	V _O = 5 V _{PP} , G = +1, f = 1 kHz, R _L = 2 kΩ		0.0004		%	
OUTPUT							
	Voltage output swing from rail	A _{OL} > 126 dB	R _L = 10 kΩ	(V ₋) + 0.2	(V ₊) - 0.2	V	
			R _L = 2 kΩ	(V ₋) + 0.35	(V ₊) - 0.35		
		T _A = - 40°C to +125°C, R _L = 10 kΩ		(V ₋) + 0.2	(V ₊) - 0.2		
I _{SC}	Short-circuit current			±25		mA	
C _{LOAD}	Capacitive load drive			See Typical Characteristics			
R _O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I _Q	Quiescent current per amplifier	I _O = 0 mA		220	240	μ A	
		I _O = 0 mA, T _A = - 40°C to +125°C		310			

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

表 6-1. Table of Graphs

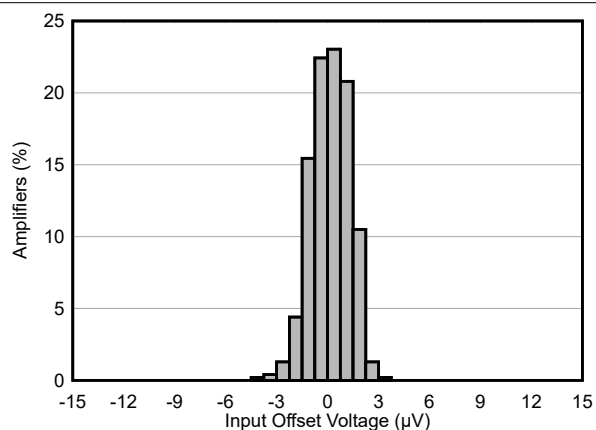
DESCRIPTION	FIGURE
Offset Voltage Production Distribution at 25°C	图 6-1
Offset Voltage at 125°C	图 6-2
Offset Voltage at -40°C	图 6-3
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6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

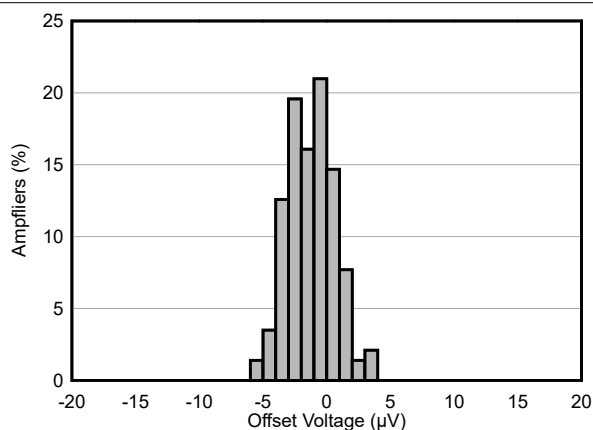
表 6-1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Quiescent Current vs Temperature	图 6-45



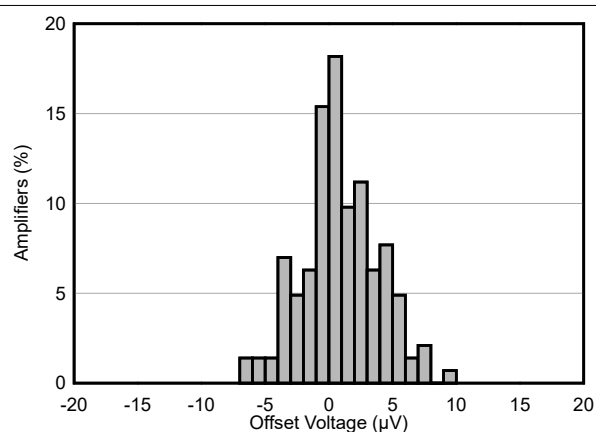
$T_A = 25^\circ\text{C}$

图 6-1. Offset Voltage Production Distribution at 25°C



$T_A = 125^\circ\text{C}$

图 6-2. Offset Voltage Distribution at 125°C



$T_A = -40^\circ\text{C}$

图 6-3. Offset Voltage Distribution at -40°C

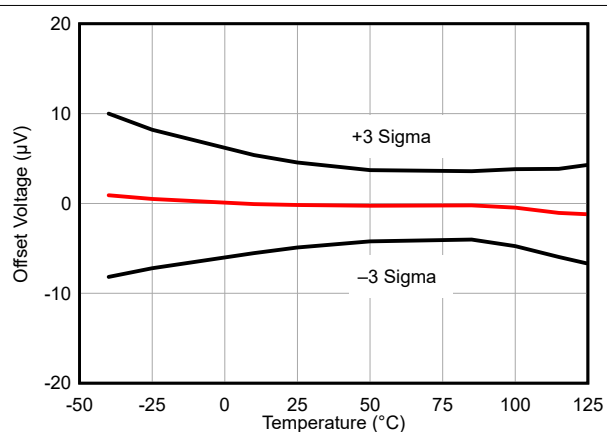


图 6-4. Offset Voltage vs Temperature

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

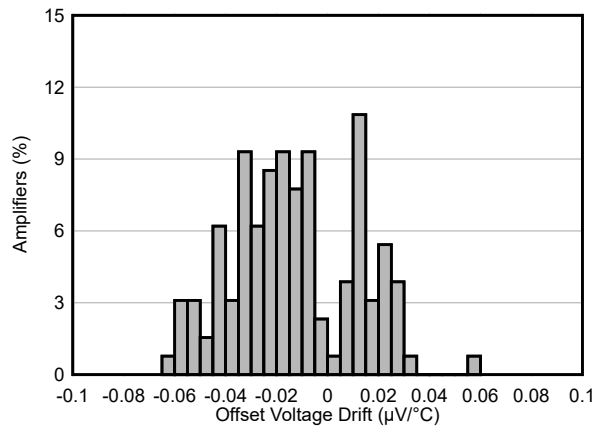


图 6-5. Offset Voltage Drift Distribution

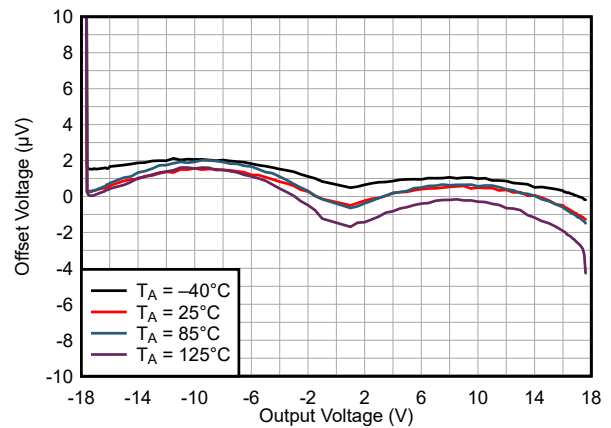


图 6-6. Offset Voltage vs Output Voltage

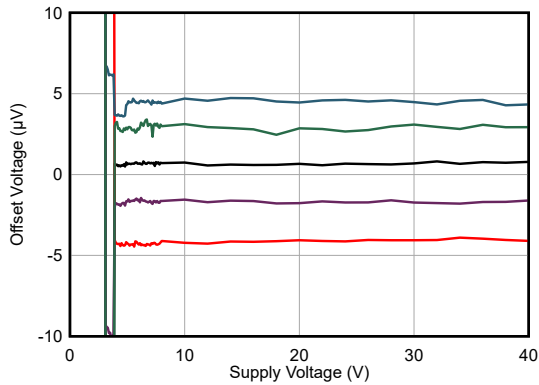


图 6-7. Offset Voltage vs Power Supply Voltage

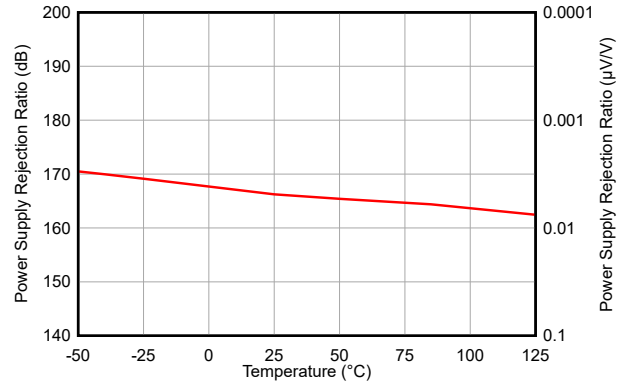


图 6-8. Power-Supply Rejection Ratio vs Temperature

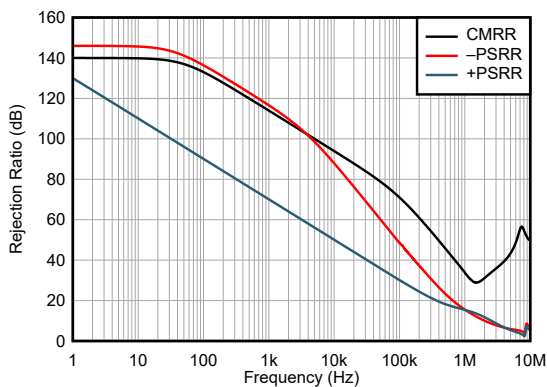


图 6-9. Power-Supply and Common-Mode Rejection Ratio vs Frequency

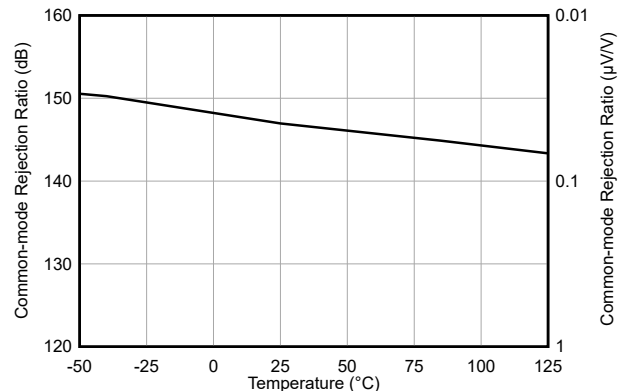


图 6-10. Common-Mode Rejection Ratio vs Temperature

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

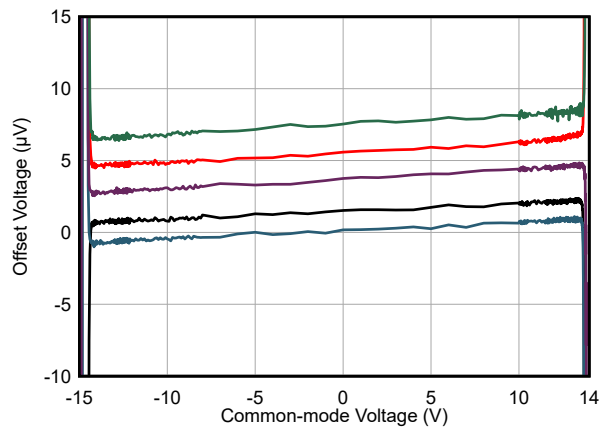


图 6-11. Offset Voltage vs Common-Mode Voltage

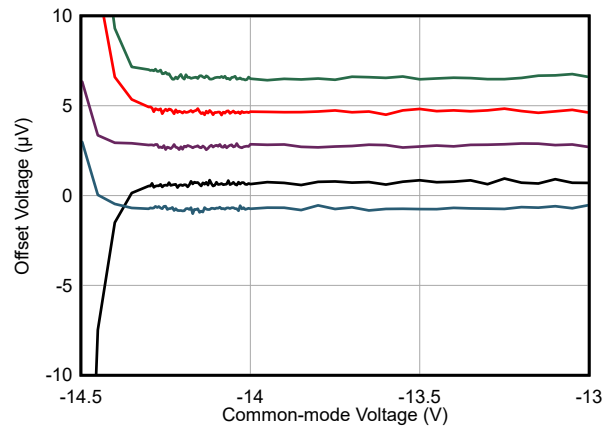


图 6-12. Offset Voltage vs V_{CM} at Low Supply

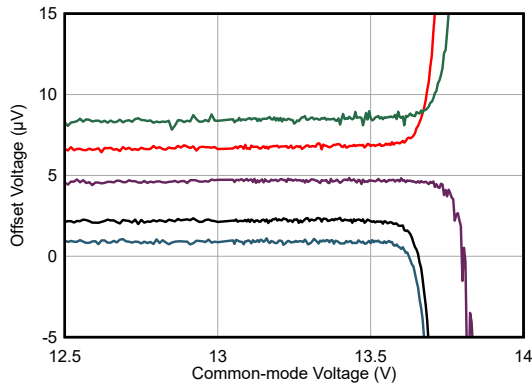


图 6-13. Offset Voltage vs V_{CM} at High Supply

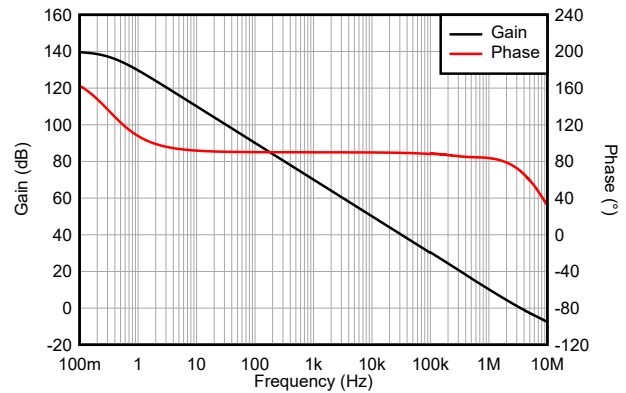


图 6-14. Open-Loop Gain and Phase vs Frequency

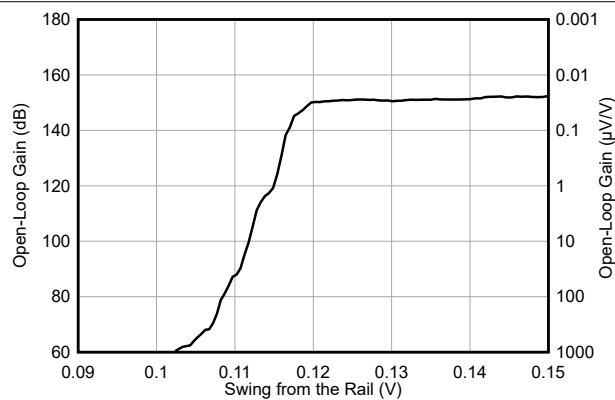


图 6-15. Open-Loop Gain vs Swing from the Rail

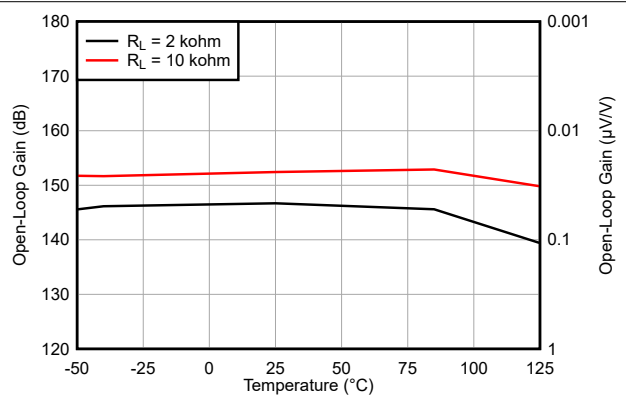


图 6-16. Open-Loop Gain vs Temperature

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

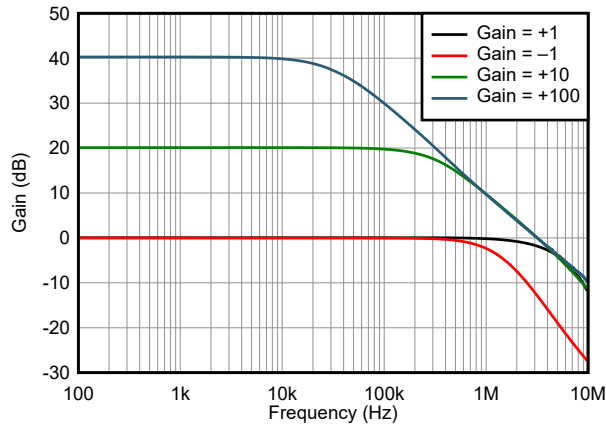


图 6-17. Closed-Loop Gain vs Frequency

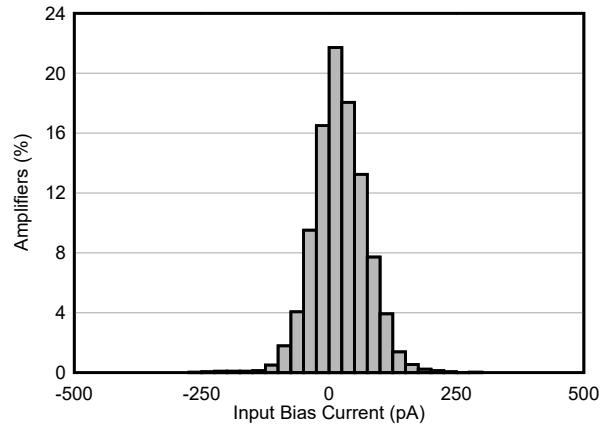


图 6-18. Input Bias Production Distribution

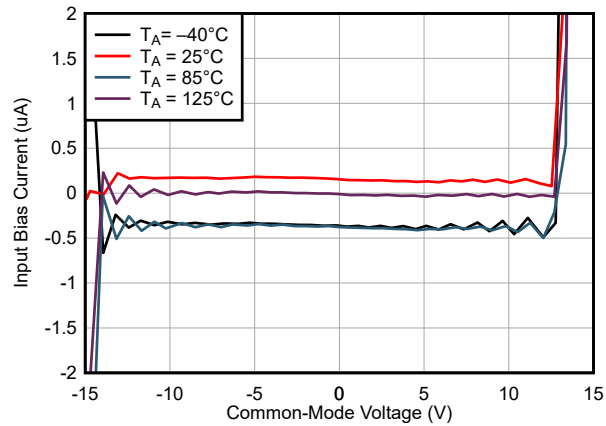


图 6-19. Input Bias vs Common-Mode Voltage

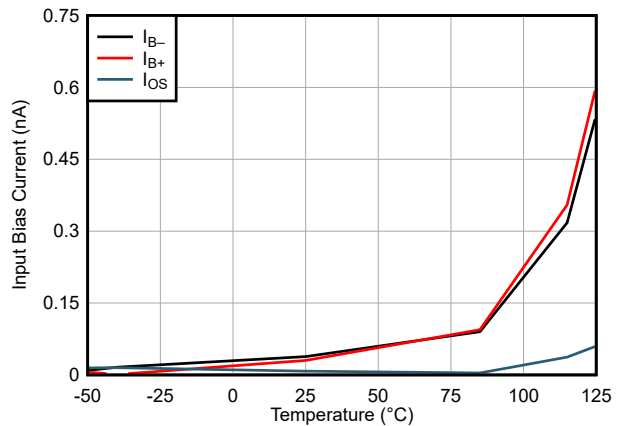


图 6-20. Input Bias and Input Offset Current vs Temperature

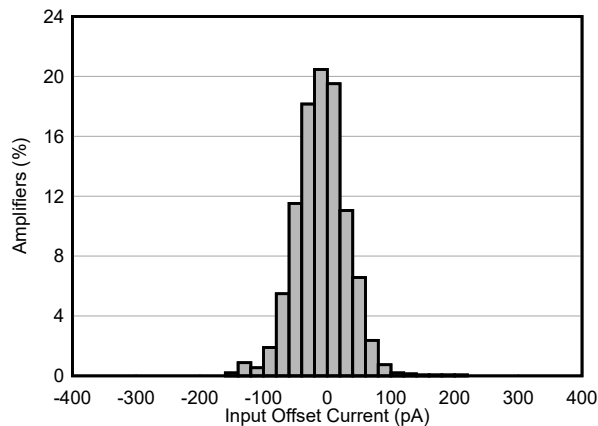


图 6-21. Input Offset Current Production Distribution

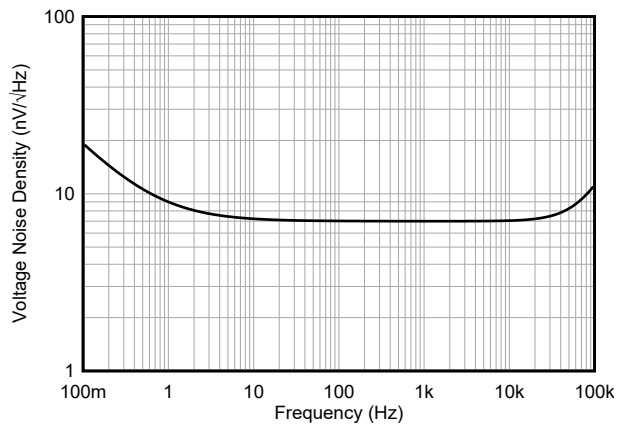


图 6-22. Voltage Noise Density vs Frequency

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

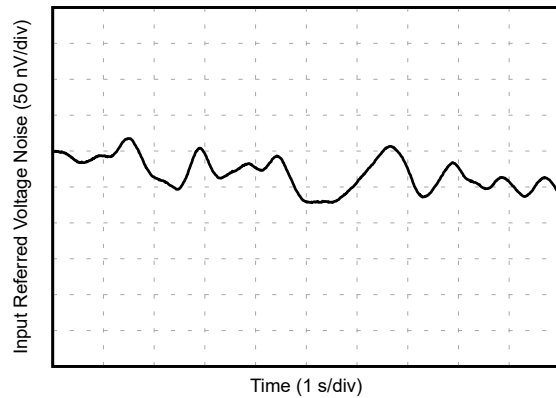


图 6-23. 0.1-Hz To 10-Hz Noise

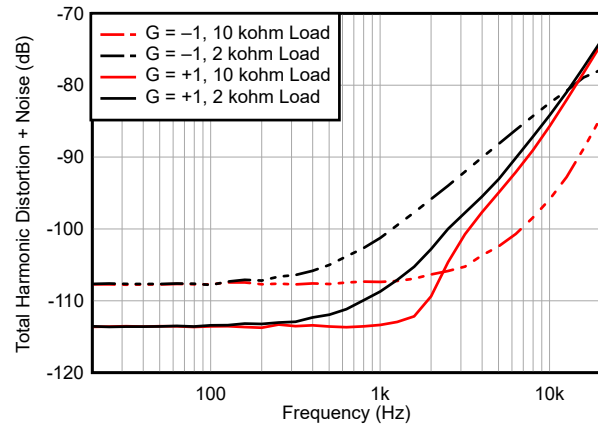


图 6-24. Total Harmonic Distortion + Noise Ratio vs Frequency

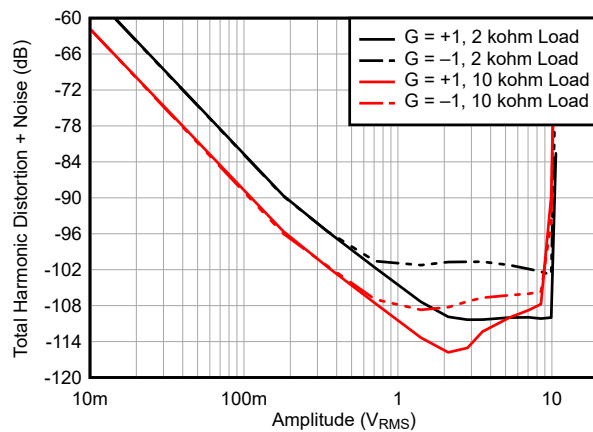


图 6-25. Total Harmonic Distortion + Noise Ratio vs Output Amplitude

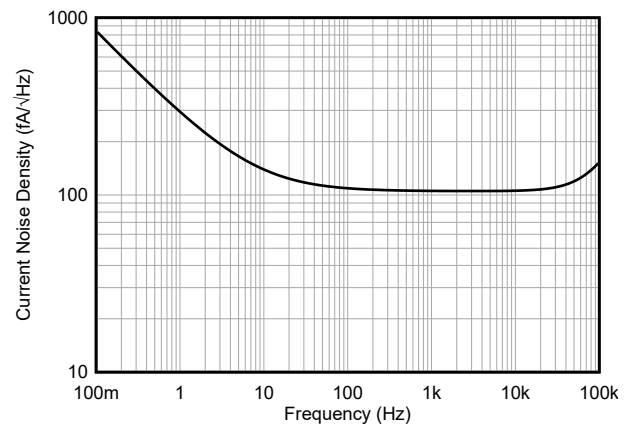


图 6-26. Current Noise vs Frequency

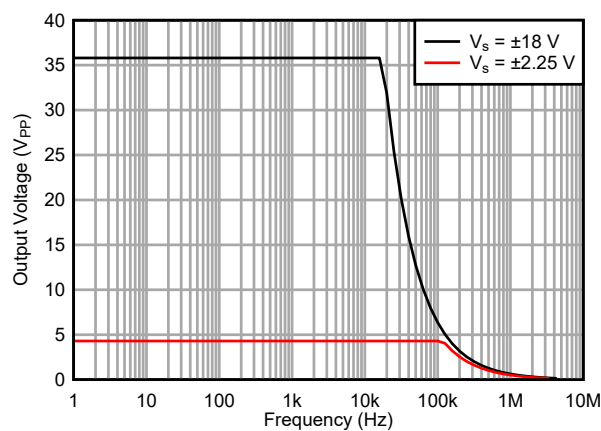


图 6-27. Maximum Output Voltage vs Frequency

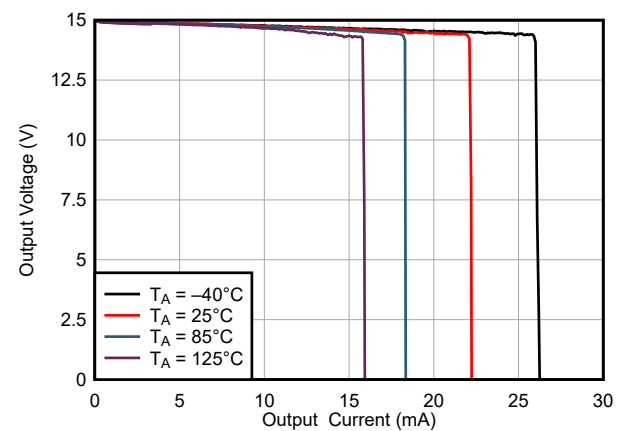


图 6-28. Output Voltage Swing vs Output Sourcing Current

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

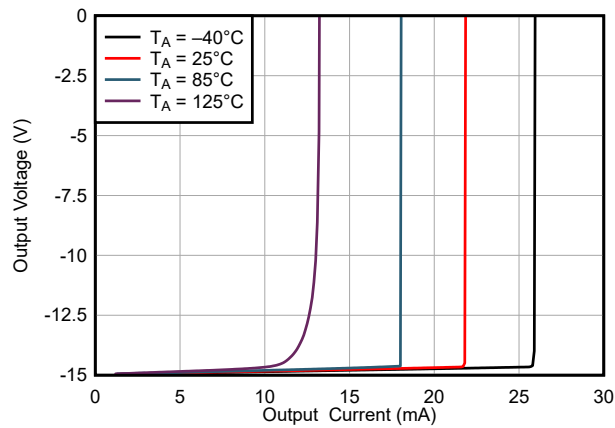


图 6-29. Output Voltage Swing vs Output Sinking Current

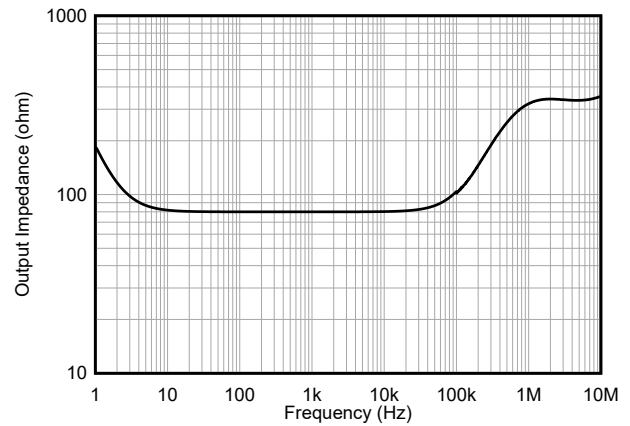


图 6-30. Open-Loop Output Impedance vs Frequency

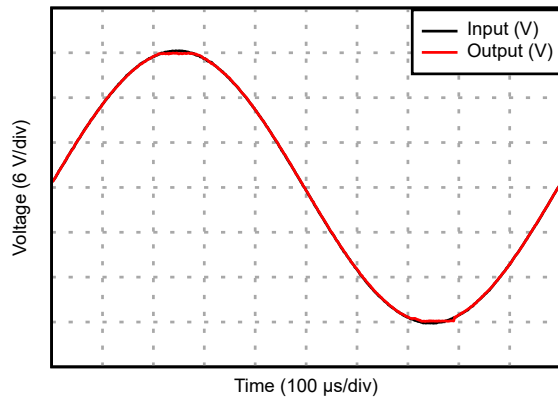


图 6-31. No Phase Reversal

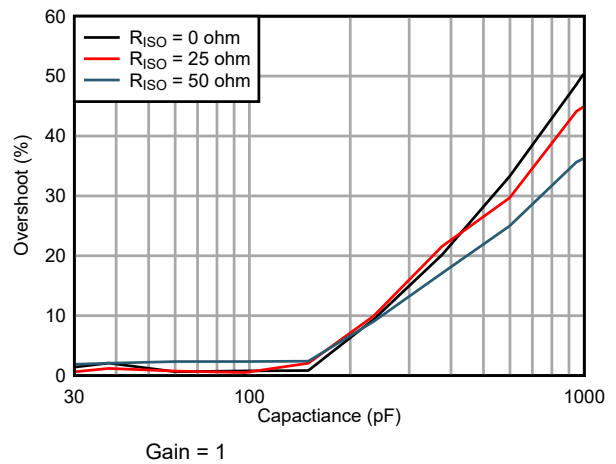


图 6-32. Small-Signal Overshoot vs Capacitive Load, Gain = +1

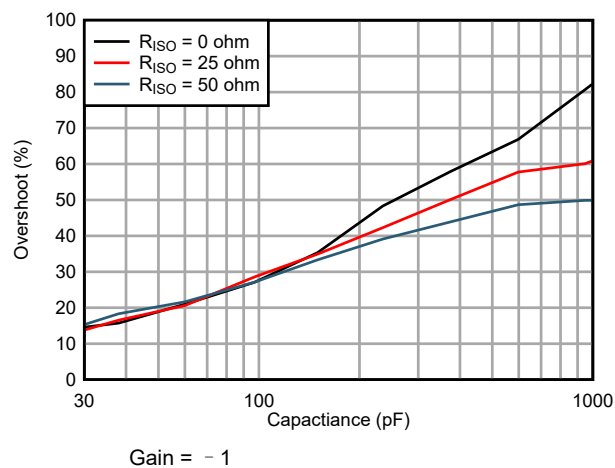


图 6-33. Small-Signal Overshoot vs Capacitive Load, Gain = -1

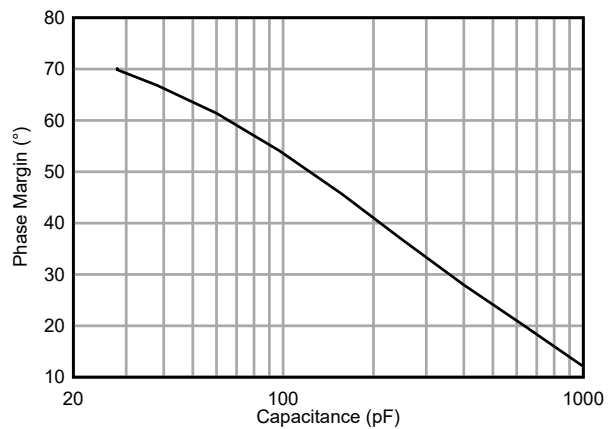
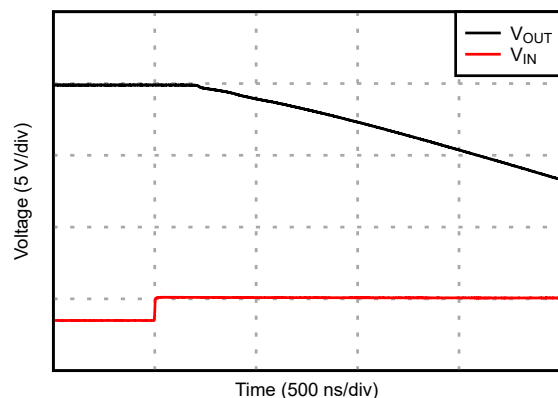


图 6-34. Phase Margin vs Capacitive Load

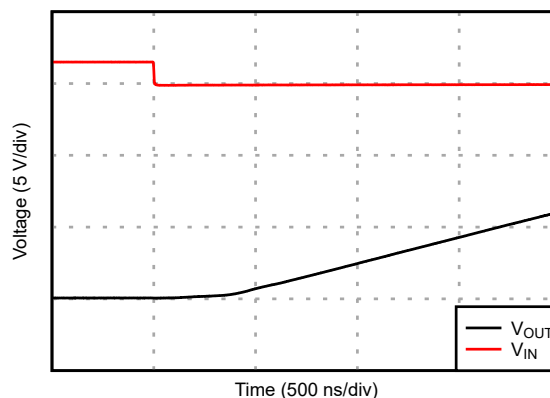
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)



Gain = -1

图 6-35. Positive Overload Recovery, Gain = -1



Gain = -1

图 6-36. Negative Overload Recovery, Gain = -1

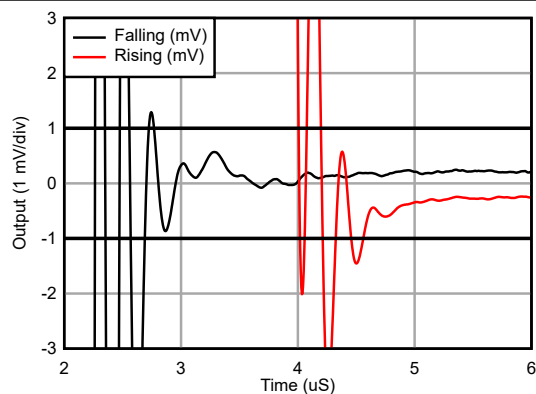
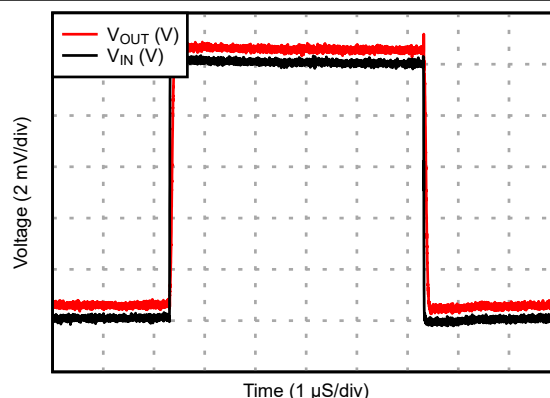
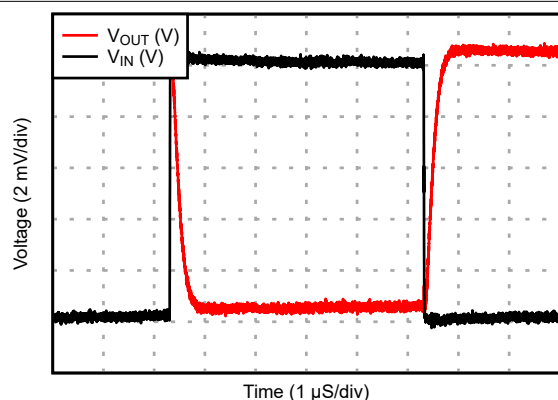


图 6-37. Settling Time



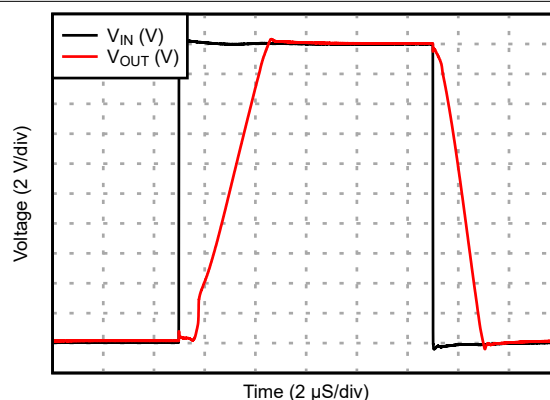
Gain = 1

图 6-38. Small-Signal Step Response, Gain = +1



Gain = -1

图 6-39. Small-Signal Step Response, Gain = -1

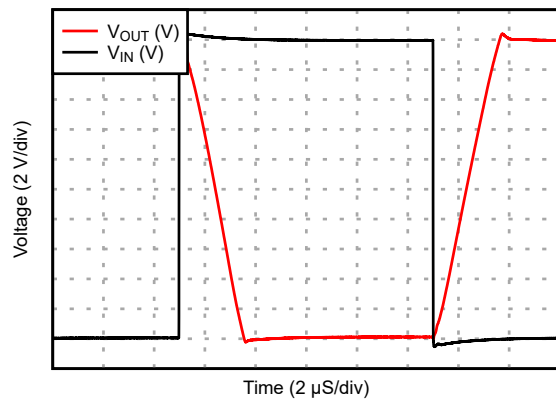


Gain = 1

图 6-40. Large-Signal Step Response, Gain = +1

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)



Gain = -1
图 6-41. Large-Signal Step Response, Gain = -1

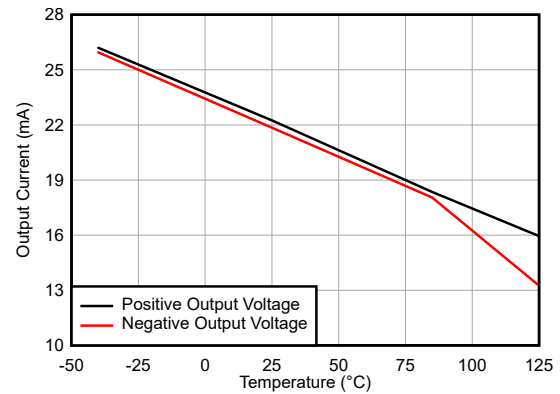


图 6-42. Short-Circuit Current vs Temperature

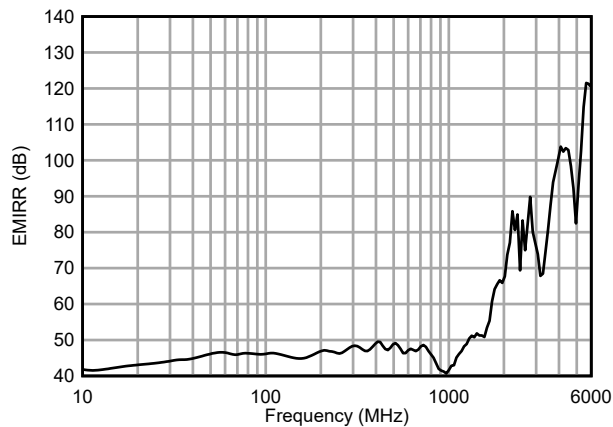


图 6-43. Electromagnetic Interference Rejection

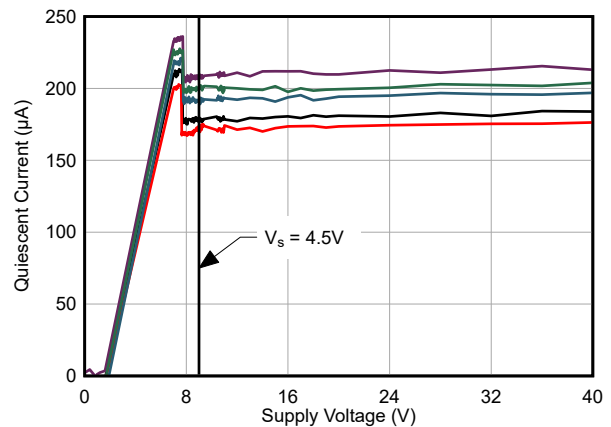


图 6-44. Quiescent Current vs Supply Voltage

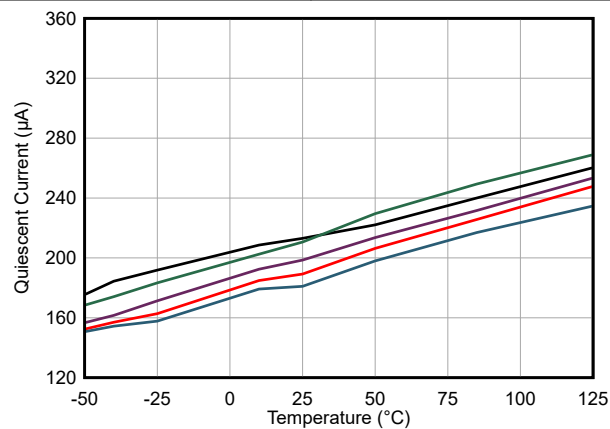


图 6-45. Quiescent Current vs Temperature

7 Parameter Measurement Information

7.1 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. As a result of natural variations in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, such as the input bias current of an amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions. Circuit designers can leverage this information to guardband their system, even when there is no minimum or maximum specification in the [Electrical Characteristics](#).

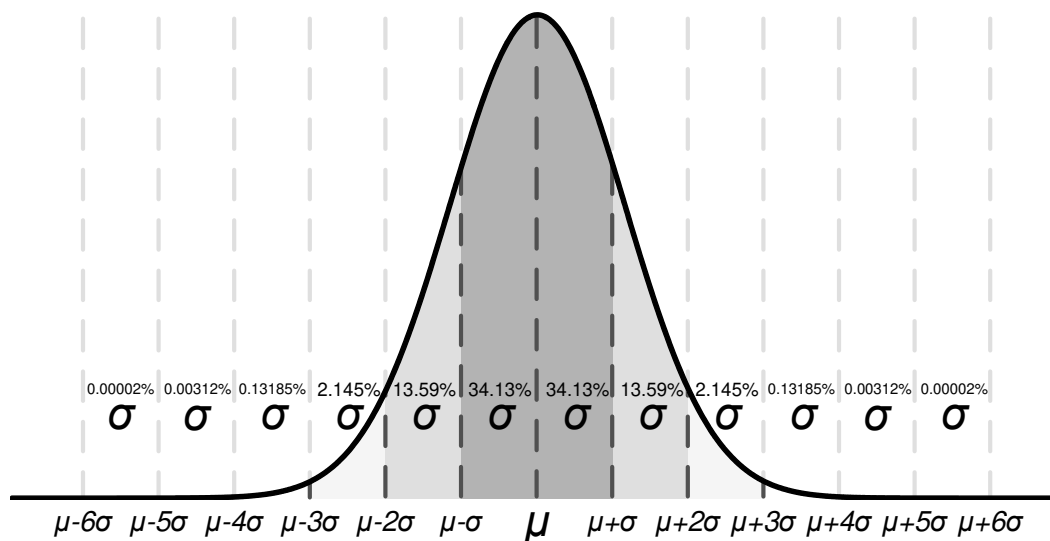


图 7-1. Ideal Gaussian Distribution

图 7-1 shows an example distribution, where μ , is the mean of the distribution, and where σ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of [Electrical Characteristics](#) are represented in different ways. As a general guideline, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (for example, input bias current), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) to most accurately represent the typical value.

Use this chart to calculate the approximate probability of a specification in a unit. For example, the OPA2205 typical input bias current is ± 0.1 nA; therefore, 68.2% of all devices are expected to have an input bias from ± 0.1 nA. At 4σ , 99.9937% of the distribution has an input bias less than ± 0.28 nA, which means that 0.0063% of the population is outside of these limits, and corresponds to approximately 1 in 15,873 units.

Units that are found to exceed any tested minimum or maximum specifications are removed from production material. For example, the OPA2205 has a maximum input bias of ± 0.4 nA at 25°C, and although this value corresponds to approximately 6σ (~1 in 500 million units), TI removes any unit with a larger input bias from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. Use this information to only estimate the performance of a device.

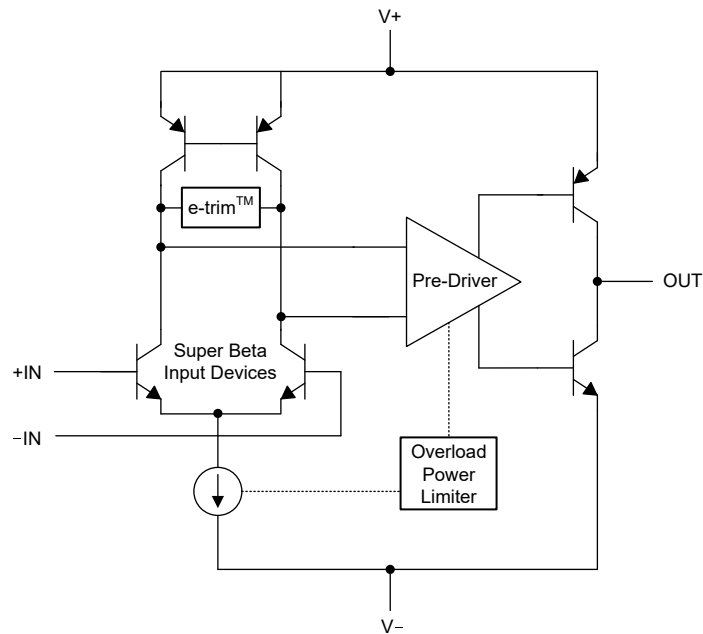
8 Detailed Description

8.1 Overview

The OPA2205 is the first 36-V bipolar, e-trim operational amplifier that uses a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device has been assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. The device also features super-beta inputs that decrease the input bias current and input current noise.

[§ 8.2](#) shows the simplified diagram of the OPA2205.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Offset Trimming

The OPA2205 is the industry's first e-trim operational amplifier built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the input transistors. The offset can be minimized using laser-trimming performed during the manufacturing process while the device is still in the bare silicon form. However, when the silicon is packaged, the packaging process introduces additional offset due to mechanic stresses. TI's new trimming processes are used to trim the offset after the packaging process is complete to minimize both inherent and package-induced offsets. After trimming, communication is disabled to make sure the amplifier operates properly in the final system.

A comparison between production offset values for the industry-popular, laser-trimmed [OPA2277](#) and the OPA2205 proprietary trim can be seen in [图 8-1](#) and [图 8-2](#).

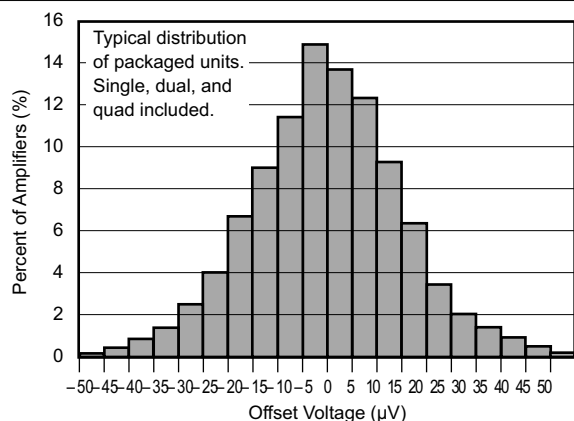


图 8-1. OPA2277 Laser-Trimmed Operational Amplifier Offset

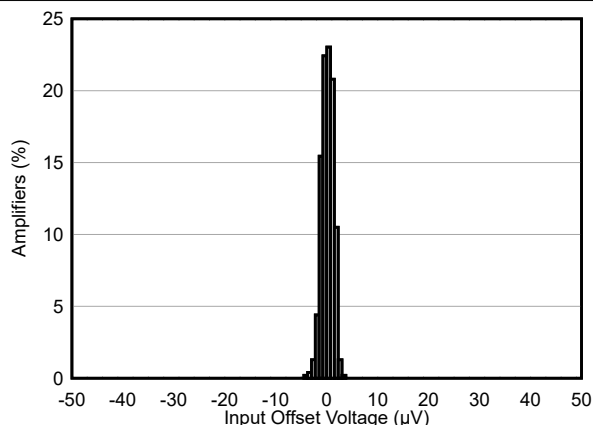


图 8-2. OPA2205 e-trim™ Operational Amplifier Offset

The OPA2205 is also trimmed at two temperatures to minimize the input offset voltage drift over temperature. The final performance of the offset drift can be seen in [图 8-3](#).

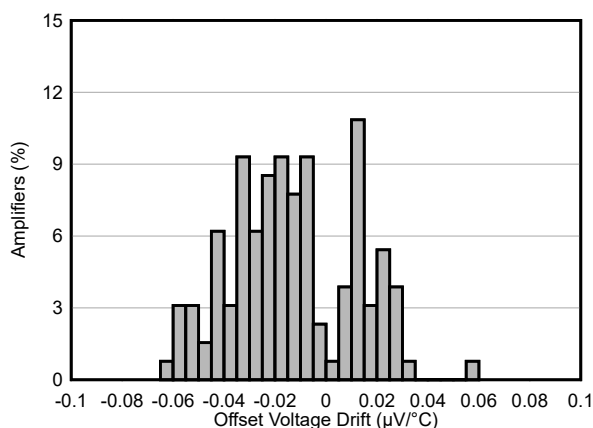


图 8-3. OPA2205 e-trim™ Operational Amplifier Drift

8.3.2 Lower Input Bias With Super-Beta Inputs

The OPA2205 has a super-beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super-beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super-beta input reduces the input bias current of the amplifier. In addition, the super-beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of the OPA2277 and the OPA2205 super-beta input bias currents can be seen in 图 8-4 and 图 8-5.

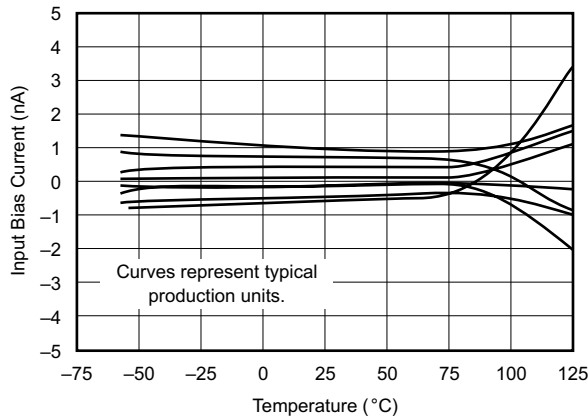


图 8-4. OPA2277 Input Bias Current

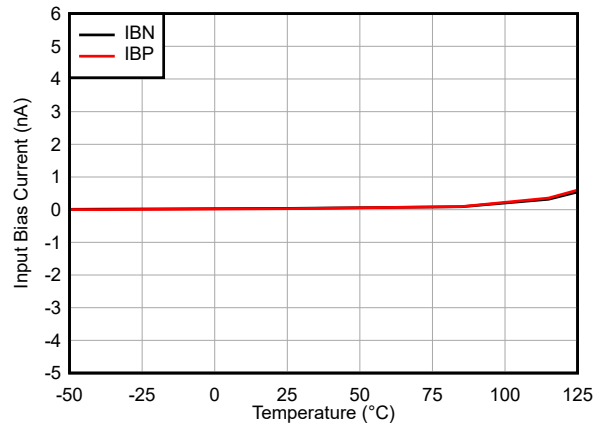


图 8-5. OPA2205 Super-Beta Input Bias Current

8.3.3 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (that is, the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPA2205 has an advanced output stage design that eliminates this problem. When the output voltage reaches either supply (V_+ or V_-), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by large external transient voltage.

8.3.4 EMI Rejection

The OPA2205 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources, such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the [EMI Rejection Ratio of Operation Amplifiers application report](#).

8.4 Device Functional Modes

The OPA2205 has a single functional mode and is operational with any supply between 4.5 V (± 2.25 V) and 36 V (± 18 V).

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The OPA2205 is a unity-gain stable operational amplifier with very low offset voltage, offset voltage drift, voltage noise, current noise and power consumption. These features make this device a great choice for a variety of space-constrained and power-constrained systems.

9.2 Typical Applications

9.2.1 High-Precision Signal-Chain Input Buffer

A common application for the OPA2205 is an input buffer for the signal chain of a data acquisition (DAQ) or field instrumentation system. This amplifier is selected because of the low offset and drift, which maintain system accuracy across a variety of operating conditions. The low power consumption of the OPA2205 enables the device to be used in battery-operated or high-density applications, where thermal dissipation is difficult. The low $1/f$ (flicker) noise and broadband noise allow for higher-accuracy signal chains, such as those using a 24-bit delta-sigma analog-to-digital converter (ADC). If a higher sampling rate is needed, the OPA2205 can be paired with a fully differential amplifier, such as the [THP210](#), to drive the ADC inputs.

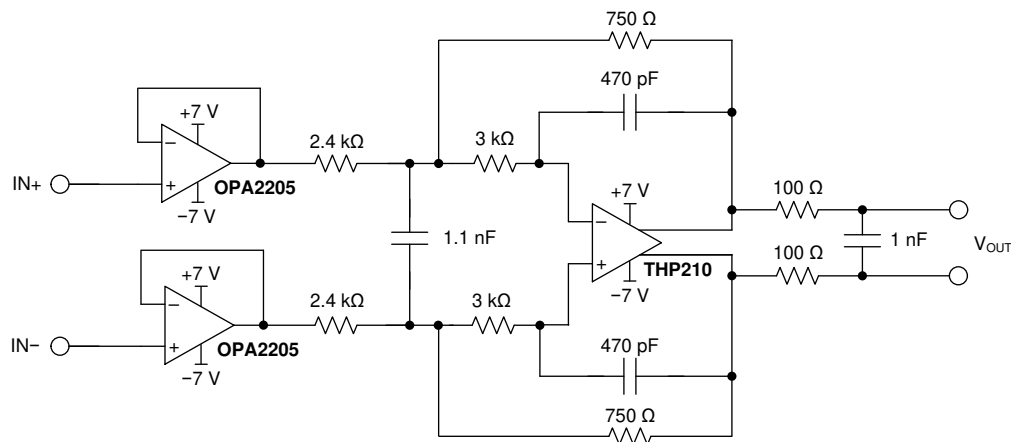


图 9-1. OPA2205 Configured as a DAQ Input Buffer

9.2.1.1 Design Requirements

The design requirements for this application are:

- Input range: ± 10 V
- Input frequency: 10 kHz
- Output voltage: ± 3.3 V
- Quiescent current: < 1.5 mA

9.2.1.2 Detailed Design Procedure

In this application, the input signal ranges from -10 V to $+10$ V with a frequency of up to 10 kHz. Because of possible portable-use cases for this data acquisition system (DAQ), low power consumption is required to minimize battery drain and thermal dissipation requirements.

To maintain high system accuracy the OPA2205 is selected as input buffers. This device is selected because of the high dc precision ($2\text{ }\mu\text{V}$ offset and $0.04\text{ }\mu\text{V}/^\circ\text{C}$ offset drift), low flicker noise ($0.2\text{ }\mu\text{Vpp}$), and low quiescent current ($220\text{ }\mu\text{A}$). The buffers are followed by a high-precision, fully differential amplifier such as the THP210, which is capable of accurately driving a 24-bit, fully differential ADC such as the [ADS127L01](#).

9.2.1.3 Application Curves

The gain plot for this system can be seen in [Figure 9-2](#). This plot shows proper attenuation of the ± 10 -V signal to the target ± 3.3 -V output, and adequate bandwidth to support the input frequency range.

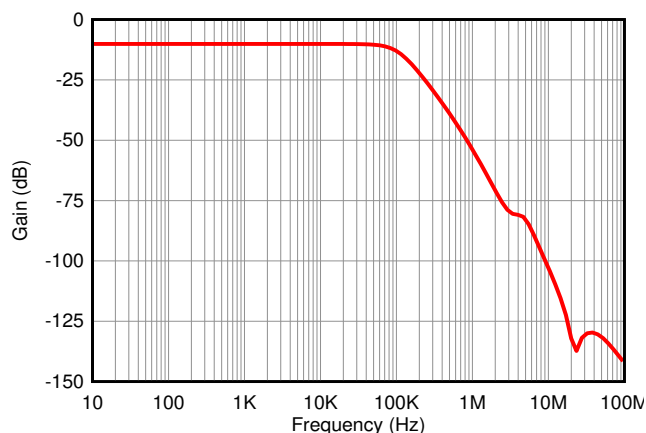


图 9-2. Gain Plot of DAQ Front End

9.2.2 Discrete, Two-Op-Amp Instrumentation Amplifier

图 9-3 shows the OPA2205 configured as a two-op-amp, discrete instrumentation amplifier. This configuration allows for a differential signal measurement, such as the signal from a load cell, with higher input impedance to the signal chain than most monolithic instrumentation amplifiers. The strong ac and dc performance of the OPA2205 enables high accuracy measurements.

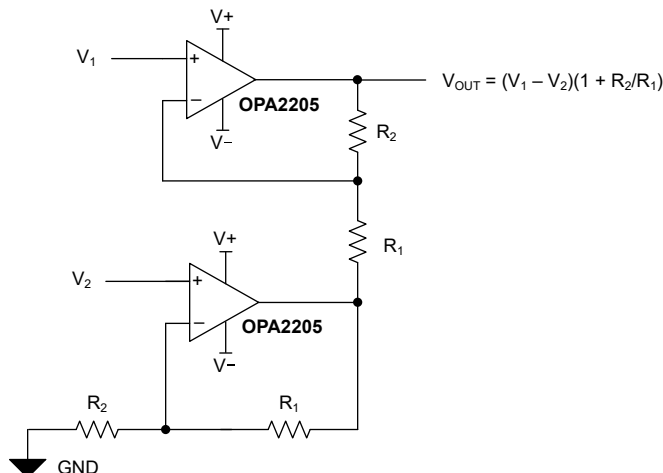


图 9-3. OPA2205 Configured as a Two-Op-Amp, Discrete Instrumentation Amplifier

9.2.3 Second-Order Low-Pass Filter

The OPA2205 has a very-low broadband voltage noise of only $7.2 \text{ nV} / \sqrt{\text{Hz}}$ and flicker noise of $0.2 \text{ } \mu\text{V}_{\text{PP}}$ given the low power consumption of only $220 \text{ } \mu\text{A}$, making this device an excellent choice for low-power filter applications. 图 9-4 is an example of one channel of the OPA2205 configured as a second-order low-pass filter with a cutoff frequency of 50 kHz.

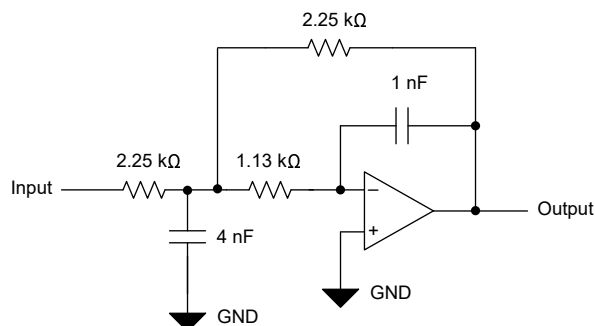


图 9-4. Second-Order Low-Pass Filter

10 Power Supply Recommendations

The OPA2205 operates with a power supply between 4.5 V to 36 V (± 2.25 V to ± 18 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in [节 6.7](#).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [节 11.1](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [图 11-1](#), keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

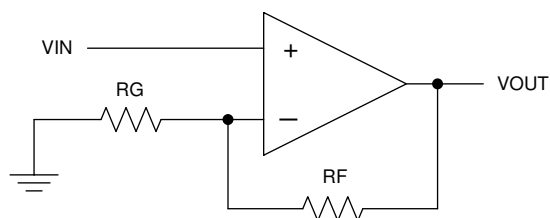


图 11-1. Schematic Representation

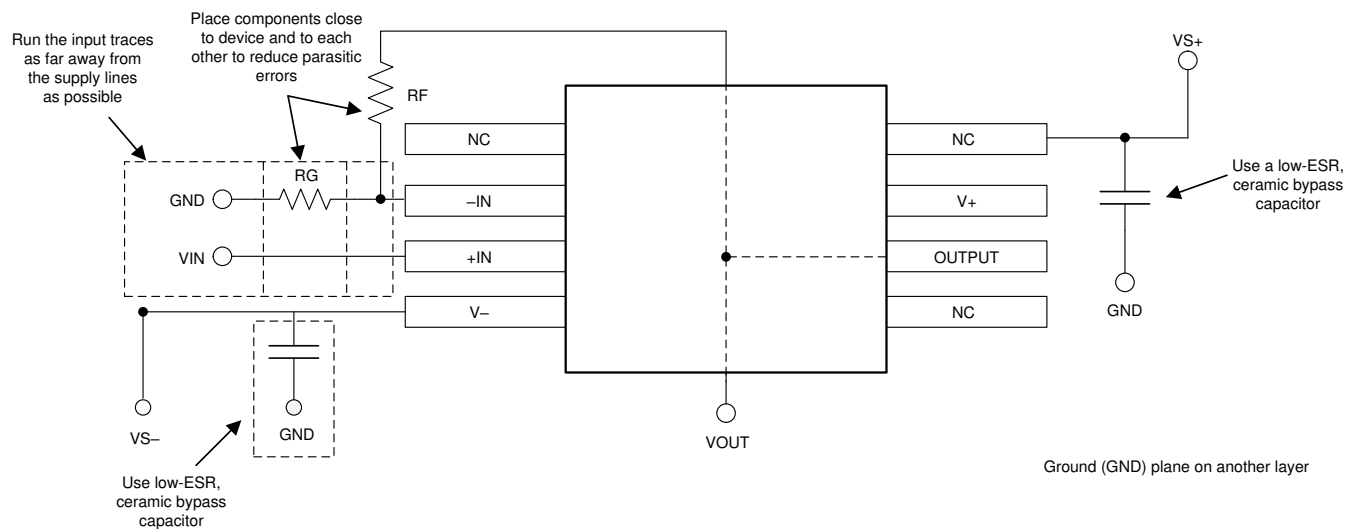


图 11-2. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

The following evaluation modules are available:

- [DIP-ADAPTER-EVM](#)
- [DIYAMP-EVM](#)

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- [DIP-ADAPTER-EVM user's guide](#)
- [DIYAMP-EVM user's guide](#)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2205ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5	Samples
OPA2205ADGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5	Samples
XOPA2205DGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

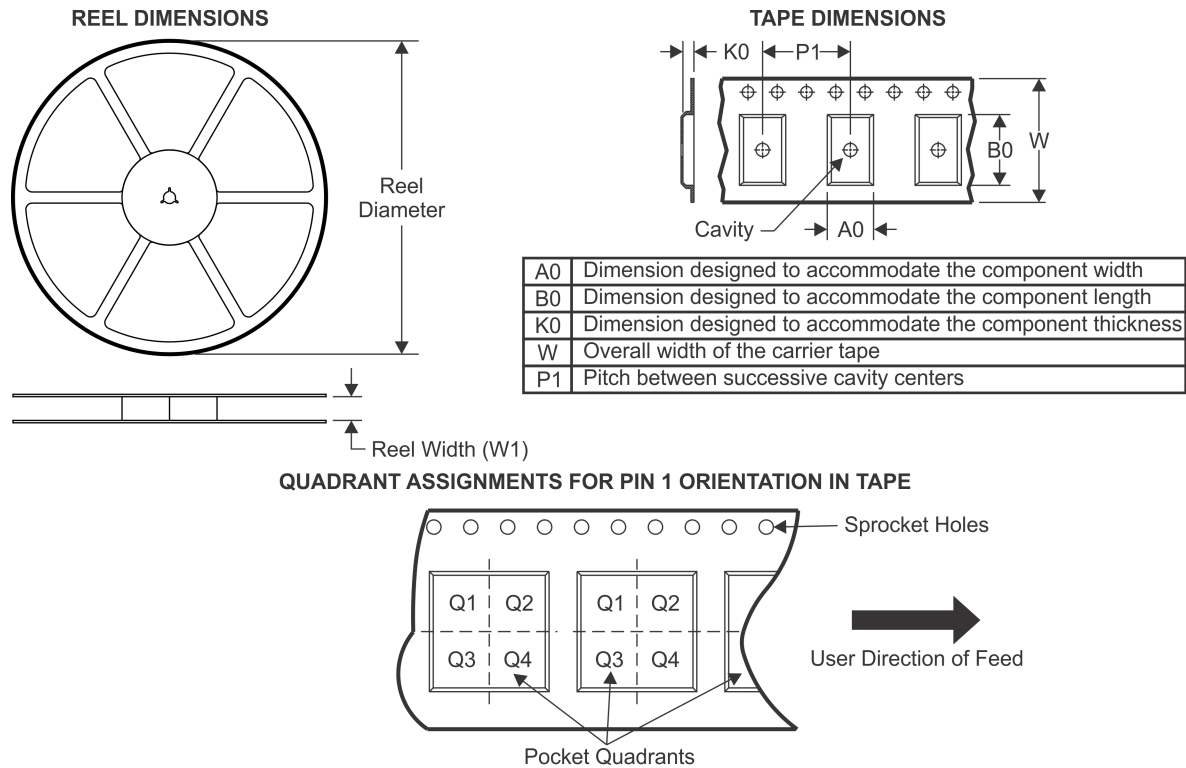
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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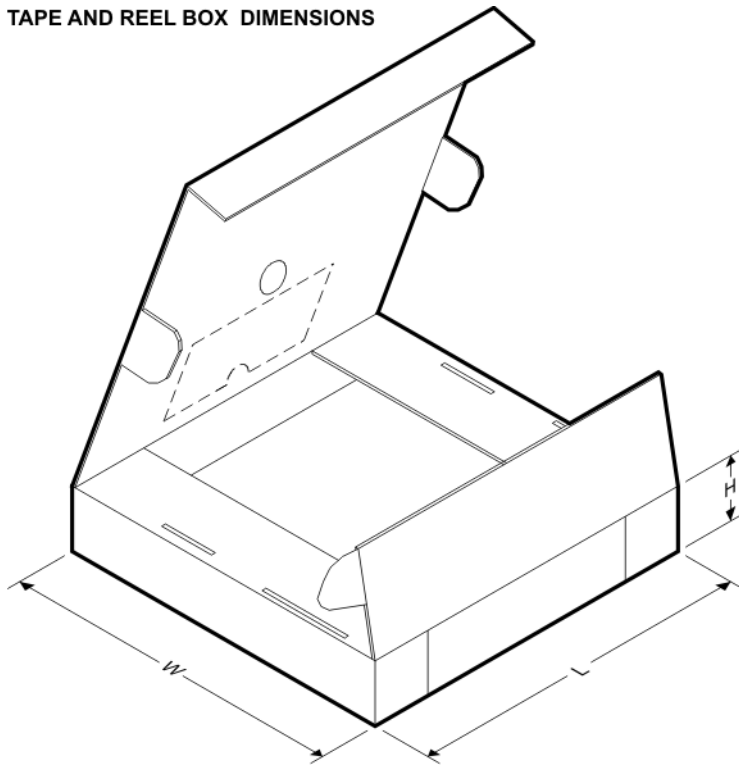
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2205ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2205ADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

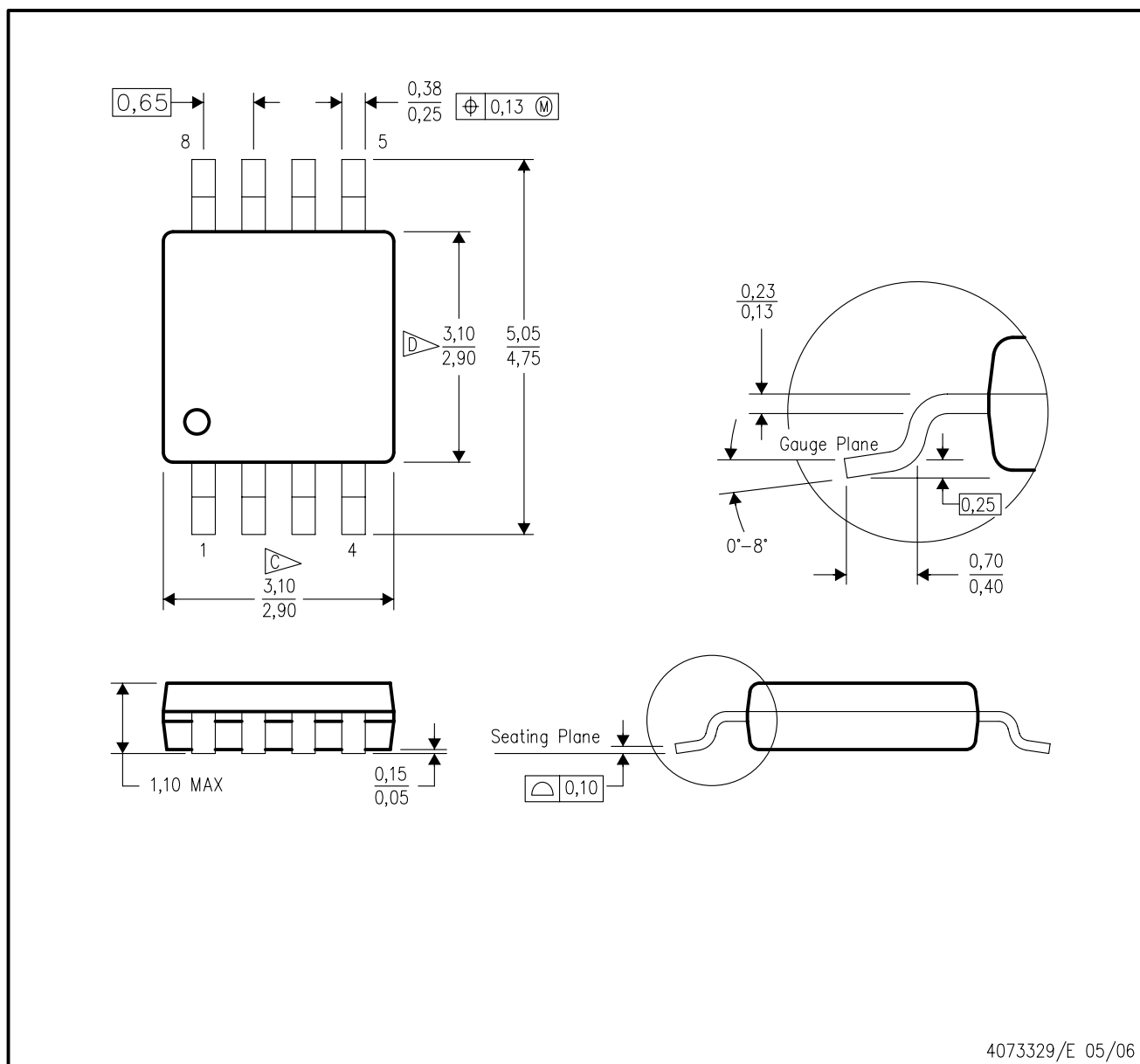


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2205ADGKR	VSSOP	DGK	8	2500	853.0	449.0	35.0
OPA2205ADGKT	VSSOP	DGK	8	250	210.0	185.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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