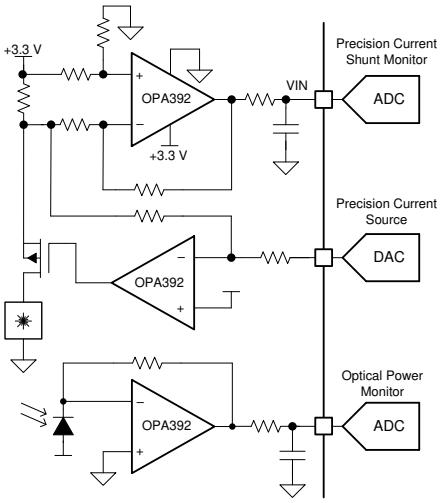
OPAx392 低失调电压、低噪声、低输入偏置电流、轨到轨 I/O、e-trim™ 精密运算放大器

1 特性

- 低失调电压：±10μV（最大值）
- 低温漂：±0.18μV/°C
- 低输入偏置电流：10fA
- 低噪声：10 kHz 时为 4.4nV/ √Hz
- 低 1/f 噪声：2μVPP（0.1Hz 至 10Hz）
- 低电源电压运行范围：1.7V 至 5.5V
- 低静态电流：1.22mA
- 快速稳定：0.75μs（1V，0.1%）
- 快速压摆率：4.5V/μs
- 高输出电流：+65/–55mA 短路
- 增益带宽：13MHz
- 轨至轨输入和输出
- 额定温度范围：–40°C 至 +125°C
- 输入已滤除 EMI 和 RFI

2 应用

- 多参数患者监护仪
- 心电图 (ECG)
- 化学/气体分析仪
- 光学模块
- 模拟输入模块
- 过程分析（pH、气体、浓度、力和湿度）
- 气体检测仪
- 模拟安防摄像机
- 商用直流/直流
- 脉搏血氧仪
- 数据中心内部互联（长距离、水下）
- 数据采集 (DAQ)



OPAx392 在光学模块中的应用

3 说明

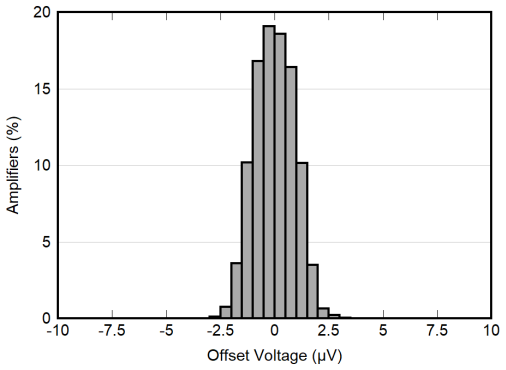
OPAx392 系列运算放大器（OPA392、OPA2392 和 OPA4392）具有超低失调电压、温漂以及输入偏置电流，可实现轨到轨输入和输出。除了精密直流精度，交流性能经优化可实现低噪声和快速稳定的瞬态响应。得益于这些特性，OPAx392 成为驱动高精度模数转换器 (ADC) 或缓冲高分辨率数模转换器 (DAC) 输出的理想选择。

OPAx392 采用 TI 的 e-trim™ 运算放大器技术，无需任何输入斩波或自动置零技术，即可实现超低失调电压以及失调电压温漂。此项技术可针对传感器输入或光电二极管电流至电压测量实现超低输入偏置电流，从而为光学模块或医疗仪表创建高性能跨阻级。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
OPA392	DSBGA (6)(3)	1.00 mm x 0.8 mm
	SC-70 (5) (3)	2.00mm x 1.25mm
	SOT-23 (5)	2.90mm x 1.60mm
OPA2392(2)	DSBGA (9)(3)	1.20 mm x 1.20 mm
	VSSOP (8)(3)	3.00mm x 3.00mm
	SOIC (8)(3)	4.90mm x 3.90mm
OPA4392(2)	TSSOP (14)(3)	5.00mm x 4.40mm
	QFN (16)(3)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 器件为预发布版。
(3) 封装为预发布版。



OPAx392 输入失调电压分布

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision * (January 2021) to Revision A (August 2021)	Page
• 将采用 DBV (SOT-23-5) 封装的 OPA392 器件从预告信息（预发布）更改为量产数据（正在供货）	1

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5 Pin Configuration and Functions

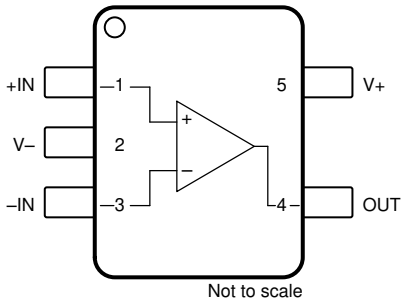


图 5-1. DCK Package (5-Pin SOT, Preview), Top View

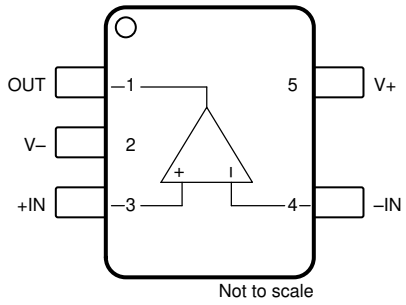


图 5-2. DBV Package (5-Pin SOT-23), Top View

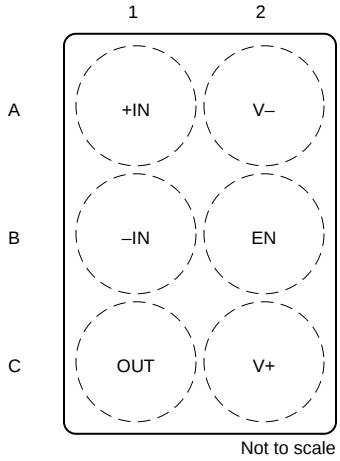


图 5-3. YCJ Package (6-Pin DSBGA, Preview), Top View

表 5-1. Pin Functions: OPA392

PIN				I/O	DESCRIPTION
NAME	NO.				
	DBV (SOT-23)	DCK (SC-70)	YCJ (DSBGA)		
–IN	4	3	B1	I	Inverting input
+IN	3	1	A1	I	Noninverting input
EN	—	—	B2	I	Enable pin. High = amplifier enabled.
OUT	1	4	C1	O	Output
V–	2	2	A2	—	Negative (lowest) power supply
V+	5	5	C2	—	Positive (highest) power supply

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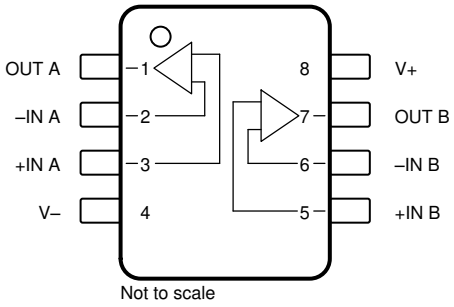


图 5-4. OPA2392 D (8-Pin SOIC, Preview) and DGK (8-Pin MSOP, Preview) Packages, Top View

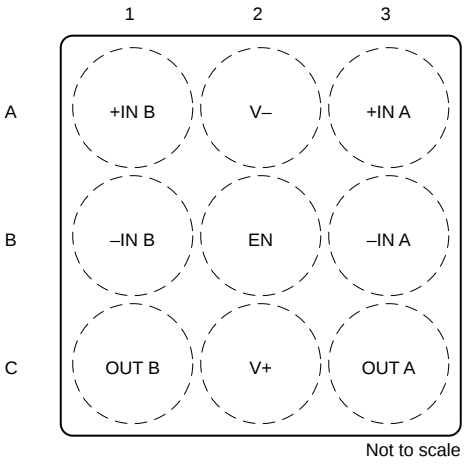


图 5-5. OPA2392 YBJ (9-Pin DSBGA, Preview) Package, Top View

表 5-2. Pin Functions: OPA2392

PIN			I/O	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	YBJ (DSBGA)		
– IN A	2	B3	I	Inverting input, channel A
– IN B	6	B1	I	Inverting input, channel B
+IN A	3	A3	I	Noninverting input, channel A
+IN B	5	A1	I	Noninverting input, channel B
EN	—	B2	I	Enable pin. High = both amplifiers enabled.
OUT A	1	C3	O	Output, channel A
OUT B	7	C1	O	Output, channel B
V –	4	A2	—	Negative (lowest) power supply
V+	8	C2	—	Positive (highest) power supply

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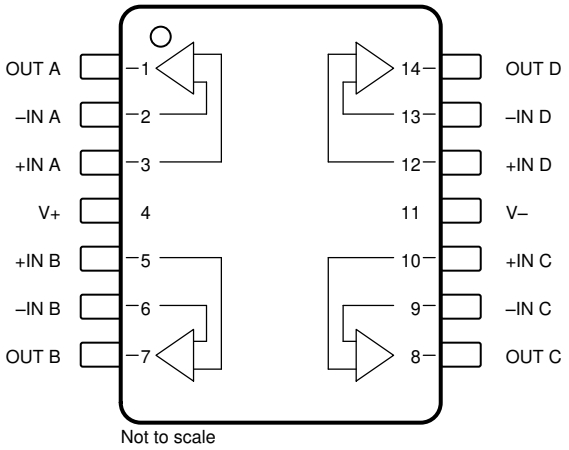


图 5-6. OPA4392 PW (14-Pin TSSOP, Preview) Package, Top View

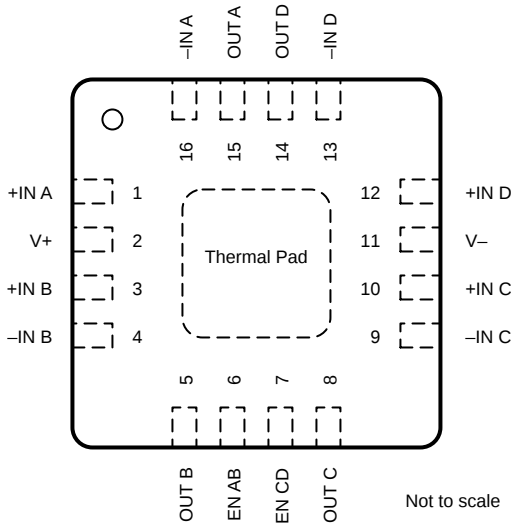


图 5-7. OPA4392 RTE (16-Pin QFN, Preview) Package, Top View

表 5-3. Pin Functions: OPA4392

PIN			I/O	DESCRIPTION
NAME	NO.			
	PW (TSSOP)	RTE (QFN)		
– IN A	2	16	I	Inverting input, channel A
– IN B	6	4	I	Inverting input, channel B
– IN C	9	9	I	Inverting input, channel C
– IN D	13	13	I	Inverting input, channel D
+IN A	3	1	I	Noninverting input, channel A
+IN B	5	3	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
EN AB	—	6	I	Enable pin for A and B amplifiers. High = amplifiers A and B are enabled.
EN CD	—	7	I	Enable pin for C and D amplifiers. High = amplifiers C and D are enabled.
OUT A	1	15	O	Output, channel A
OUT B	7	5	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
Thermal Pad	—	Thermal Pad	—	Connect thermal pad to V –
V –	11	11	—	Negative (lowest) power supply
V+	4	2	—	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Input current, all pins			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
T_A	Specified temperature	Specified temperature	–40		+125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA392 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

at T_A = 25°C, V_S = 1.7 V to 5.5 V (single-supply) or V_S = ±0.85 V to ±2.75 V (dual-supply), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.0 V			±1	±10	µV
			V_{CM} = (V+) – 200 mV		±2	±30	
			T_A = –40°C to +125°C			±100	
		V_{CM} = (V–), T_A = –40°C to 125°C				±125	
dV_{OS}/dT	Input offset voltage drift	V_S = 5.0 V	T_A = 0°C to 85°C		±0.16		µV/°C
			T_A = –40°C to +125°C			±0.6	
			V_{CM} = 5.0 V, T_A = –40°C to +125°C		±0.18	±0.9	
PSRR	Power supply rejection ratio	V_{CM} = (V–)				±30	µV/V
			T_A = –40°C to +125°C			±80	
INPUT BIAS CURRENT							
I_B	Input bias current				±0.01	±0.8	pA
		T_A = –40°C to +85°C				±5	
		T_A = –40°C to +125°C				±30	
I_{OS}	Input offset current				±0.01	±0.8	pA
		T_A = –40°C°C to +85°C				±5	
		T_A = –40°C to +125°C				±30	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.0		µV_{PP}
			V_{CM} = (V+) – 0.3		3.2		
e_N	Input voltage noise density	f = 10 Hz			42		nV/√Hz
			V_{CM} = (V+) – 0.3		80		
		f = 1 kHz			6.5		
			V_{CM} = (V+) – 0.3		10.4		
		f = 10 kHz			4.4		
			V_{CM} = (V+) – 0.3		5.8		
i_N	Input current noise	f = 1 kHz			70		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V		75	120		dB
			T_A = –40°C to +125°C		113		
		(V–) < V_{CM} < (V+), T_A = –40°C to +125°C		66	97		
			V_S = 5.5 V	88	111		
INPUT CAPACITANCE							
Z_{ID}	Differential				10^{13} || 2.8		Ω || pF
Z_{ICM}	Common-mode				10^{13} || 3.5		Ω || pF

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6.5 Electrical Characteristics (continued)

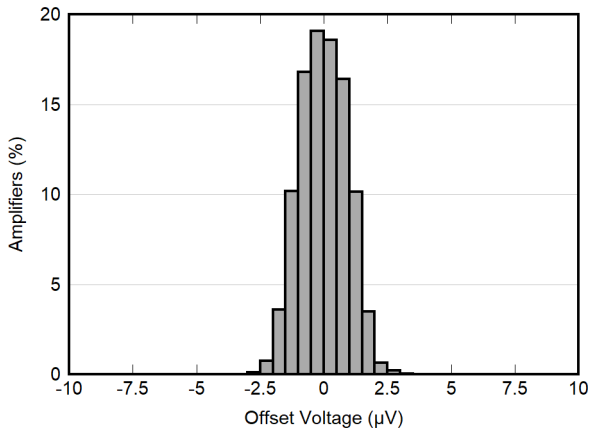
at T_A = 25°C, V_S = 1.7 V to 5.5 V (single-supply) or V_S = ±0.85 V to ±2.75 V (dual-supply), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5	(V–) + 50 mV < V_{OUT} < (V+) – 50 mV, R_L = 10 kΩ	115	132		dB
			(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ	110	128		
			(V–) + 100 mV < V_{OUT} < (V+) – 100 mV, R_L = 2 kΩ, T_A = –40°C to +125°C	100			
		V_S = 1.7	(V–) + 50 mV < V_{OUT} < (V+) – 50 mV, R_L = 10 kΩ, V_{CM} = (V+) – 1.15 V	106	124		
			(V–) + 100 mV < V_{OUT} < (V+) – 100 mV, R_L = 2 kΩ, V_{CM} = (V+) – 1.15 V	106	124		
			(V–) + 100 mV < V_{OUT} < (V+) – 100 mV, R_L = 2 kΩ, V_{CM} = (V+) – 1.15 V, T_A = –40°C to +125°C	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	A_V = 1000 V/V			13		MHz
SR	Slew rate	4-V step, gain = +1	falling		4.5		V/μs
			rising		3.5		V/μs
	Phase margin	C_L = 100 pF			45		°
t_S	Settling time	To 0.1%, 2-V step, gain = +1			0.75		μs
		To 0.01%, 2-V step, gain = +1			1		
	Overload recovery time	V_{IN} × gain > V_S			0.45		μs
THD+N	Total harmonic distortion + noise	V_{OUT} = 1 V_{RMS}, gain = +1, f = 1 kHz, R_L = 10 kΩ, V_{CM} = (V–) + 1.5 V			–112		dB
					0.00025		%
OUTPUT							
	Voltage output swing from both rails	V_S = 1.7 V	R_L = 10 kΩ			20	mV
			R_L = 2 kΩ			30	
		V_S = 5.5 V	R_L = 10 kΩ			20	
			R_L = 2 kΩ			35	
I_{SC}	Short-circuit current	Sinking, V_S = 5.5 V			–55		mA
		Sourcing, V_S = 5.5 V			65		
R_O	Open-loop output impedance	f = 1 MHz			120		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			1.22	1.4	mA
		I_O = 0 mA, T_A = –40°C to +125°C				1.5	

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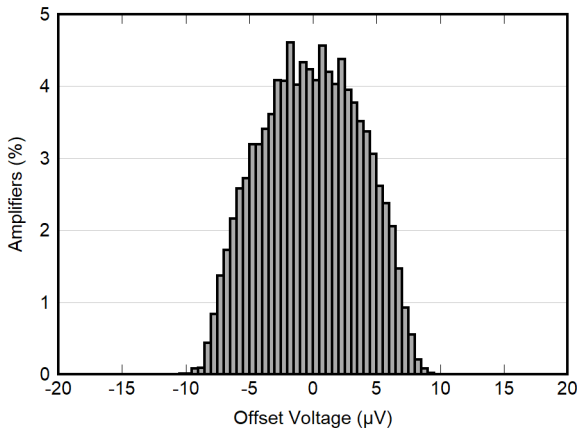
6.6 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



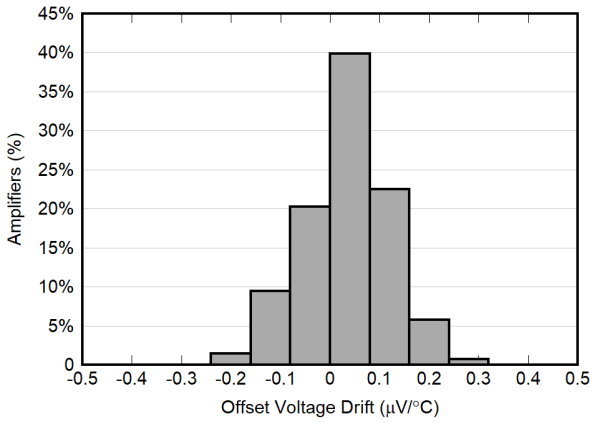
V_S = 5.0 V

图 6-1. Offset Voltage Distribution



V_S = 5.0 V, V_{CM} = 4.8 V

图 6-2. Offset Voltage Distribution



V_S = 5.0 V

图 6-3. Offset Voltage Distribution

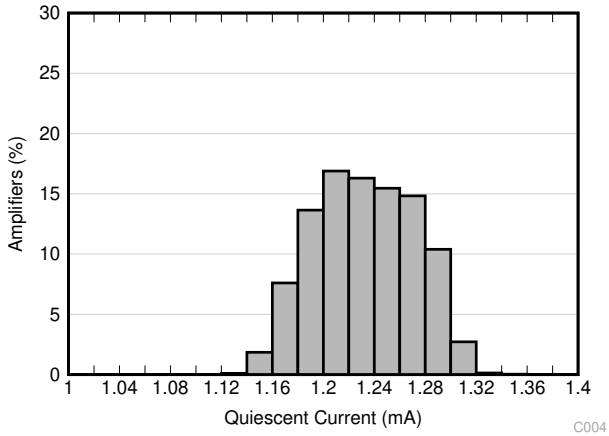
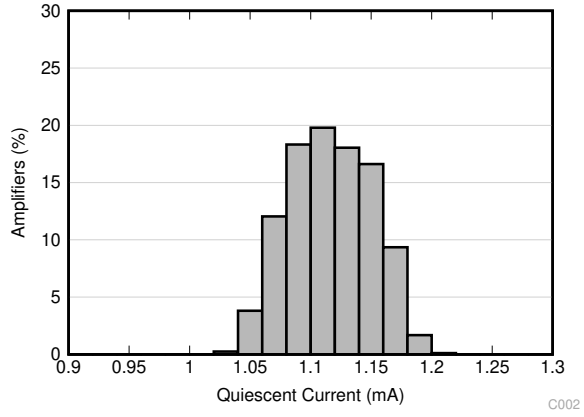


图 6-4. Quiescent Current Distribution



V_S = 1.7 V

图 6-5. Quiescent Current Distribution

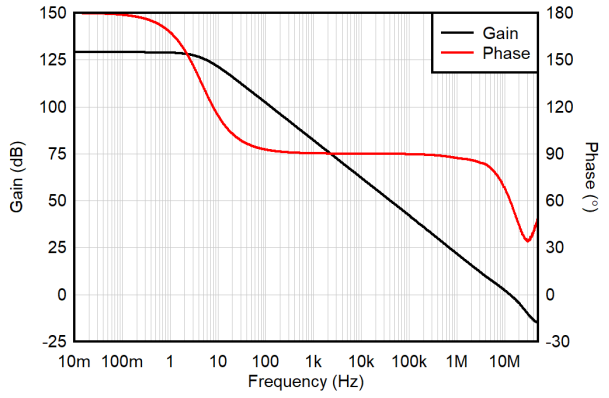


图 6-6. Open-Loop Gain and Phase vs Frequency

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

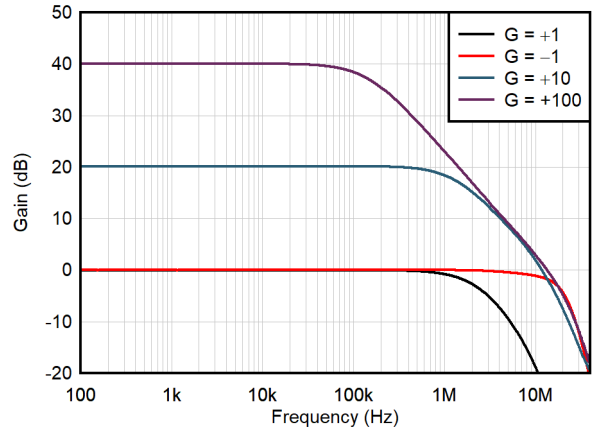
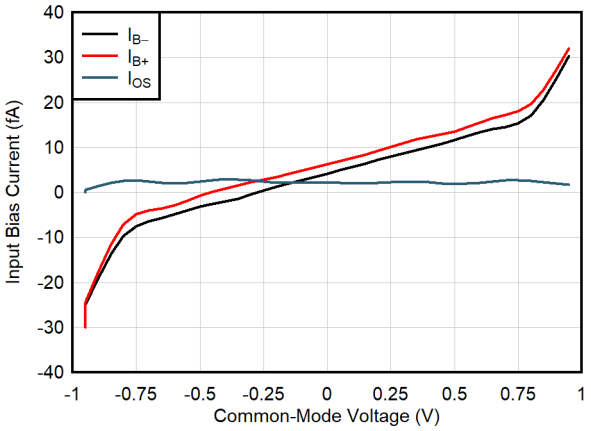
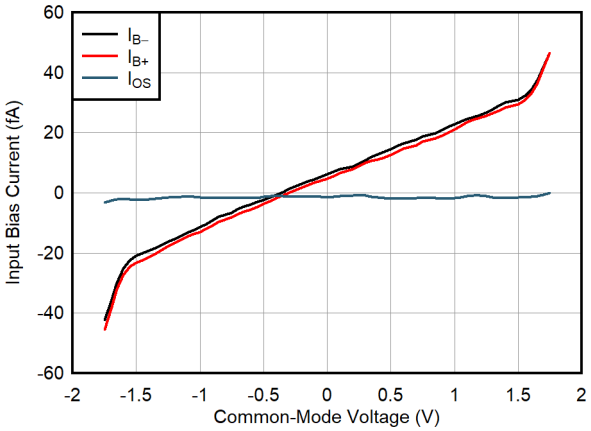


图 6-7. Closed-Loop Gain and Phase vs Frequency



V_S = 1.7 V

图 6-8. Input Bias Current vs Common-Mode Voltage



V_S = 3.3 V

图 6-9. Input Bias Current vs Common-Mode Voltage

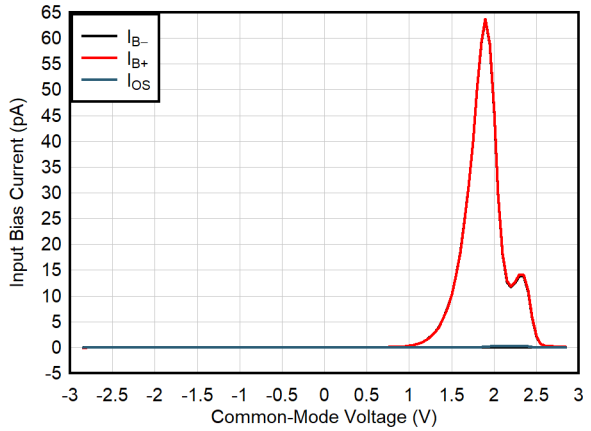


图 6-10. Input Bias Current vs Temperature

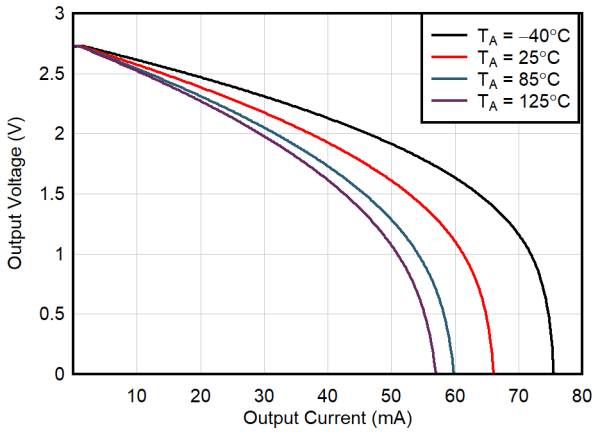


图 6-11. Output Voltage Swing vs Output Current (Sourcing)

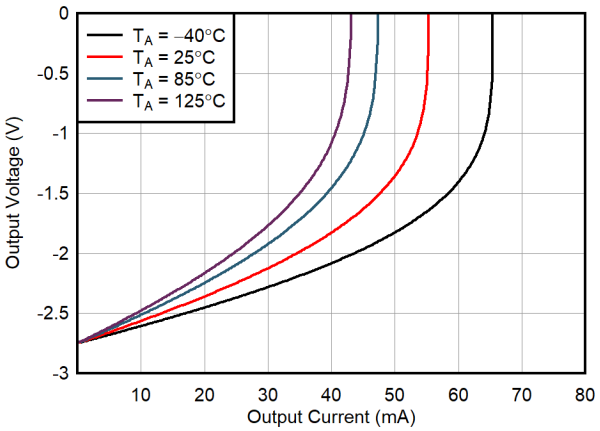
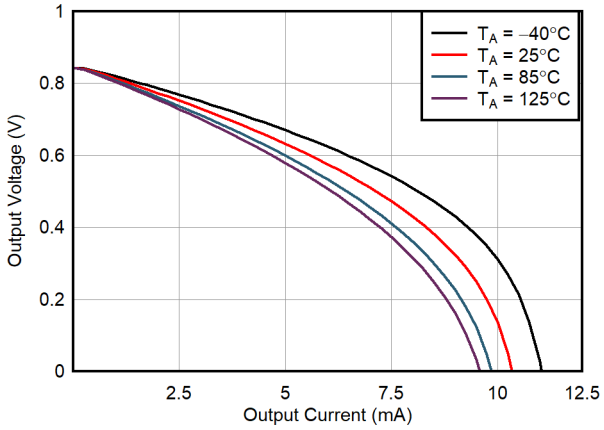


图 6-12. Output Voltage Swing vs Output Current (Sinking)

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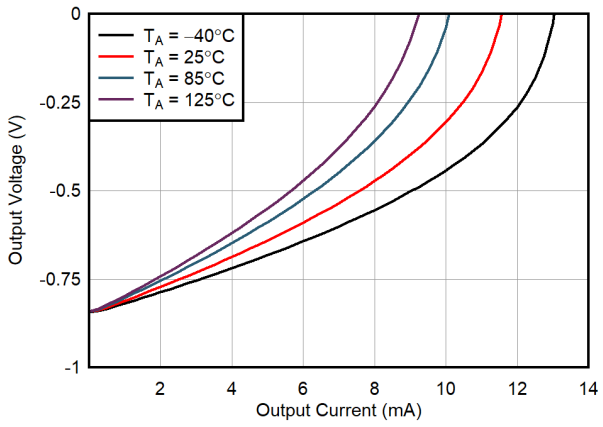
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



V_S = ±0.85 V

图 6-13. Output Voltage Swing vs Output Current (Sourcing)



V_S = ±0.85 V

图 6-14. Output Voltage Swing vs Output Current (Sinking)

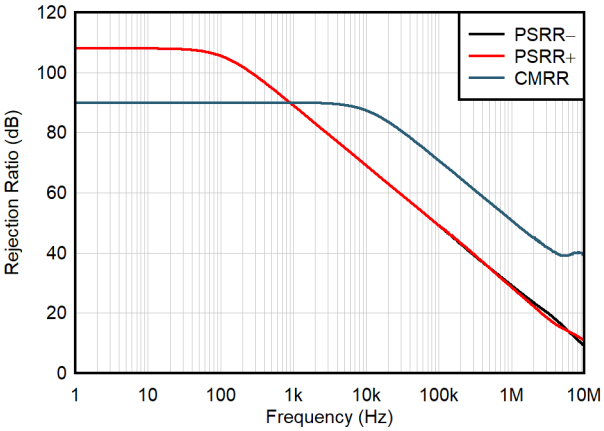
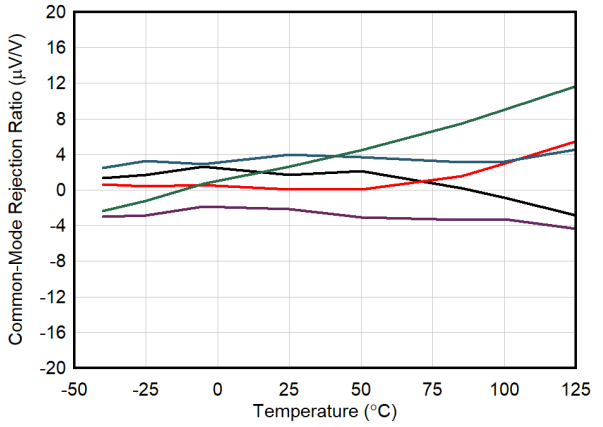
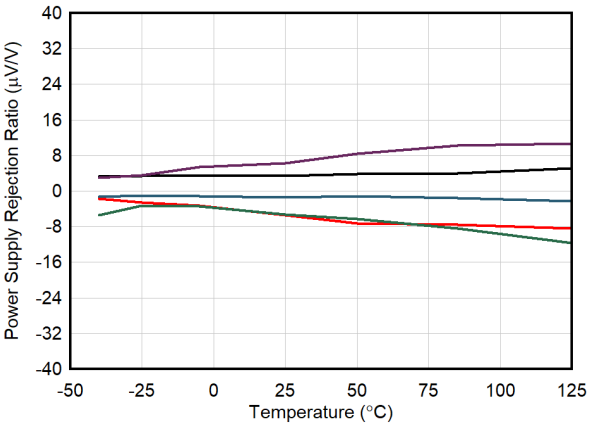


图 6-15. CMRR and PSRR vs Frequency



5 Units

图 6-16. CMRR vs Temperature



5 Units

图 6-17. PSRR vs Temperature

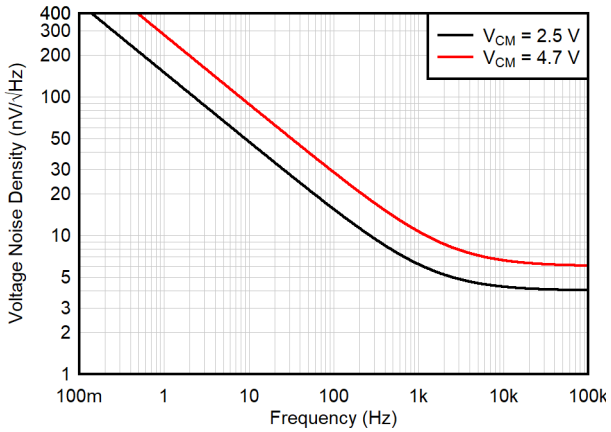
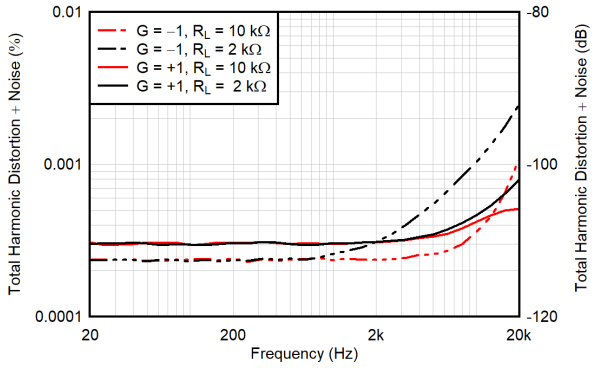


图 6-18. Voltage Noise vs Frequency

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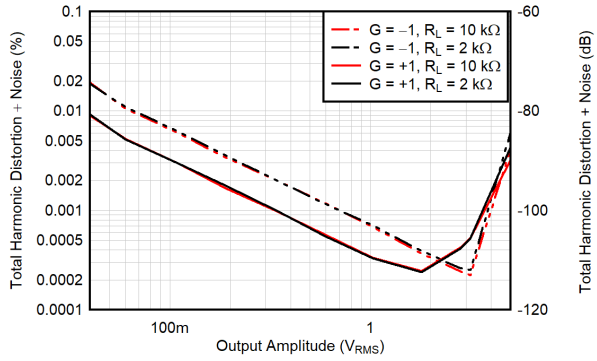
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



V_{OUT} = 1 V_{RMS}

图 6-19. THD+N Ratio vs Frequency



f = 1 kHz

图 6-20. THD+N vs Output Amplitude

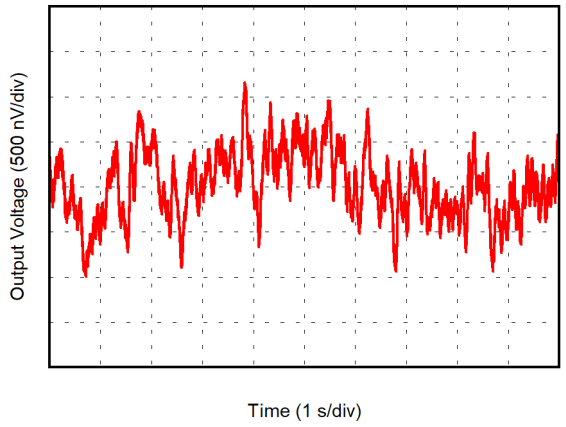
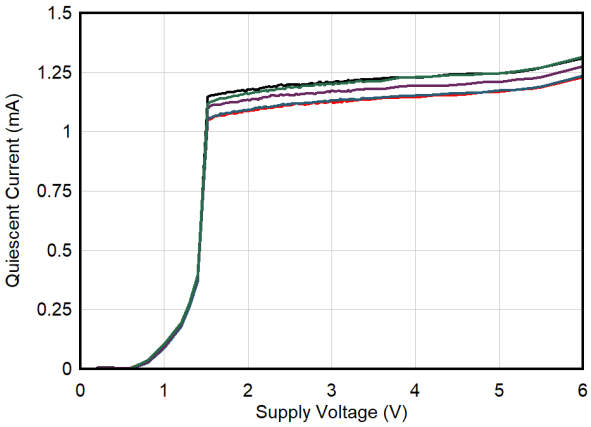
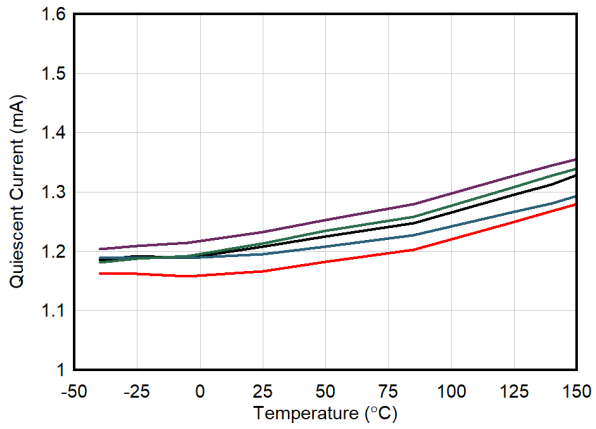


图 6-21. 0.1-Hz to 10-Hz Noise



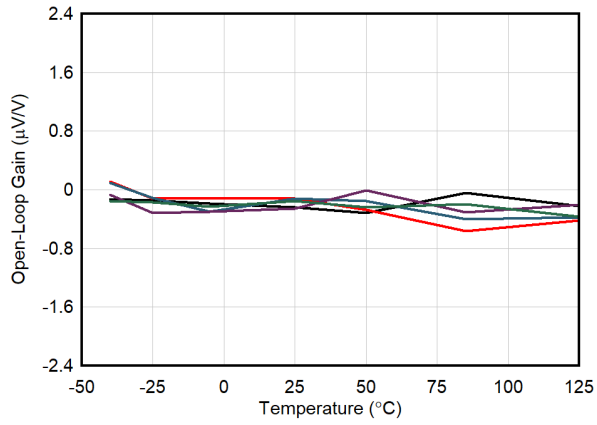
5 Units

图 6-22. Quiescent Current vs Supply Voltage



5 Units

图 6-23. Quiescent Current vs Temperature



5 Units

图 6-24. Open-Loop Gain vs Temperature

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

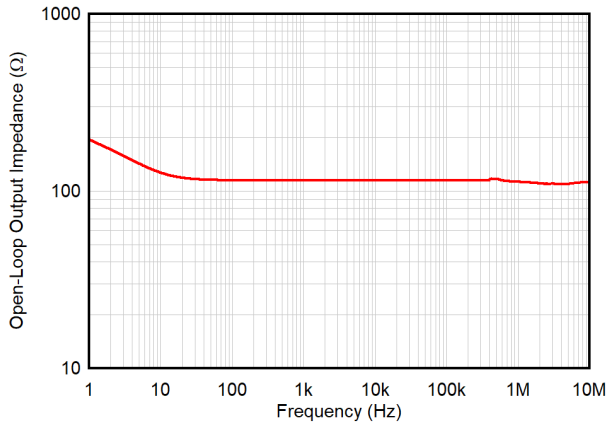
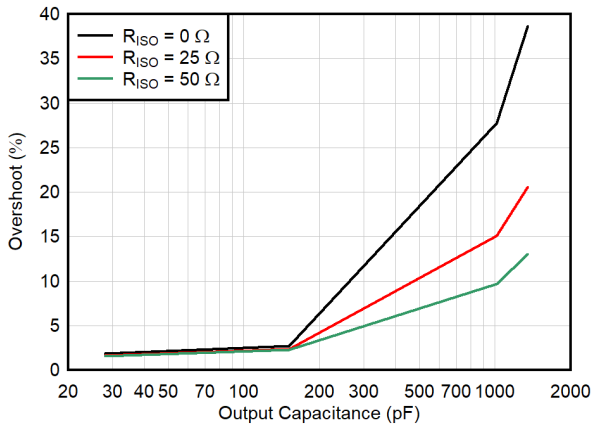
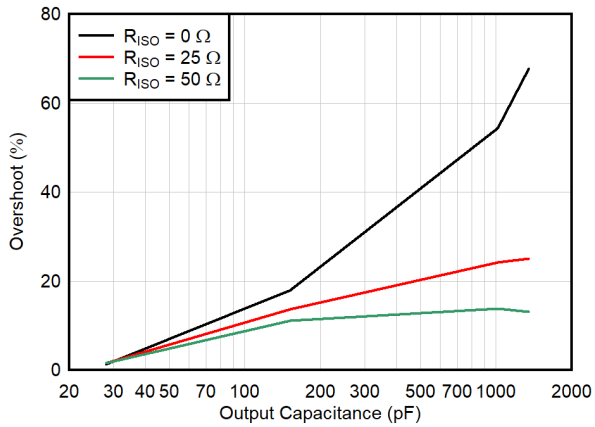


图 6-25. Open-Loop Output Impedance vs Frequency



G = –1

图 6-26. Small-Signal Overshoot vs Capacitive Load (10-mV Step)



G = 1

图 6-27. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

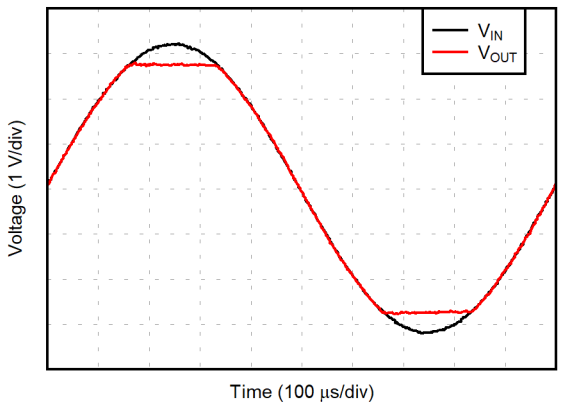


图 6-28. No Phase Reversal

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

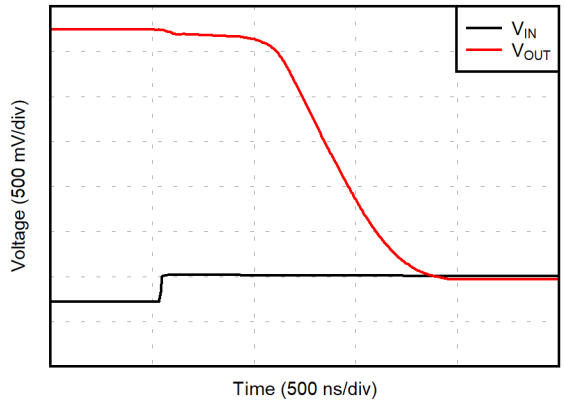


图 6-29. Positive Overload Recovery

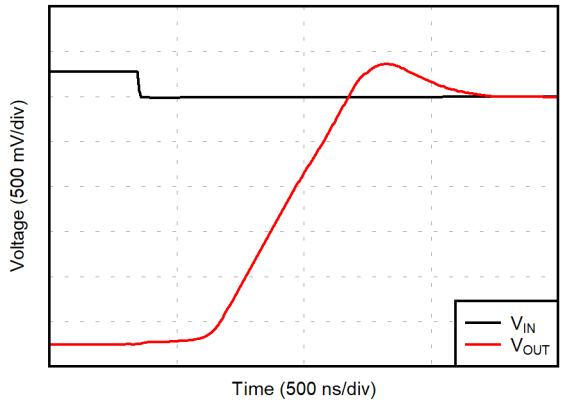
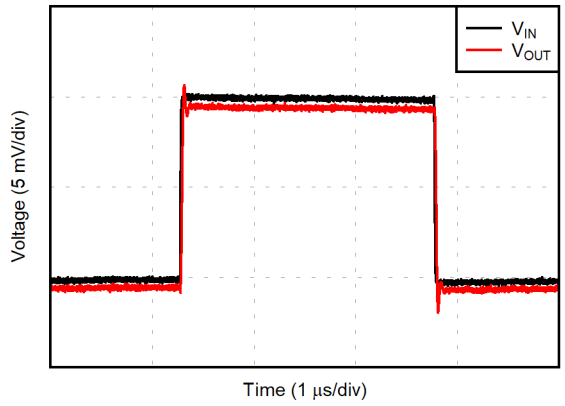
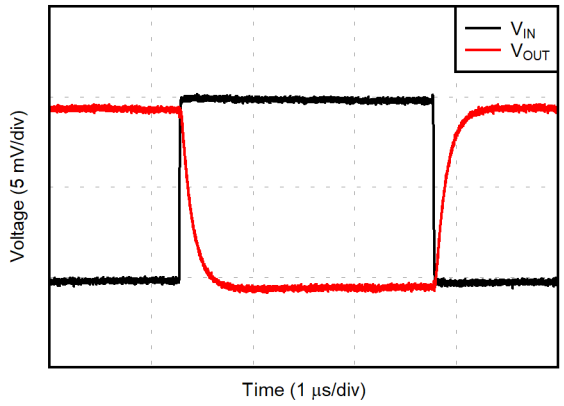


图 6-30. Negative Overload Recovery



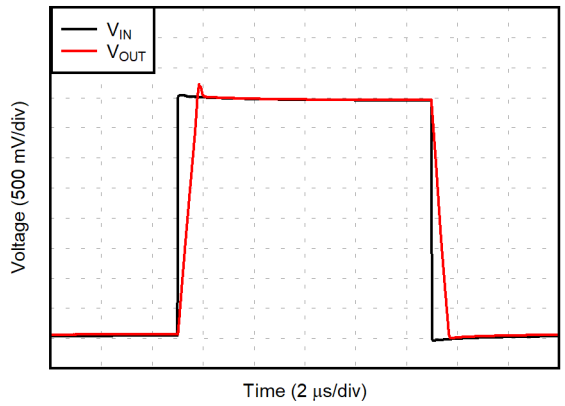
G = 1

图 6-31. Small-Signal Step Response (10-mV Step)



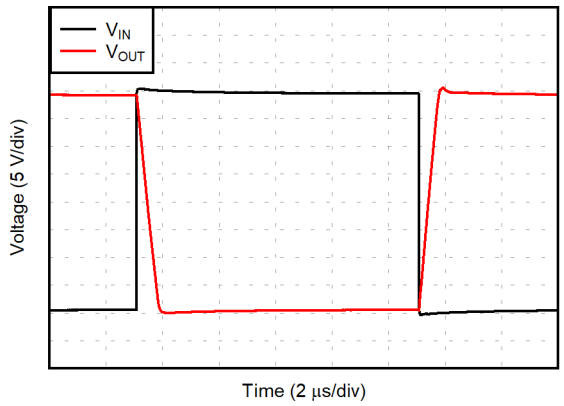
G = –1

图 6-32. Small-Signal Step Response (10-mV Step)



G = 1

图 6-33. Large-Signal Step Response (4-V Step)



G = –1

图 6-34. Large-Signal Step Response (4-V Step)

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

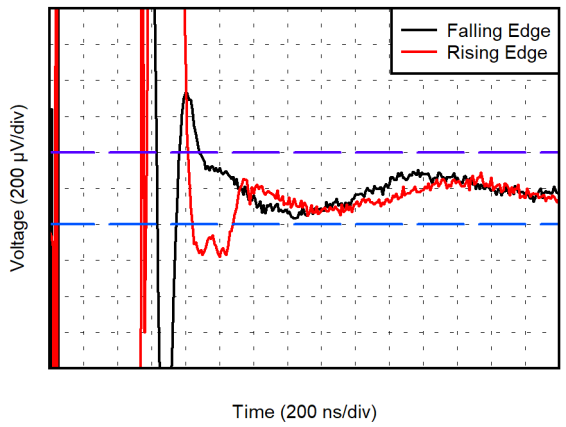
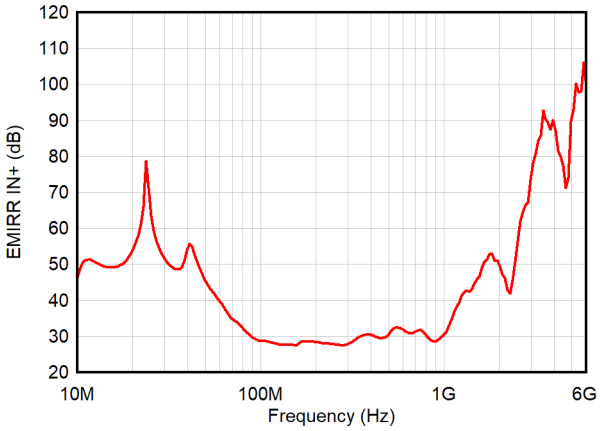


图 6-35. Settling Time



P_{RF} = – 10 dBm

图 6-36. EMIRR vs Frequency

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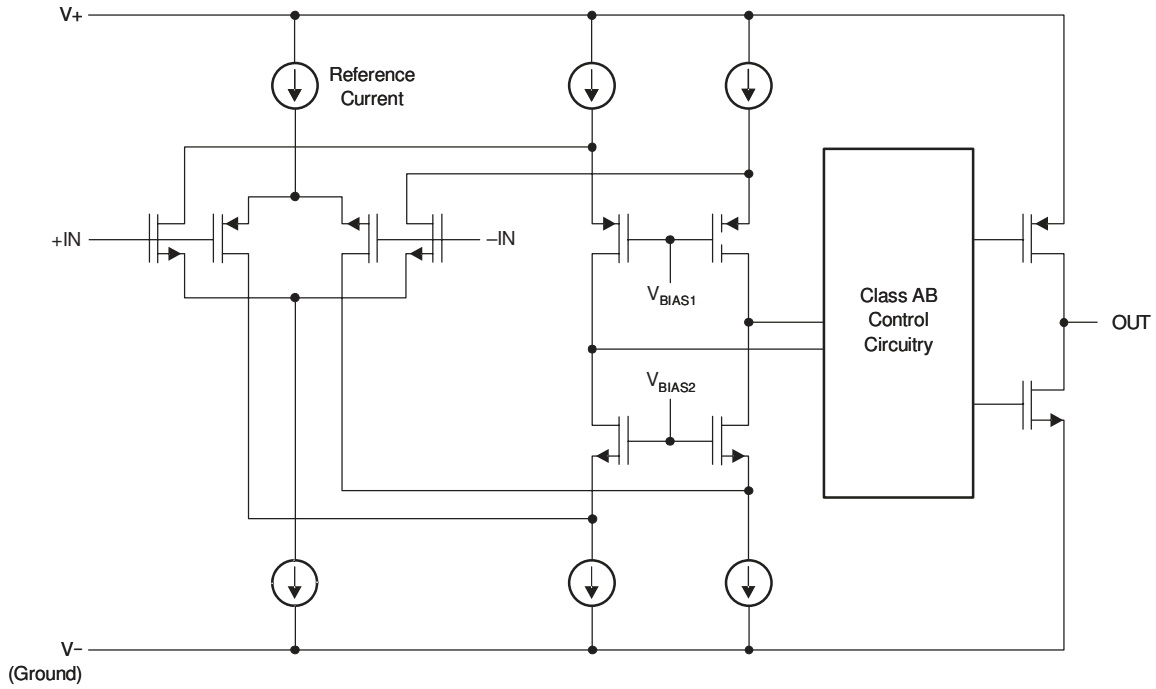
7 Detailed Description

7.1 Overview

The OPAx392 is a family of low offset, low-noise e-trim operational amplifiers (op amps) that uses a proprietary offset trim technique. These op amps offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx392 operate from 1.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve extremely low input bias current, wide input and output voltage ranges, high loop gain, and low, flat output impedance in small package options. The OPAx392 strengths also include 13-MHz bandwidth, 4.4-nV/ $\sqrt{\text{Hz}}$ noise spectral density, and low 1/f noise. These features make the OPAx392 optimal for interfacing with sensors, photodiodes, and high-performance analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Low Operating Voltage

The OPAx392 family can be used with single or dual supplies from an operating range of V_S = 1.7 V (±0.85 V) up to 5.5 V (±2.75 V). The offset voltage is trimmed at 5.0 V, however, the device maintains ultra-low offset voltages down to V_S = 1.7 V.

Key parameters that vary over the supply voltage or temperature range are shown in 节 6.6.

7.3.2 Low Input Bias Current

The typical input bias current of the OPAx392 is extremely low (typically 10 fA). Input bias current is dominated by leakage current from the ESD protection diodes, which is proportional to the area of the diode. The OPAx392 is able to achieve ultra-low input bias current as a result of modern process technology and advanced ESD protection design that minimizes the area of the diode.

In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in the forward-biasing of the ESD cells. The equivalent circuit is shown in 图 7-1.

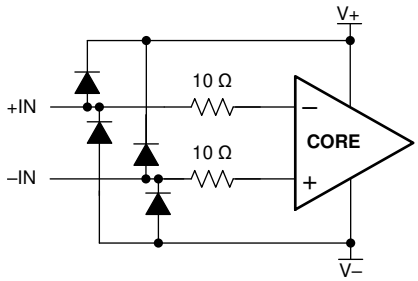


图 7-1. Equivalent Input Circuit

7.4 Device Functional Modes

The OPAx392 family is operational when the power-supply voltage is greater than 1.7 V (±0.85 V). For devices that use the EN function (see 节 5), the devices are disabled when the EN pin is low. In this state, quiescent current is significantly reduced, and the output is high impedance. The maximum specified power-supply voltage for the OPAx392 is 5.5 V (±2.75 V).

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8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The OPAx392 is a unity-gain stable, precision operational amplifier family free from unexpected output and phase reversal. The use of proprietary e-trim operational amplifier technology gives the benefit of low input offset voltage over time and temperature, along with ultra-low input bias current. The OPAx392 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range to the supply rail, with low offset across the supply range, and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx392 precision amplifiers are designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

8.2 Typical Application

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA392 because of the low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

图 8-1 shows the schematic.

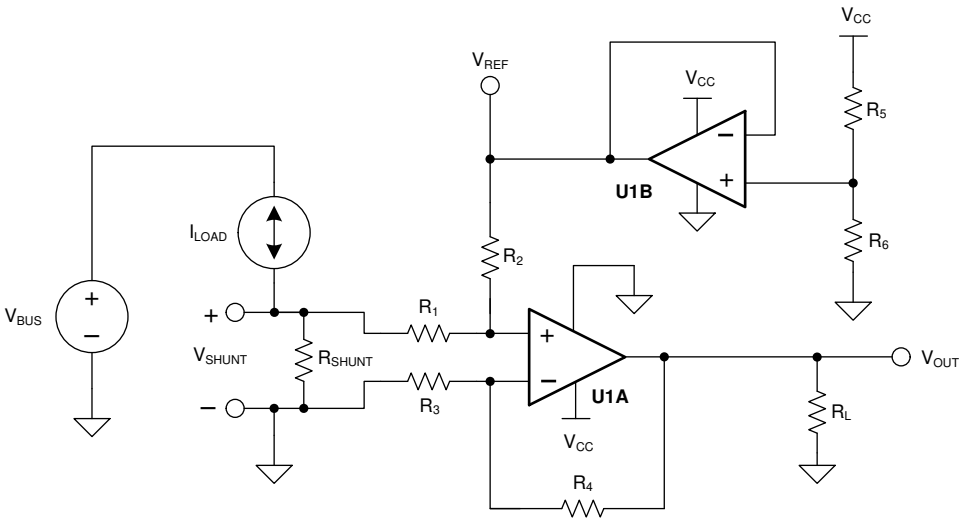


图 8-1. Bidirectional Current-Sensing Schematic

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8.2.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to +1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor, R_{SHUNT}, to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by 方程式 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff_Amp} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. 方程式 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% is selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to +100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA392, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, the OPA392 has a typical offset voltage of merely ±0.25 µV (±5 µV maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10-kΩ resistors are used.

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To set the gain of the difference amplifier, the common-mode range and output swing of the OPA392 must be considered. 方程式 3 and 方程式 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA392 given a 3.3-V supply.

$$-100\ mV < V_{CM} < 3.4\ V \tag{3}$$

$$100\ mV < V_{OUT} < 3.2\ V \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in 方程式 5:

$$Gain_{Diff_Amp} = \frac{V_{OUT_Max} - V_{OUT_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-1A)]} = 15.5\ \frac{V}{V} \tag{5}$$

The resistor value selected for R_1 and R_3 is 1 kΩ. 15.4 kΩ is selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors are selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.3 Application Curve

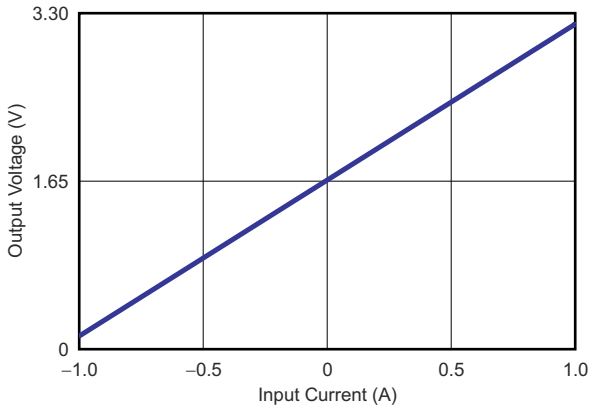


图 8-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

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9 Power Supply Recommendations

The OPAx392 are specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.75 V).

CAUTION

Exceeding supply voltages listed in the *Absolute Maximum Ratings* table can permanently damage the device.

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short, and when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by making sure these potentials are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Use guard traces to minimize leakage current when ultra-low bias current is required.
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher, depending on materials used.

10.2 Layout Example

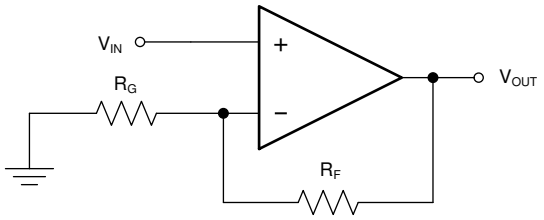


图 10-1. OPA392 Layout Schematic

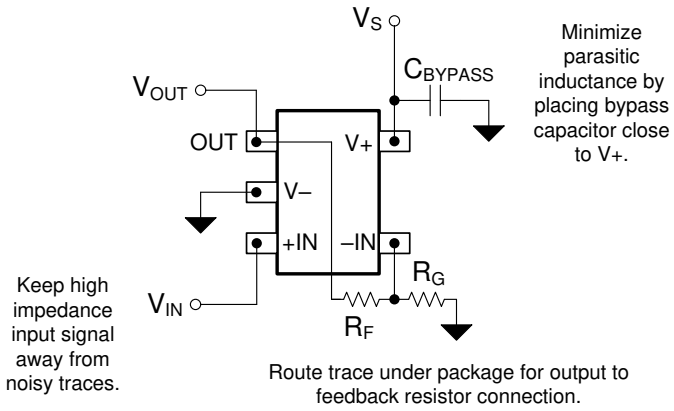


图 10-2. OPA392 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI™ folder.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA392DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23GT	Samples
OPA392DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23GT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

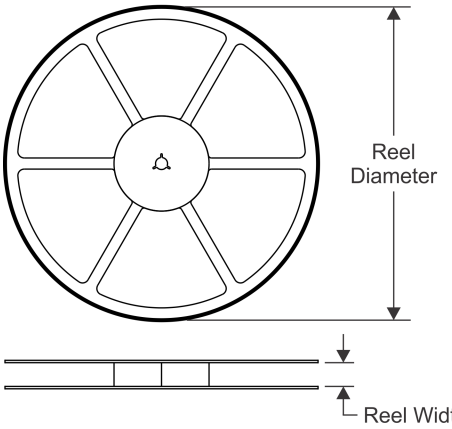
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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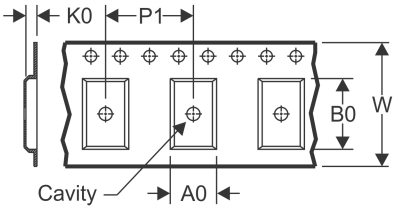
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

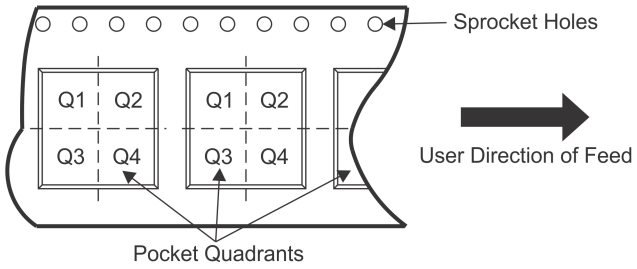


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

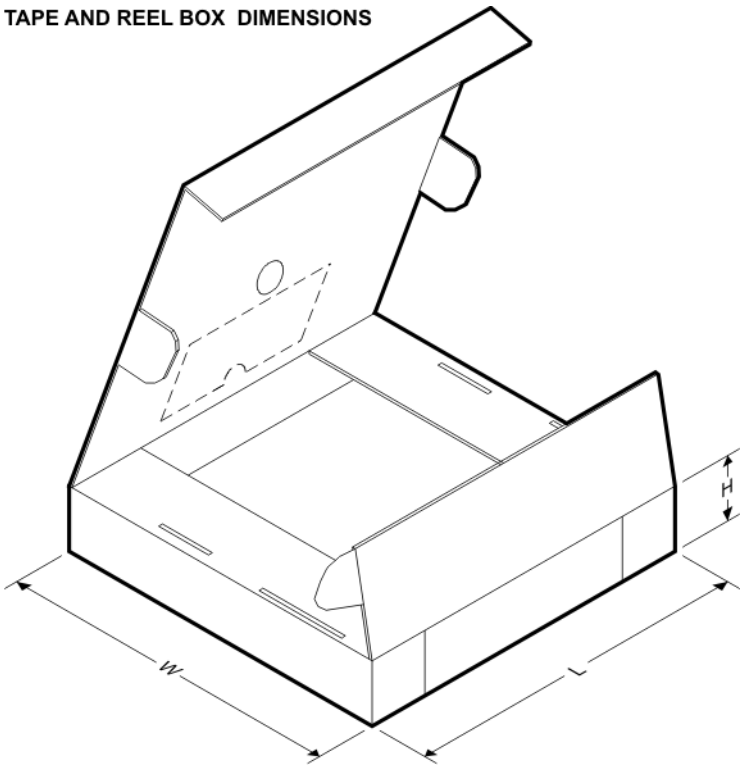
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA392DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA392DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

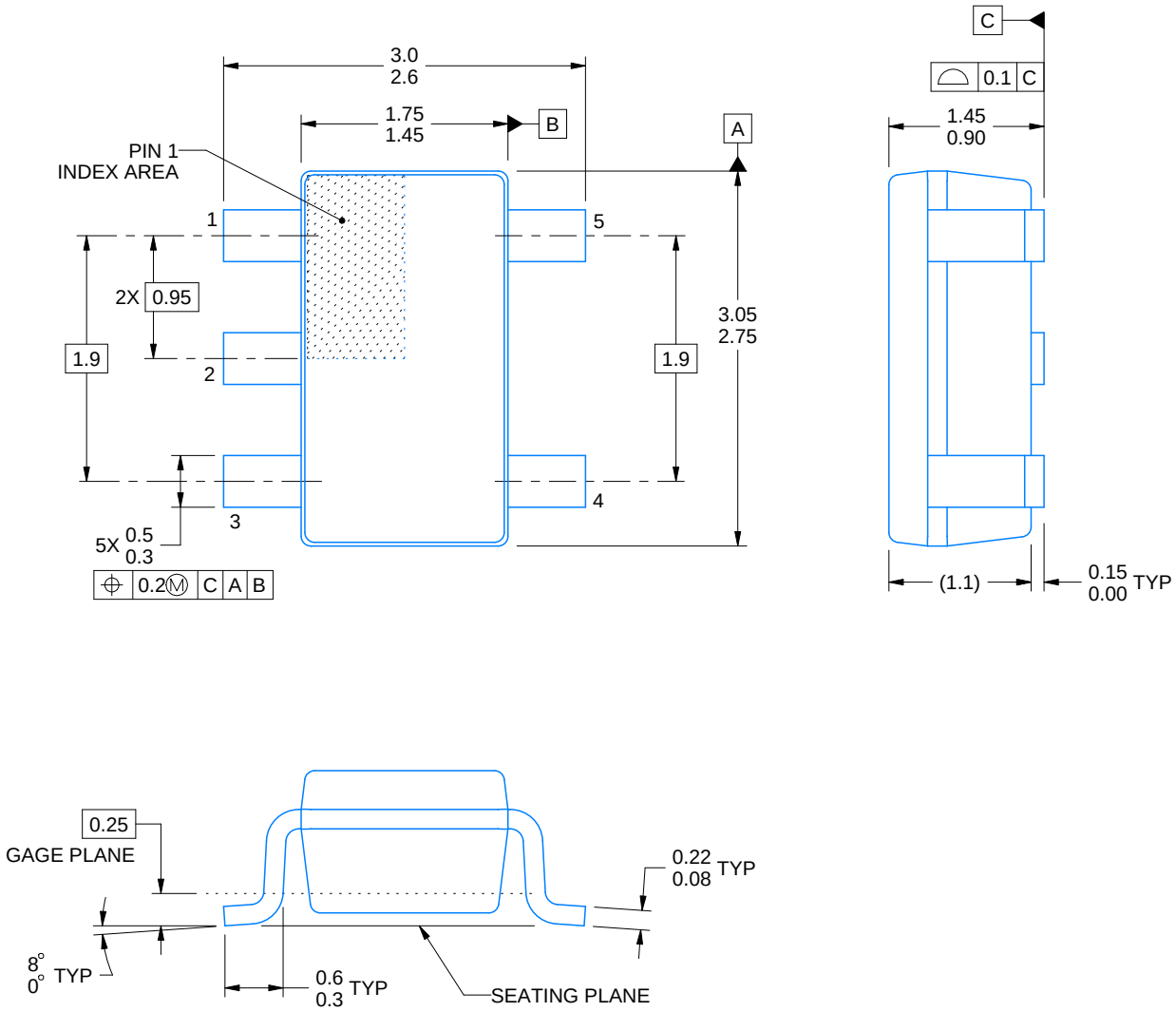
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA392DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA392DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

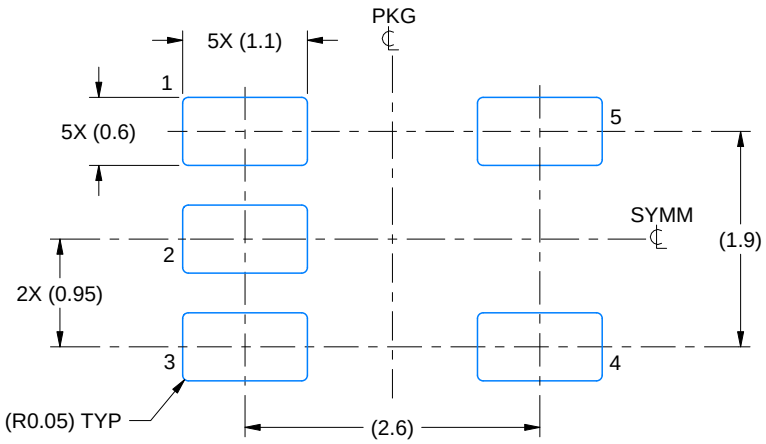
SMALL OUTLINE TRANSISTOR



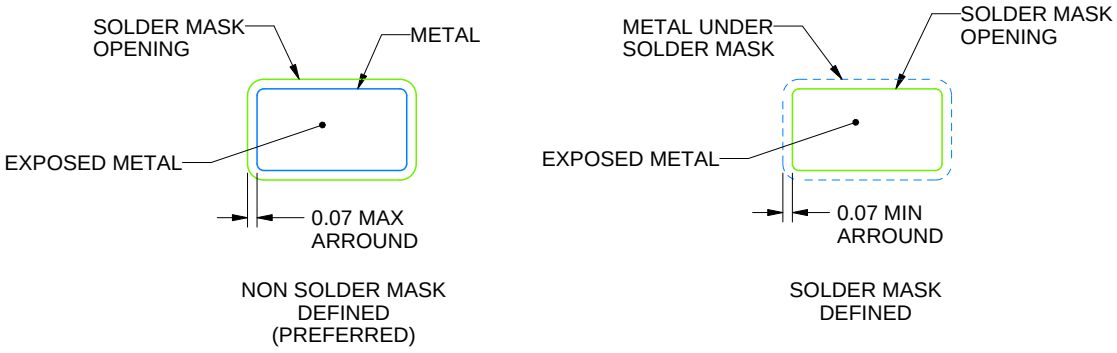
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

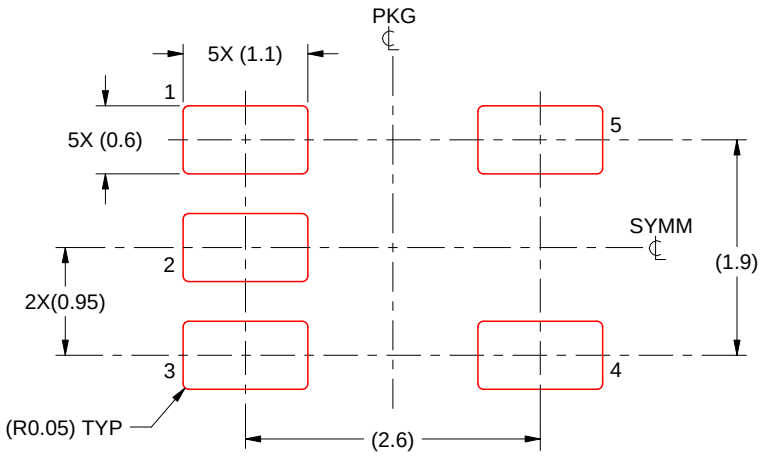


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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