OPA627 and OPA637 Precision High-Speed Difet® Operational Amplifiers

1 Features

- Very Low Noise: 4.5 nV/√Hz at 10 kHz
- Fast Settling Time:
  - OPA627—550 ns to 0.01%
  - OPA637—450 ns to 0.01%
- Low V_{OS}: 100-µV maximum
- Low Drift: 0.8-µV/°C maximum
- Low I_B: 5-pA maximum
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

2 Applications

- Precision Instrumentation
- Fast Data Acquisition
- DAC Output Amplifier
- Optoelectronics
- Sonar, Ultrasound
- High-Impedance Sensor Amps
- High-Performance Audio Circuitry
- Active Filters

3 Description

The OPA6x7 Difet® operational amplifiers provide a new level of performance in a precision FET operational amplifier. When compared to the popular OPA111 operational amplifier, the OPA6x7 has lower noise, lower offset voltage, and higher speed. The OPA6x7 is useful in a broad range of precision and high speed analog circuitry.

The OPA6x7 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage of ±4.5 V to ±18 V. Laser-trimmed Difet input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input operational amplifiers.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET operational amplifiers. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

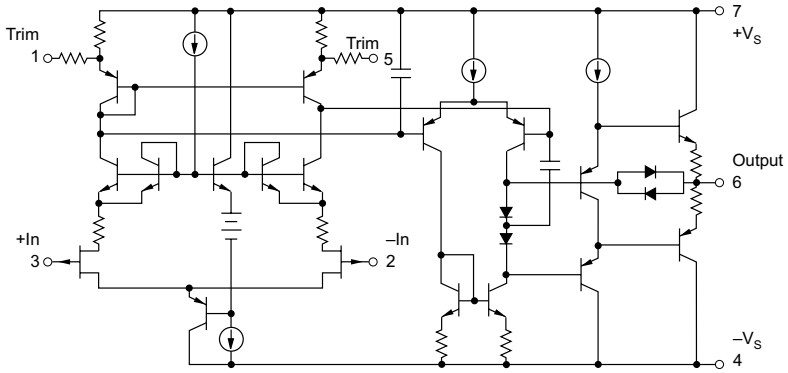
The OPA6x7 is available in plastic PDIP, SOIC, and metal TO-99 packages. Industrial and military temperature range models are available.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA627 OPA637	SOIC (8)	3.91 mm × 4.9 mm
	PDIP (8)	6.35 mm × 9.81 mm
	TO-99 (8)	8.95 mm (metal can diameter)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

OPA627 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

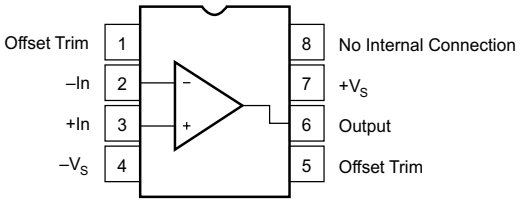
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2000) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Removed Lead Temperature from Absolute Maximum Ratings table.	3

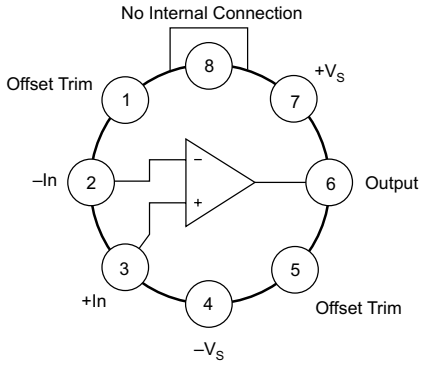
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5 Pin Configuration and Functions

P and D Packages
8-Pin PDIP and SOIC
Top View



LMC Package
8-Pin TO-99
Top View



Case connected to $-V_S$.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Offset Trim	—	Input offset voltage trim (leave floating if not used)
2	–In	I	Inverting input
3	+In	I	Noninverting input
4	$-V_S$	—	Negative (lowest) power supply
5	Offset Trim	—	Input offset voltage trim (leave floating if not used)
6	Output	O	Output
7	$+V_S$	—	Positive (highest) power supply
8	NC	—	No internal connection (can be left floating)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage			±18	V
Input Voltage Range		$+V_S + 2$	$-V_S - 2$	V
Differential Input			Total $V_S + 4$	V
Power Dissipation			1000	mW
Operating Temperature	LMC Package	–55	125	°C
	P, D Package	–40	125	
Junction Temperature	LMC Package		175	°C
	P, D Package		150	
Storage temperature, T_{stg}	LMC Package	–65	150	°C
	P, D Package	–40	125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

			VALUE	UNIT
OPA627 and OPA637 in PDIP and SOIC Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
OPA627 and OPA637 in SOIC Packages				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) - (V-)		9 (±4.5)	30 (±15)	36 (±18)	V
Specified temperature	P and D packages	–25	25	85	°C
	LMC package	–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		OPA627, OPA637			UNIT
		P (DIP)	D (SOIC)	LMC (TO-99)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.2	107.9	200	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.5	57.3	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	49.7	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.7	11.7	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.3	48.9	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE(1)							
Input offset voltage	BM, SM grades				40	100	µV
	AM grade				130	250	
	BP grade				100	250	
	AP, AU grades				280	500	
Average drift	BM, SM grades				0.4	0.8	µV/°C
	AM grade				1.2	2	
	BP grade				0.8	2	
	AP, AU grades				2.5		
Power supply rejection	V_S = ±4.5 to ±18 V	BM, BP, SM grades		106	120		dB
		AM, AP, AU grades		100	116		
INPUT BIAS CURRENT(2)							
Input bias current	V_{CM} = 0 V	T_A = 25°C	BM, BP, SM grades		1	5	pA
			AM, AP, AU grades		2	10	
		Over specified temperature	BM, BP grades			1	nA
			SM grade			50	
			AM, AP, AU grades			2	
	V_{CM} = ±10 V, over common-mode voltage		BM, BP, SM grades		1		pA
			AM, AP, AU grades		2		
Input offset current	V_{CM} = 0 V	T_A = 25°C	BM, BP, SM grades		0.5	5	pA
			AM, AP, AU grades		1	10	
		Over specified temperature	BM, BP grades			1	nA
			SM grade			50	
			AM, AP, AU grades			2	
NOISE							
Input voltage noise density	f = 10 Hz	BM, BP, SM grades			15	40	nV/√Hz
		AM, AP, AU grades			20		
	f = 100 Hz	BM, BP, SM grades			8	20	
		AM, AP, AU grades			10		
	f = 1 kHz	BM, BP, SM grades			5.2	8	
		AM, AP, AU grades			5.6		
	f = 10 kHz	BM, BP, SM grades			4.5	6	
		AM, AP, AU grades			4.8		
Input voltage noise	BW = 0.1 Hz to 10 Hz	BM, BP, SM grades			0.6	1.6	µVp-p
		AM, AP, AU grades			0.8		
Input bias-current noise density	f = 100 Hz	BM, BP, SM grades			1.6	2.5	fA/√Hz
		AM, AP, AU grades			2.5		
Input bias-current noise	BW = 0.1 Hz to 10 Hz	BM, BP, SM grades			30	60	fAp-p
		AM, AP, AU grades			48		
INPUT IMPEDANCE							
Differential					10^{13} || 8		Ω || pF
Common-mode					10^{13} || 7		Ω || pF
INPUT VOLTAGE RANGE							
Common-mode input range	T_A = 25°C			±11	±11.5		V
	Over specified temperature			±10.5	±11		
Common-mode rejection	V_{CM} = ±10.5 V	BM, BP, SM grades		106	116		dB
		AM, AP, AU grades		100	110		

(1) Offset voltage measured fully warmed-up.
(2) High-speed test at T_J = 25°C. See Typical Characteristics for warmed-up performance.

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Electrical Characteristics (continued)

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
Open-loop voltage gain	V_O = ±10 V, R_L = 1kΩ	T_A = 25°C	BM, BP, SM grades	112	120		dB
			AM, AP, AU grades	106	116		
		Over specified temperature	BM, BP grades	106	117		
			SM grade	100	114		
			AM, AP, AU grades	100	110		
FREQUENCY RESPONSE							
Slew rate	G = –1, 10-V step, OPA627			40	55		V/µs
	G = –4, 10-V step, OPA637			100	135		
Settling time	G = –1, 10-V step, OPA627	0.01%			550		ns
		0.1%			450		
	G = –4, 10-V step, OPA637	0.01%			450		
		0.1%			300		
Gain-bandwidth product	G = 1, OPA627				16		MHz
	G = 10, OPA637				80		
Total harmonic distortion + noise	G = 1, f = 1 kHz				0.00003%		
POWER SUPPLY							
Specified operating voltage					±15		V
Operating voltage range				±4.5		±18	V
Current					±7	±7.5	mA
OUTPUT							
Voltage output	**R_L = 1 kΩ**			±11.5	±12.3		V
	Over specified temperature			±11	±11.5		
Current output	V_O = ±10 V				±45		mA
Short-circuit current				±35	±70/–55	±100	mA
Output impedance, open-loop	1 MHz				55		Ω
TEMPERATURE RANGE							
Temperature range specification	AP, BP, AM, BM, AU grades			–25		85	°C
	SM grade			–55		125	

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6.6 Typical Characteristics

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

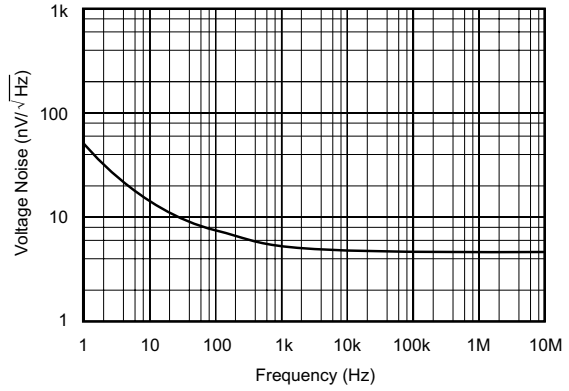


Figure 1. Input Voltage Noise Spectral Density vs Frequency

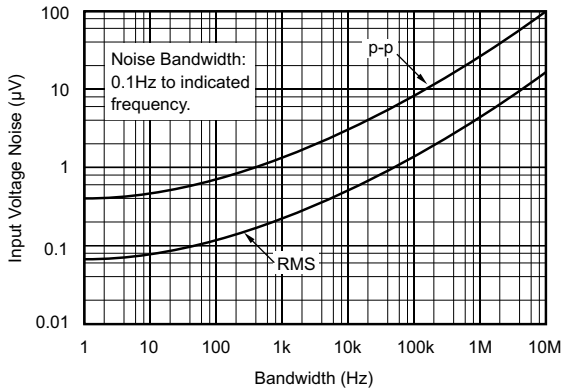


Figure 2. Total Input Voltage Noise vs Bandwidth

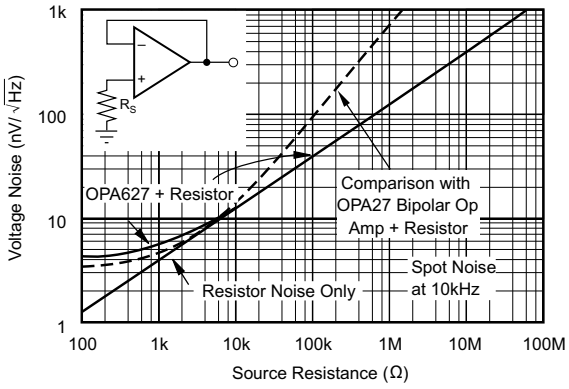


Figure 3. Voltage Noise vs Source Resistance

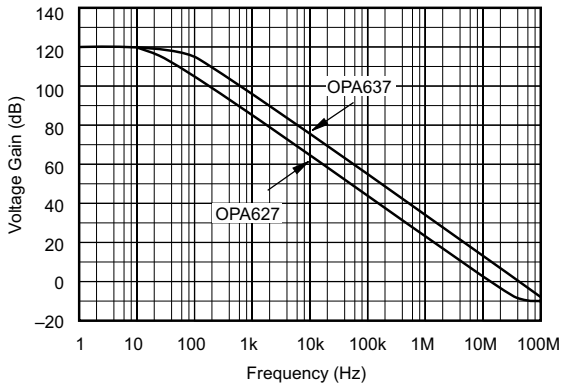


Figure 4. Open-Loop Gain vs Frequency

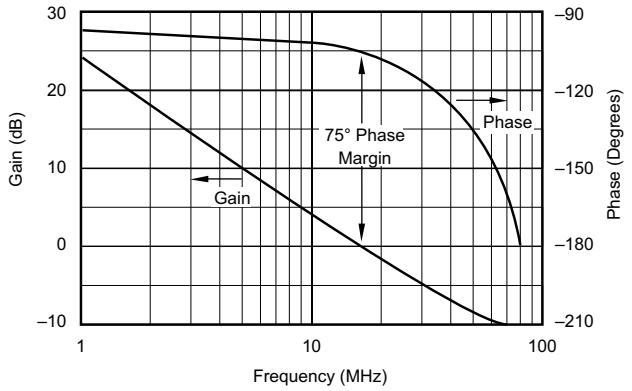


Figure 5. OPA627 Gain/Phase vs Frequency

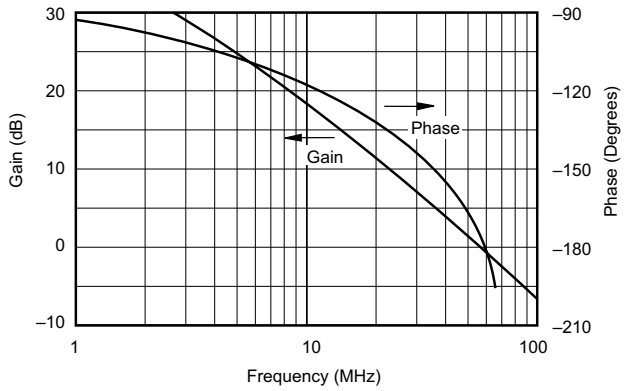


Figure 6. OPA637 Gain/Phase vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

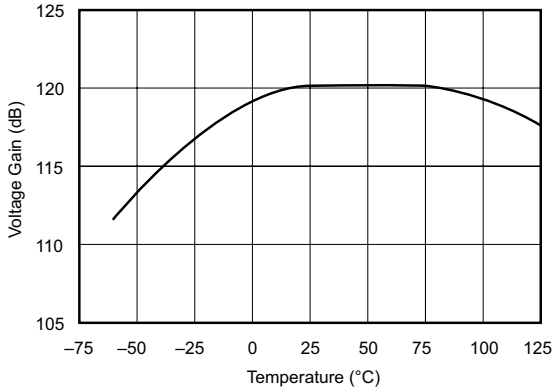


Figure 7. Open-Loop Gain vs Temperature

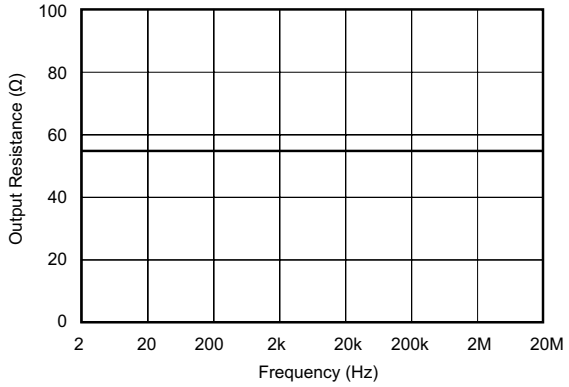


Figure 8. Open-Loop Output Impedance vs Frequency

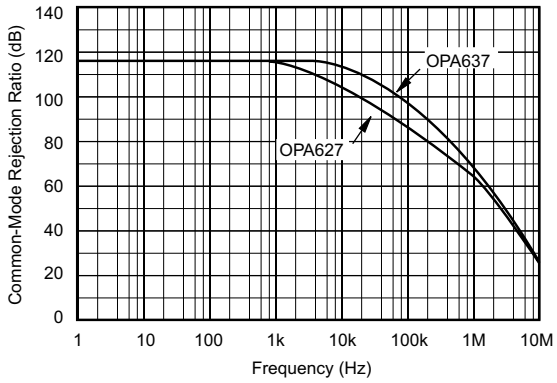


Figure 9. Common-Mode Rejection vs Frequency

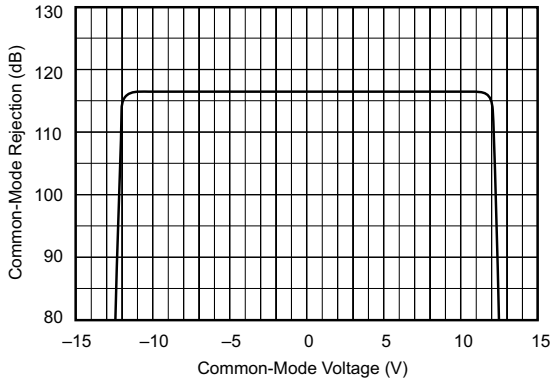


Figure 10. Common-Mode Rejection vs Input Common-Mode Voltage

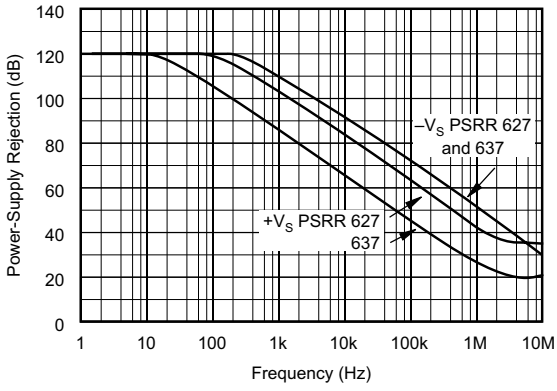


Figure 11. Power-Supply Rejection vs Frequency

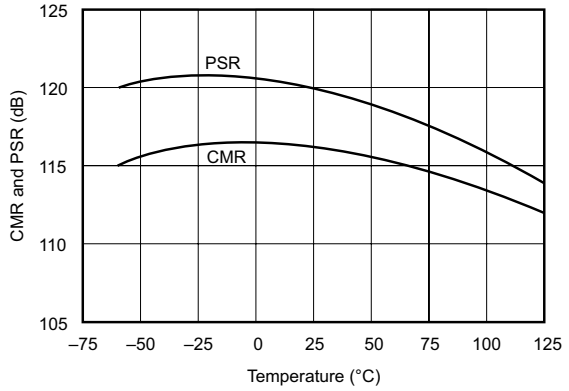


Figure 12. Power-Supply Rejection and Common-Mode Rejection vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

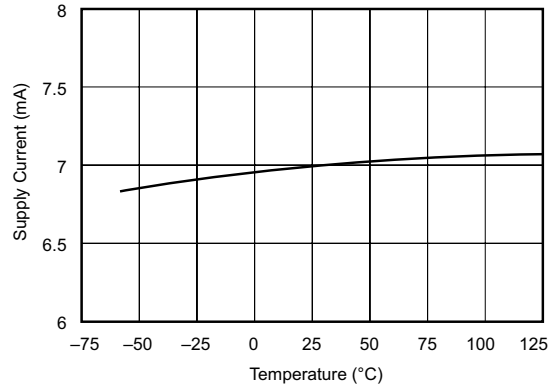


Figure 13. Supply Current vs Temperature

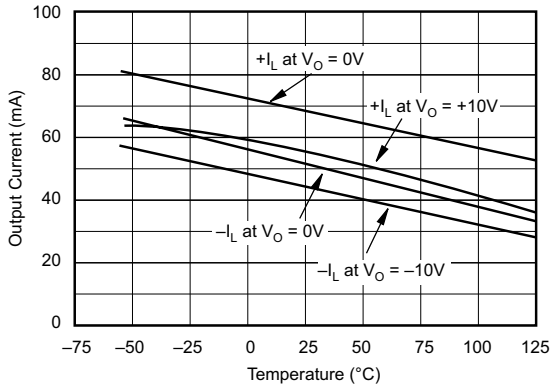


Figure 14. Output Current Limit vs Temperature

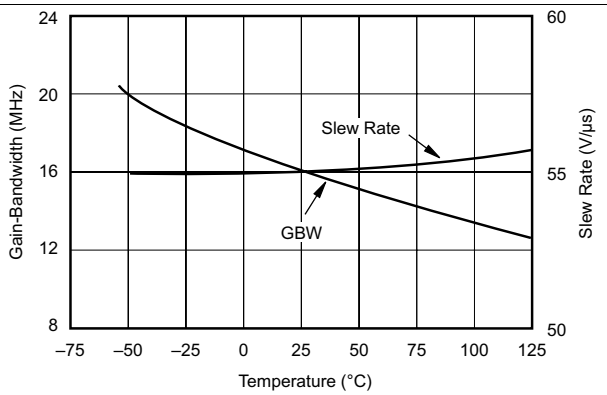


Figure 15. OPA627 Gain-Bandwidth and Slew Rate vs Temperature

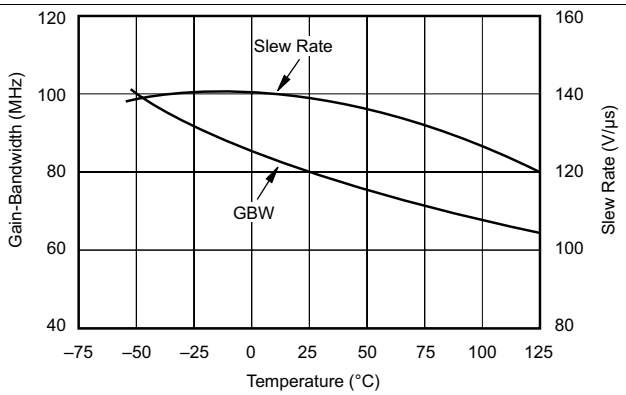


Figure 16. OPA637 Gain-Bandwidth and Slew Rate vs Temperature

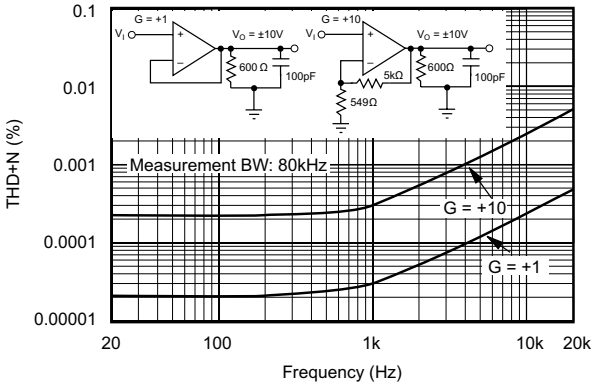


Figure 17. OPA627 Total Harmonic Distortion + Noise vs Frequency

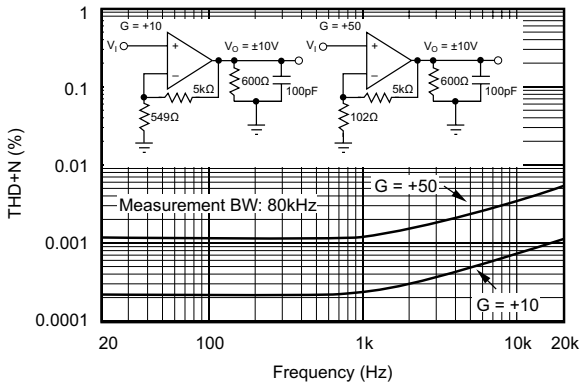


Figure 18. OPA637 Total Harmonic Distortion + Noise vs Frequency

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Typical Characteristics (continued)

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

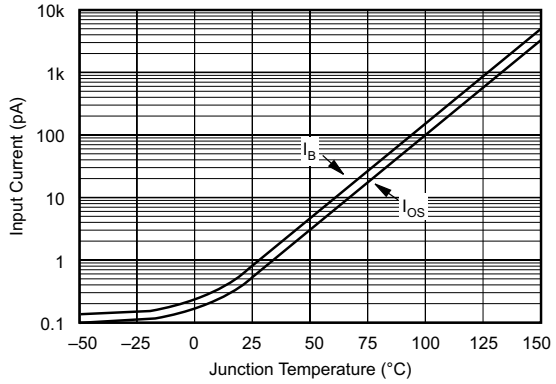


Figure 19. Input Bias and Offset Current vs Junction Temperature

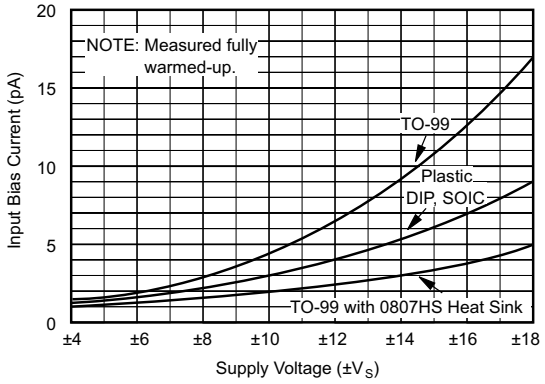


Figure 20. Input Bias Current vs Power Supply Voltage

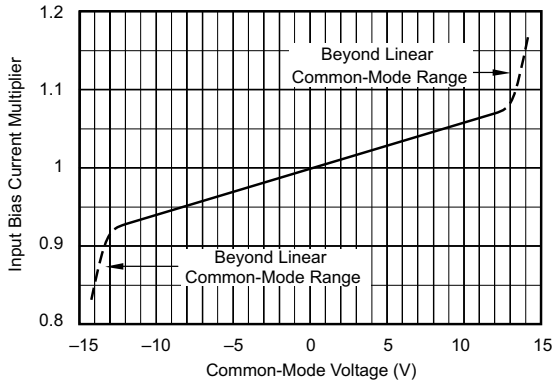


Figure 21. Input Bias Current vs Common-Mode Voltage

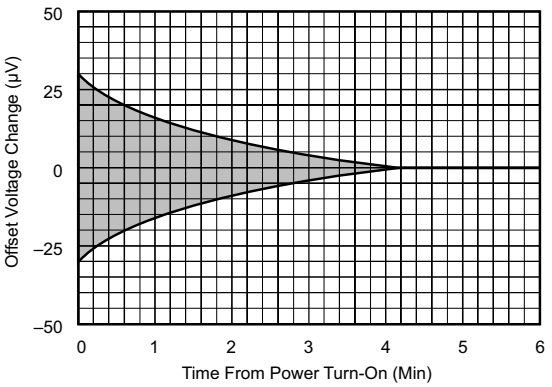


Figure 22. Input Offset Voltage Warm-up vs Time

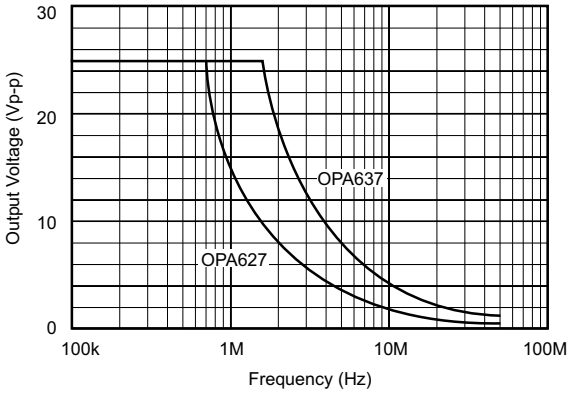


Figure 23. Maximum Output Voltage vs Frequency

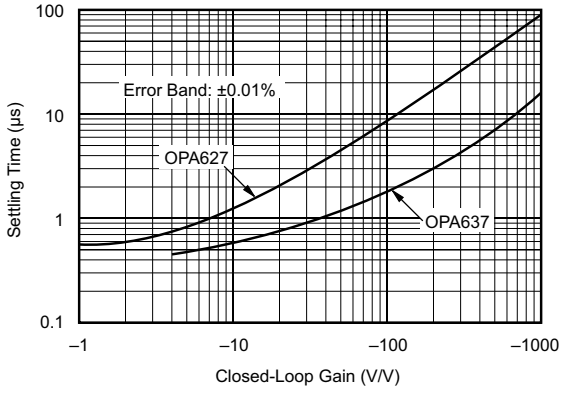


Figure 24. Settling Time vs Closed-Loop Gain

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Typical Characteristics (continued)

At T_A = 25°C, and V_S = ±15 V, unless otherwise noted.

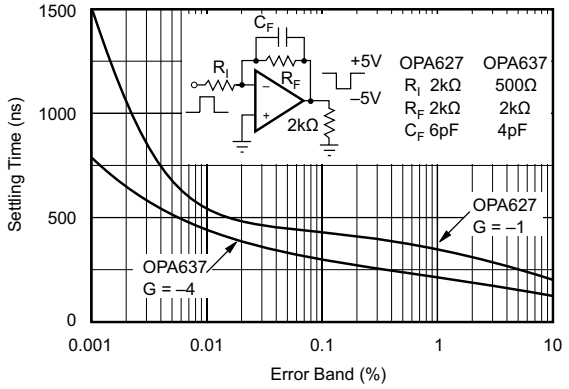


Figure 25. Settling Time vs Error Band

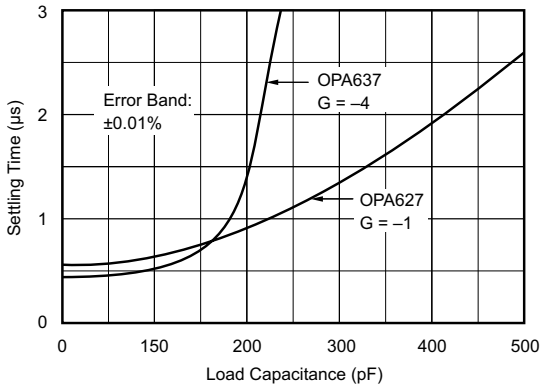


Figure 26. Settling Time vs Load Capacitance

7 Detailed Description

7.1 Overview

The OPA6x7 Difet operational amplifiers provide a new level of performance in a precision FET operational amplifier. When compared to the popular OPA111 operational amplifier, the OPA6x7 has lower noise, lower offset voltage, and higher speed. The OPA6x7 is useful in a broad range of precision and high speed analog circuitry.

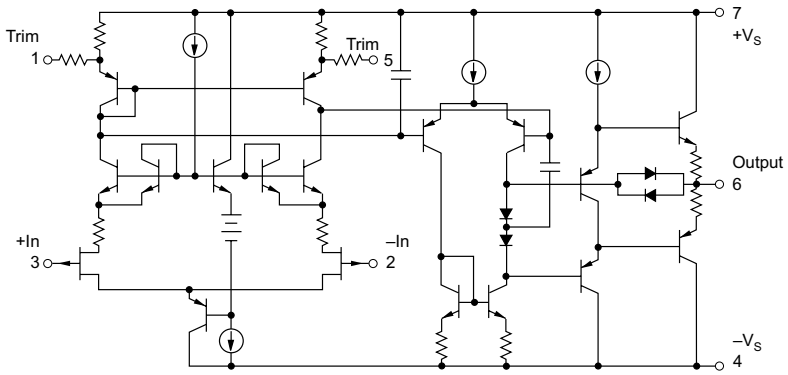
The OPA6x7 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage of ±4.5 V to ±18 V. Laser-trimmed Difet input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input operational amplifiers.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET operational amplifiers. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA6x7 is available in plastic PDIP, SOIC, and metal TO-99 packages. Industrial and military temperature range models are available.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA627 is unity-gain stable. The OPA637 may achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit, as if the noninverting operational amplifier input were being driven. For example, the OPA637 may be used in a noninverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (see Figure 27) place the operational amplifier in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 28, where a small feedback capacitance is used to compensate for the input capacitance at the inverting input of the operational amplifier. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

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Feature Description (continued)

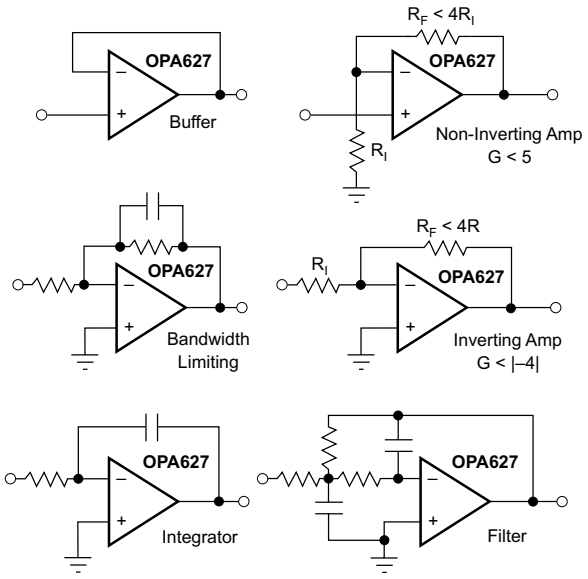


Figure 27. Circuits With Noise Gain Less Than Five Require the OPA627 for Proper Stability

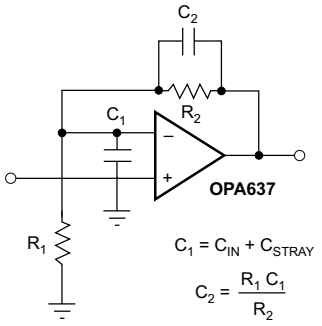


Figure 28. Circuits With Noise Gain Equal to or Greater Than Five May Use the OPA637

7.3.1 Offset Voltage Adjustment

The OPA6x7 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 29 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter), because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately 4 µV/°C for 1 mV of change in the offset voltage due to an offset adjustment (as shown in Figure 29).

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Feature Description (continued)

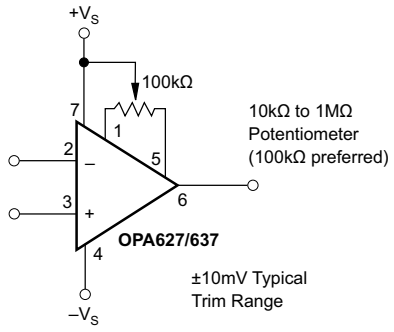


Figure 29. Optional Offset Voltage Trim Circuit

7.3.2 Noise Performance

Some bipolar operational amplifiers may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA6x7 provides both low voltage noise and low current noise. This provides optimum noise performance over a wide range of sources, including reactive-source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2-kΩ source resistance, the operational amplifier contributes little additional noise. Below 1 kΩ, operational amplifier noise dominates over the resistor noise, but compares favorably with precision bipolar operational amplifiers.

7.3.3 Input Bias Current

Difet fabrication of the OPA6x7 provides low input bias current. Because the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, keep the die temperature as low as possible. The high speed, and therefore higher quiescent current, of the OPA6x7 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic PDIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces also help dissipate heat.

The OPA6x7 may also be operated at reduced power supply voltage, to minimize power dissipation and temperature rise. Using ±5-V power supplies reduces power dissipation to one-third of that at ±15 V. This reduces the I_B of TO- 99 metal package devices to approximately one-fourth the value at ±15 V.

Leakage currents between printed-circuit-board traces can easily exceed the input bias current of the OPA6x7. A circuit board *guard* pattern (see Figure 30) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case (TO-99 metal package only) is internally connected to $–V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input operational amplifiers exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA6x7 virtually constant with wide common-mode voltage changes. This is ideal for accurate, high input-impedance buffer applications.

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Feature Description (continued)

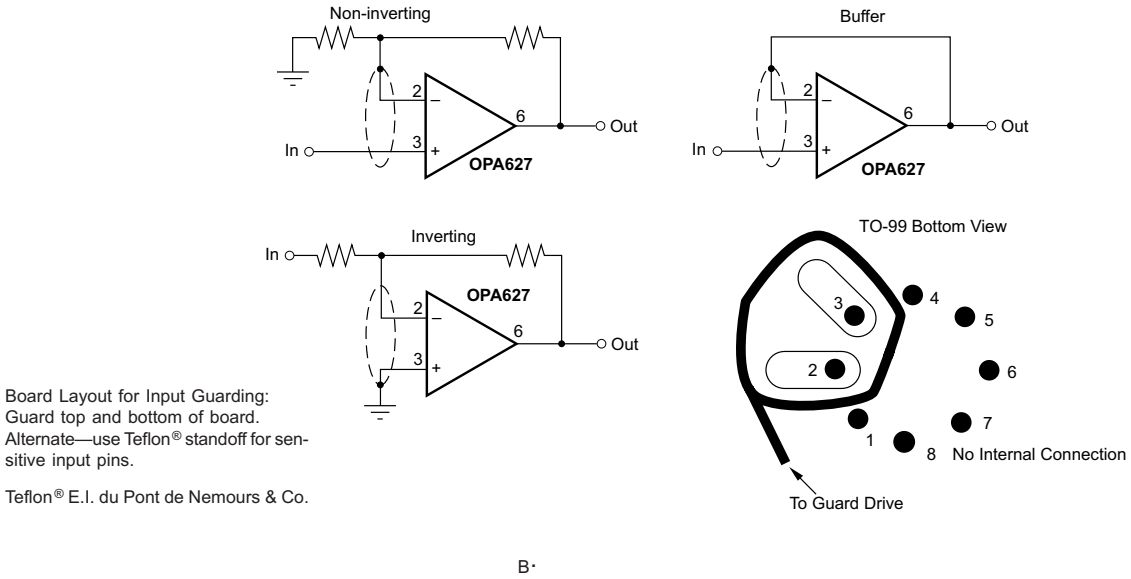


Figure 30. Connection of Input Guard for Lowest I_B

7.3.4 Phase-Reversal Protection

The OPA6x7 has internal phase-reversal protection. Many FET-input operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in noninverting circuits when the input is driven below –12 V, causing the output to reverse into the positive rail. The input circuitry of the OPA6x7 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

7.3.5 Output Overload

When the inputs to the OPA6x7 are overdriven, the output voltage of the OPA6x7 smoothly limits at approximately 2.5 V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500 ns. When the output is driven into the positive limit, recovery takes approximately 6 µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 31. Placing diodes at the inverting input prevent degradation of input bias current.

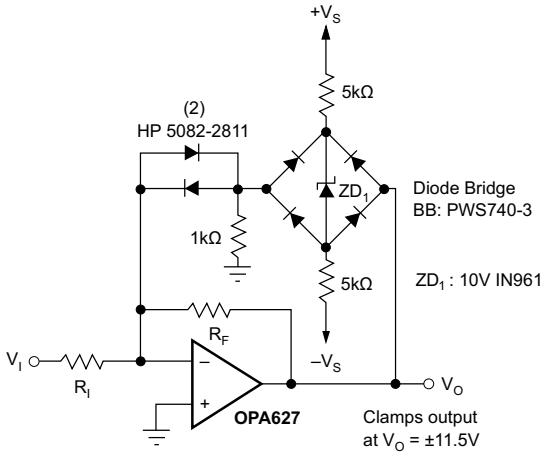


Figure 31. Clamp Circuit for Improved Overload Recovery

Feature Description (continued)

7.3.6 Capacitive Loads

As with any high-speed operational amplifier, best dynamic performance can be achieved by minimizing the capacitive load. Because a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow operational amplifier can cause a high-speed operational amplifier to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 32 shows a circuit for driving very large load capacitance. The two-pole response of this circuit can also be used to sharply limit system bandwidth, often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

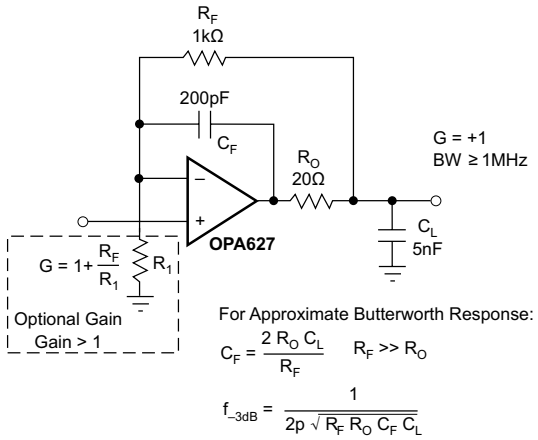


Figure 32. Driving Large Capacitive Loads

7.3.7 Input Protection

The inputs of the OPA6x7 are protected for voltages from $+V_S$ + 2 V to $–V_S$ – 2 V. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in (a) in Figure 33 prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies, which is well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input increases noise. The 4-nV/√Hz theoretical thermal noise of a 1-kΩ resistor will add to the 4.5-nV/√Hz noise of the OPA6x7 (by the square-root of the sum of the squares), producing a total noise of 6 nV/√Hz. Resistors less than 100 Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25 nA, more than a thousand times larger than the input bias current of the OPA6x7. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1 pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers; see (b) in Figure 33. Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), and large input transients may cause this node to exceed 2 V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Because the reverse voltage on these diodes is clamped, a diode-connected signal transistor can act as an inexpensive low leakage diode; see (b) in Figure 33.

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Feature Description (continued)

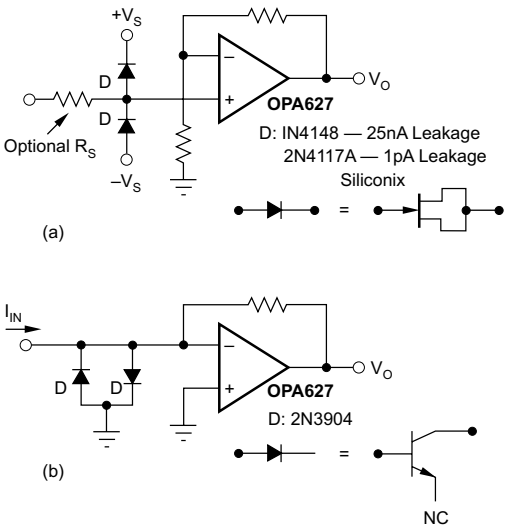


Figure 33. Input Protection Circuits

7.3.8 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download at www.ti.com.

The EMIRR IN+ of the OPA627 is plotted versus frequency as shown in Figure 34. If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA627 unity-gain bandwidth is 16 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

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Feature Description (continued)

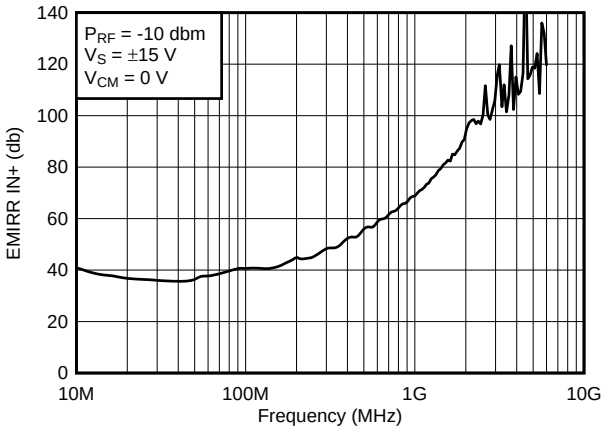


Figure 34. OPA627 EMIRR IN+ vs Frequency

Table 1 shows the EMIRR IN+ values for the OPA627 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA627 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION / ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	46.2 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	60.3 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	81 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio/satellite, S-band	96.9 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	108.9 dB
5 Ghz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	116.8 dB

7.3.8.1 EMIRR IN+ Test Configuration

Figure 35 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy. Refer to SBOA128 for more details.

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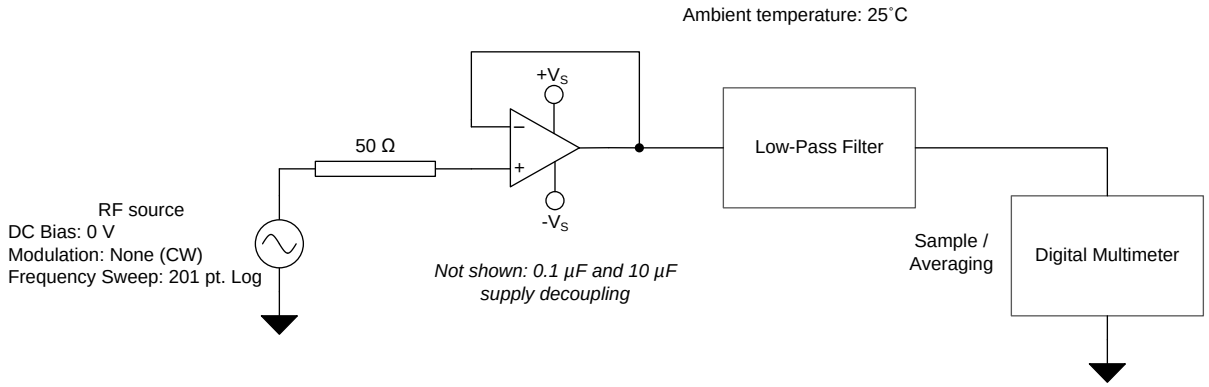
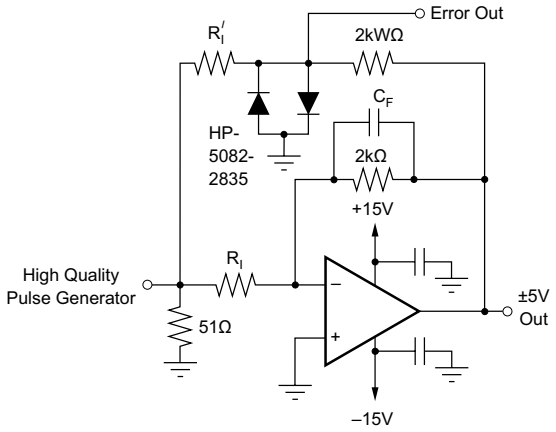


Figure 35. EMIRR IN+ Test Configuration Schematic

7.4 Settling Time

The OPA627 and OPA637 have fast settling times, as low as 300 ns. Figure 36 illustrates the circuit used to measure settling time for the OPA627 and OPA637.



	OPA627	OPA637
R_I, R_1'	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimum value is determined, a fixed capacitor may be used.

Figure 36. Settling Time and Slew Rate Test Circuit

7.5 Device Functional Modes

The OPA627 and OPA6377 have a single functional mode and are operational when the power-supply voltage is greater than 9V (±4.5 V). The maximum power supply voltage for the OPA627 and OPA637 are 36 V (±18 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA627 and OPA637 are ideally suited to use as input amplifiers in instrumentation amplifier configurations requiring high speed, fast settling and high input impedance.

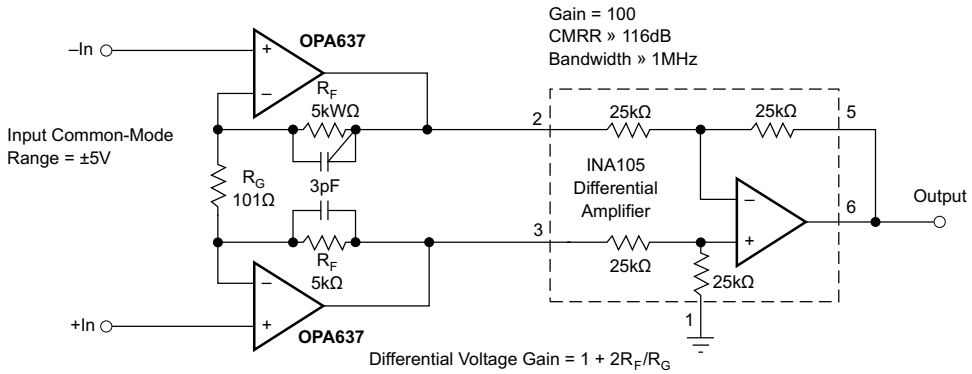


Figure 37. High Speed Instrumentation Amplifier, Gain = 100

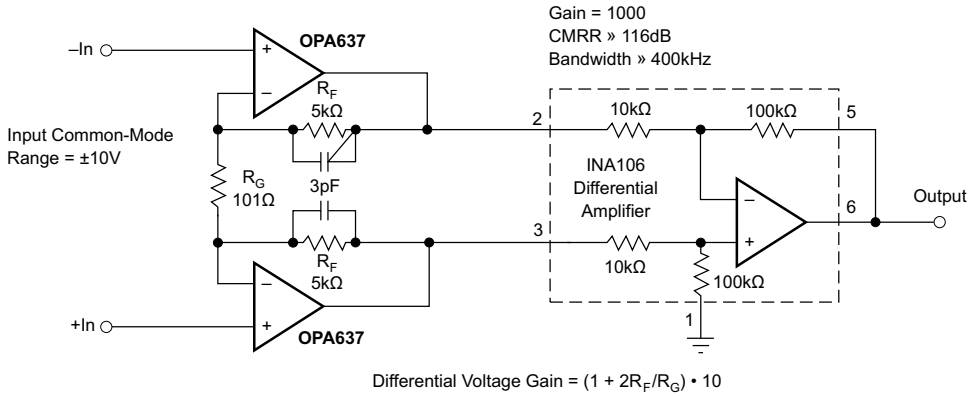
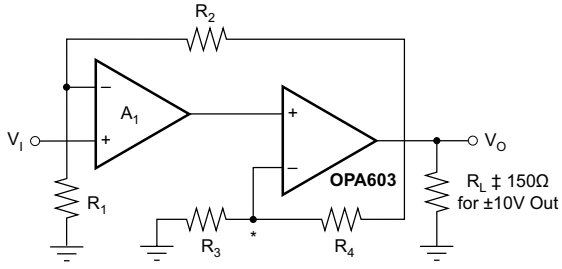


Figure 38. High Speed Instrumentation Amplifier, Gain = 1000



This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

∗Minimize capacitance at this node.

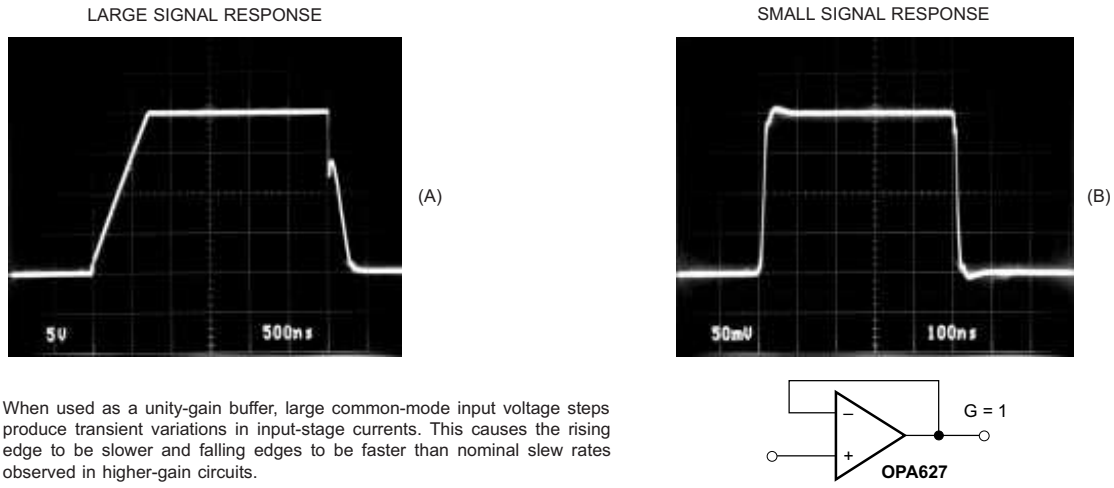
GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

Figure 39. Composite Amplifier for Wide Bandwidth

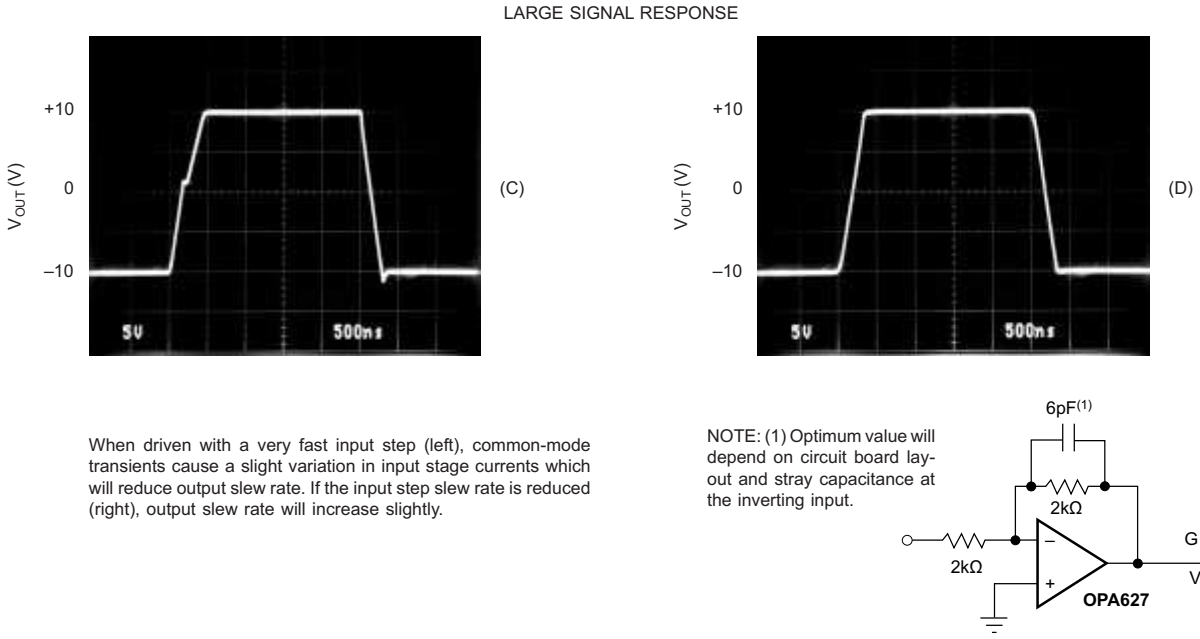
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Application Information (continued)



When used as a unity-gain buffer, large common-mode input voltage steps produce transient variations in input-stage currents. This causes the rising edge to be slower and falling edges to be faster than nominal slew rates observed in higher-gain circuits.

Figure 40. OPA627 Dynamic Performance, G = 1



When driven with a very fast input step (left), common-mode transients cause a slight variation in input stage currents which will reduce output slew rate. If the input step slew rate is reduced (right), output slew rate will increase slightly.

NOTE: (1) Optimum value will depend on circuit board lay-out and stray capacitance at the inverting input.

Figure 41. OPA627 Dynamic Performance, G = –1

Application Information (continued)

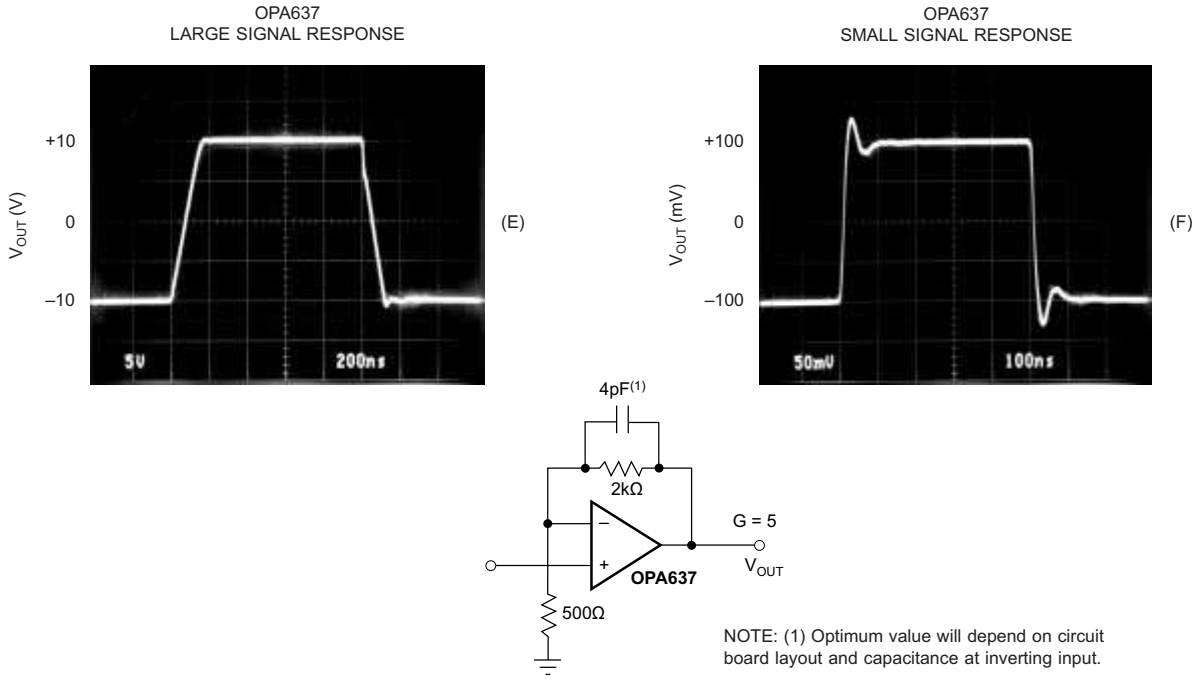


Figure 42. OPA637 Dynamic Response, G = 5

8.2 Typical Application

Low pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA627 and OPA637 are ideally suited to construct high speed, high precision active filters. Figure 43 illustrates a second order low pass filter commonly encountered in signal processing applications.

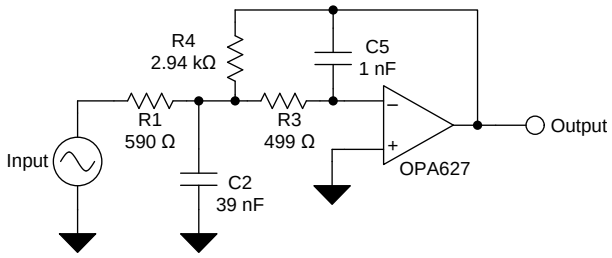


Figure 43. Second Order Low Pass Filter

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low pass cutoff frequency = 25 kHz
- Second order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 43. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

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Typical Application (continued)

This circuit produces a signal inversion. For this circuit the gain at DC and the low pass cutoff frequency can be calculated using Equation 2.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{\left(1/R_3R_4C_2C_5\right)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

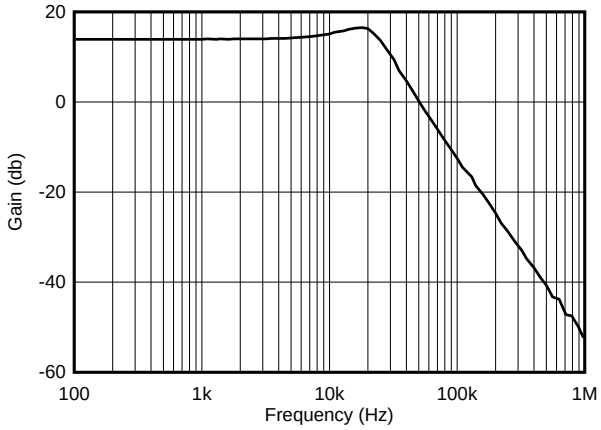


Figure 44. OPA627 2nd Order 25 kHz, Chebyshev, Low Pass Filter

9 Power Supply Recommendations

The OPA627 and OPA637 are specified for operation from 9 V to 36 V (±4.5 V to ±18 V); many specifications apply from –25°C to 85°C (P and D packages) and –55°C to 125°C (LMC package). Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

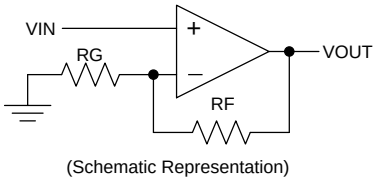
10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The OPA6x7 is capable of high-output current (in excess of 45 mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1-µF solid tantalum capacitors may improve dynamic performance in these applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 45, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- The case (TO-99 metal package only) is internally connected to the negative power supply, as with most common operational amplifiers.
- Pin 8 of the plastic PDIP, SOIC, and TO-99 packages has no internal connection.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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10.2 Layout Example



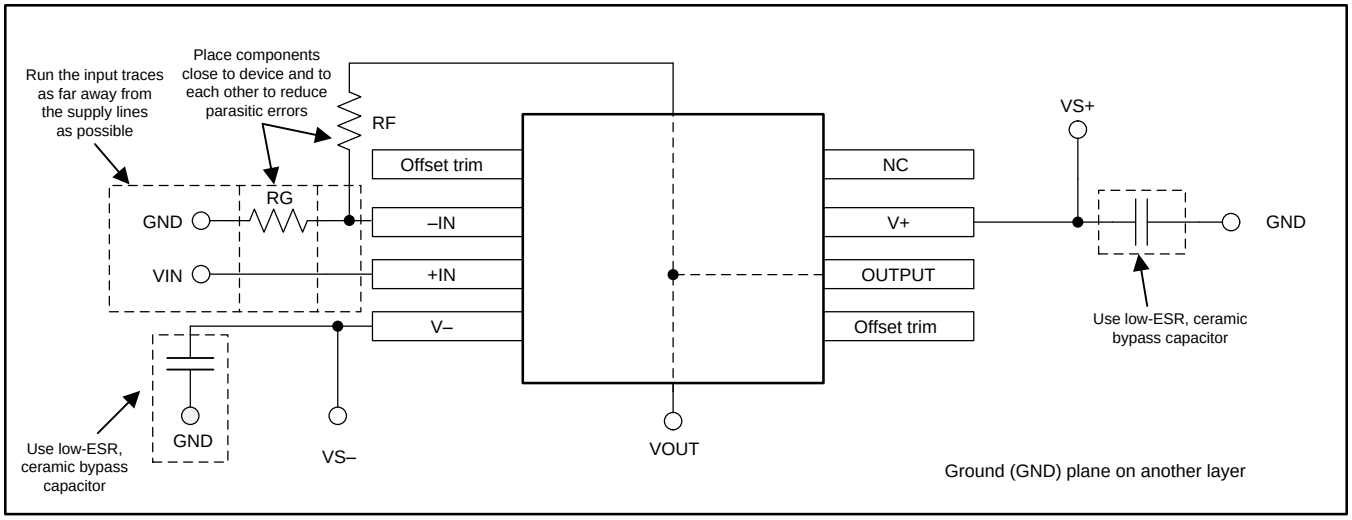


Figure 45. OPA627 Layout Example for the Noninverting Configuration

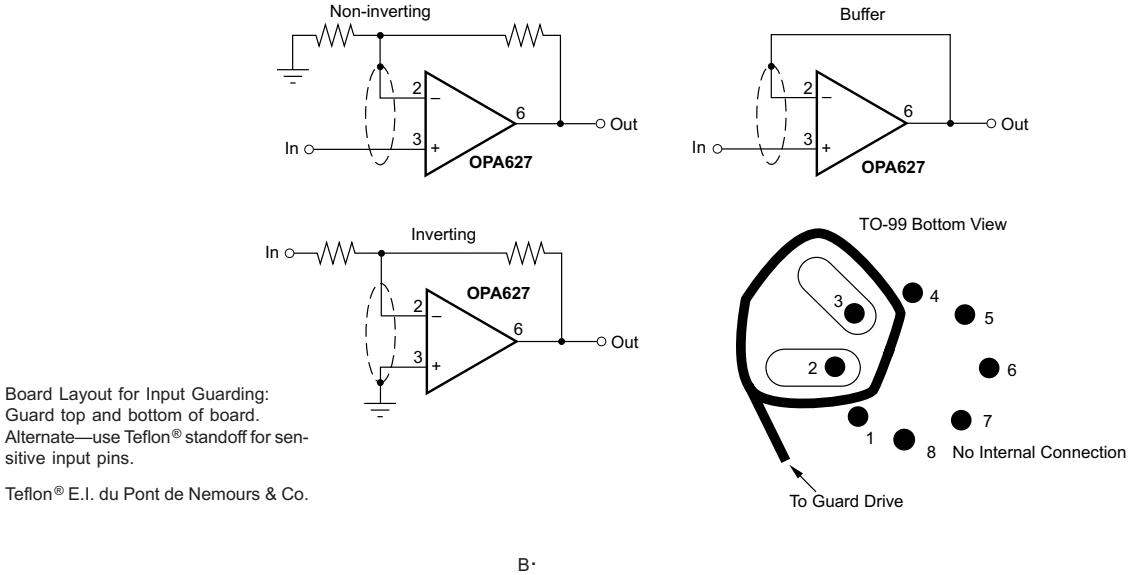


Figure 46. Board Layout for Input Guarding (LMC Package)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

The OPA627 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, SLOA089.
- *Op Amps for Everyone*, SLOD006.
- *Compensate Transimpedance Amplifiers Intuitively*, SBOS055.
- *Noise Analysis for High Speed op Amps*, SBOA066.

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA627	Click here	Click here	Click here	Click here	Click here
OPA637	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Difet is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

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11.4 Trademarks (continued)

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA627AM	NRND	TO-99	LMC	8	20	RoHS & Green	Call TI	N / A for Pkg Type		OPA627AM	
OPA627AP	NRND	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA627AP	
OPA627APG4	NRND	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA627AP	
OPA627AU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AU/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AUE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627BM	NRND	TO-99	LMC	8	1	RoHS & Green	Call TI	N / A for Pkg Type		OPA627BM	
OPA627BP	NRND	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA627BP	
OPA627SM	NRND	TO-99	LMC	8	20	RoHS & Green	AU	N / A for Pkg Type		OPA627SM	
OPA637AM	NRND	TO-99	LMC	8	20	RoHS & Green	Call TI	N / A for Pkg Type		OPA637AM	
OPA637AP	NRND	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA637AP	
OPA637AU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU	Samples
OPA637AU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU	Samples
OPA637AUG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	-25 to 85		Samples
OPA637BM	NRND	TO-99	LMC	8	20	RoHS & Green	Call TI	N / A for Pkg Type		OPA637BM	
OPA637BP	NRND	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA637BP	
OPA637BPG4	NRND	PDIP	P	8	50	TBD	Call TI	Call TI			
OPA637SM	NRND	TO-99	LMC	8	20	RoHS & Green	AU	N / A for Pkg Type		OPA637SM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

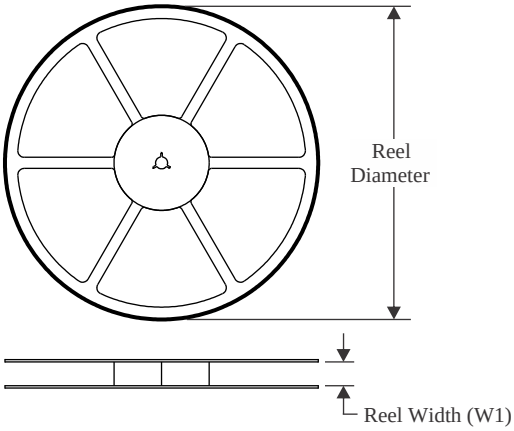
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

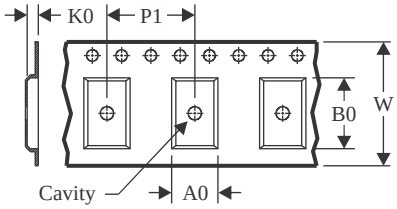
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

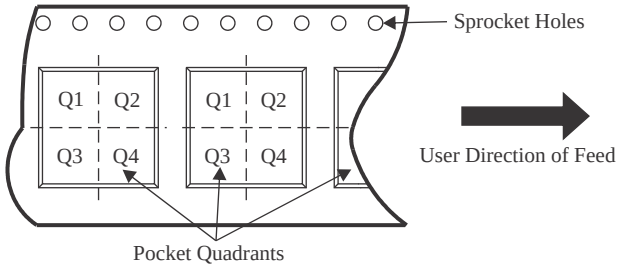


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

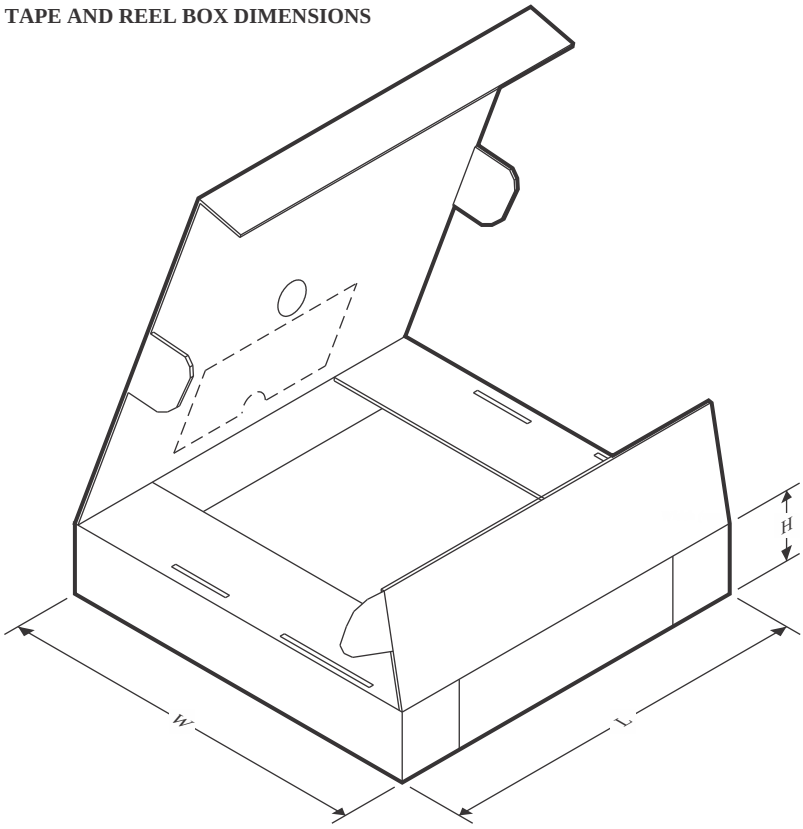
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA627AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA637AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

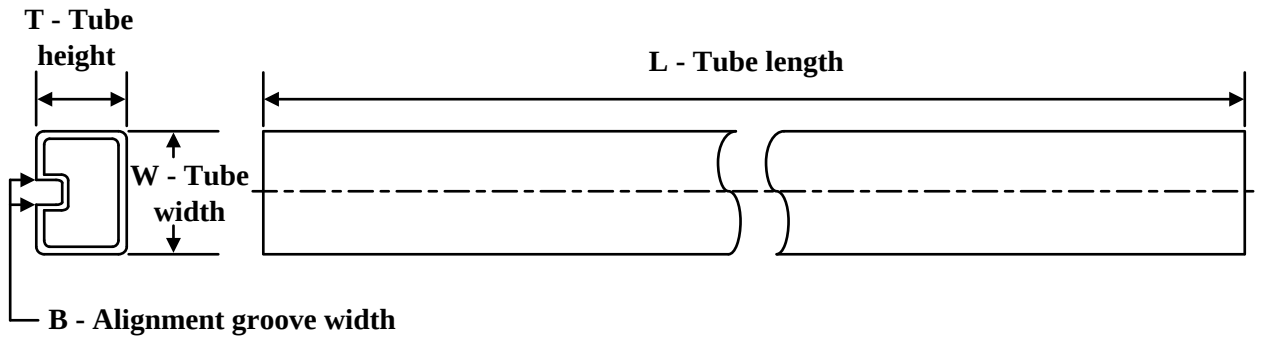
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

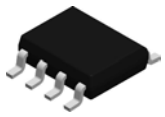
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA627AU/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA637AU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA627AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA627AP	P	PDIP	8	50	506.1	13.97	11230	NA
OPA627APG4	P	PDIP	8	50	506.1	13.97	11230	NA
OPA627AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA627AUE4	D	SOIC	8	75	506.6	8	3940	4.32
OPA627AUG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA627BM	LMC	TO-CAN	8	1	532.13	21.59	889	NA
OPA627BP	P	PDIP	8	50	506.1	13.97	11230	NA
OPA627SM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637AP	P	PDIP	8	50	506.1	13.97	11230	NA
OPA637AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA637BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637BP	P	PDIP	8	50	506.1	13.97	11230	NA
OPA637SM	LMC	TO-CAN	8	20	532.13	21.59	889	NA

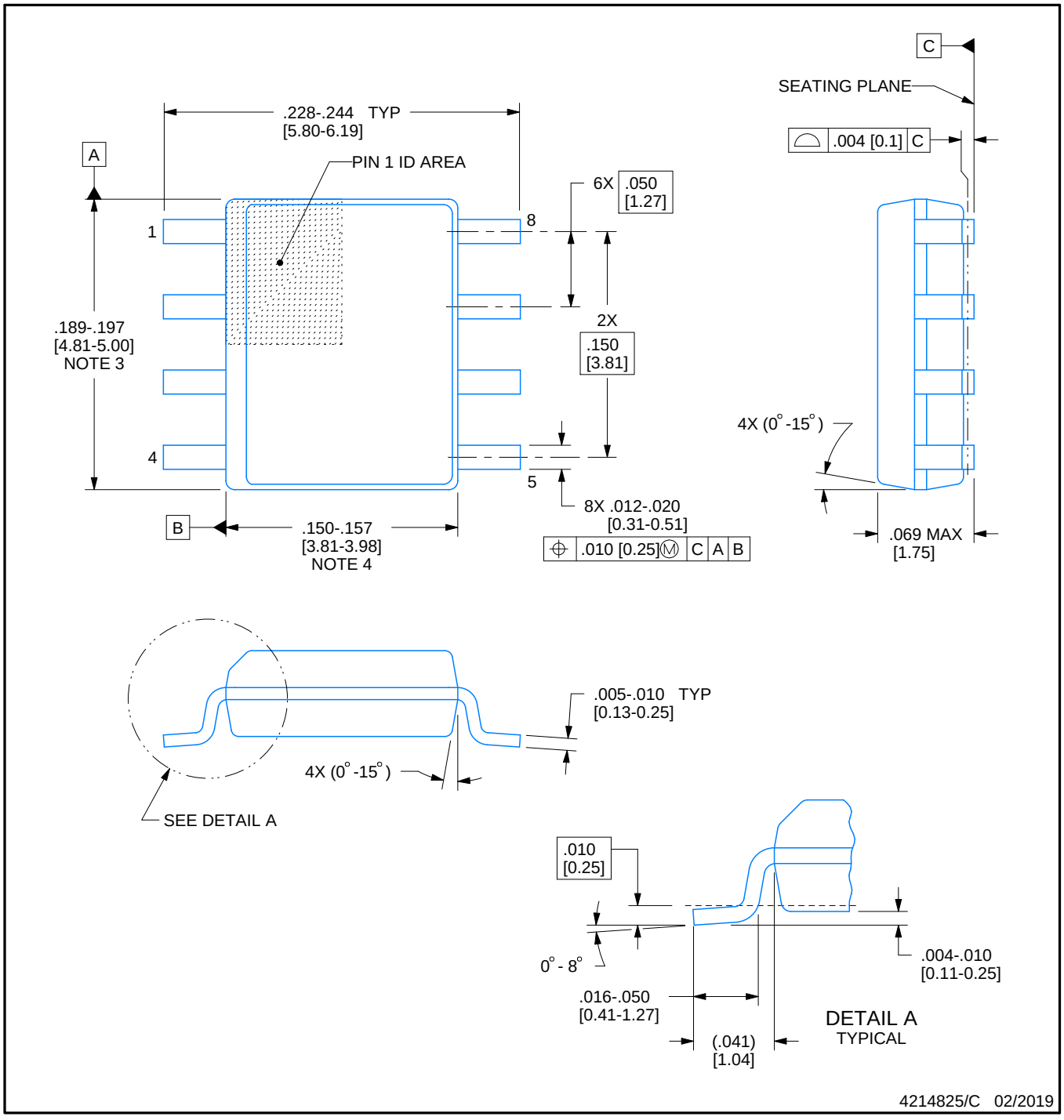


PACKAGE OUTLINE

D0008A

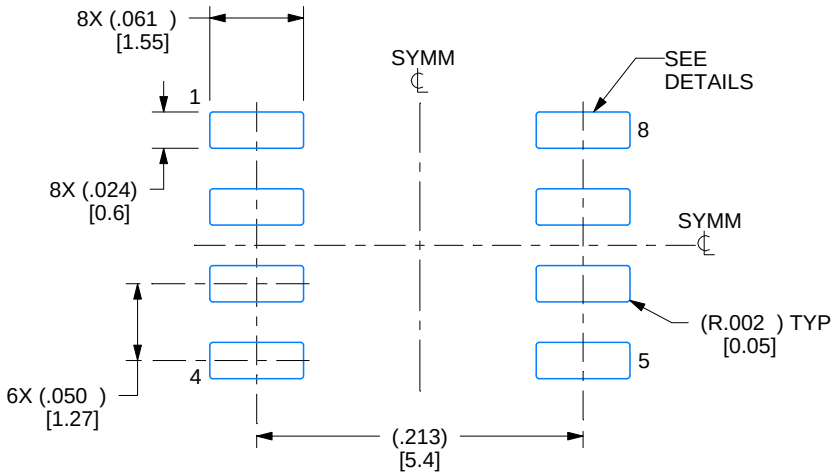
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

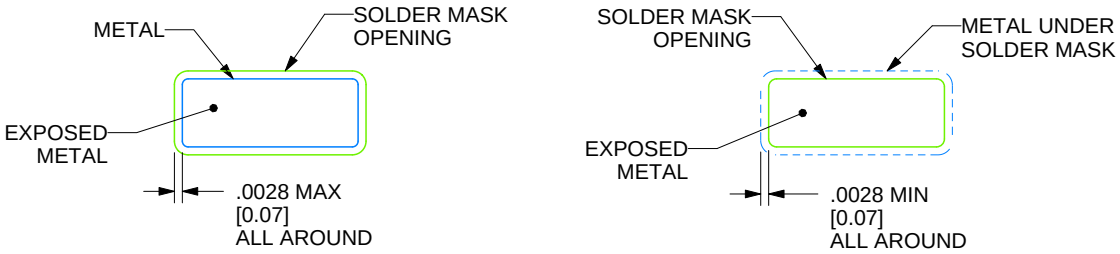


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

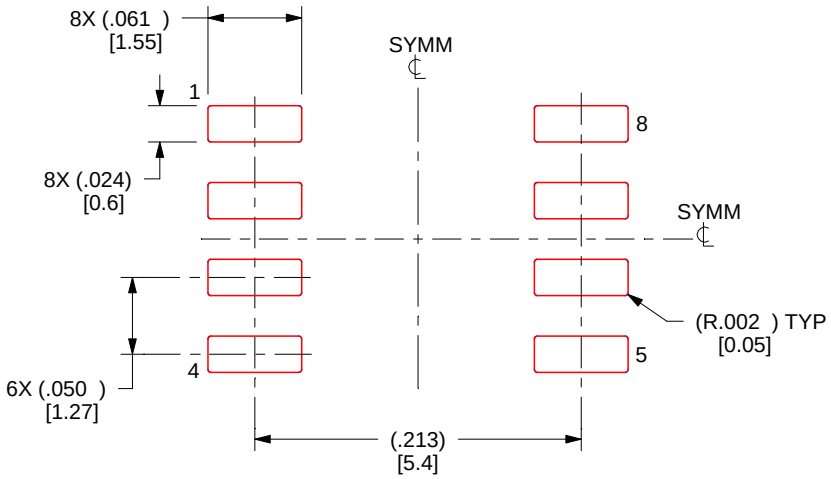
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



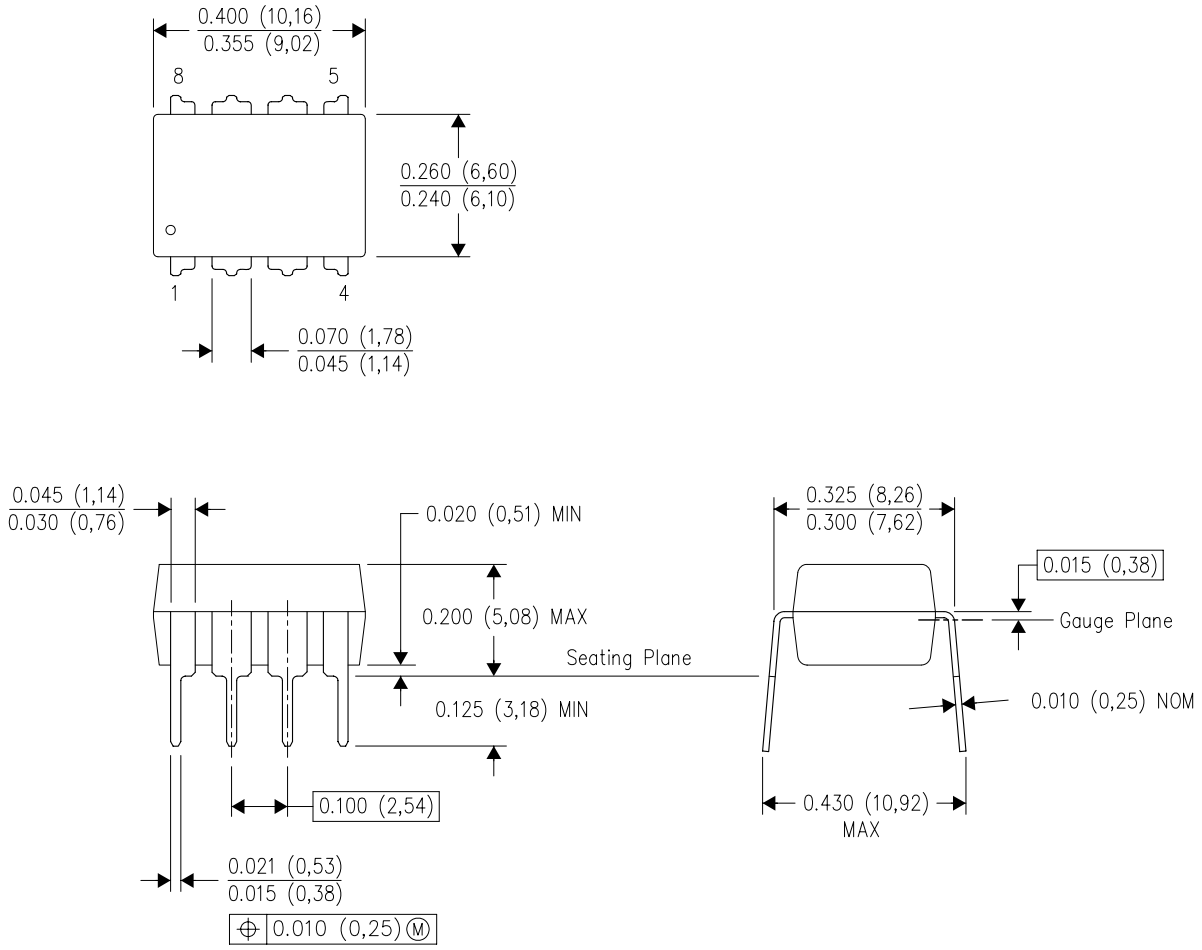
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

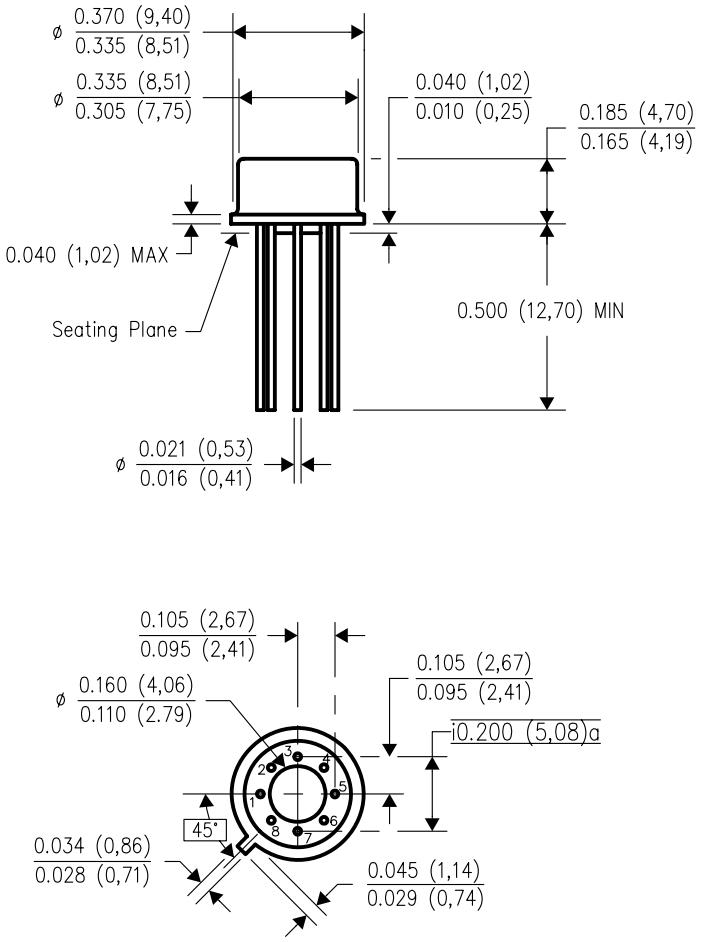
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

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