OPAx992 40V 轨到轨输入/输出、低失调电压、低噪声运算放大器

1 特性

- 低失调电压：±210μV
- 低失调电压漂移：±0.25μV/°C
- 低噪声：1kHz 时为 7nV/√Hz，4.4nV/√Hz 宽带
- 高共模抑制：115dB
- 低偏置电流：±10pA
- 轨至轨输入和输出
- 支持多路复用器/比较器的输入
  - 放大器以最高达到电源轨的差分输入工作
  - 放大器可用于开环中，也可用作比较器
- 高带宽：10.6MHz GBW，单位增益稳定
- 高压摆率：32 V/μs
- 低静态电流：每个放大器 2.4mA
- 宽电源电压：±1.35V 至 ±20V，2.7V 至 40V
- 强大的 EMIRR 性能

2 应用

- 多路复用数据采集系统
- 测试和测量设备
- 电机驱动：功率级和控制模块
- 电力输送：UPS、服务器和商用网络电源
- ADC 驱动器和基准缓冲放大器
- 可编程逻辑控制器
- 模拟输入和输出模块
- 高侧和低侧电流检测
- 高精度比较器

3 说明

OPAx992（OPA992、OPA2992 和 OPA4992）是高电压 (40V) 通用运算放大器系列。这些器件具有出色的直流精度和交流性能，包括轨到轨输入/输出、低失调电压（±210 μV，典型值）、低温漂（±0.25 μV/°C，典型值）、低噪声（1 kHz 时为 7nV/√Hz，10 kHz 时为 4.4nV/√Hz）。

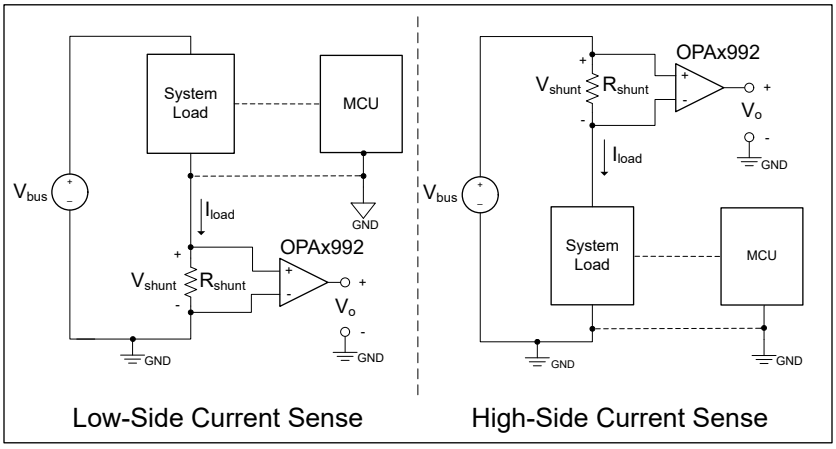
OPAx992 具有诸多特性，例如电源轨的差分和共模输入电压范围、高短路电流 (±65 mA) 和高压摆率 (32 V/μs)，因此是一款灵活可靠的高性能运算放大器，适用于各种高电压工业应用。

OPAx992 运算放大器系列采用*微型*封装（例如 WSON）以及标准封装（例如 SOT-23、SOIC 和 TSSOP），额定工作温度范围为 -40°C 至 125°C。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
OPA992	SOT-23 (5)	2.90mm × 1.60mm
	SOT-23 (6)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
OPA2992	SOIC (8)	4.90mm × 3.90mm
	SOT-23 (8)	2.90mm × 1.60mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	2.00mm × 2.00mm
OPA4992	SOIC (14)	8.65mm × 3.90mm
	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



适用于电流感测应用的 OPAx992

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (December 2021) to Revision C (March 2022) **Page**

- Adjusted the typical CMRR value for V_S = 2.7 – 40 V, (V+) – 1 < V_{CM} < V+ (NMOS pair) from "90 dB" to "79 dB" in the *Electrical Characteristics* section 8
- Adjusted the A_{OL} test condition from "V_S = 40 V, V_{CM} = V_S / 2, (V –) + 0.1 V < V_O < (V+) – 0.1 V" to "V_S = 40 V, V_{CM} = V_S / 2, (V –) + 0.12 V < V_O < (V+) – 0.12 V" in the *Electrical Characteristics* section 8
- Adjusted the typical t_{ON} Amplifier Enable Time value from "15 µs" to "5 µs" in the *Electrical Characteristics* section 8
- Adjusted the typical SHDN pin input bias current value for V_S = 2.7 V to 40 V, (V –) ≤ SHDN ≤ (V –) + 0.7 V from "150 nA" to "400 nA" in the *Electrical Characteristics* section 8
- Removed "Open-Loop Gain and Phase vs Frequency" figure in *Typical Characteristics* section 11

Changes from Revision A (October 2021) to Revision B (December 2021) **Page**

- Added PSRR specification for OPA4992 release in *Electrical Characteristics* section 8
- Added clarification to V_S = 2.7 V to 40 V PSRR specification noting that specification is for all channel variants 8
- Changed y-axis from linear scale to logarithmic scale in "Input Voltage Noise Spectral Density vs Frequency" figure in *Typical Characteristics* section 11
- Corrected typo in *Shutdown* of *Feature Description* section from "...specified 10-kΩ load to midsupply (V_S / 2)" to "...specified 10-kΩ load to V-" 28

Changes from Revision * (June 2021) to Revision A (October 2021) **Page**

- 将器件状态从*预告信息*更改为*量产数据* 1

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5 Pin Configuration and Functions

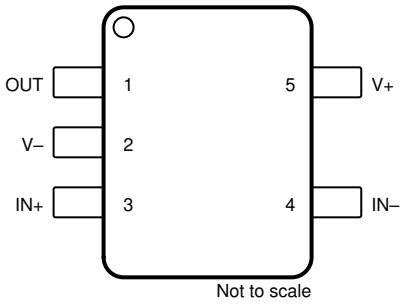


图 5-1. OPA992 DBV Package
5-Pin SOT-23
(Top View)

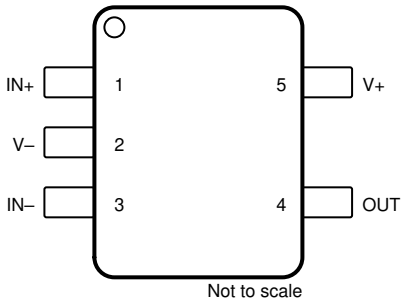


图 5-2. OPA992 DCK Package
5-Pin SC70
(Top View)

表 5-1. Pin Functions: OPA992

PIN			I/O	DESCRIPTION
NAME	SOT-23	SC70		
IN+	3	1	I	Noninverting input
IN –	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V –	2	2	—	Negative (lowest) power supply

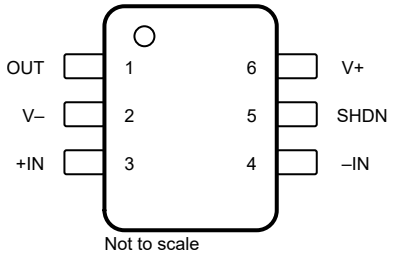


图 5-3. OPA992S DBV Package
6-Pin SOT-23
(Top View)

表 5-2. Pin Functions: OPA992S

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
– IN	4	I	Inverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amplifier enabled, high = amplifier disabled
V+	6	—	Positive (highest) power supply
V –	2	—	Negative (lowest) power supply

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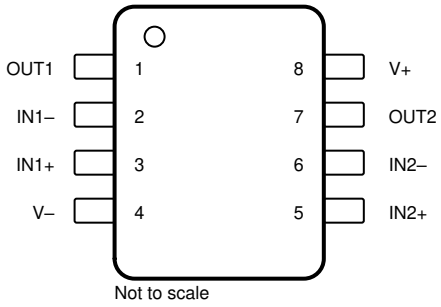
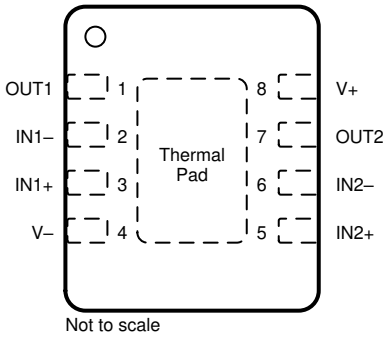


图 5-4. OPA2992 D, DDF, PW, and DGK Package 8-Pin SOIC, SOT-23, TSSOP, and VSSOP (Top View)



A. Connect thermal pad to V – . See 节 7.3.10 for more information.

图 5-5. OPA2992 DSG Package(A) 8-Pin WSON With Exposed Thermal Pad (Top View)

表 5-3. Pin Functions: OPA2992

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V –	4	—	Negative (lowest) power supply

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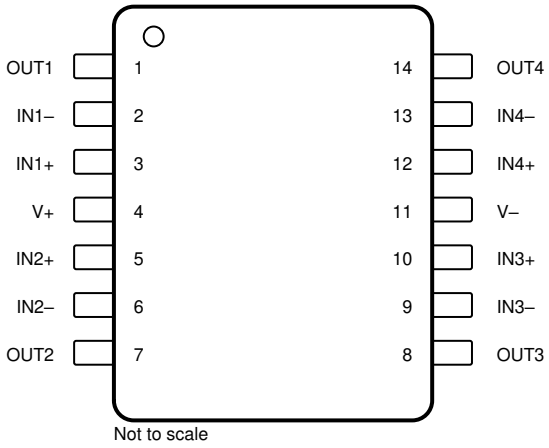


图 5-6. OPA4992 D and PW Package
14-Pin SOIC and TSSOP
(Top View)

表 5-4. Pin Functions: OPA4992

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Shutdown pin voltage(4)		V–	(V–) + 20	V
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(4) Cannot exceed V+.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	40	V
V_I	Common mode voltage range	(V–)	(V+)	V
V_{IH}	High level input voltage at shutdown pin (amplifier disabled)	1.1	(V–) + 20 (1)	V
V_{IL}	Low level input voltage at shutdown pin (amplifier enabled)	(V–)	0.2	V
T_A	Specified temperature	–40	125	°C

(1) Cannot exceed V+.

6.4 Thermal Information for Single Channel

THERMAL METRIC(1)		OPA992, OPA992S			UNIT
		DBV (SOT-23)		DCK (SC70)	
		5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.4	166.9	198.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.9	83.9	94.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	47.1	45.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.4	25.9	16.9	°C/W

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6.4 Thermal Information for Single Channel (continued)

THERMAL METRIC(1)		OPA992, OPA992S			UNIT
		DBV (SOT-23)		DCK (SC70)	
		5 PINS	6 PINS	5 PINS	
ψ_{JB}	Junction-to-board characterization parameter	52.1	47.0	45.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		OPA2992					Unit
		D (SOIC)	DDF (SOT-23)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.0	149.6	174.2	74.8	183.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.0	85.3	65.9	93.6	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	68.6	95.9	42.1	114.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.0	7.9	11.0	3.8	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.8	68.4	94.4	41.9	112.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	17.0	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		OPA4992		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.0	118.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	47.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.4	61.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.21	±1	mV
			T_A = –40°C to 125°C			±1.2	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±0.25		µV/℃
PSRR	Input offset voltage versus power supply	OPA992, OPA2992, V_{CM} = V–, V_S = 5 V to 40 V	T_A = –40°C to 125°C		±0.2	±1.3	µV/V
		OPA4992, V_{CM} = V–, V_S = 5 V to 40 V			±0.4	±1.8	
		OPA992, OPA2992, OPA4992, V_{CM} = V–, V_S = 2.7 V to 40 V(1)			±0.8	±7	
	DC channel separation				0.4		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			2.77		μV_{PP}
					0.49		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			7		nV/√Hz
		f = 10 kHz			4.4		
i_N	Input current noise density	f = 1 kHz			60		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 40 V, V– < V_{CM} < (V+) – 2 V (PMOS pair)	T_A = –40°C to 125°C	100	115		dB
		V_S = 5 V, V– < V_{CM} < (V+) – 2 V (PMOS pair)(1)		75	98		
		V_S = 2.7 V, V– < V_{CM} < (V+) – 2 V (PMOS pair)			90		
		V_S = 2.7 – 40 V, (V+) – 1 V < V_{CM} < V+ (NMOS pair)			79		
		(V+) – 2 V < V_{CM} < (V+) – 1 V		See Offset Voltage vs Common-Mode Voltage (Transition Region)			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V		120	142		dB
		V_S = 40 V, V_{CM} = V_S / 2, (V–) + 0.12 V < V_O < (V+) – 0.12 V	T_A = –40°C to 125°C		142		
		V_S = 5 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V(1)		104	125		
			T_A = –40°C to 125°C		125		
		V_S = 2.7 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V(1)		90	105		
			T_A = –40°C to 125°C		105		

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6.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				10.6		MHz
SR	Slew rate	V_S = 40 V, G = +1, V_{STEP} = 10 V, C_L = 20 pF(5)			32		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			0.65		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			0.3		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			0.86		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			0.44		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			64		°
	Overload recovery time	V_{IN} × gain > V_S			170		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ			0.00005%		
					126		dB
		V_S = 10 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 128 Ω			0.0032%		
					90		dB
		V_S = 10 V, V_O = 0.4 V_{RMS}, G = 1, f = 1 kHz, R_L = 32 Ω			0.00032%		
					110		dB
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load		7		mV
			V_S = 40 V, R_L = 10 kΩ		48	60	
			V_S = 40 V, R_L = 2 kΩ		220	300	
			V_S = 2.7 V, R_L = no load		0.5		
			V_S = 2.7 V, R_L = 10 kΩ		5	20	
			V_S = 2.7 V, R_L = 2 kΩ		20	50	
I_{SC}	Short-circuit current				±65(3)		mA
C_{LOAD}	Capacitive load drive				See *Phase Margin vs Capacitive Load*		pF
Z_O	Open-loop output impedance	I_O = 0 A			See *Open-Loop Output Impedance vs Frequency*		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	OPA2992, OPA4992, I_O = 0 A			2.4	2.8	mA
			T_A = –40°C to 125°C			2.84	
		OPA992, I_O = 0 A			2.48	2.92	
			T_A = –40°C to 125°C			2.98	
SHUTDOWN							
I_{QSD}	Quiescent current per amplifier	V_S = 2.7 V to 40 V, all amplifiers disabled, SHDN = V– + 2 V			40	45	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 2.7 V to 40 V, amplifier disabled			10 || 2		GΩ || pF
V_{IH}	Logic high threshold voltage (amplifier disabled)	For valid input high, the SHDN pin voltage should be greater than the maximum threshold but less than or equal to V+ or (V–) + 20 V, whichever is less				(V–) + 1.1 V	V
V_{IL}	Logic low threshold voltage (amplifier enabled)	For valid input low, the SHDN pin voltage should be less than the minimum threshold but greater than or equal to V–		(V–) + 0.2 V			V
t_{ON}	Amplifier enable time (from shutdown) (2)	V_S = ±20 V, G = +1, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V–			5		µs
t_{OFF}	Amplifier disable time (2)	V_S = ±20 V, G = +1, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V–			3		µs
	SHDN pin input bias current (per pin)	V_S = 2.7 V to 40 V, (V–) + 20 V (4) ≥ SHDN ≥ (V–) + 0.9 V			500		nA
		V_S = 2.7 V to 40 V, (V–) ≤ SHDN ≤ (V–) + 0.7 V			400		

(1) Specified by characterization only.
(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches 10% (disable) or 90% (enable) of its final value.

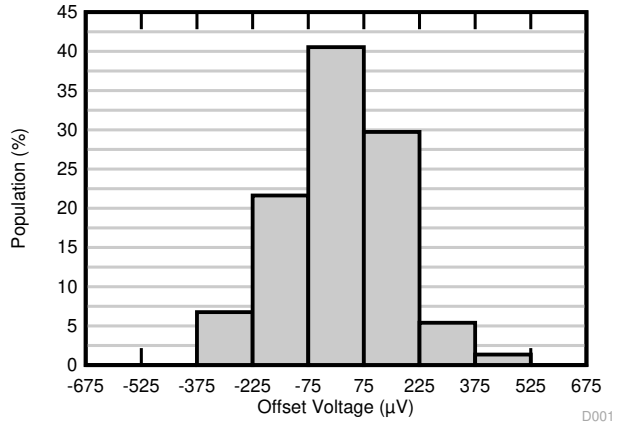
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(3) At high supply voltage, placing the OPAx992 in a sudden short to mid-supply or ground will lead to rapid thermal shutdown. Output current greater than I_{SC} can be achieved if rapid thermal shutdown is avoided as per *Output Voltage Swing vs Output Current*.
(4) SHDN pin should not exceed V+ or (V-) + 20 V, whichever is less.
(5) See *Slew Rate vs Input Step Voltage* for more information.

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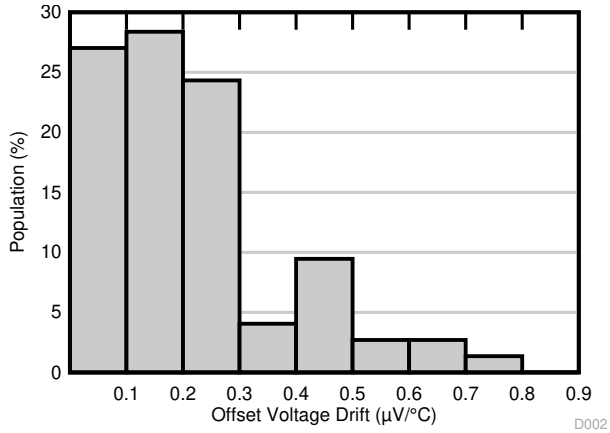
6.8 Typical Characteristics

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



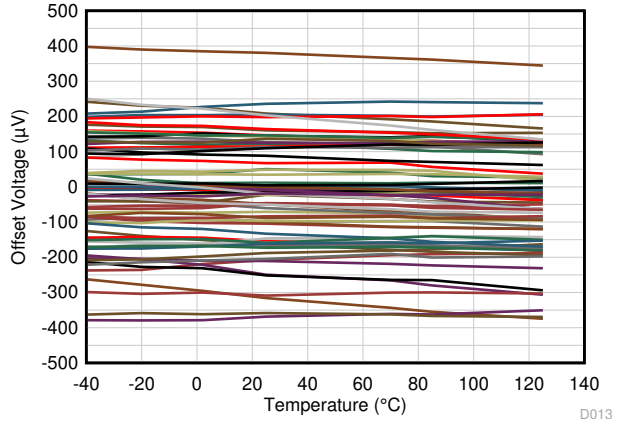
Distribution from 74 amplifiers, T_A = 25°C

图 6-1. Offset Voltage Production Distribution



Distribution from 74 amplifiers

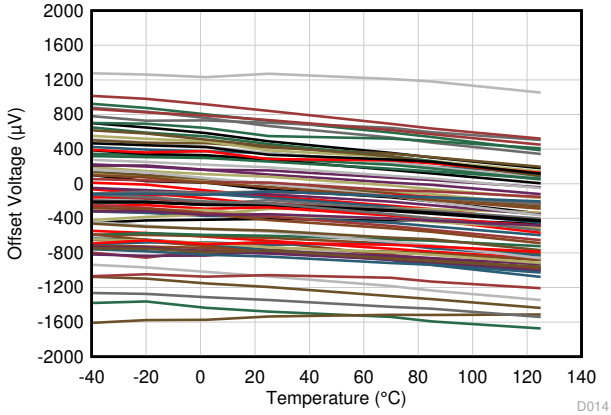
图 6-2. Offset Voltage Drift Distribution



V_{CM} = V-

Data from 74 amplifiers

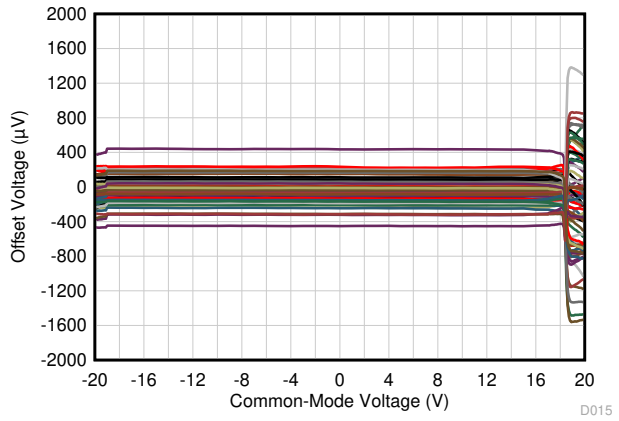
图 6-3. Offset Voltage vs Temperature



V_{CM} = V+

Data from 74 amplifiers

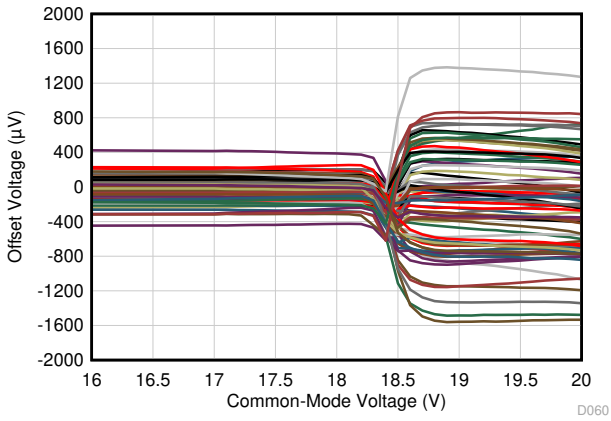
图 6-4. Offset Voltage vs Temperature



T_A = 25°C

Data from 74 amplifiers

图 6-5. Offset Voltage vs Common-Mode Voltage



T_A = 25°C

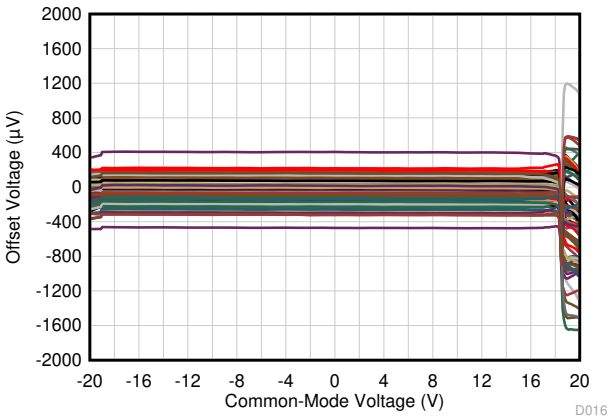
Data from 74 amplifiers

图 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

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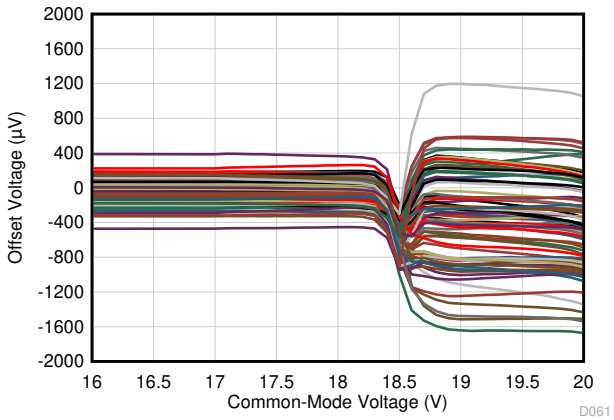
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



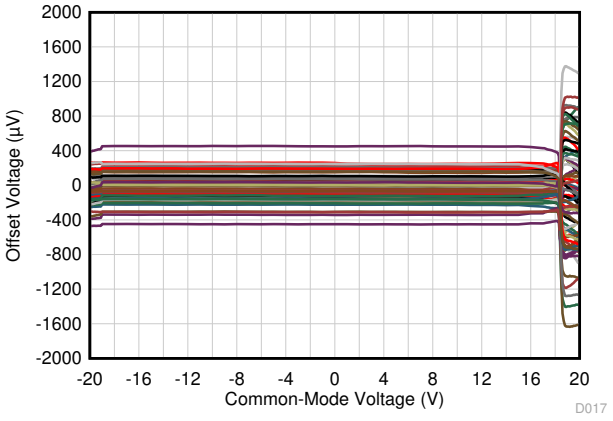
T_A = 125°C
Data from 74 amplifiers

图 6-7. Offset Voltage vs Common-Mode Voltage



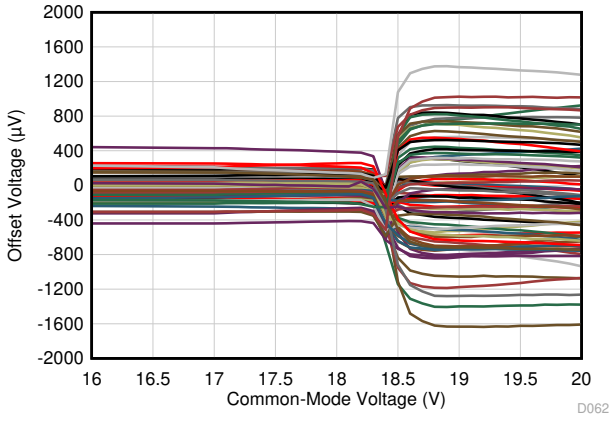
T_A = 125°C
Data from 74 amplifiers

图 6-8. Offset Voltage vs Common-Mode Voltage (Transition Region)



T_A = –40°C
Data from 74 amplifiers

图 6-9. Offset Voltage vs Common-Mode Voltage



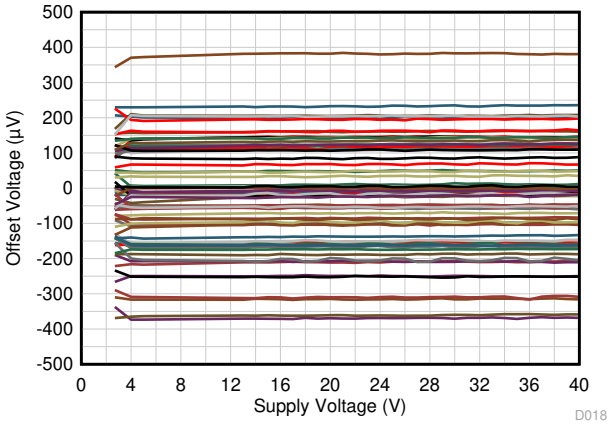
T_A = –40°C
Data from 74 amplifiers

图 6-10. Offset Voltage vs Common-Mode Voltage (Transition Region)

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



V_{CM} = V –

Data from 74 amplifiers

图 6-11. Offset Voltage vs Power Supply

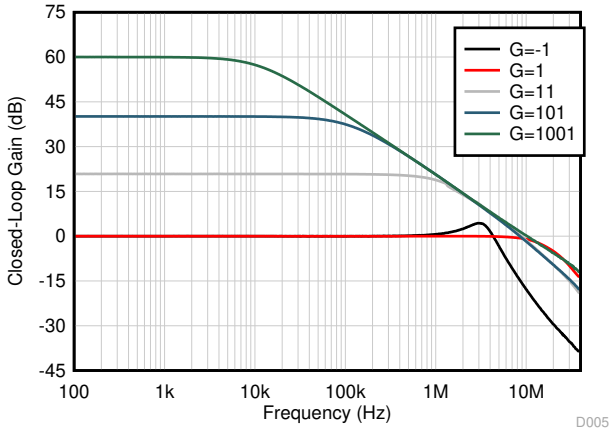


图 6-12. Closed-Loop Gain vs Frequency

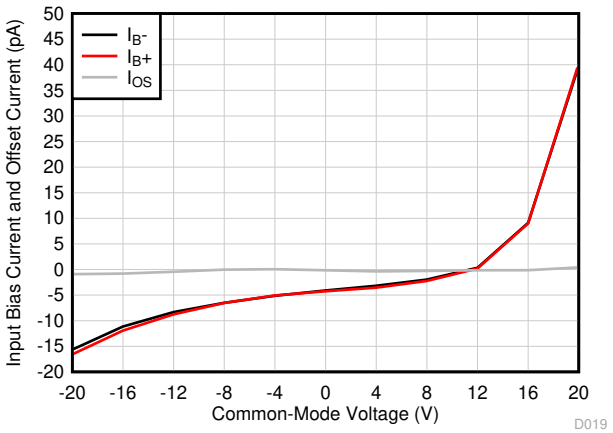


图 6-13. Input Bias Current and Offset Current vs Common-Mode Voltage

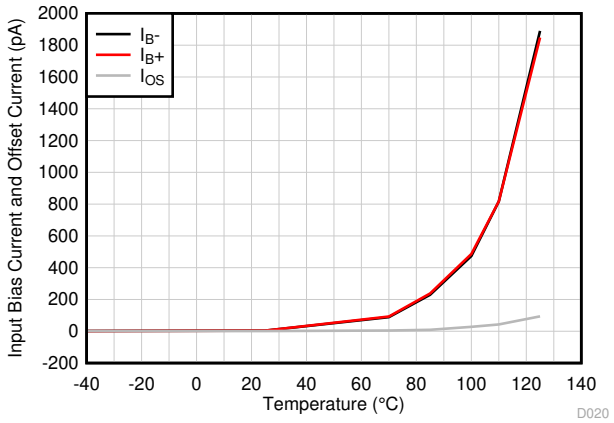


图 6-14. Input Bias Current and Offset Current vs Temperature

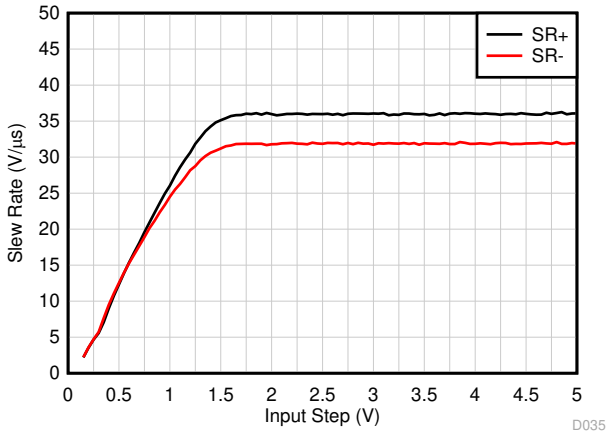
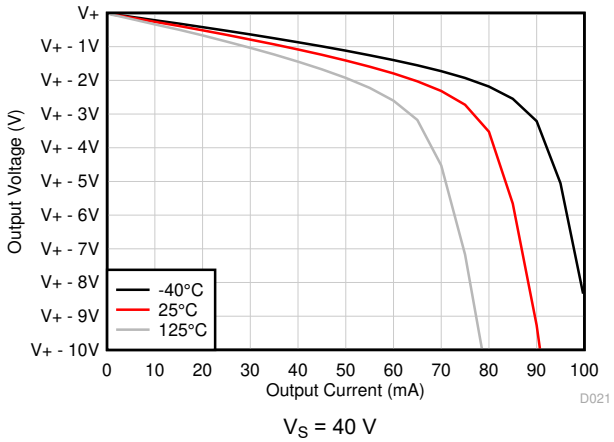


图 6-15. Slew Rate vs Input Step Voltage



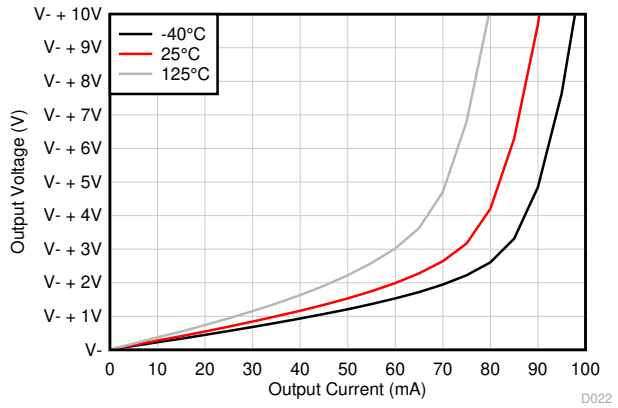
V_S = 40 V

图 6-16. Output Voltage Swing vs Output Current (Sourcing)

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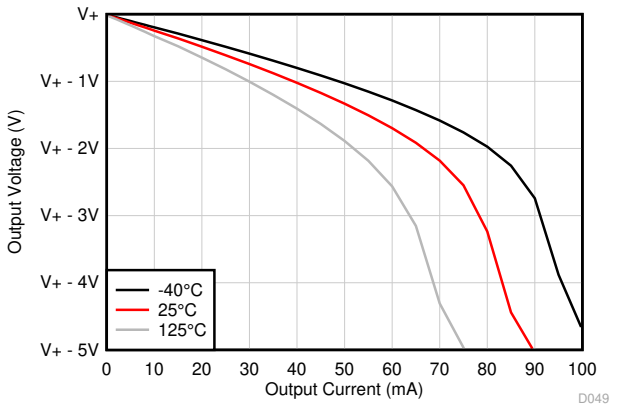
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



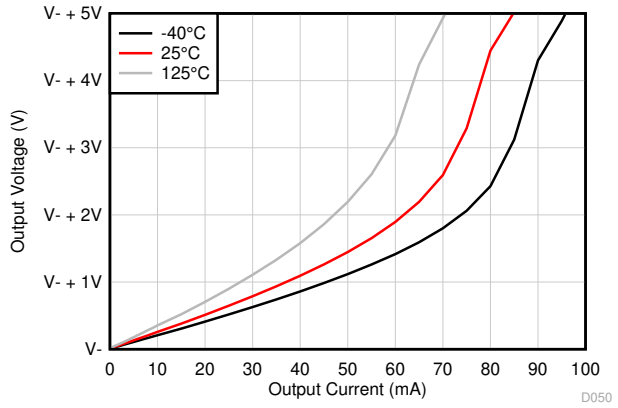
V_S = 40 V

图 6-17. Output Voltage Swing vs Output Current (Sinking)



V_S = 5 V

图 6-18. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5 V

图 6-19. Output Voltage Swing vs Output Current (Sinking)

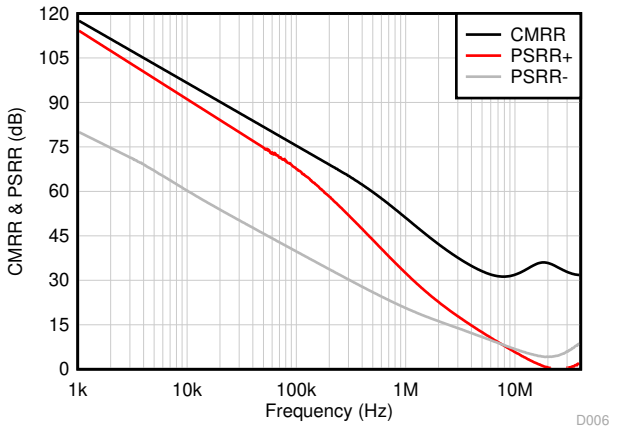
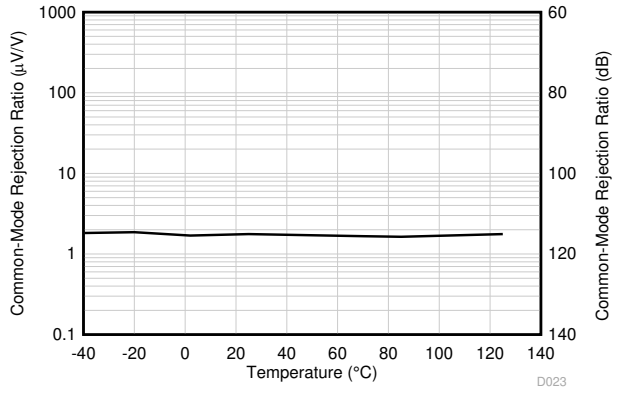
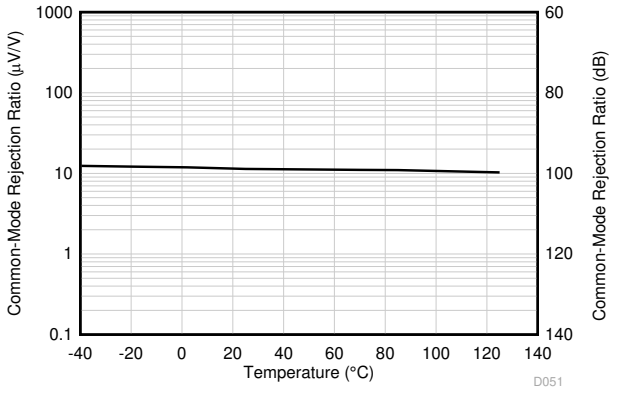


图 6-20. CMRR and PSRR vs Frequency



V_S = 40 V

图 6-21. CMRR vs Temperature



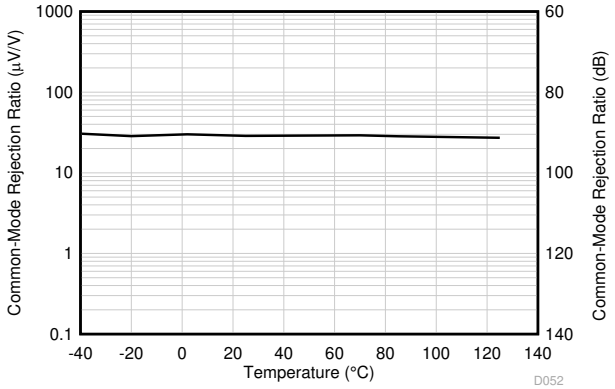
V_S = 5 V

图 6-22. CMRR vs Temperature

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



V_S = 2.7 V

图 6-23. CMRR vs Temperature

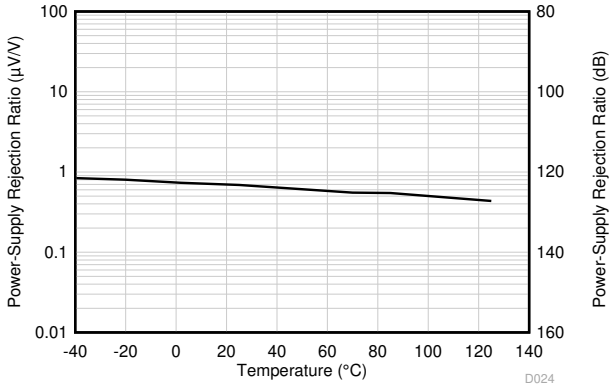


图 6-24. PSRR vs Temperature

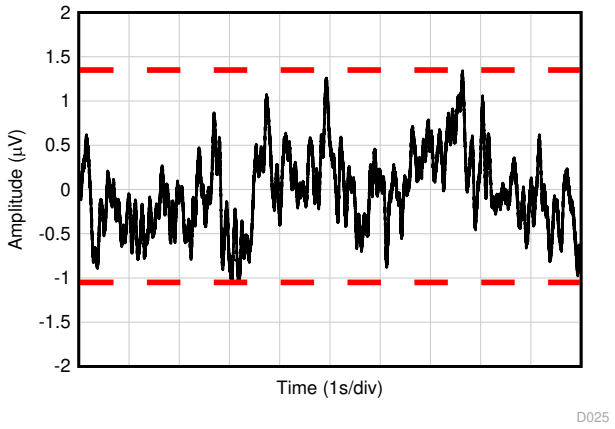


图 6-25. 0.1-Hz to 10-Hz Noise

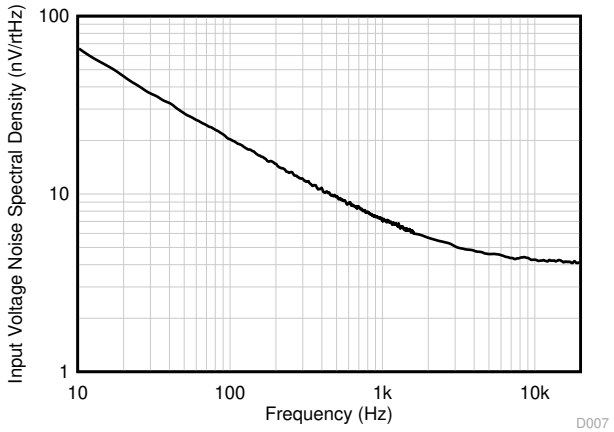
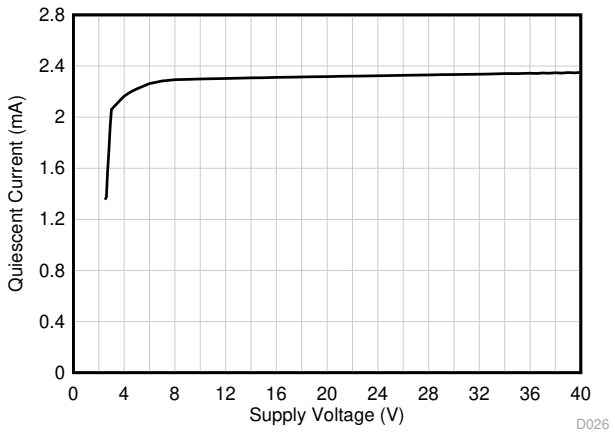
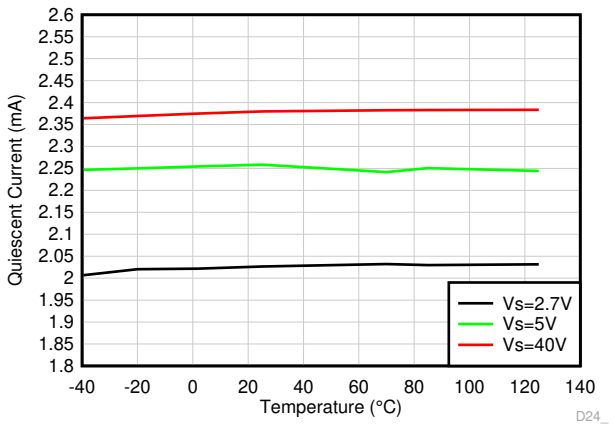


图 6-26. Input Voltage Noise Spectral Density vs Frequency



V_{CM} = V –

图 6-27. Quiescent Current vs Supply Voltage



V_{CM} = V –

图 6-28. Quiescent Current vs Temperature

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)

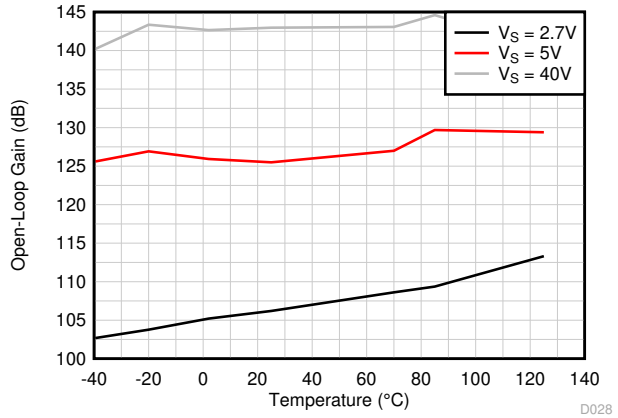


图 6-29. Open-Loop Voltage Gain vs Temperature (dB)

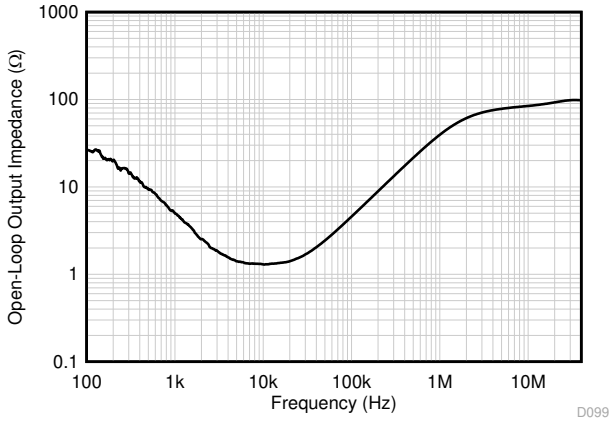
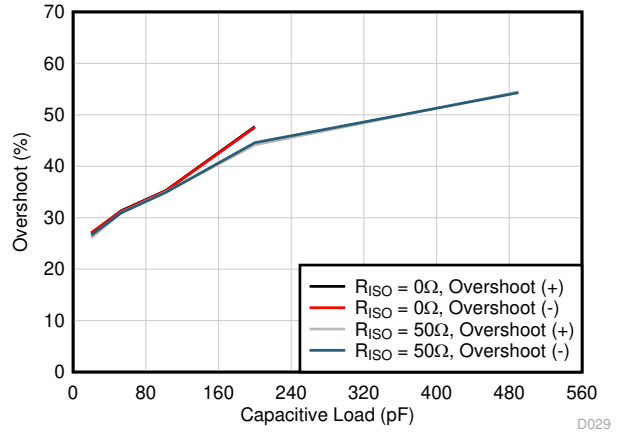
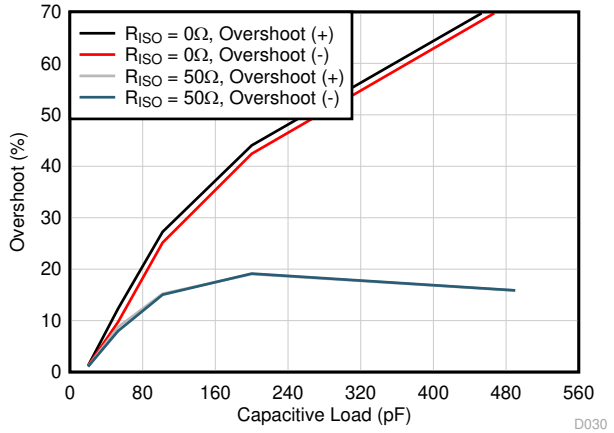


图 6-30. Open-Loop Output Impedance vs Frequency



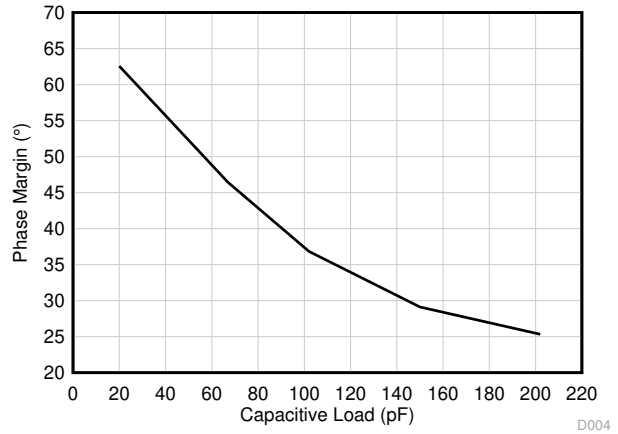
20-mV_{pp} Output Step, G = -1

图 6-31. Small-Signal Overshoot vs Capacitive Load



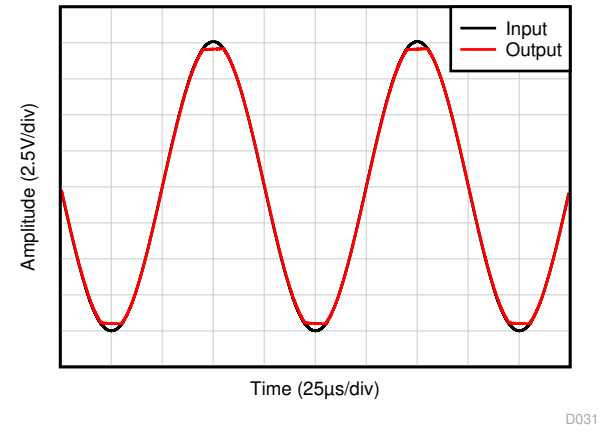
20-mV_{pp} Output Step, G = +1

图 6-32. Small-Signal Overshoot vs Capacitive Load



G = +1

图 6-33. Phase Margin vs Capacitive Load



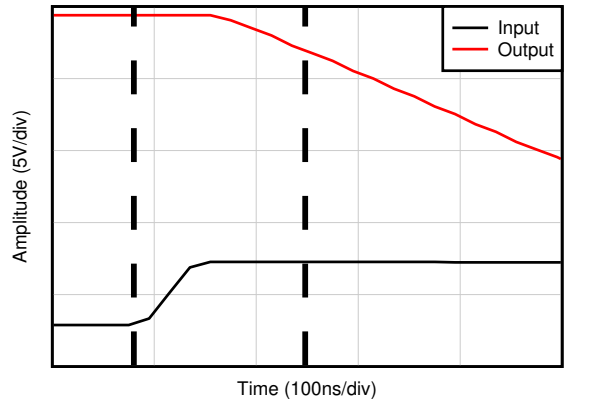
V_{IN} = ±10 V_{pp}; V_S = V_{OUT} = ±9.55 V

图 6-34. No Phase Reversal

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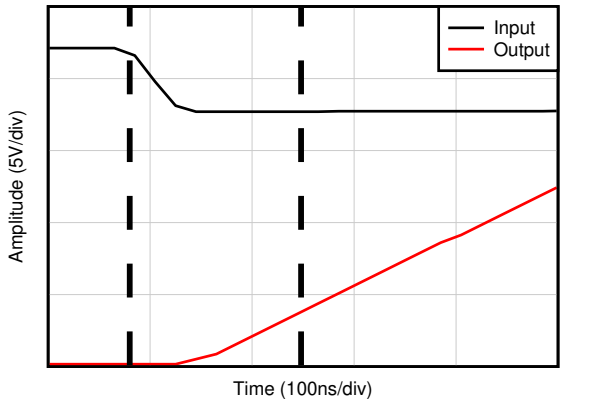
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



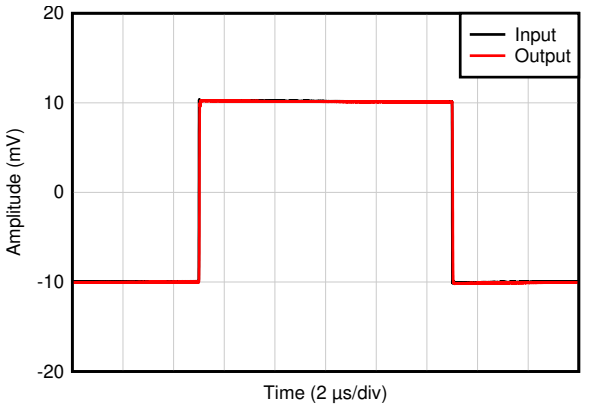
G = –10

图 6-35. Positive Overload Recovery



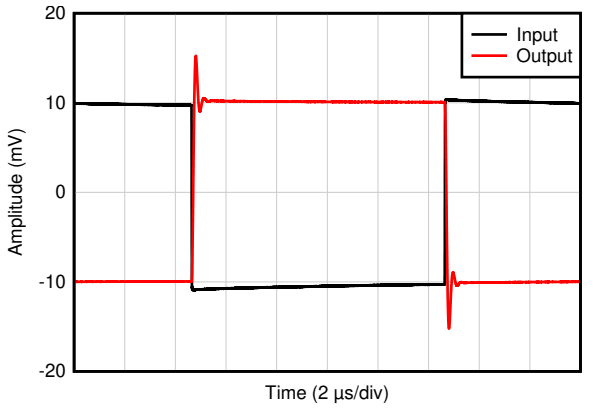
G = –10

图 6-36. Negative Overload Recovery



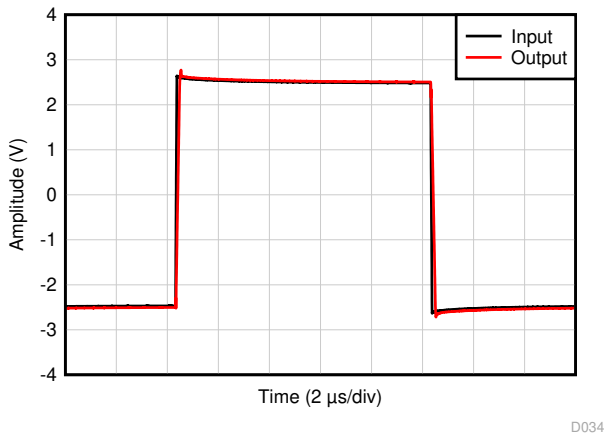
C_L = 20 pF, G = 1, 20-mV_{pp} step response

图 6-37. Small-Signal Step Response



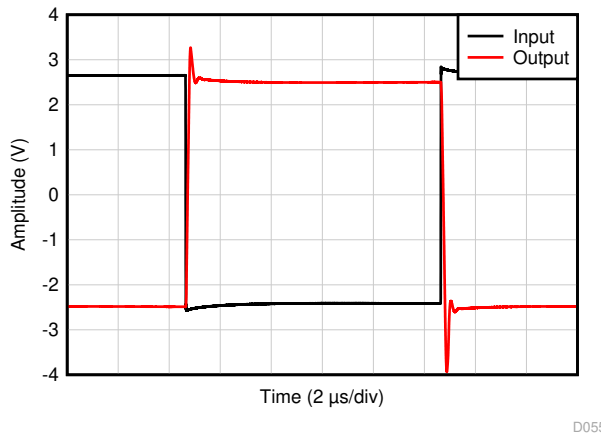
C_L = 20 pF, G = -1, 20-mV_{pp} step response

图 6-38. Small-Signal Step Response



C_L = 20 pF, G = 1, 5-V_{pp} step response

图 6-39. Large-Signal Step Response



C_L = 20 pF, G = -1, 5-V_{pp} step response

图 6-40. Large-Signal Step Response

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)

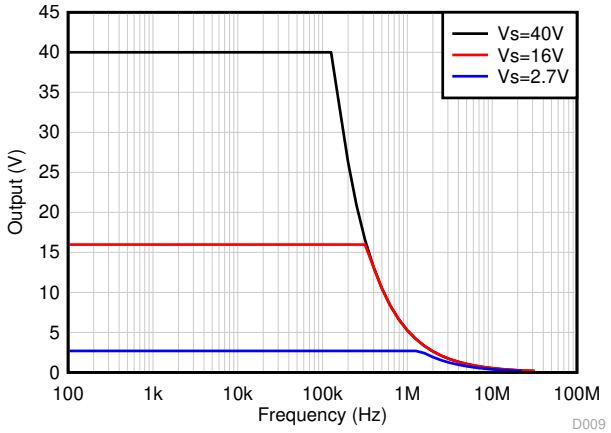


图 6-41. Maximum Output Voltage vs Frequency

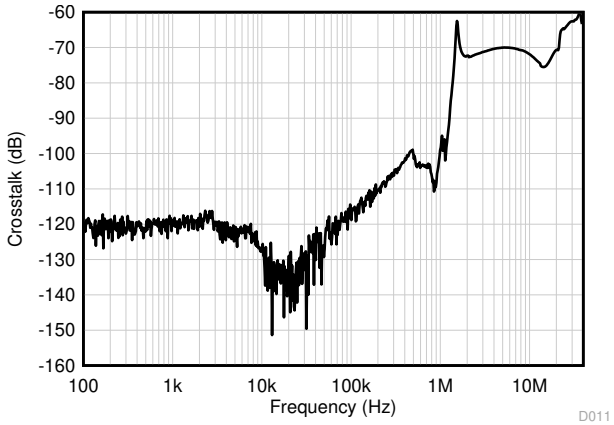


图 6-42. Channel Separation vs Frequency

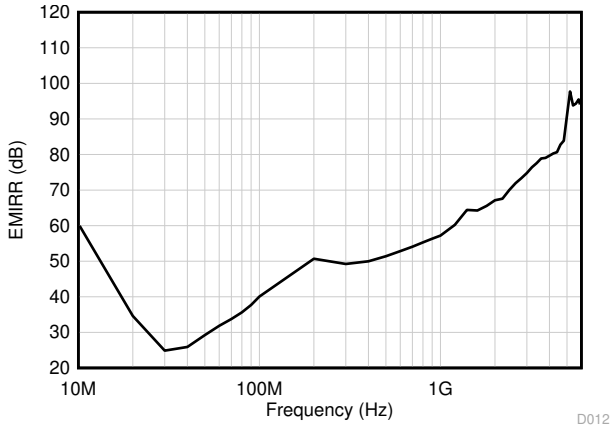


图 6-43. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

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7 Detailed Description

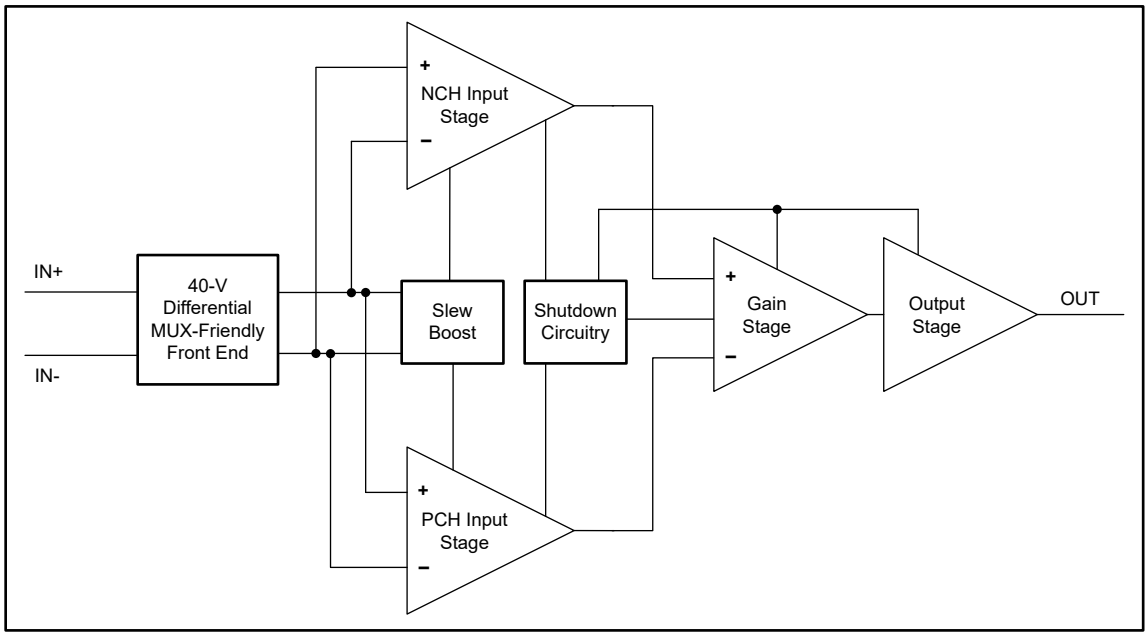
7.1 Overview

The OPAx992 family (OPA992, OPA2992, and OPA4992) is a family of high voltage (40-V) general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±210 µV, typ), and low offset drift (±0.25 µV/°C, typ).

Special features such as differential and common-mode input voltage range to the supply rail, high short-circuit current (±65 mA), high slew rate (32 V/µs), and shutdown make the OPAx992 an extremely flexible, robust, and high-performance operational amplifier for high-voltage industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The OPAx992 uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 图 7-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 图 7-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

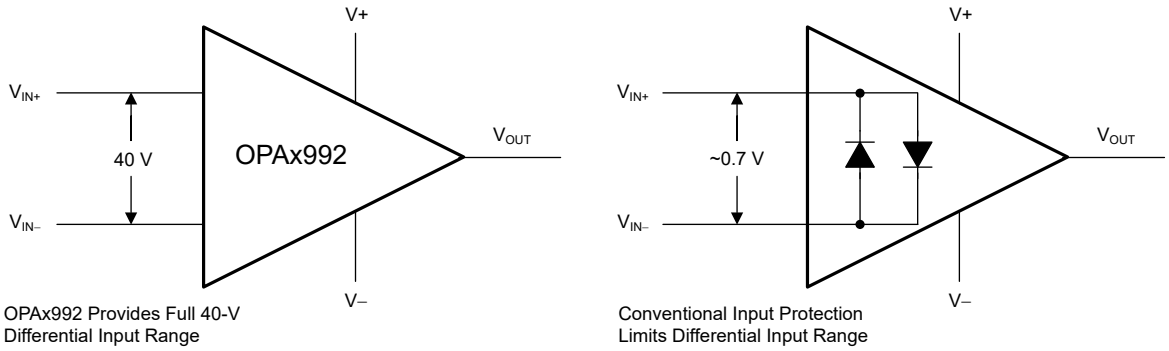


图 7-1. OPAx992 Input Protection Does Not Limit Differential Input Capability

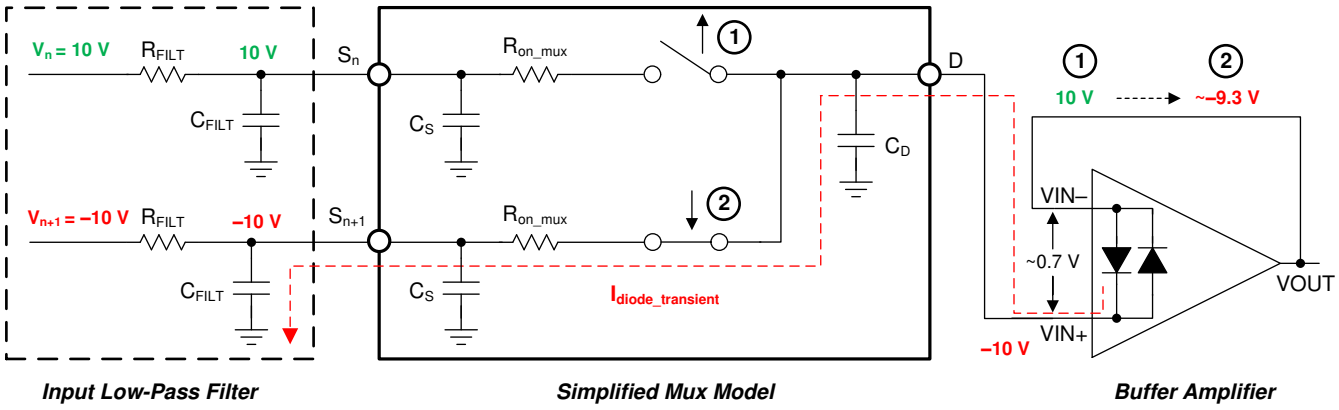


图 7-2. Back-to-Back Diodes Create Settling Issues

The OPAx992 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx992 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

7.3.2 EMI Rejection

The OPAx992 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx992 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 7-3 shows the results of this testing on the OPAx992. 表 7-1 shows the EMIRR IN+ values for the OPAx992 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational*

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Amplifiers application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

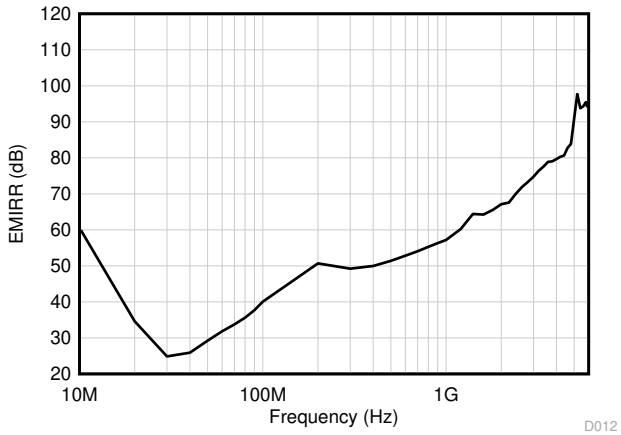


图 7-3. EMIRR Testing

表 7-1. OPAx992 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	56.3 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	65.6 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	70.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	91.0 dB

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7.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx992 is 150°C. Exceeding this temperature causes damage to the device. The OPAx992 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 7-4 shows an application example for the OPA2992 that has significant self heating because of its power dissipation (0.954 W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 55°C, the device junction temperature reaches 180°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 7-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the SOIC (8) package.

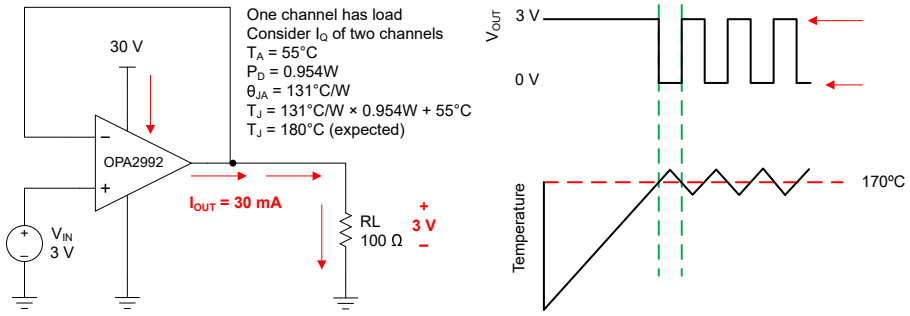


图 7-4. Thermal Protection

7.3.4 Capacitive Load and Stability

The OPAx992 features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive larger capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 7-5 and 图 7-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

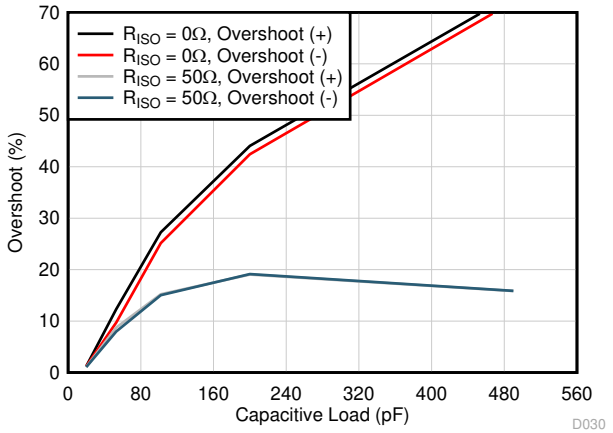


图 7-5. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = +1)

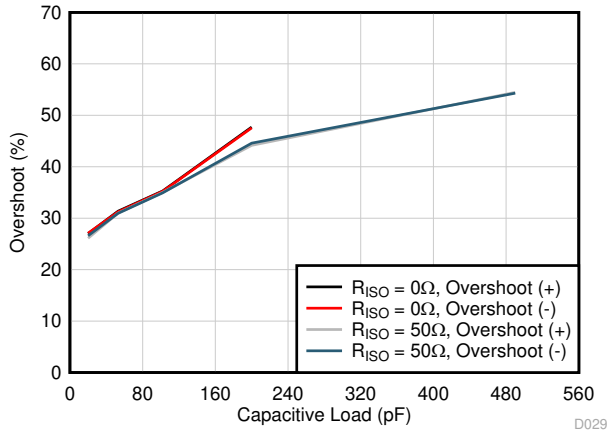


图 7-6. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = -1)

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For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 图 7-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx992 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 7-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

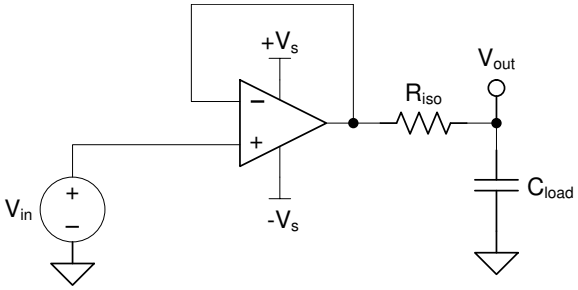


图 7-7. Extending Capacitive Load Drive With the OPA992

7.3.5 Common-Mode Voltage Range

The OPAx992 is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 图 7-8. The N-channel pair is active for input voltages close to the positive rail, typically from (V+) – 1 V to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

图 6-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

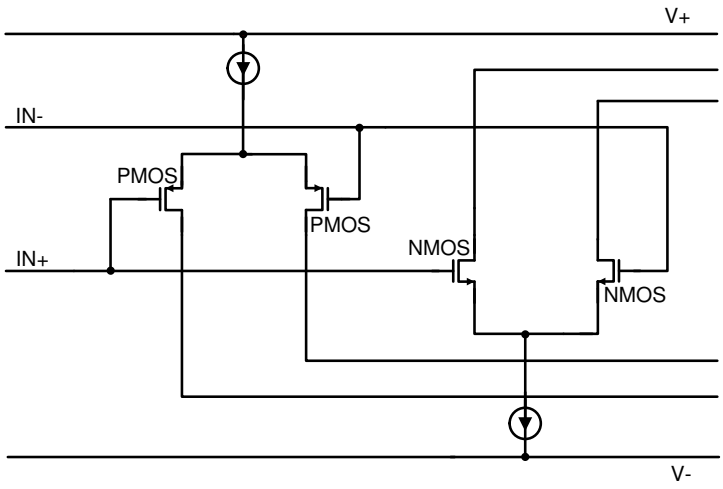


图 7-8. Rail-to-Rail Input Stage

7.3.6 Phase Reversal Protection

The OPAx992 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx992 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 图 7-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

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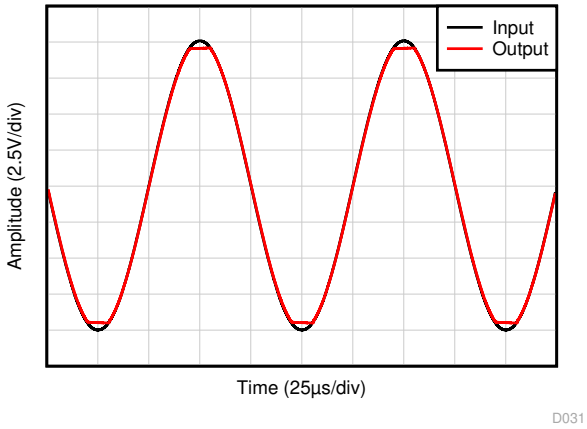


图 7-9. No Phase Reversal

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 7-10 shows an illustration of the ESD circuits contained in the OPAx992 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

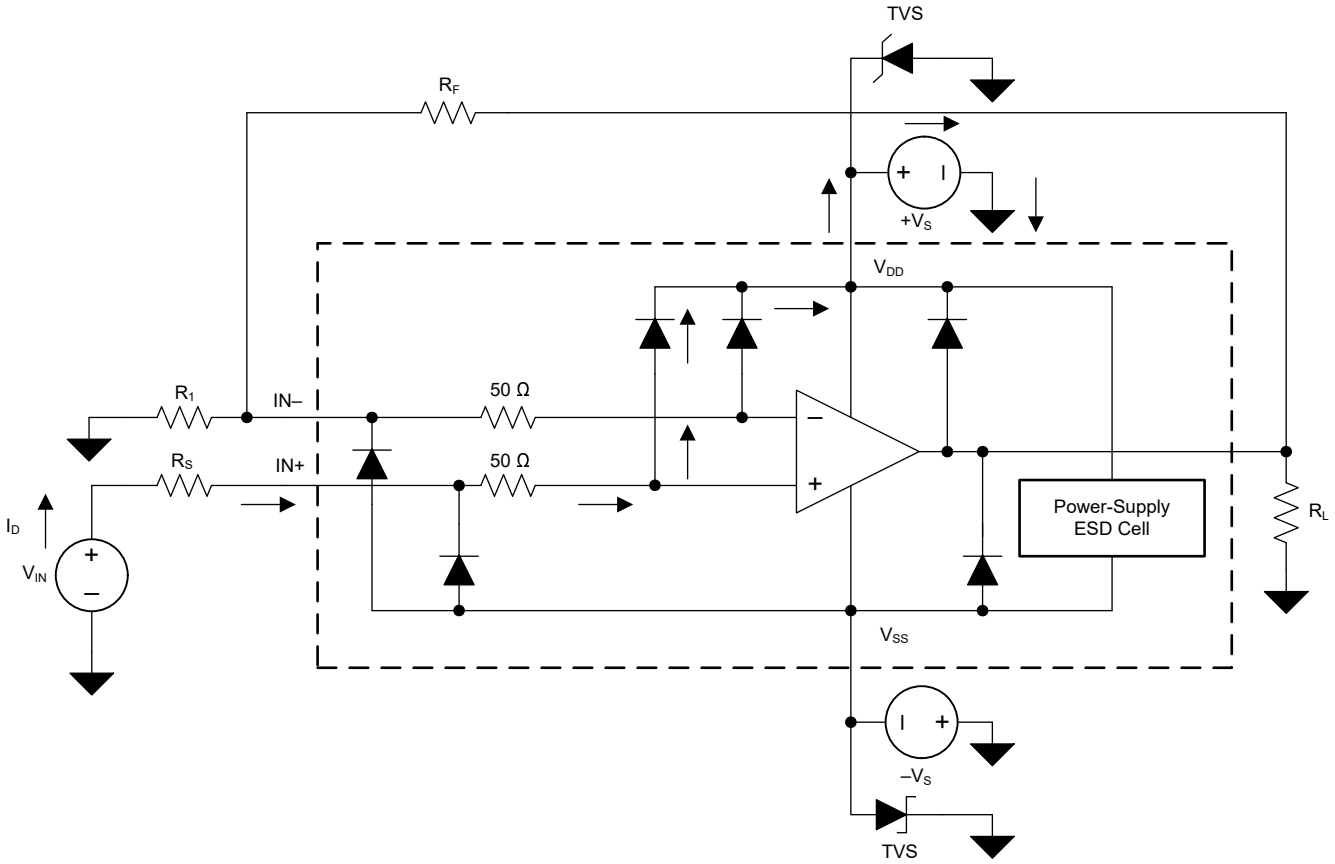


图 7-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

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7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx992 is approximately 170 ns.

7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

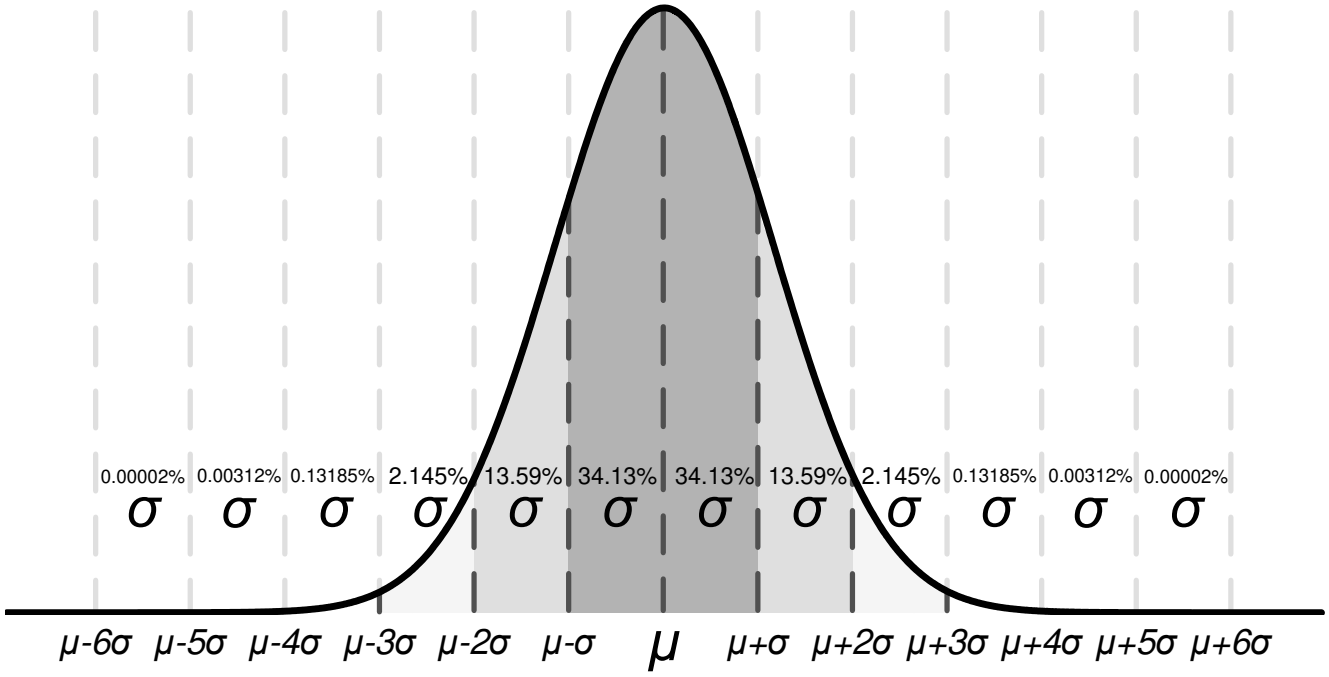


图 7-11. Ideal Gaussian Distribution

The 图 7-11 figure shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx992, the typical input voltage offset is 210 μV. So 68.2% of all OPAx992 devices are expected to have an offset from

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–210 µV to +210 µV. At 4 σ (±840 µV), 99.9937% of the distribution has an offset voltage less than ±840 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the OPAx992 family has a maximum offset voltage of 1 mV at 25°C, and even though this corresponds to slightly less than 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAx992 family does not have a maximum or minimum for offset voltage drift. But based on the typical value of 0.25 µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 1.5 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

Note that process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.3.10 Packages With an Exposed Thermal Pad

The OPAx992 family is available in the WSON-8 (DSG) package which features an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

7.3.11 Shutdown

The OPAx992S devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 40 µA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V– + 20 V. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V– + 20 V or V+, whichever is lower. Exceeding V– + 20V or V+, whichever is lower, will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 15 µs; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx992S family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to V- is required. If using the OPAx992S without a load, the resulting turnoff time significantly increases.

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7.4 Device Functional Modes

The OPAx992 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx992 is 40 V (±20 V).

The OPAx992S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode.

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8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx992 family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 10.6-MHz bandwidth and high output drive. These features make the OPAx992 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Low-Side Current Measurement

图 8-1 shows the OPA992 configured in a low-side current sensing application. For a full analysis of the circuit shown in 图 8-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

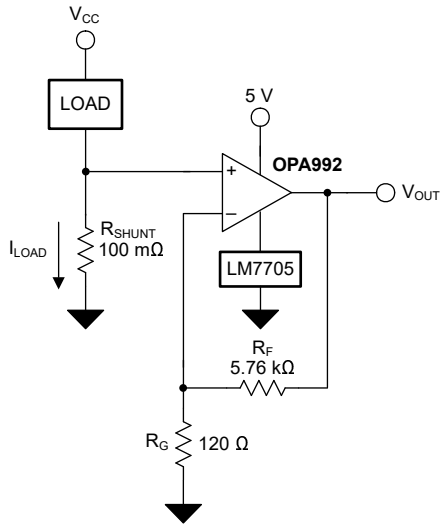


图 8-1. OPAx992 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Max output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 8-1 is given in 方程式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

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The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 方程式 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using 方程式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA992 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA992 to produce the necessary output voltage is calculated using 方程式 3:

$$Gain = \frac{\left(V_{OUT_MAX} - V_{OUT_MIN}\right)}{\left(V_{IN_MAX} - V_{IN_MIN}\right)} \quad (3)$$

Using 方程式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 方程式 4 is used to size the resistors, R_F and R_G, to set the gain of the OPA992 to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \quad (4)$$

Choosing R_F as 5.76 kΩ, R_G is calculated to be 120 Ω. R_F and R_G were chosen as 5.76 kΩ and 120 Ω because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors will generate thermal noise that exceeds the intrinsic noise of the op amp. 图 8-2 shows the measured transfer function of the circuit shown in 图 8-1.

8.2.1.3 Application Curve

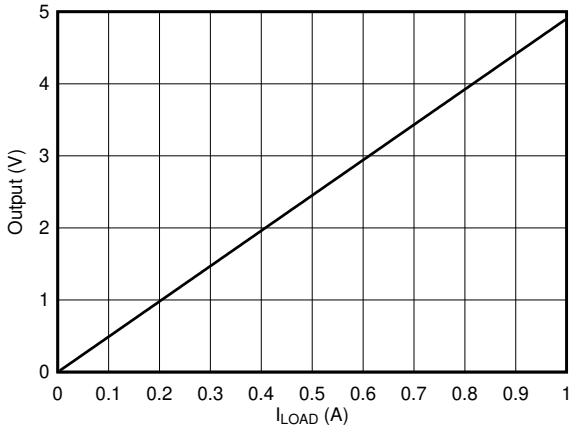


图 8-2. Low-Side, Current-Sense, Transfer Function

8.2.2 High Voltage Buffered Multiplexer

The OPAx992S shutdown devices can be configured to create a high voltage, buffered multiplexer. Outputs can be connected together on a common bus and the shutdown pins can be used to select the desired channel to pass through. Since the amplifier circuitry has been designed such that disable transitions occur significantly faster than enable transitions, the amplifier naturally exhibits a "break before make" switch topology. Amplifier outputs enter a high impedance state when placed in shutdown, so there is no risk of bus contention when connecting multiple channel outputs together. Additionally, because outputs are isolated from inputs, there is no concern about the impedance at the input of each channel interacting undesirably with the impedance at the output, like an amplifier gain stage or ADC driver circuit. Also, because this topology uses amplifiers instead of

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MOSFET switches, other common issues with multiplexers such as charge injection or signal error due to R_{ON} effects are eliminated.

图 8-3 shows an example topology for a basic 2:1 multiplexer. When SEL is low, channel 1 is selected and active; when SEL is high, channel 2 is selected and active. For more information on how to use the OPAx992S shutdown function, see the shutdown section in 节 6.7.

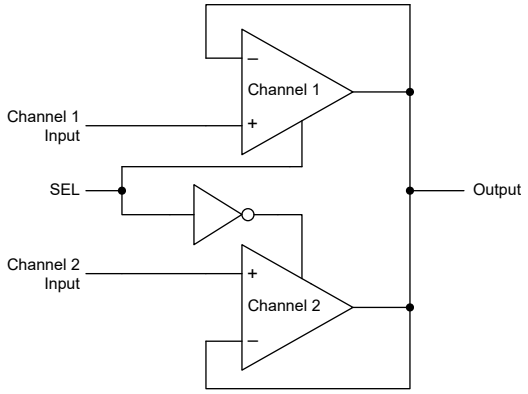


图 8-3. High Voltage Buffered Multiplexer

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9 Power Supply Recommendations

The OPAx992 is specified for operation from 2.7 V to 40 V (±1.35 V to ±20 V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see 节 6.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to 节 10.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 10-2, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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10.2 Layout Example

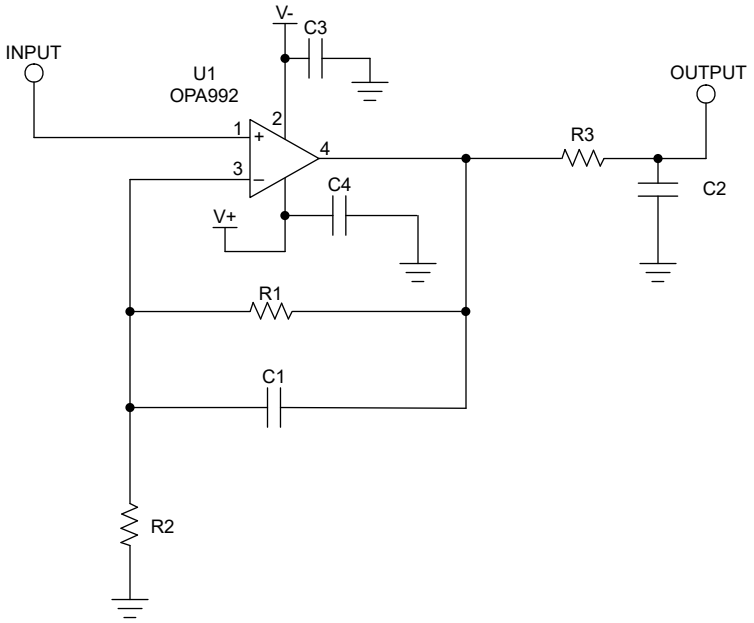


图 10-1. Schematic for Noninverting Configuration Layout Example

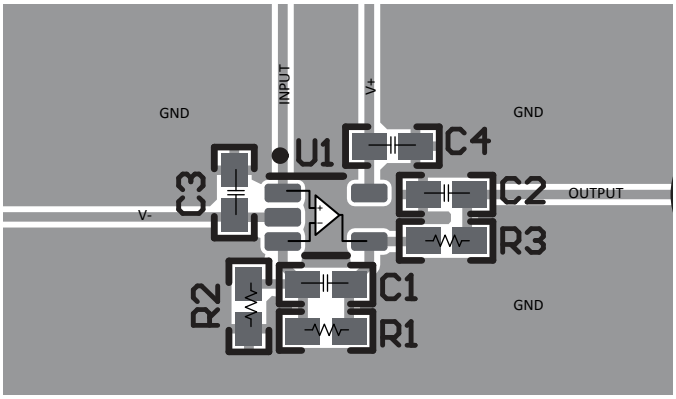


图 10-2. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.2 Documentation Support

11.2.1 Related Documentation

Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

Texas Instruments, *0-1-A, Single-Supply, Low-Side, Current Sensing Solution* reference design (TIPD129)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

TINA-TI™ is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
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TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2992IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92F	Samples
OPA2992IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2JUT	Samples
OPA2992IDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992D	Samples
OPA2992IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92G	Samples
OPA2992IPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2992PW	Samples
OPA4992IDR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4992D	Samples
OPA4992IPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4992PW	Samples
OPA992IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92DB	Samples
OPA992IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1JS	Samples
OPA992SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O92SD	Samples
POPA2992IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2992IDGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2992IDR	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2992IDSGR	ACTIVE	WSON	DSG	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2992IPWR	ACTIVE	TSSOP	PW	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2992SIRUGR	ACTIVE	X2QFN	RUG	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA4992IPWR	ACTIVE	TSSOP	PW	14	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA992IDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA992IDCKR	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA992SIDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

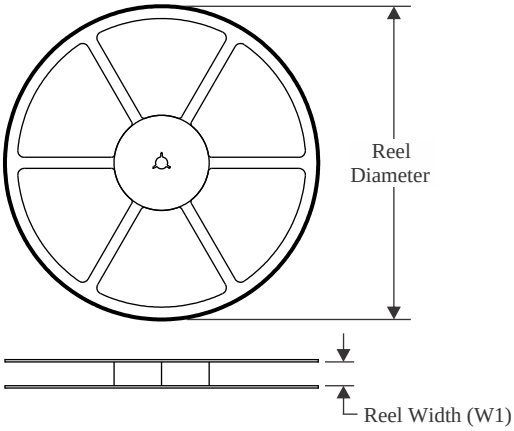
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

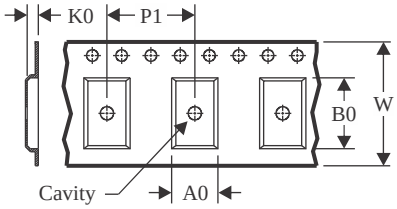
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

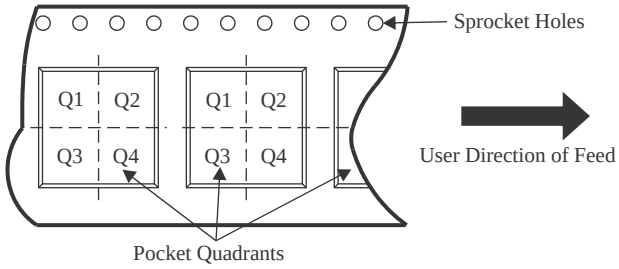


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

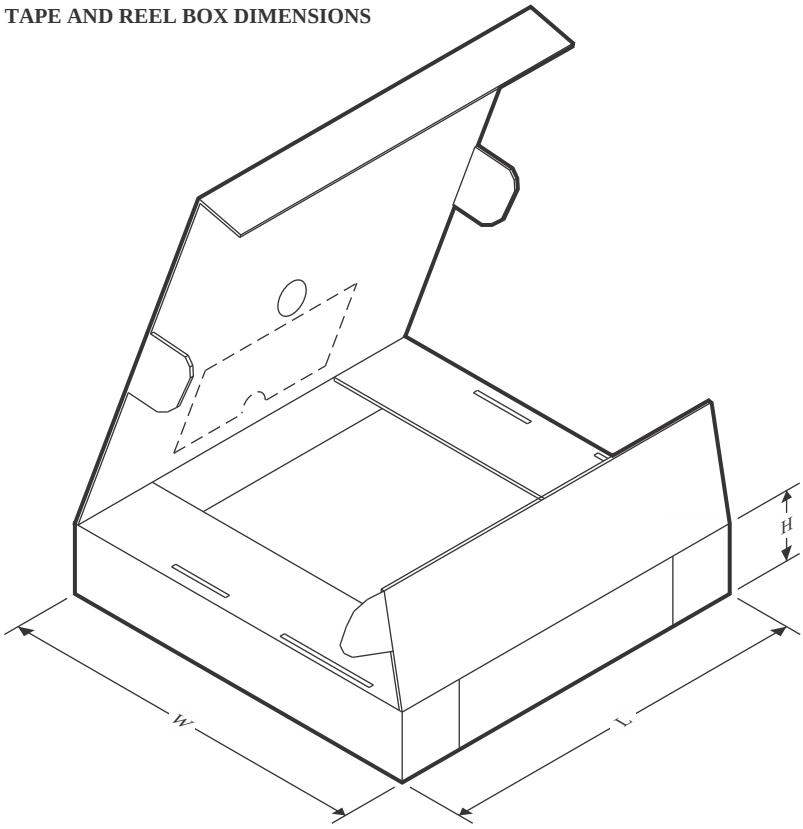
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2992IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2992IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2992IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2992IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2992IPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
OPA4992IDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4992IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA992IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA992SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

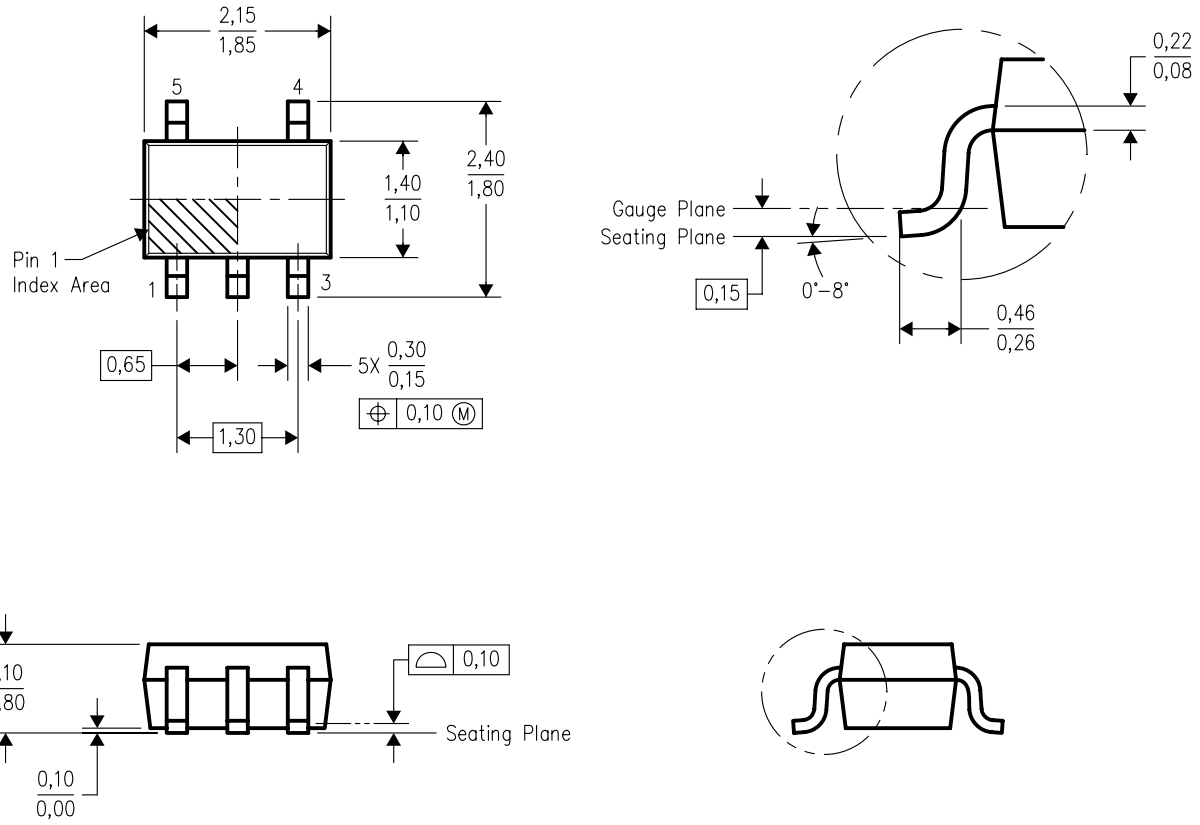
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2992IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
OPA2992IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2992IDR	SOIC	D	8	3000	356.0	356.0	35.0
OPA2992IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2992IPWR	TSSOP	PW	8	3000	356.0	356.0	35.0
OPA4992IDR	SOIC	D	14	3000	356.0	356.0	35.0
OPA4992IPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
OPA992IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA992SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0

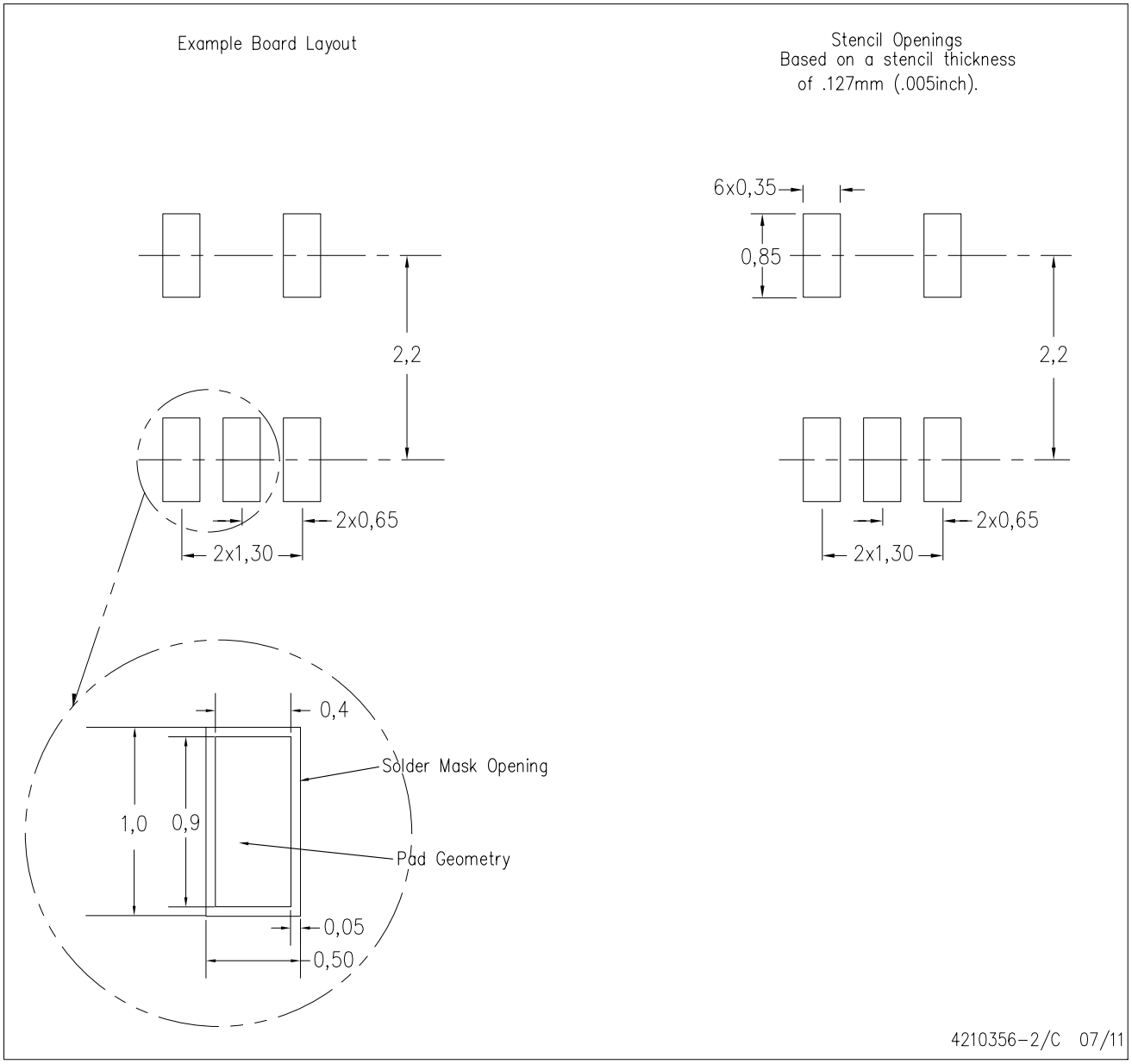
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



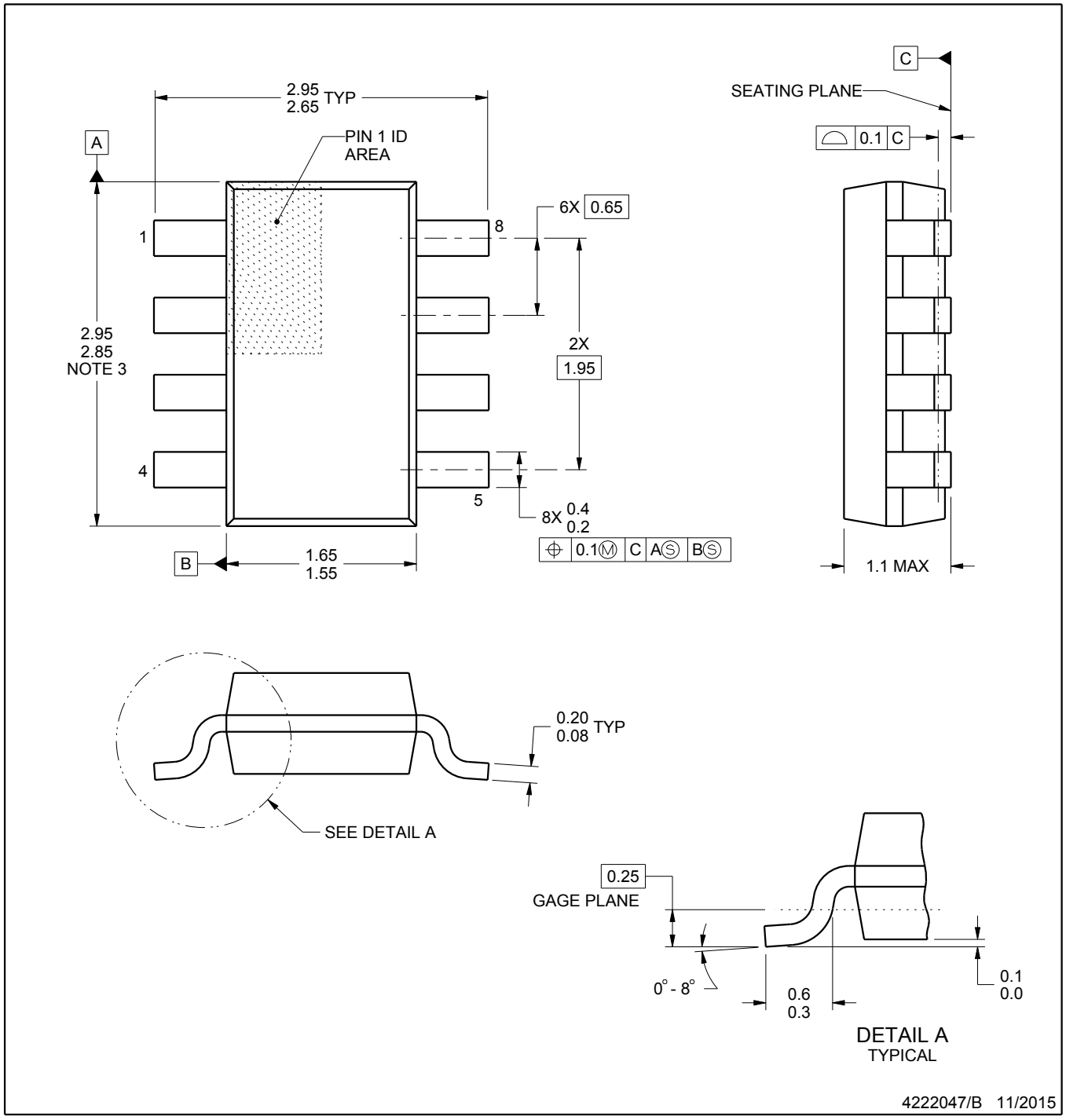
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DDF0008A

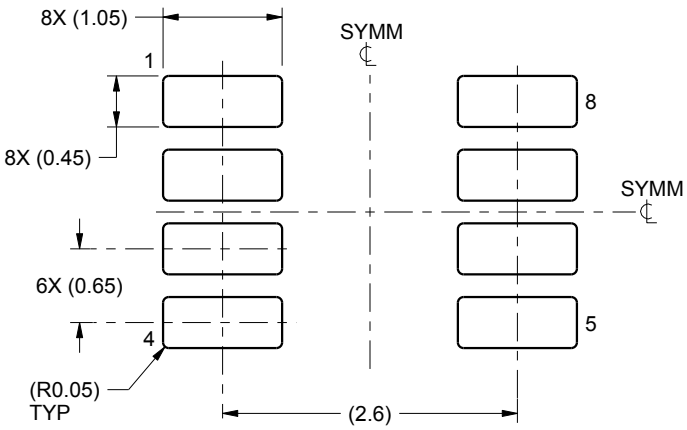
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

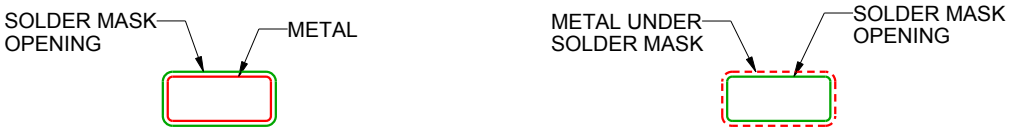


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

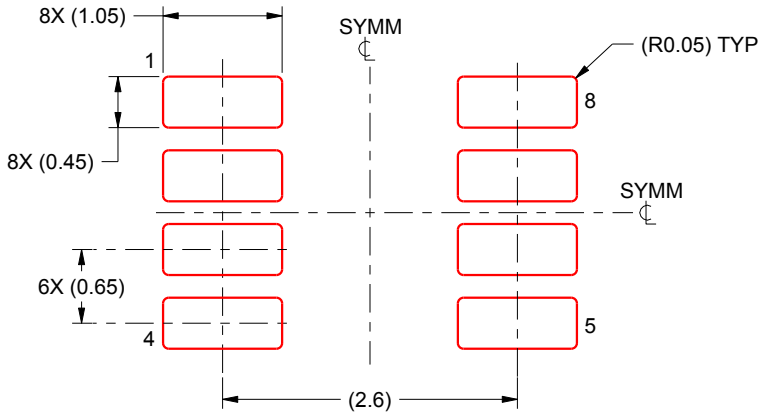
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

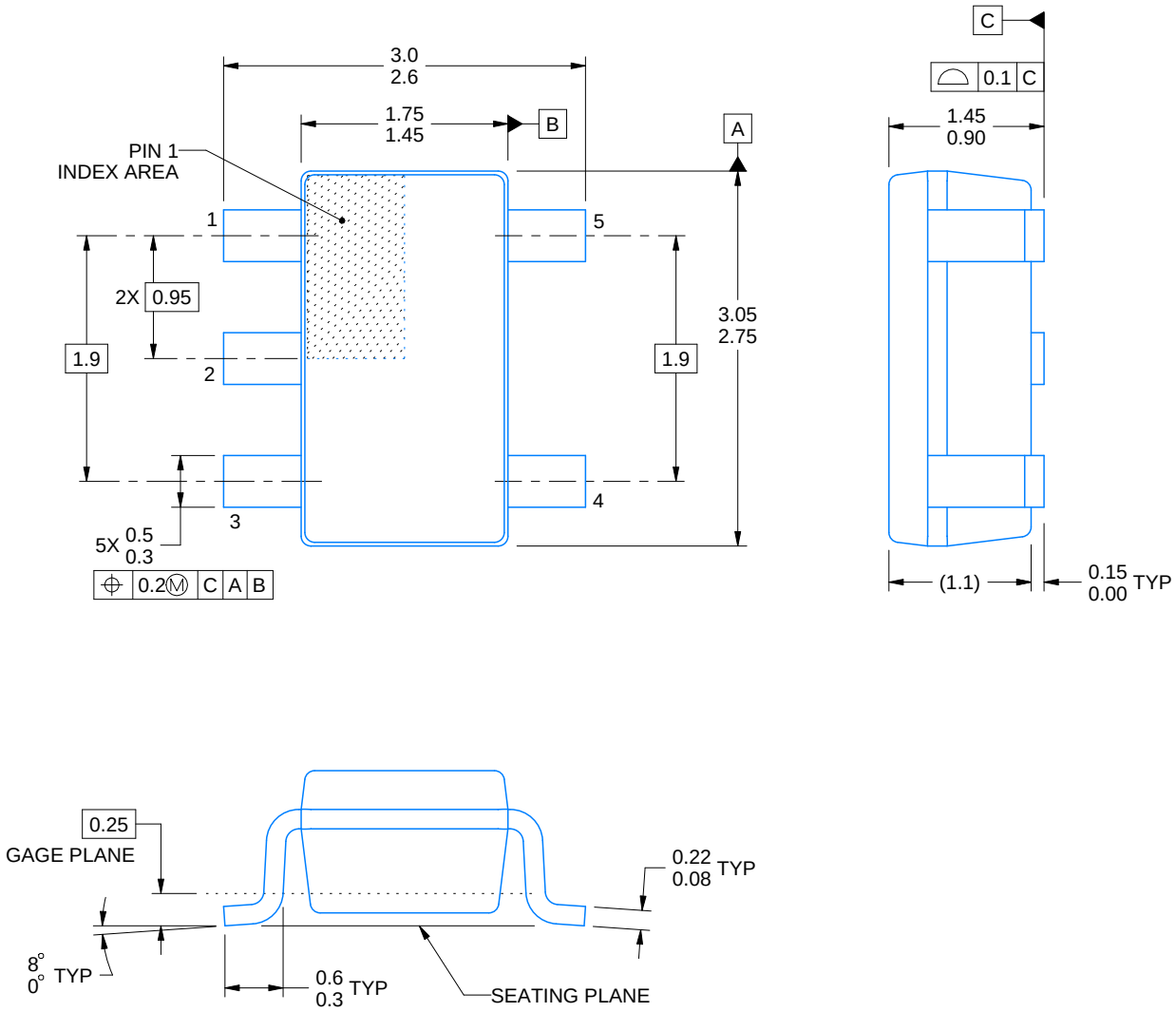
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

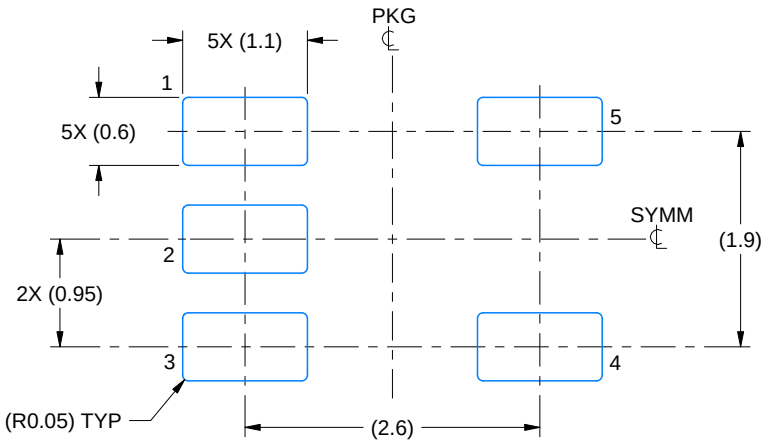
SMALL OUTLINE TRANSISTOR



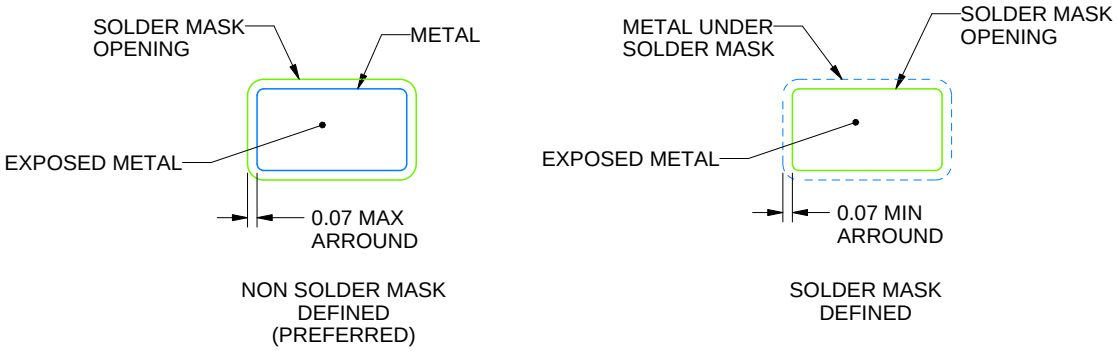
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

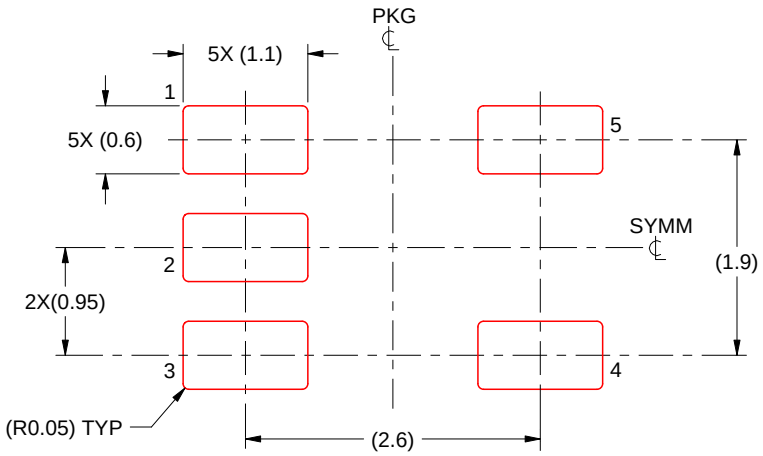


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



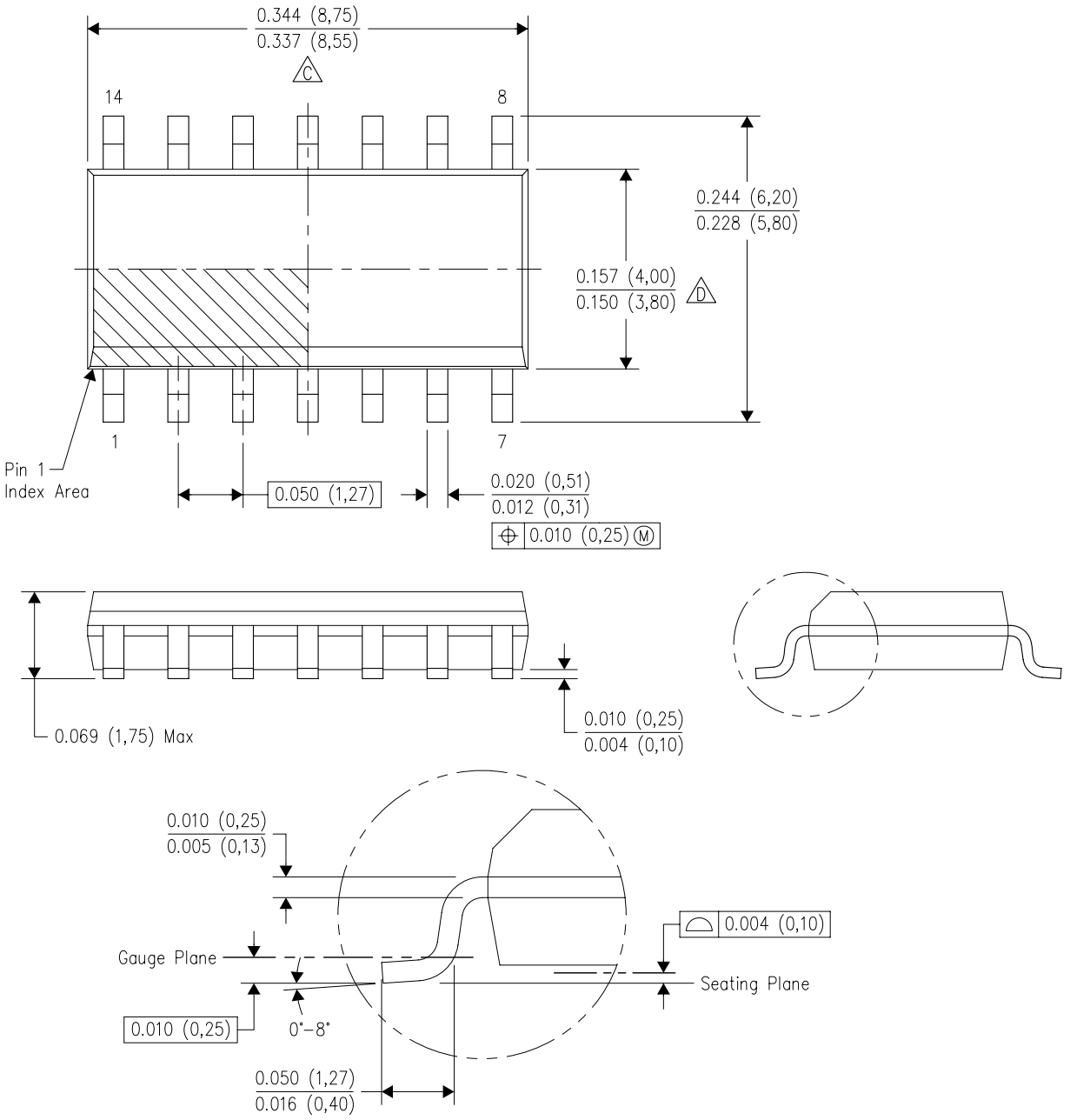
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

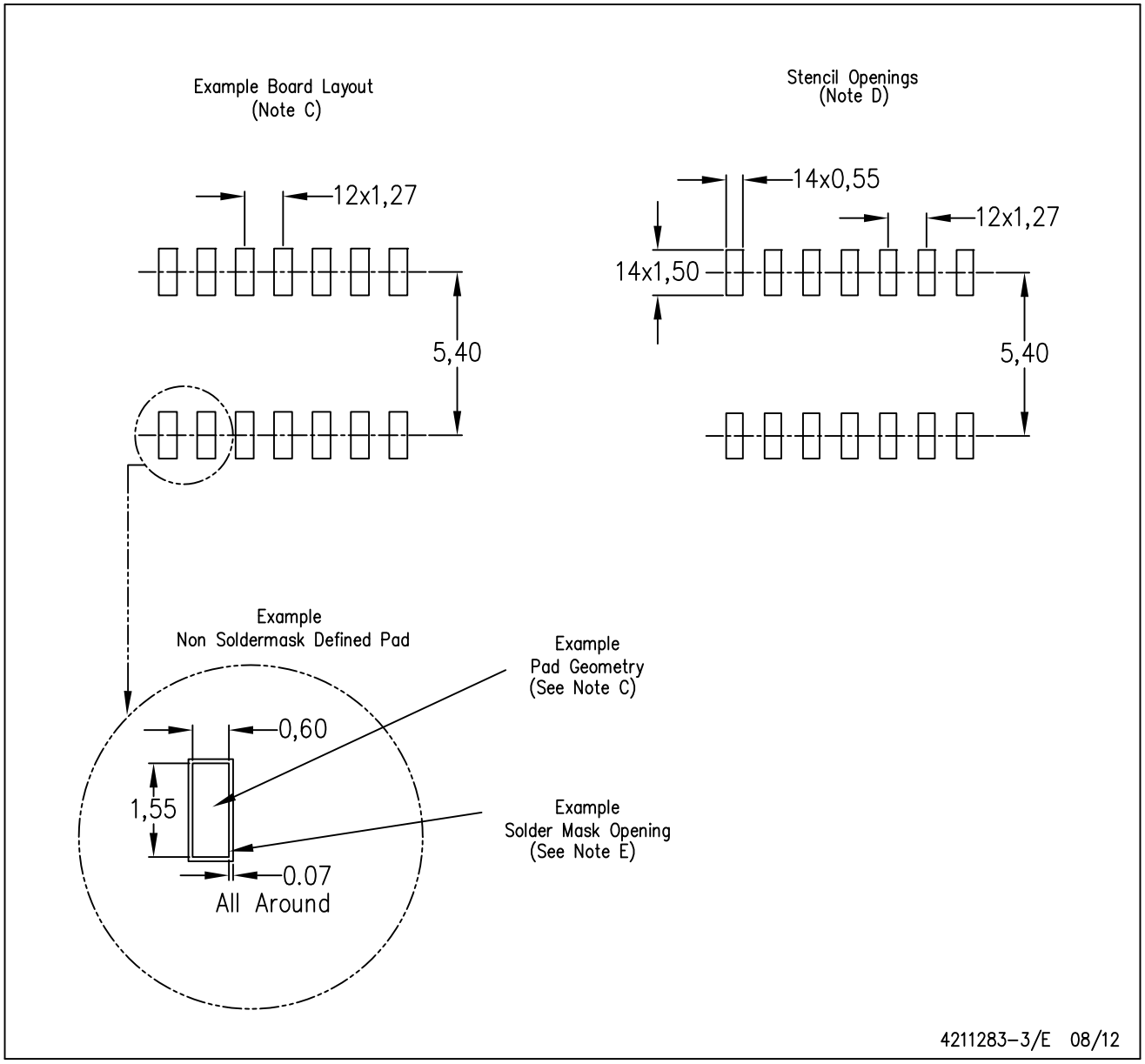
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

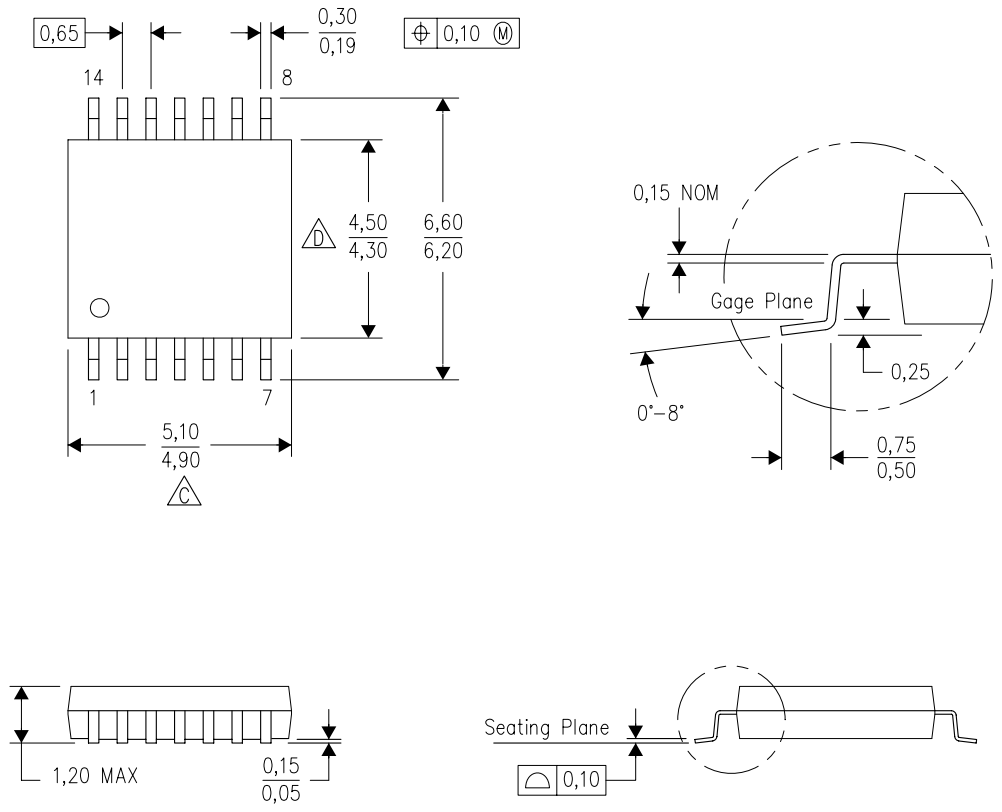
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

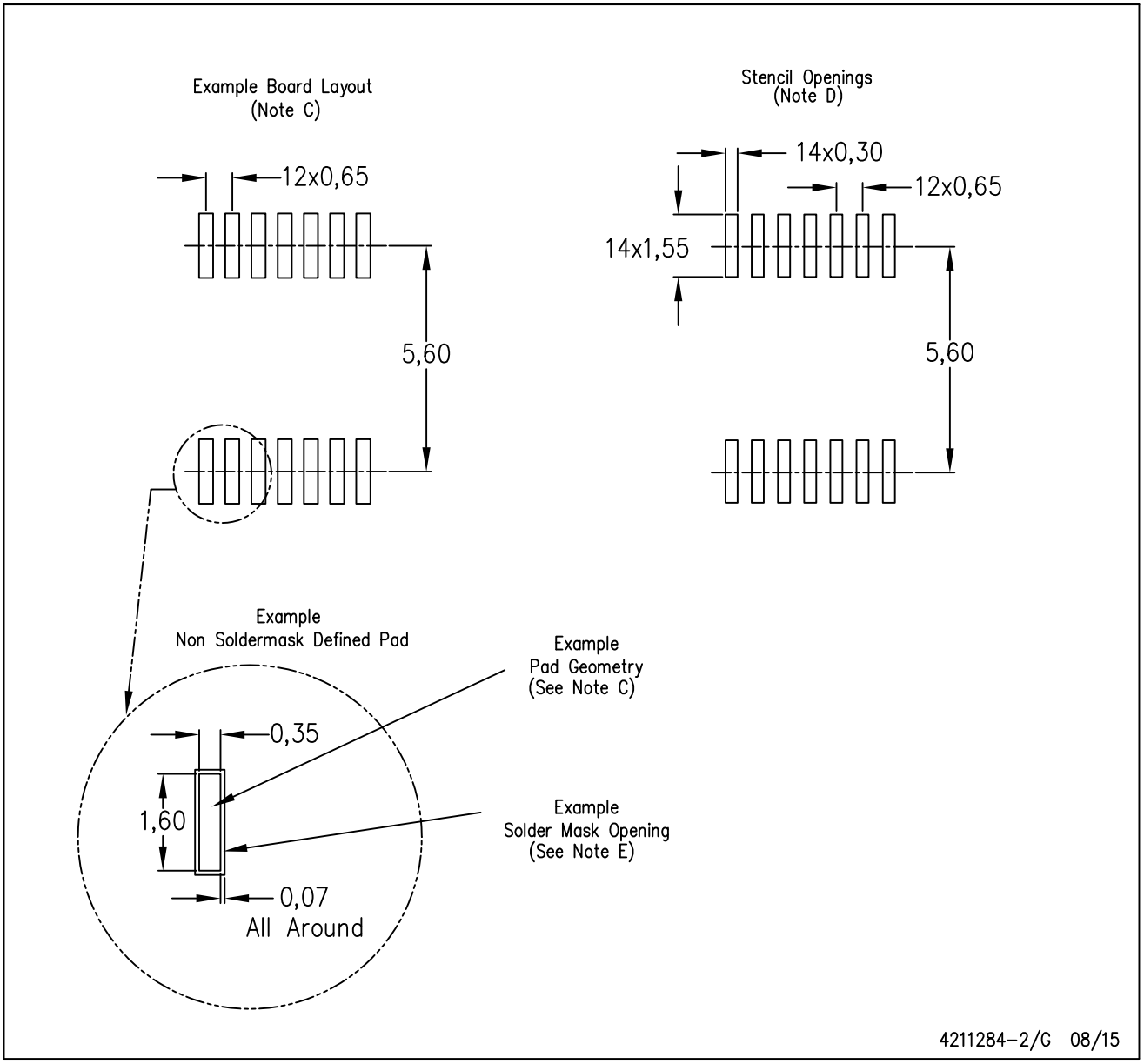
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

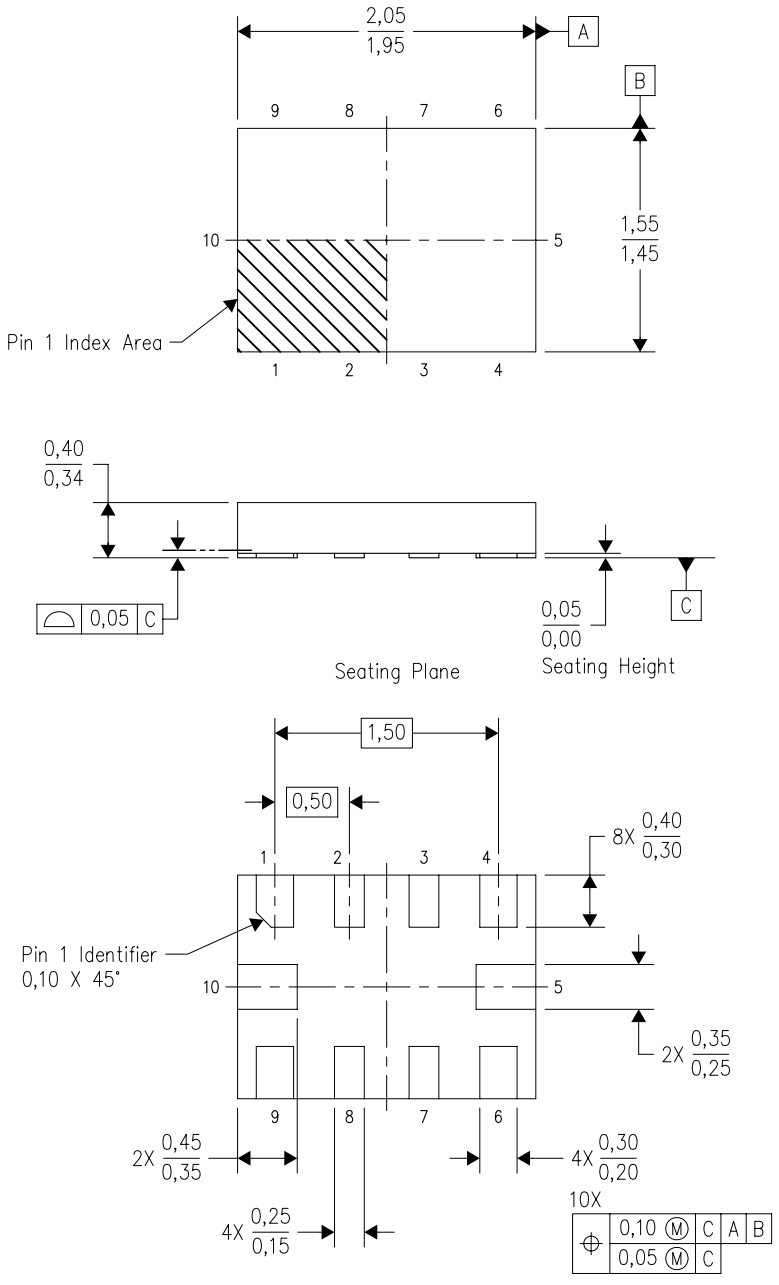
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



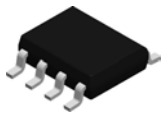
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

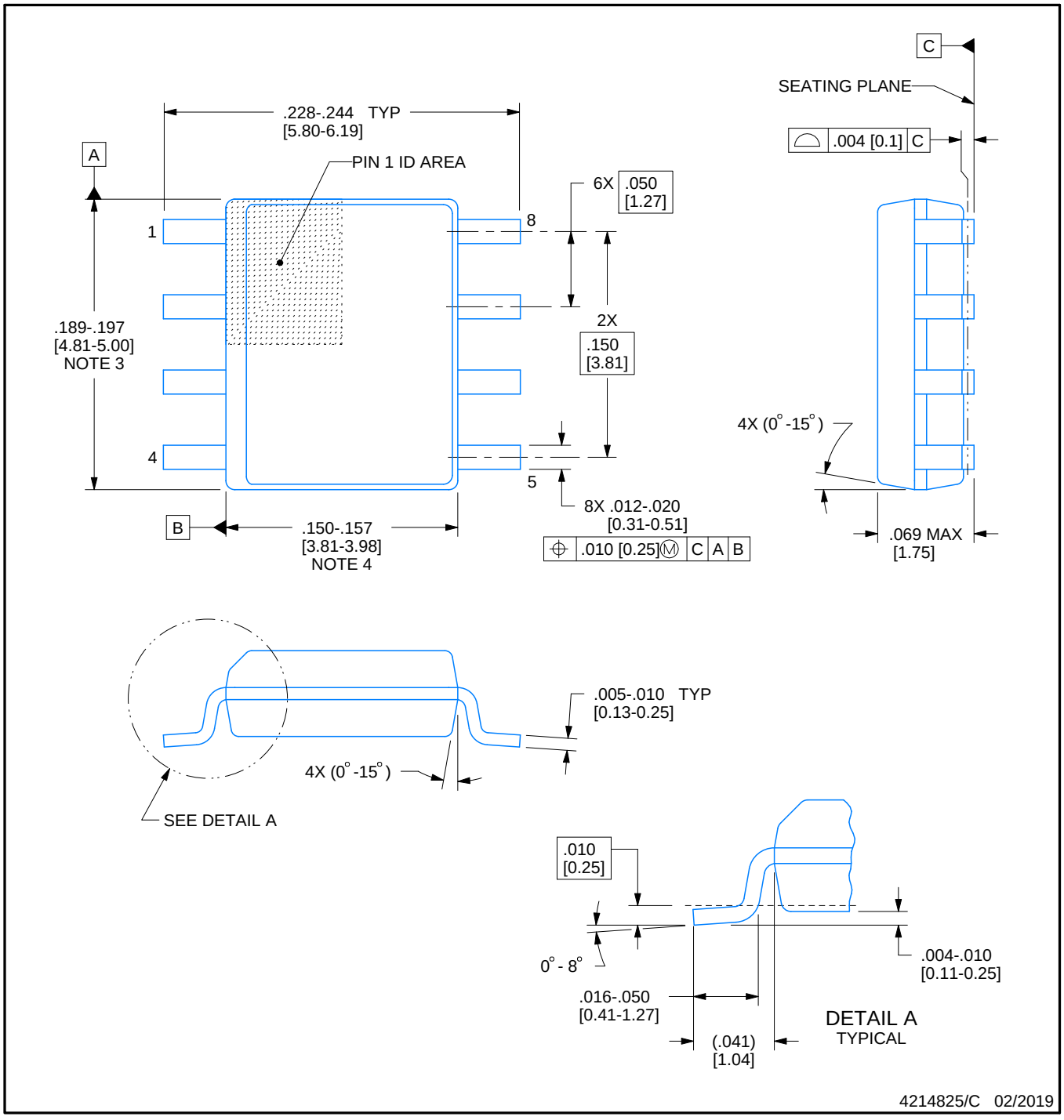


PACKAGE OUTLINE

D0008A

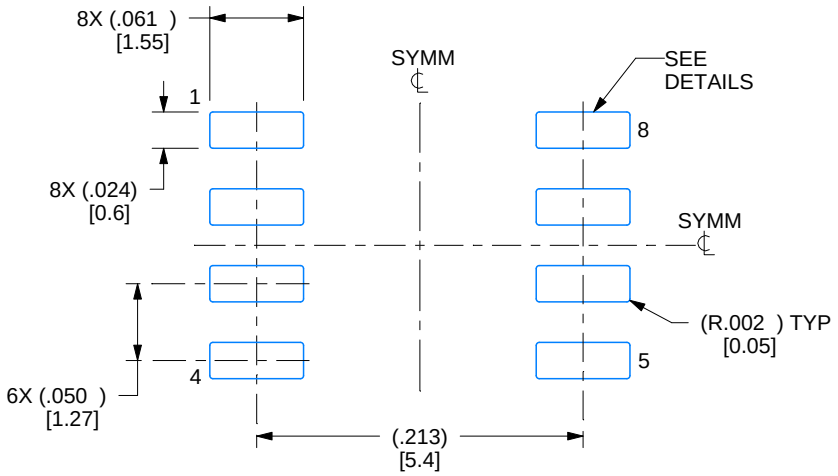
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

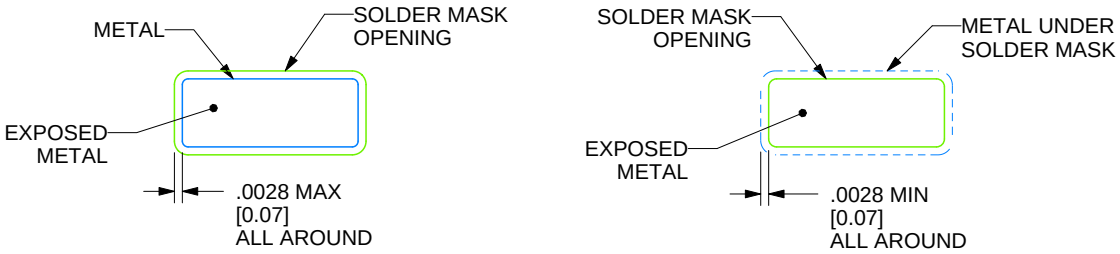


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

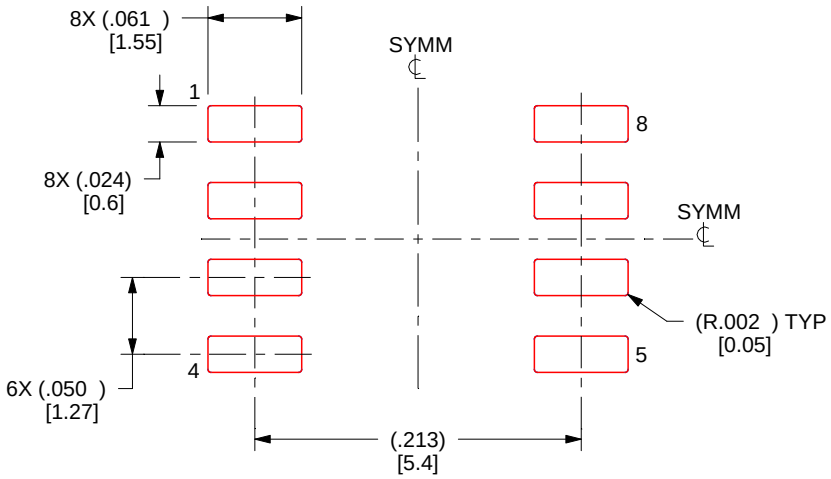
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

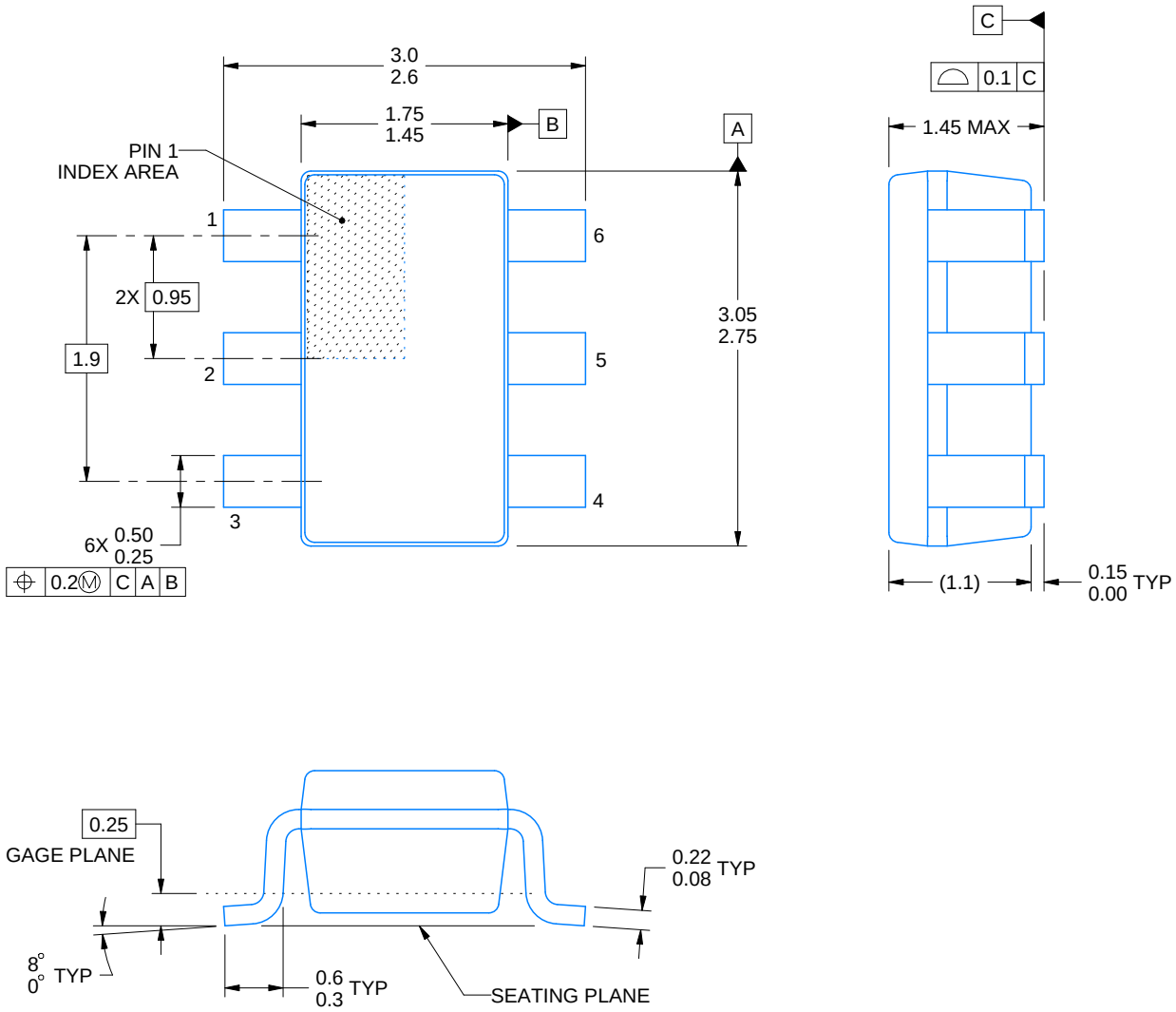
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

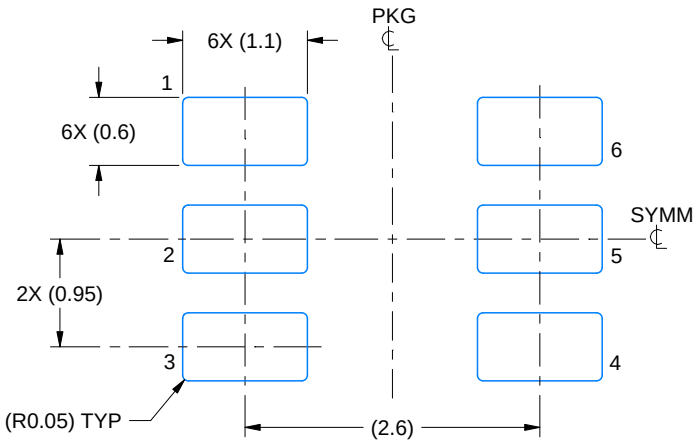
SMALL OUTLINE TRANSISTOR



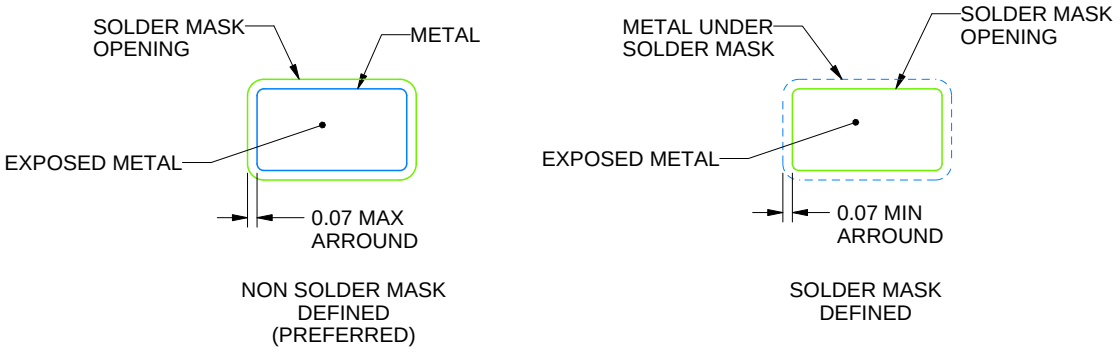
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

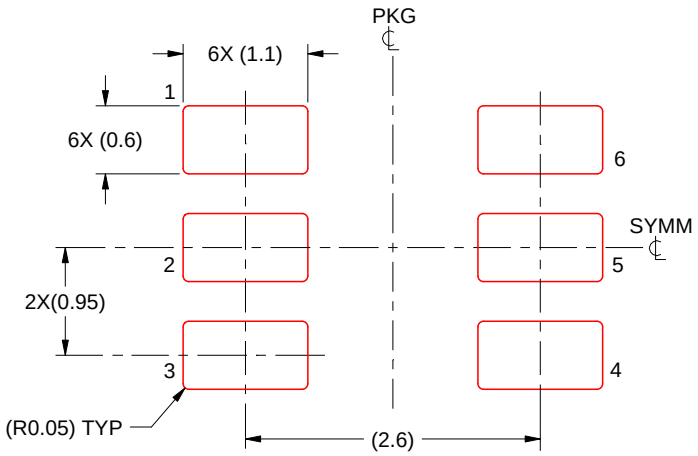


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



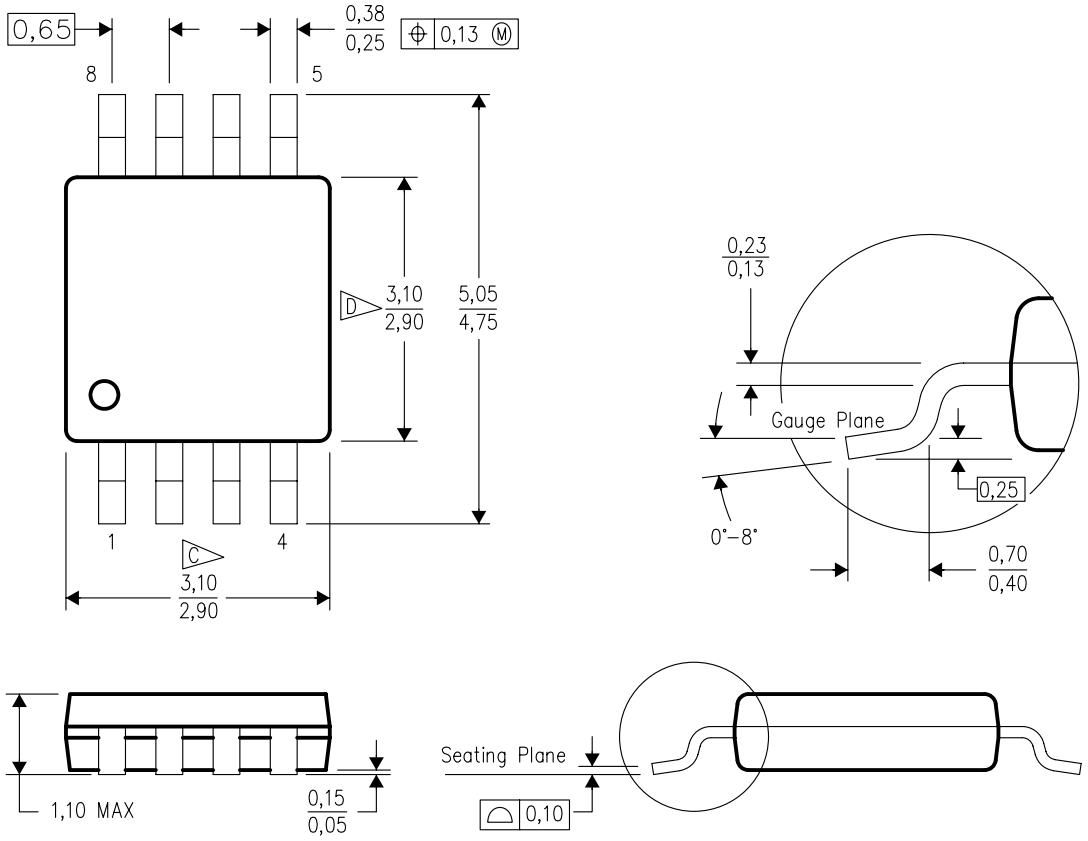
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

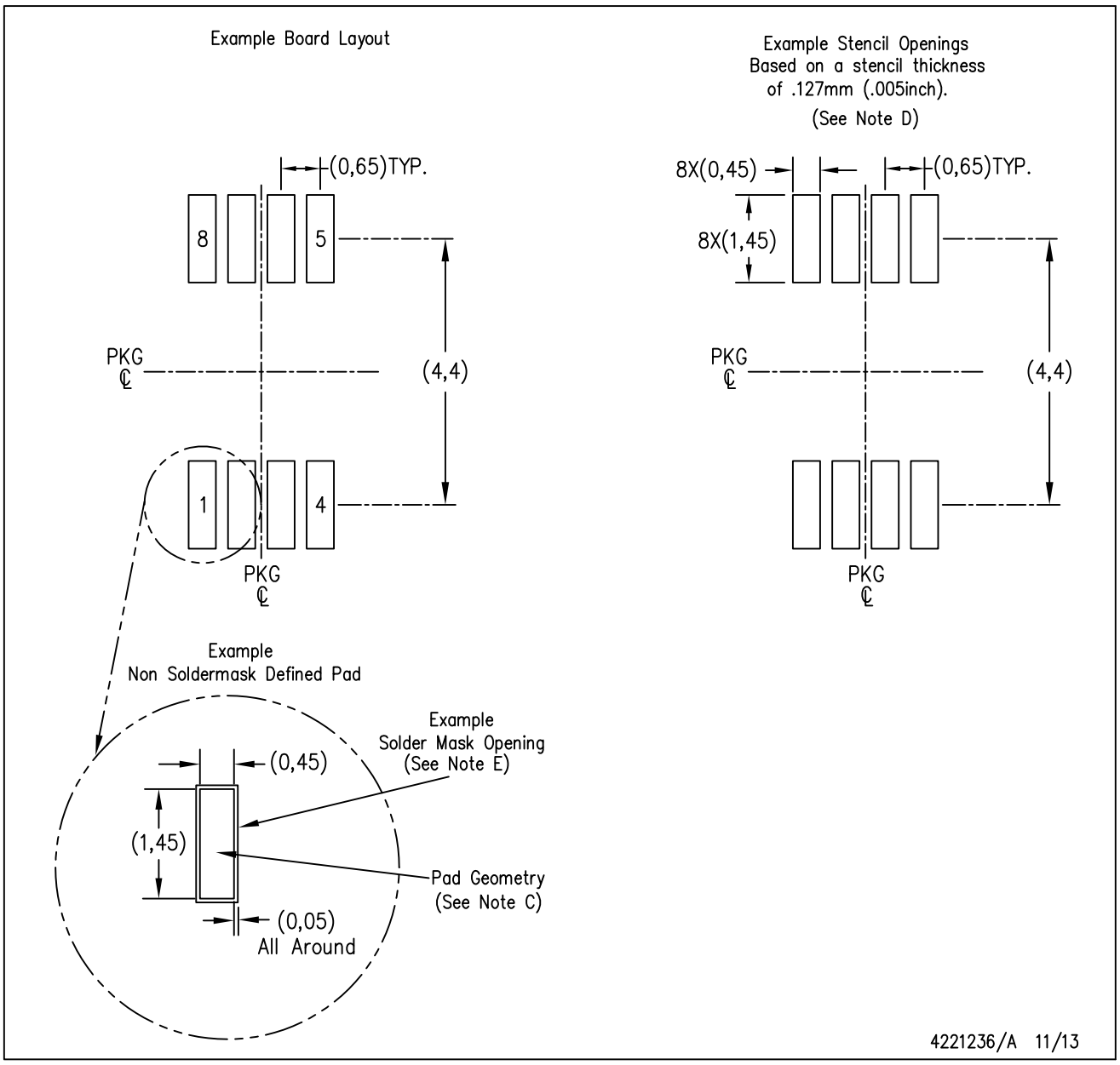
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

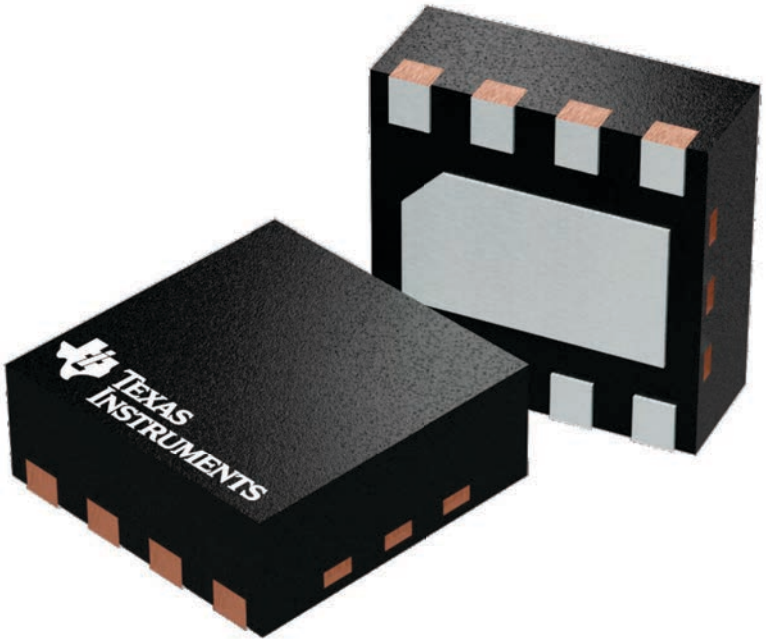
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



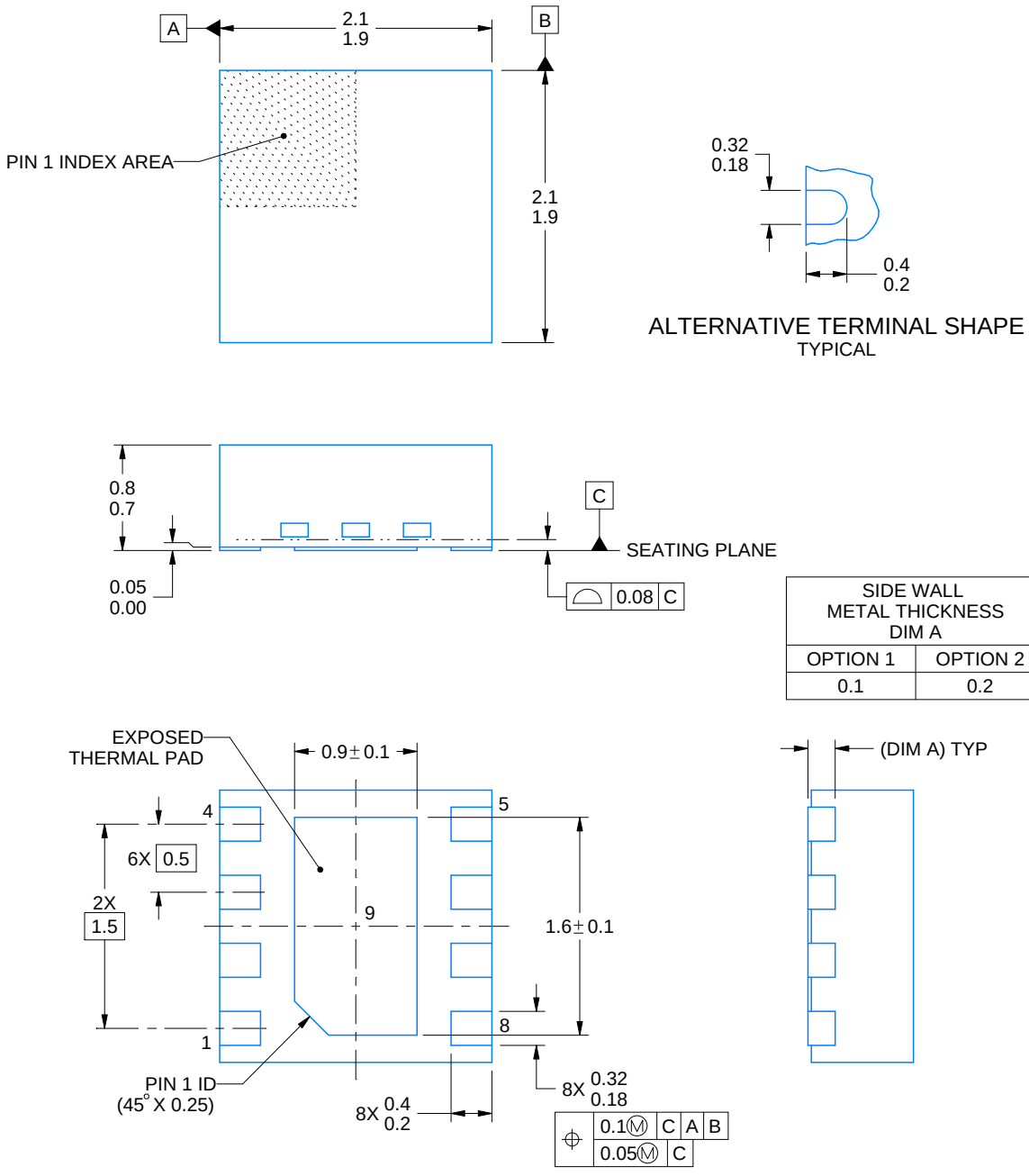
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

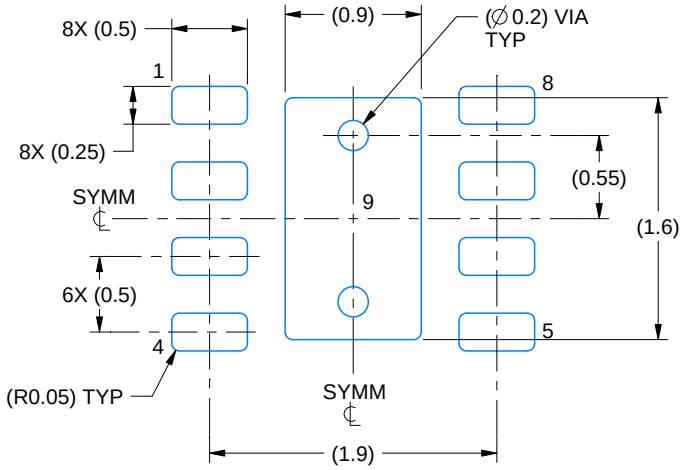
PLASTIC SMALL OUTLINE - NO LEAD



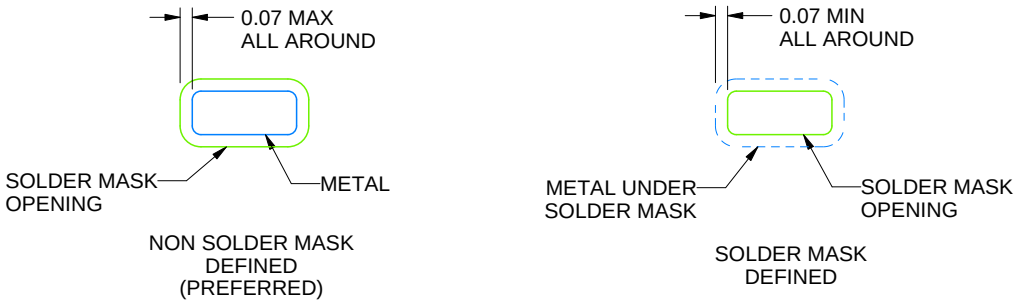
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

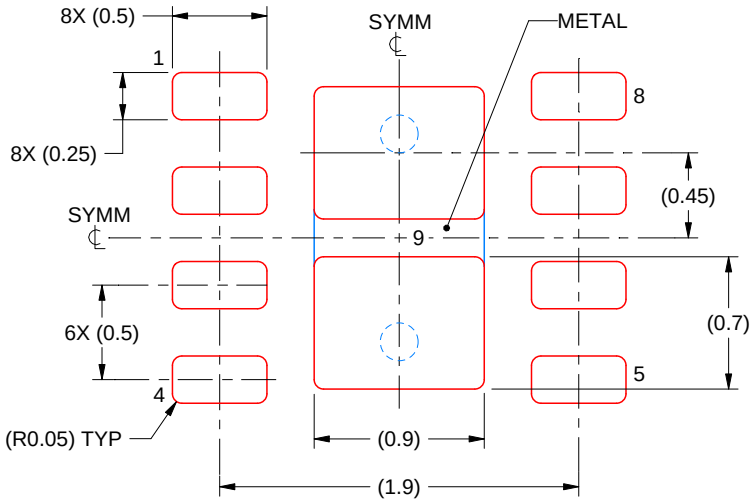


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

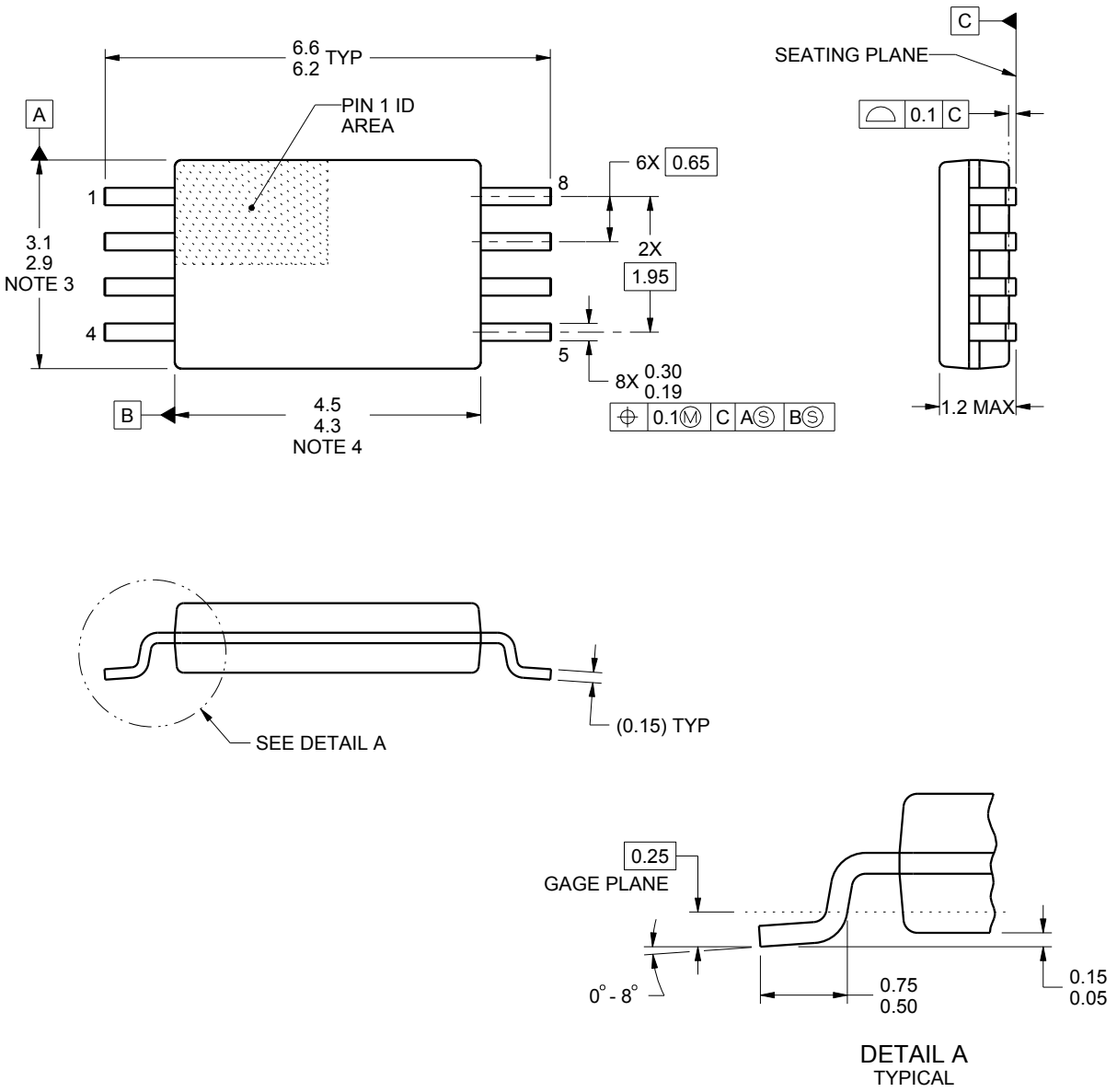
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

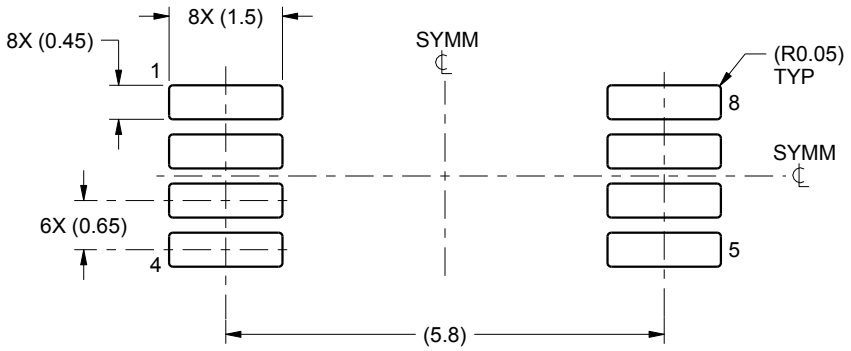
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

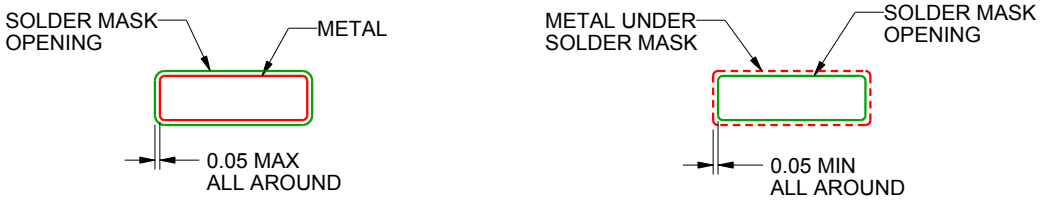


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

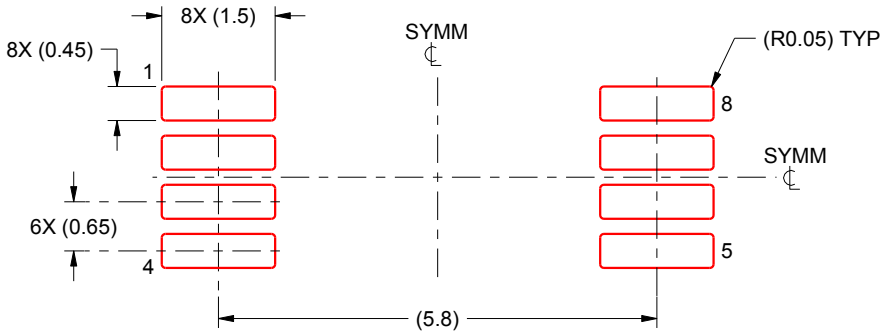


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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