



DMOS

400mA Low-Dropout Regulator

FEATURES

- **CAP-FREE DMOS TOPOLOGY:**
Ultra Low Dropout Voltage:
250mV typ at 400mA
Output Capacitor *not* Required for Stability
- **UP TO 500mA PEAK, TYPICAL**
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE: 28μVrms**
- **HIGH ACCURACY: ±1.5% max**
- **HIGH EFFICIENCY:**
 $I_{GND} = 850\mu A$ at $I_{OUT} = 400mA$
Not Enabled: $I_{GND} = 0.01\mu A$
- **2.5V, 2.85V, 3.0V, 3.3V, AND 5.0V OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**
SOT23-5 and MSOP-8

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

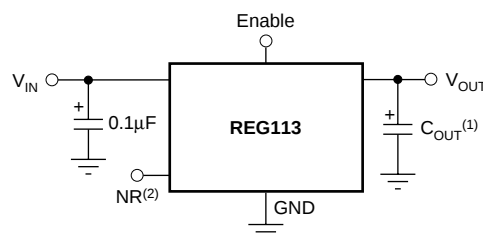
DESCRIPTION

The REG113 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 250mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1μF.

Typical ground pin current is only 850μA (at $I_{OUT} = 400mA$) and drops to 10nA when not enabled. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG113 has very low output noise (typically 28μVrms for $V_{OUT} = 3.3V$ with $C_{NR} = 0.01\mu F$), making it ideal for use in portable communications equipment. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG113 is well protected—internal circuitry provides a current limit which protects the load from damage, furthermore, thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG113 is available in SOT23-5 and MSOP-8 packages.



NOTES: (1) Optional. (2) NR = Noise Reduction.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Input Voltage, V_{IN}	–0.3V to 12V
Enable Input Voltage, V_{EN}	–0.3V to V_{IN}
NR Pin Voltage, V_{NR}	–0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (T_J)	–55°C to +125°C
Storage Temperature Range (T_A)	–65°C to +150°C
Lead Temperature (soldering, 3s)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC
DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	V_{OUT} ⁽²⁾
REG113xx-yyyy/zzz	XX is package designator. YYYY is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). ZZZ is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

PIN CONFIGURATIONS

Top View

SOT

(N Package)

MSOP

(E Package)

NOTE: Leads 5 through 8 are fused to the lead frame and can be used for improved thermal dissipation.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

At $T_J = +25^{\circ}\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $V_{ENABLE} = 1.8\text{V}$, $I_{OUT} = 5\text{mA}$, $C_{NR} = 0.01\mu\text{F}$, and $C_{OUT} = 0.1\mu\text{F}^{(1)}$, unless otherwise noted.

PARAMETER	CONDITION	REG113NA REG113EA			UNITS
		MIN	TYP	MAX	
OUTPUT VOLTAGE Output Voltage Range REG113-2.5 REG113-2.85 REG113-3 REG113-3.3 REG113-5 Accuracy Over Temperature vs Temperature vs Line and Load Over Temperature	V_{OUT} dV_{OUT}/dT $I_{OUT} = 5\text{mA to } 400\text{mA}$, $V_{IN} = (V_{OUT} + 0.4\text{V})$ to 10V $I_{OUT} = 5\text{mA to } 400\text{mA}$, $V_{IN} = (V_{OUT} + 0.6\text{V})$ to 10V		2.5 2.85 3.0 3.3 5.0 ± 0.5 50 ± 1	 ± 1.5 ± 2.3 ± 2.3 ± 2.3 ± 3.0	V V V V V % % ppm/ $^{\circ}\text{C}$ % %
DC DROPOUT VOLTAGE ⁽²⁾ For all models Over Temperature	V_{DROP} $I_{OUT} = 5\text{mA}$ $I_{OUT} = 400\text{mA}$ $I_{OUT} = 400\text{mA}$		4 250	10 325 410	mV mV mV
VOLTAGE NOISE $f = 10\text{Hz to } 100\text{kHz}$ Without C_{NR} With C_{NR}	V_N $C_{NR} = 0$, $C_{OUT} = 0$ $C_{NR} = 0.01\mu\text{F}$, $C_{OUT} = 10\mu\text{F}$		$23\mu\text{Vrms/V} \cdot V_{OUT}$ $7\mu\text{Vrms/V} \cdot V_{OUT}$		μVrms μVrms
OUTPUT CURRENT Current Limit ⁽³⁾ Over Temperature Short-Circuit Current Limit	I_{CL} I_{SC}	425	500 200	575 600	mA mA mA
RIPPLE REJECTION $f = 120\text{Hz}$			65		dB
ENABLE CONTROL V_{ENABLE} HIGH (output enabled) V_{ENABLE} LOW (output disabled) I_{ENABLE} HIGH (output enabled) I_{ENABLE} LOW (output disabled) Output Disable Time Output Enable Softstart Time	V_{ENABLE} I_{ENABLE} $V_{ENABLE} = 1.8\text{V to } V_{IN}$, $V_{IN} = 1.8\text{V to } 6.5^{(4)}$ $V_{ENABLE} = 0\text{V to } 0.5\text{V}$ $C_{OUT} = 1.0\mu\text{F}$, $R_{LOAD} = 13\Omega$ $C_{OUT} = 1.0\mu\text{F}$, $R_{LOAD} = 13\Omega$	1.8 -0.2	1 2 50 1.5	V_{IN} 0.5 100 100	V V nA nA μs ms
THERMAL SHUTDOWN Junction Temperature Shutdown Reset from Shutdown			160 140		$^{\circ}\text{C}$ $^{\circ}\text{C}$
GROUND PIN CURRENT Ground Pin Current Enable Pin LOW	I_{GND} $I_{OUT} = 5\text{mA}$ $I_{OUT} = 400\text{mA}$ $V_{ENABLE} \leq 0.5\text{V}$		400 850 0.01	500 1000 0.2	μA μA μA
INPUT VOLTAGE Operating Input Voltage Range ⁽⁵⁾ Specified Input Voltage Range Over Temperature	V_{IN} $V_{IN} > 1.8\text{V}$ $V_{IN} > 1.8\text{V}$	1.8 $V_{OUT} + 0.4$ $V_{OUT} + 0.6$		10 10 10	V V V
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT23-5 Surface-Mount MSOP-8 Surface-Mount	T_J T_J T_A θ_{JA} θ_{JC} θ_{JA} Junction-to-Ambient Junction-to-Case Junction-to-Ambient	-40 -55 -65	 200 35 ⁽⁶⁾ 160 ⁽⁶⁾	+85 +125 +150	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$

NOTES: (1) The REG113 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.

(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at $V_{IN} = V_{OUT} + 1\text{V}$ at fixed load.

(3) Current limit is the output current that produces a 10% change in output voltage from $V_{IN} = V_{OUT} + 1\text{V}$ and $I_{OUT} = 5\text{mA}$.

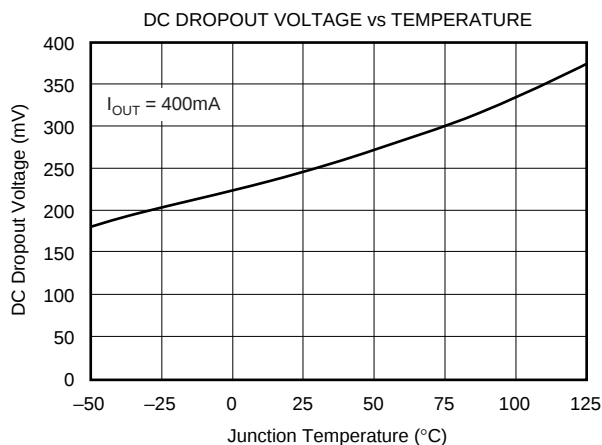
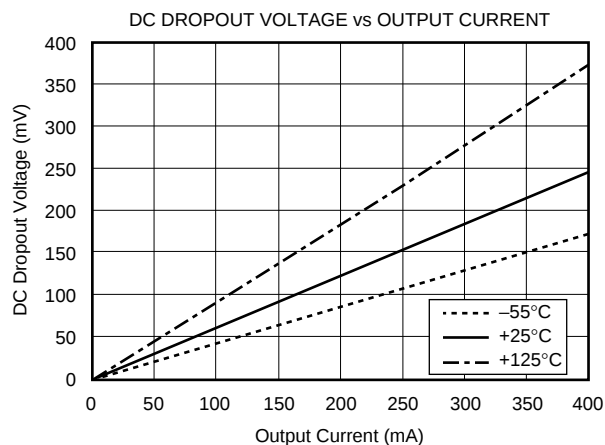
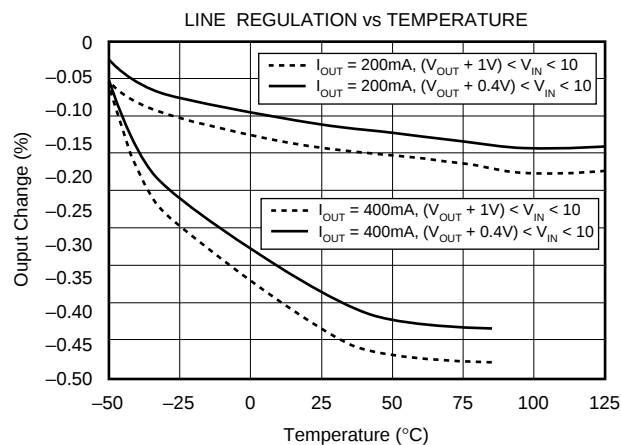
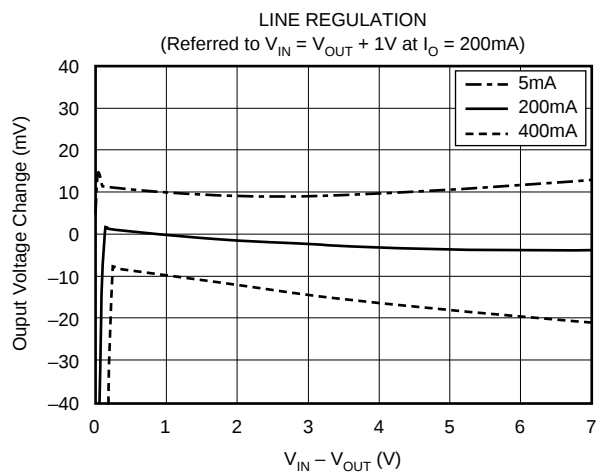
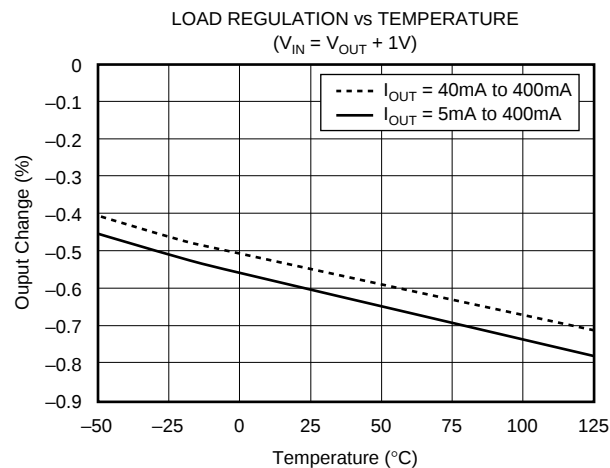
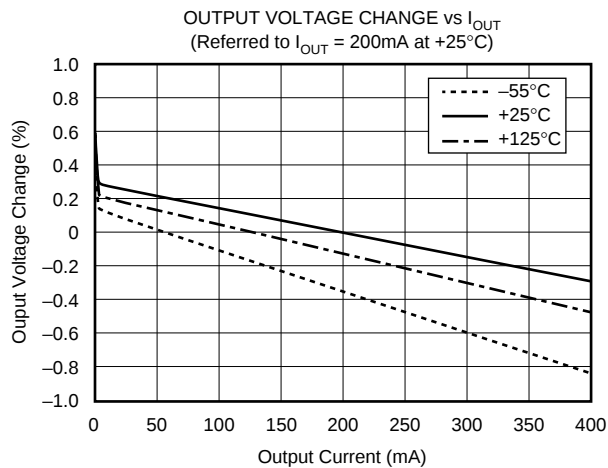
(4) For $V_{ENABLE} > 6.5\text{V}$, see typical characteristic I_{ENABLE} vs V_{ENABLE} .

(5) The REG113 no longer regulates when $V_{IN} < V_{OUT} + V_{DROP(MAX)}$. In dropout, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at $T_J = +25^{\circ}\text{C}$.

(6) See Figure 7.

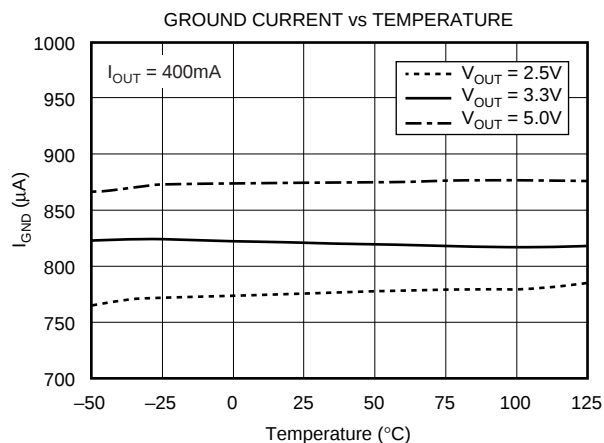
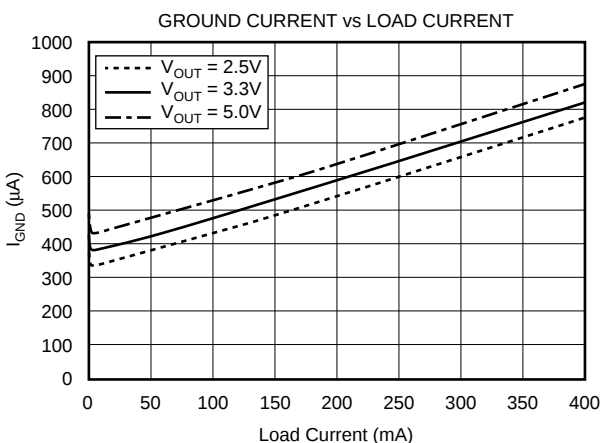
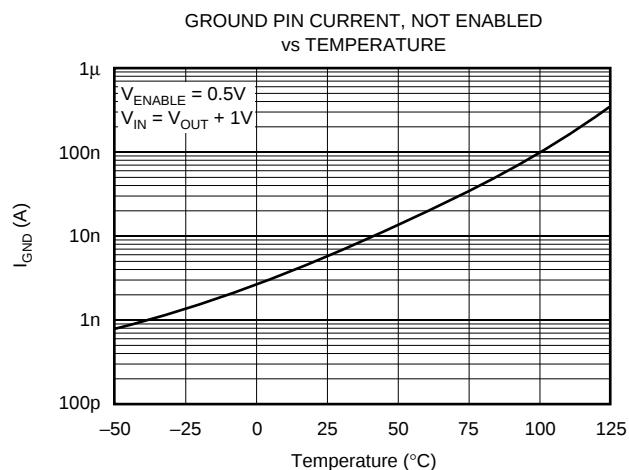
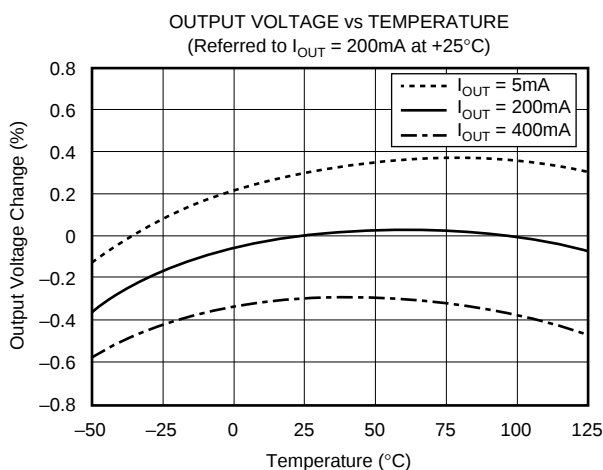
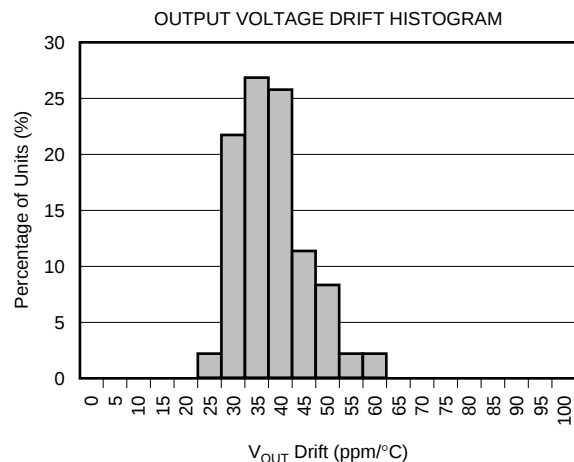
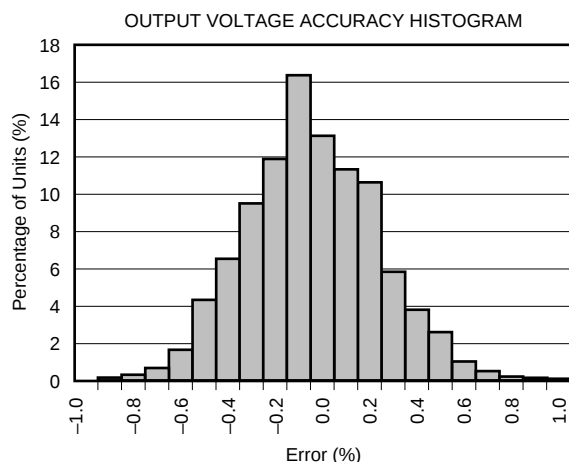
TYPICAL CHARACTERISTICS

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



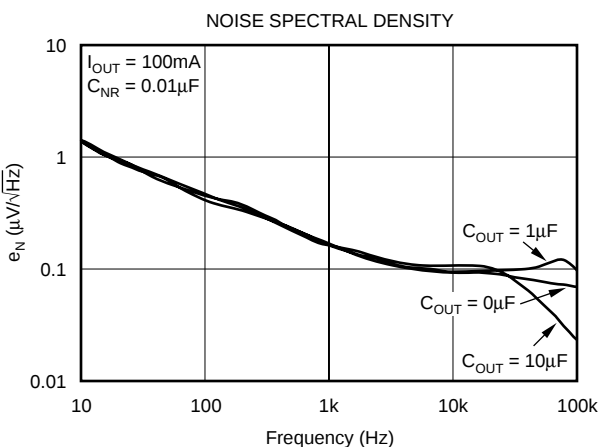
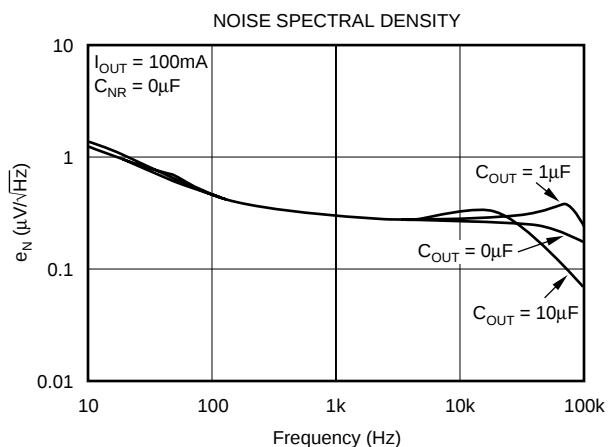
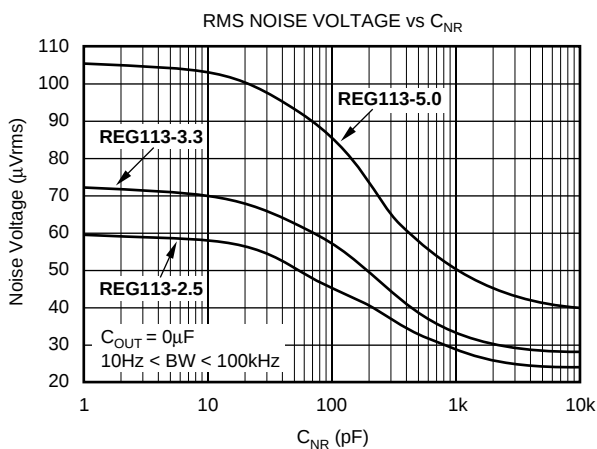
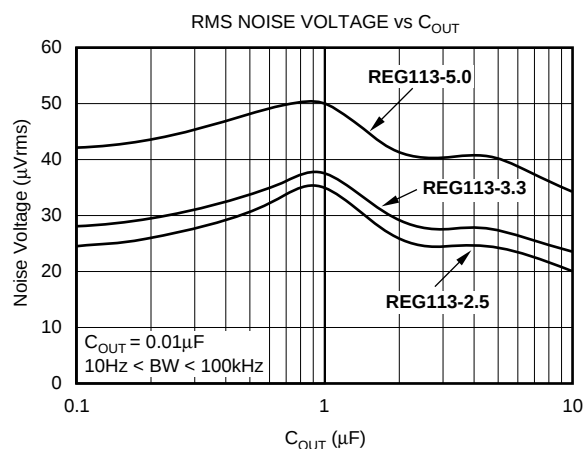
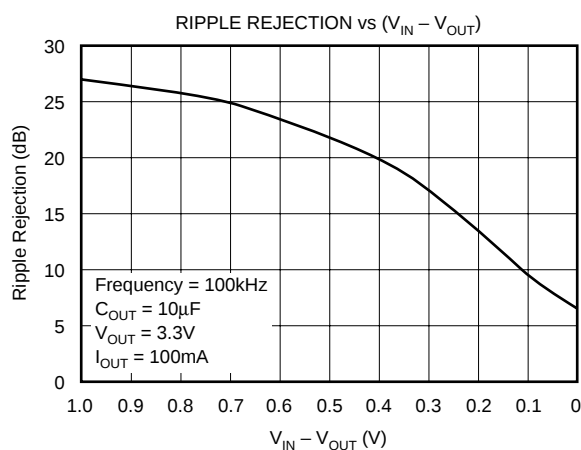
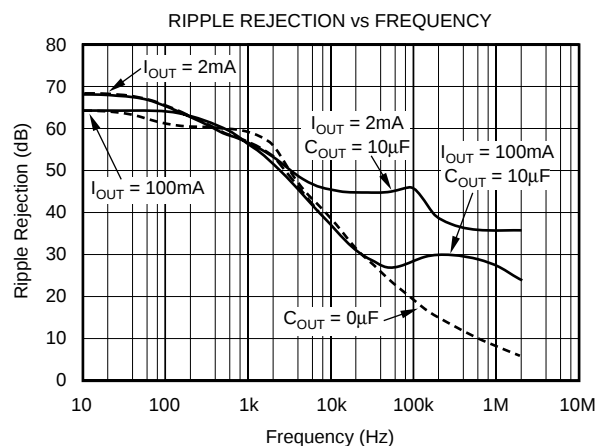
TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



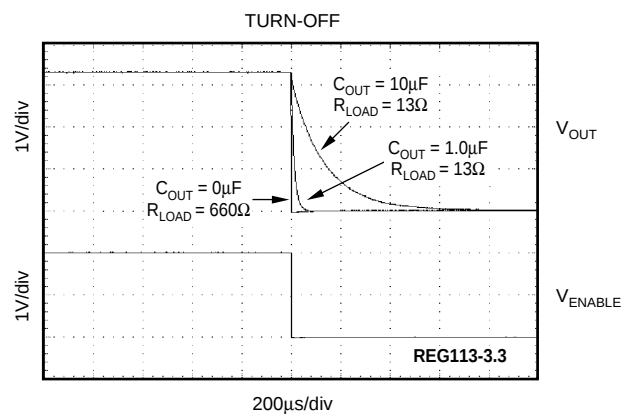
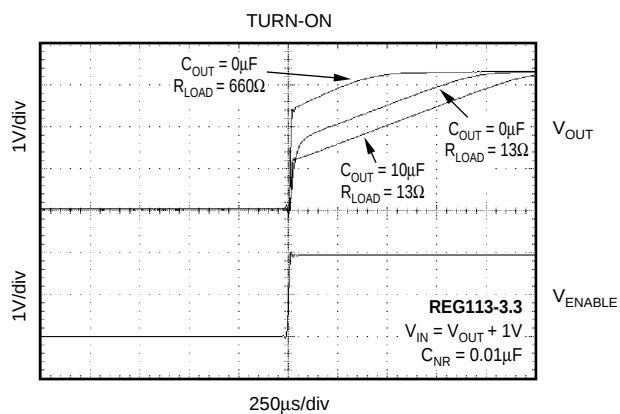
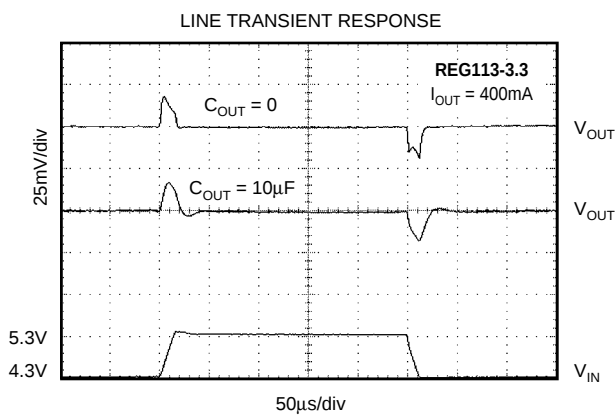
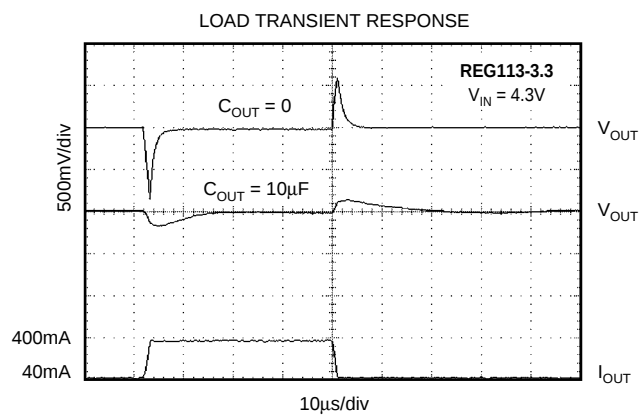
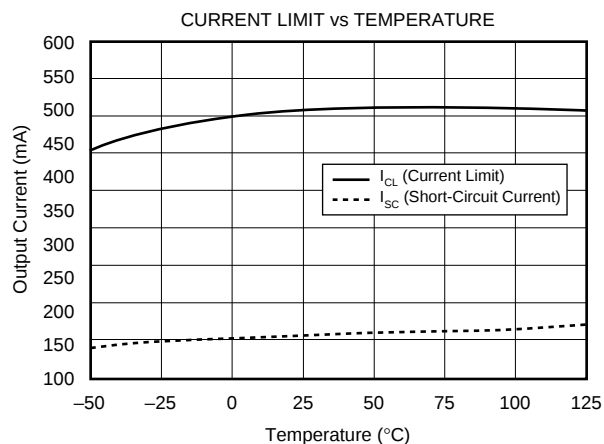
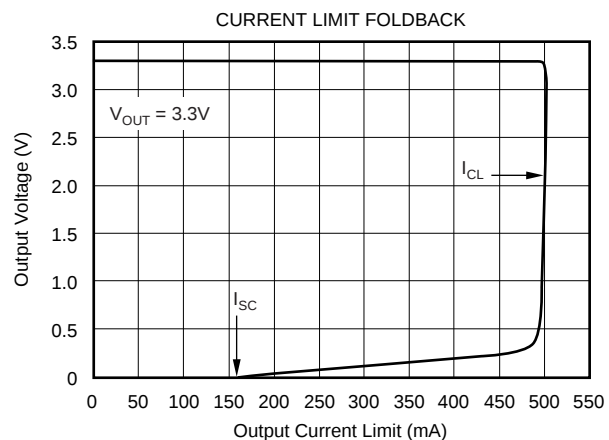
TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



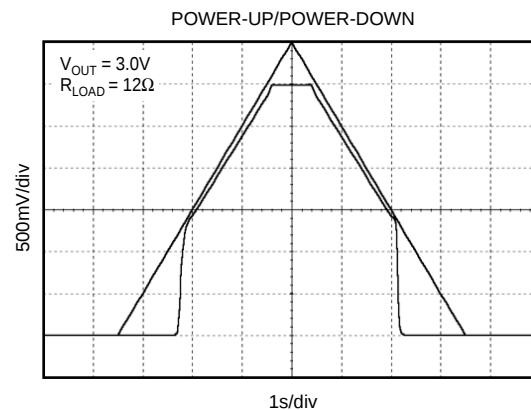
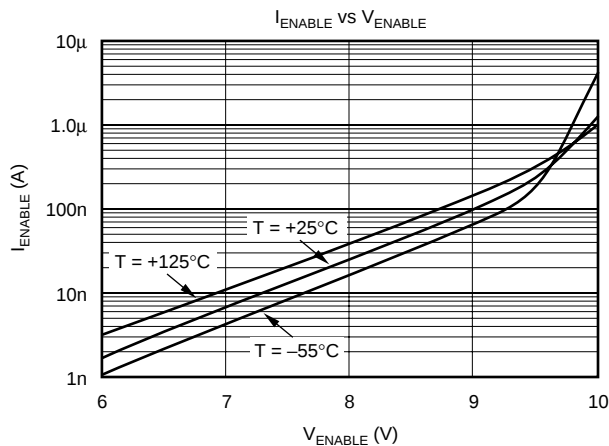
TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



BASIC OPERATION

The REG113 series of LDO (low dropout) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version. The REG113 belongs to a family of new generation LDO regulators that use a DMOS pass transistor to achieve ultra low-dropout performance and freedom from output capacitor constraints. Ground pin current remains under 1mA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG113 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to $10\mu\text{F}$ or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by adding a $1\text{k}\Omega$ to $2\text{k}\Omega$ load resistor, using capacitance values smaller than $10\mu\text{F}$, or keeping the effective series resistance greater than 0.05Ω including the capacitor ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is a good standard analog design practice to connect a $0.1\mu\text{F}$ low ESR capacitor across the input supply voltage; this is recommended to counteract reactive input sources and improve ripple rejection by reducing input voltage ripple. Figure 1 shows the basic circuit connections for the fixed voltage models.

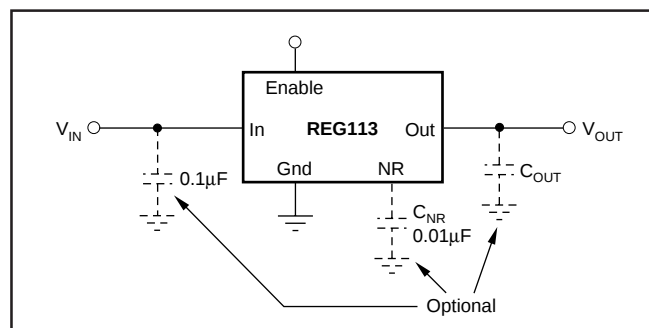


FIGURE 1. Fixed Voltage Nominal Circuit for the REG113.

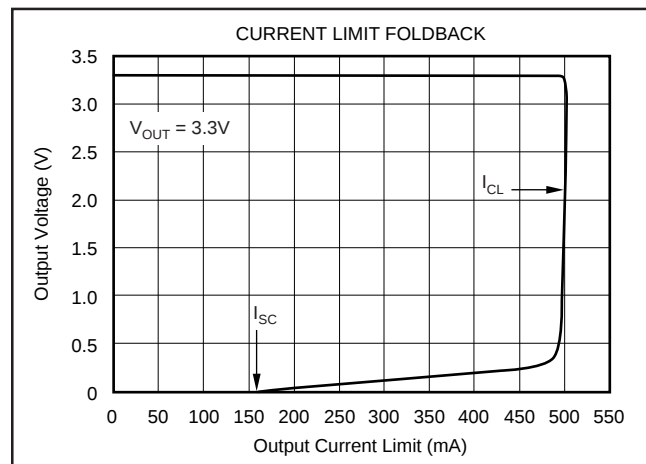


FIGURE 2. Foldback Current Limit of the REG113-3.3 at 25°C .

INTERNAL CURRENT LIMIT

The REG113 internal current limit has a typical value of 500mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 200mA. A curve of V_{OUT} versus I_{OUT} is given in Figure 2, and in the Typical Characteristics section.

ENABLE

The Enable pin is active high and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When not used, the Enable pin can be connected to V_{IN} .

OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the REG113 and generates approximately $29\mu V_{rms}$ in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu V_{rms} \frac{R_1 + R_2}{R_2} = 29\mu V_{rms} \cdot \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.26V, this relationship reduces to:

$$V_N = 23 \frac{\mu V_{rms}}{V} \cdot V_{OUT} \quad (2)$$

Connecting a capacitor, C_{NR} , from the Noise Reduction (NR) pin to ground (as shown in Figure 3) forms a low-pass filter for the voltage reference. For $C_{NR} = 10nF$, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for $V_{OUT} = 3.3V$. This noise reduction effect is shown in Figure 4, and as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

Noise can be further reduced by carefully choosing an output capacitor, C_{OUT} . Best overall noise performance is achieved with very low ($< 0.22\mu F$) or very high ($> 2.2\mu F$) values of C_{OUT} (see the *RMS Noise Voltage vs C_{OUT}* typical characteristic).

The REG113 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN} . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of I_{OUT} and C_{OUT} .

DROPOUT VOLTAGE

The REG113 uses an N-channel DMOS as the pass element. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DROP}), the DMOS pass device behaves like a resistor; therefore, for low values of $(V_{IN} - V_{OUT})$, the regulator input-to-output resistance is the $R_{DS(ON)}$ of the DMOS pass element (typically $600m\Omega$). For static (DC) loads, the REG113 will

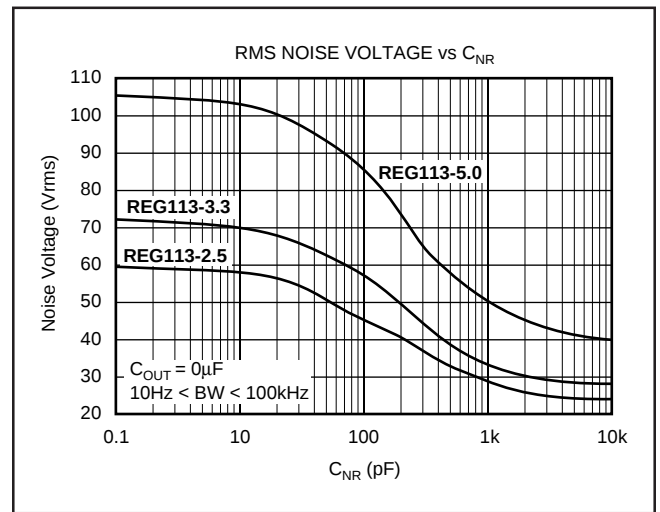


FIGURE 4. Output Noise versus Noise Reduction Capacitor.

typically maintain regulation down to a $(V_{IN} - V_{OUT})$ voltage drop of 250mV at full rated output current. In Figure 5, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent dropout under DC load conditions.

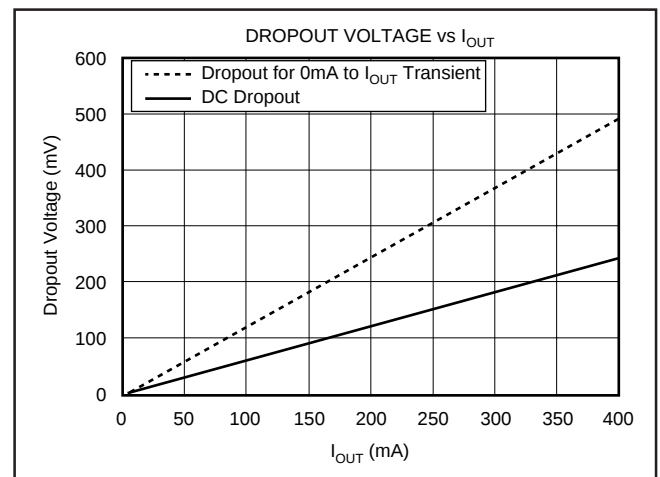


FIGURE 5. Transient and DC Dropout.

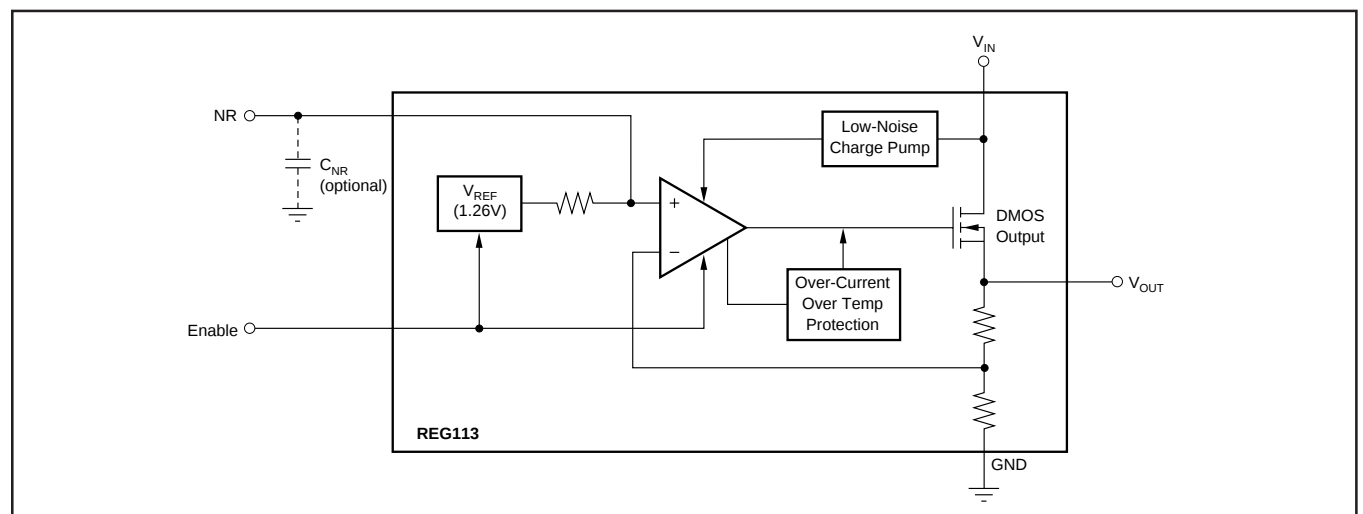


FIGURE 3. Block Diagram.

For large step changes in load current, the REG113 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient dropout region is shown as the top line in Figure 5. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

In the transient dropout region between DC and Transient, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available headroom V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with $(V_{IN} - V_{OUT})$ voltage drop close to DC dropout levels), the REG113 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG113 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value $0.47\mu\text{F}$) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin also improves the transient response.

THERMAL PROTECTION

Power dissipated within the REG113 can cause the junction temperature to rise, however, the REG113 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C , allowing the device to cool. When the junction temperature cools to approximately 140°C , the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, but can have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C , maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG113 is designed to protect against overload conditions and is not intended to replace proper heat sinking. Continuously running the REG113 into thermal shutdown will degrade reliability.

POWER DISSIPATION

The REG113 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. On the MSOP-8 package, leads 5 through 8 are fused to the lead frame and may be used to improve the thermal performance of the package. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Although it is difficult or impossible to quantify all of the variables in a thermal design of this type, performance data for several simplified configurations are shown in Figure 6. In all cases the PCB copper area is bare copper, free of solder resist mask, and not solder plated. All examples are for 1-ounce copper and in the case of the MSOP-8, the copper area is connected to fused leads 5 to 8. See Figure 7 for thermal resistance for varying areas of copper. Using heavier copper can increase the effectiveness in removing the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

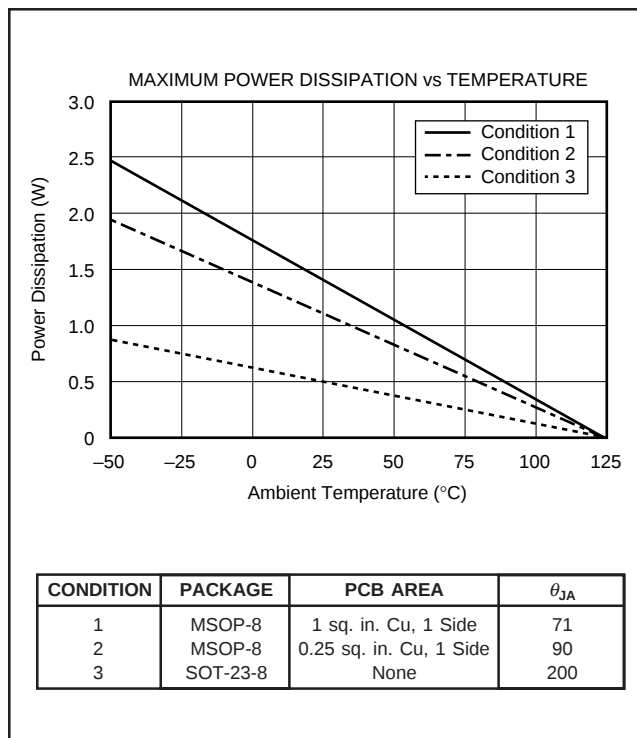


FIGURE 6. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

Power dissipation depends on input voltage, load conditions, and duty cycle and is equal to the product of the average output current times the voltage across the output element (V_{IN} to V_{OUT} voltage drop):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (3)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

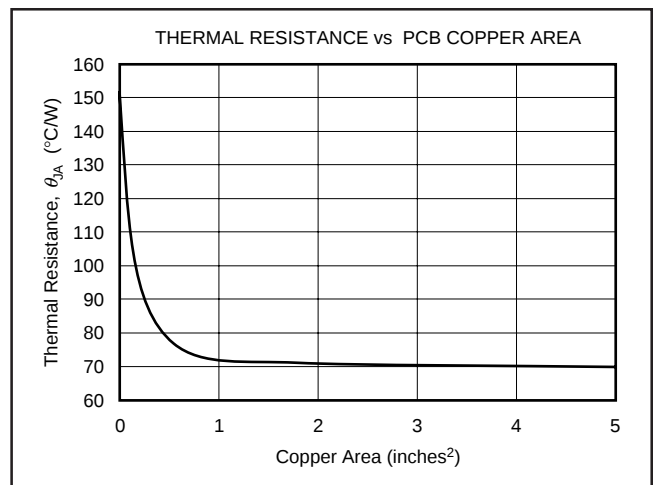


FIGURE 7. Thermal Resistance versus PCB Area for the MSOP-8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG113EA-2.5/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-2.5/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-2.5/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-3.3/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13C	Samples
REG113EA-3.3/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13C	Samples
REG113EA-3/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13D	Samples
REG113EA-5/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113EA-5/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113EA-5/2K5G4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113NA-2.5/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13G	Samples
REG113NA-2.5/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13G	Samples
REG113NA-2.85/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13N	Samples
REG113NA-2.85/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13N	Samples
REG113NA-3.3/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3.3/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3.3/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-3/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-3/3KG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-5/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG113NA-5/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples
REG113NA-5/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

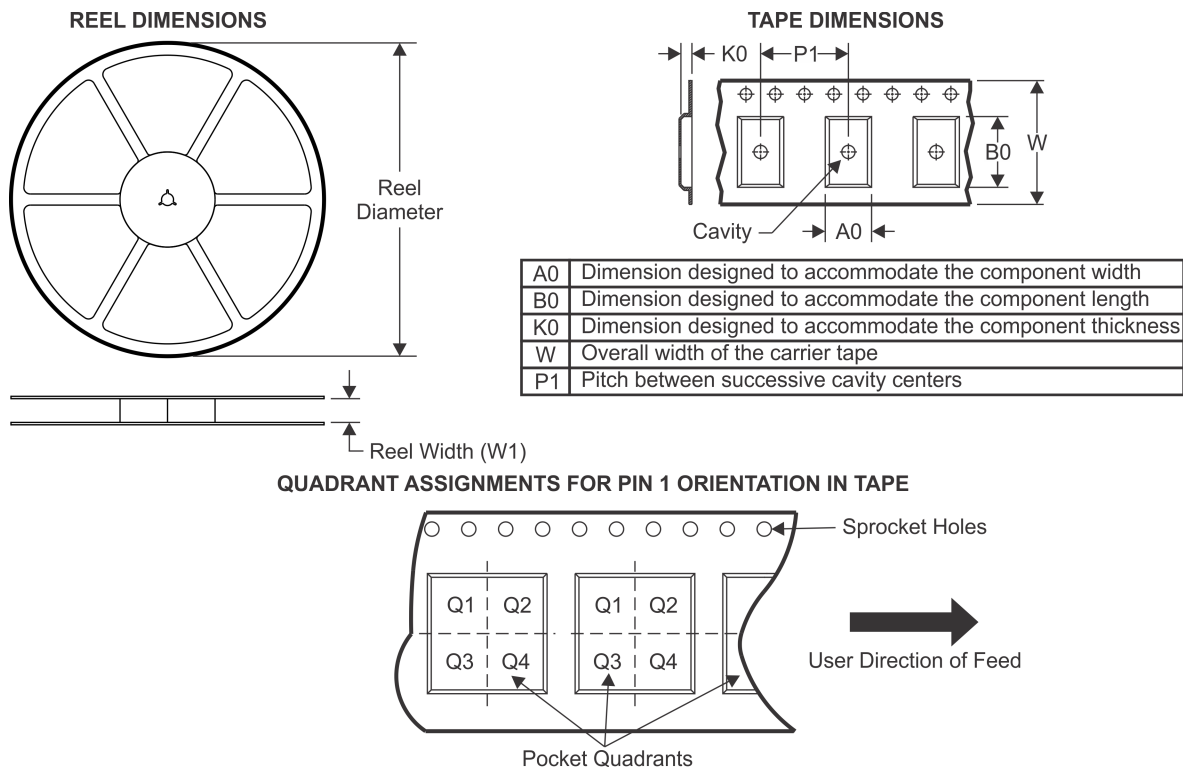
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

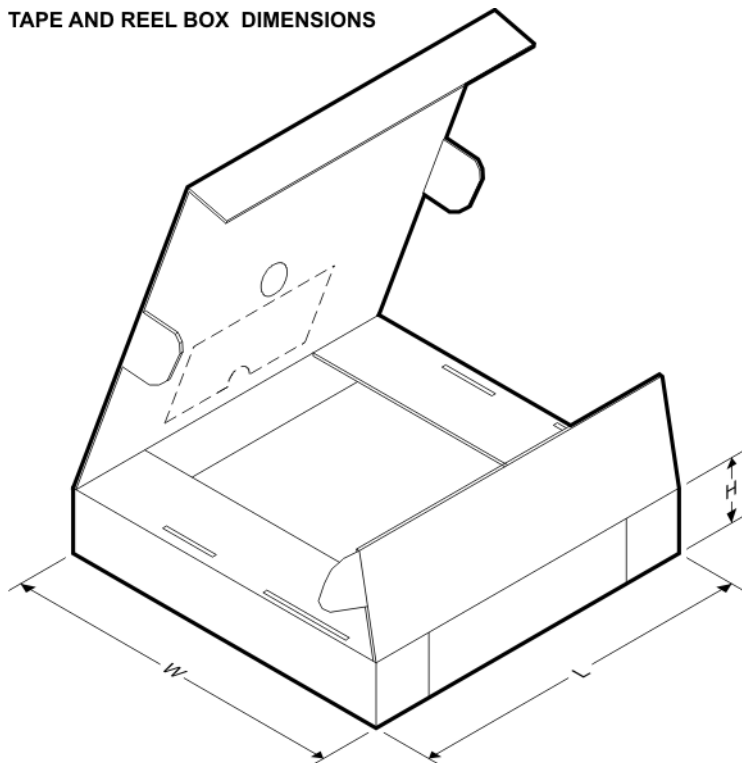
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG113EA-2.5/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-2.5/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3.3/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3.3/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-5/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-5/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113NA-2.5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-2.5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-2.85/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-2.85/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3.3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3.3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG113EA-2.5/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-2.5/2K5	VSSOP	DGK	8	2500	853.0	449.0	35.0
REG113EA-3.3/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-3.3/2K5	VSSOP	DGK	8	2500	853.0	449.0	35.0
REG113EA-3/2K5	VSSOP	DGK	8	2500	853.0	449.0	35.0
REG113EA-5/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-5/2K5	VSSOP	DGK	8	2500	853.0	449.0	35.0
REG113NA-2.5/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG113NA-2.5/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG113NA-2.85/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG113NA-2.85/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG113NA-3.3/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG113NA-3.3/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG113NA-3/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG113NA-3/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG113NA-5/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG113NA-5/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0

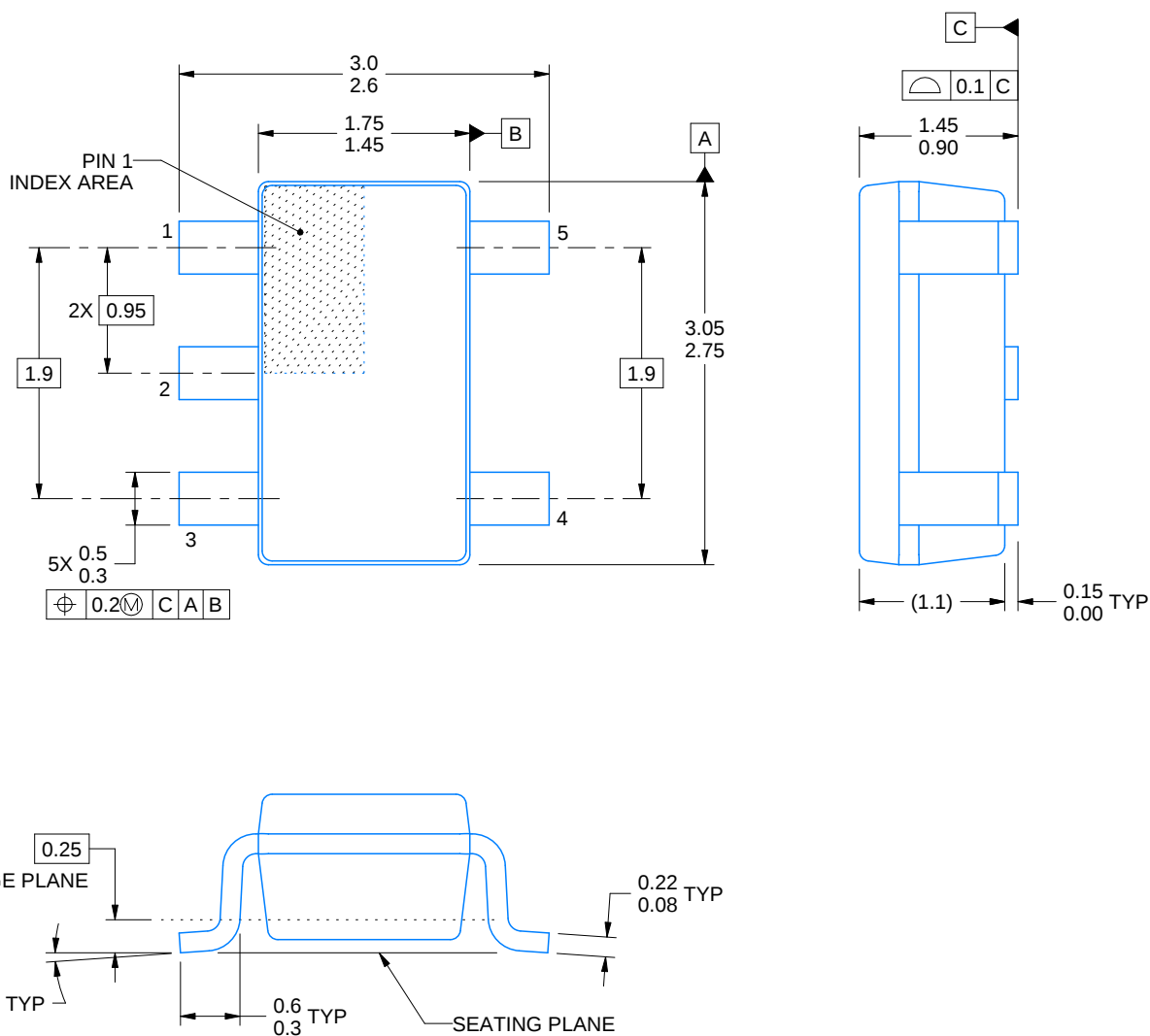


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

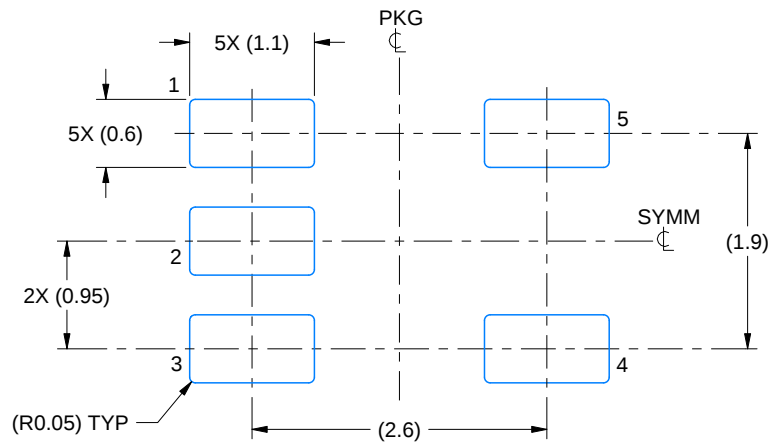
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

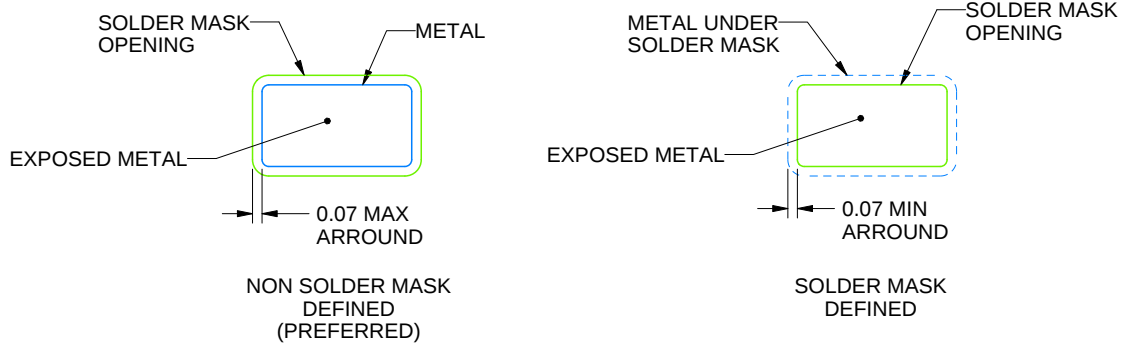
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

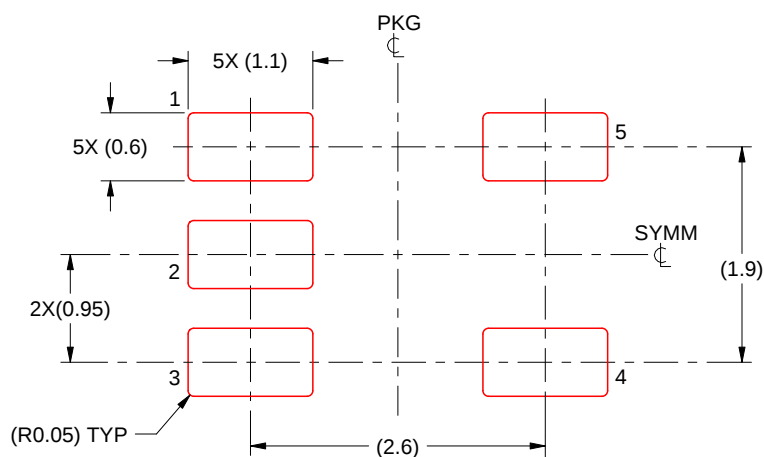
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



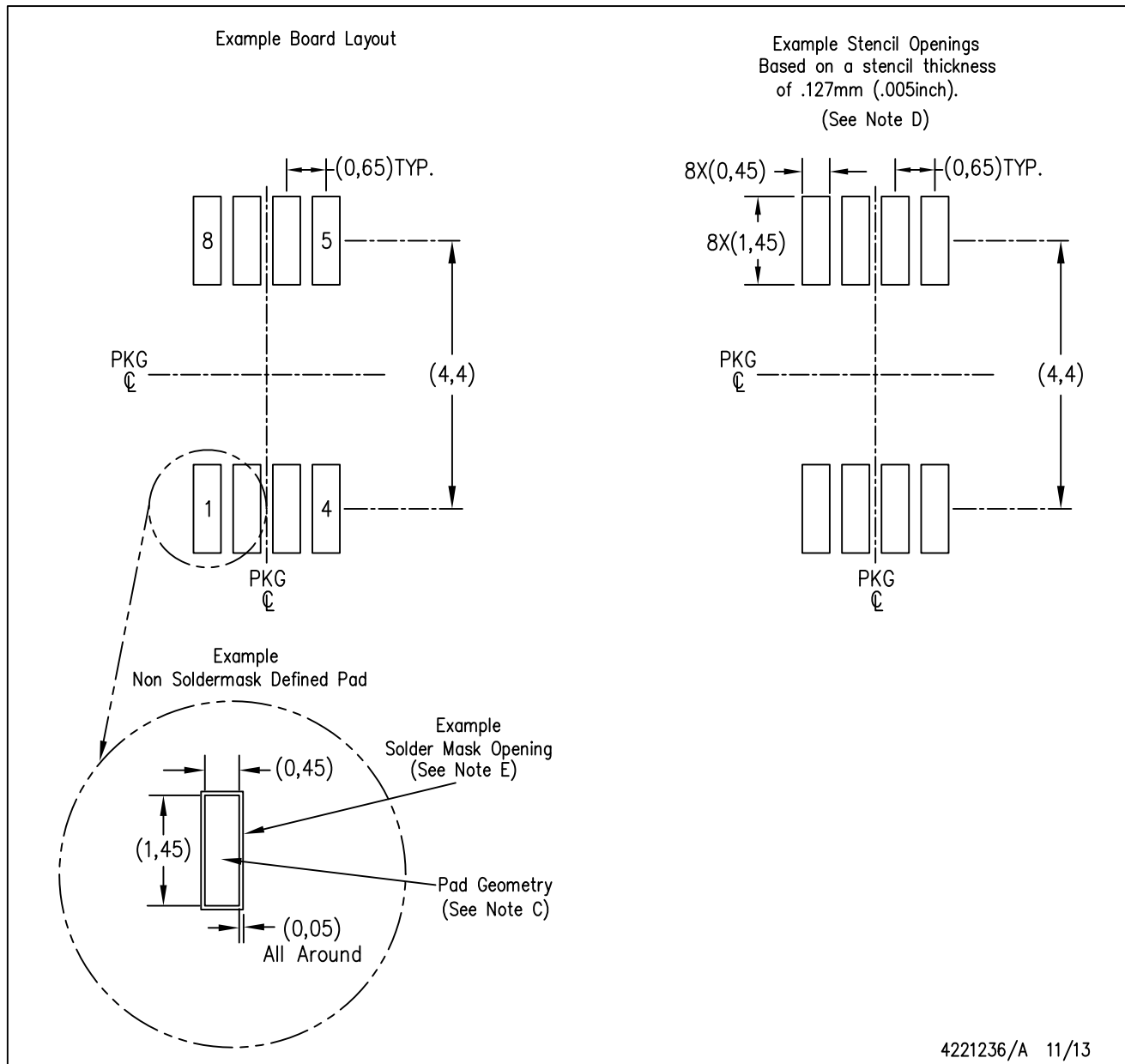
4073329/E 05/06

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated