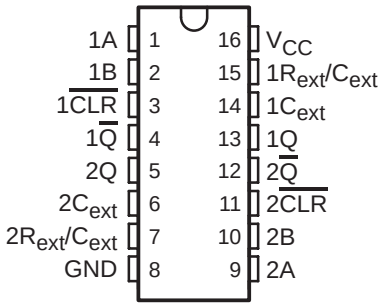
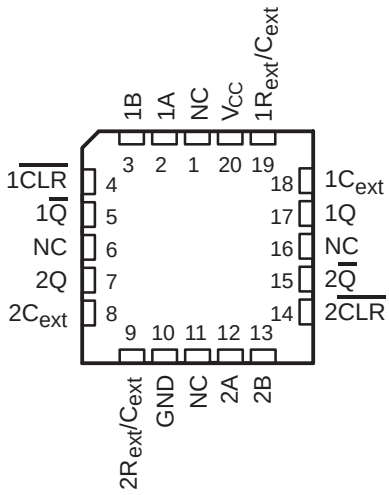
- **Dual Versions of Highly Stable SN54121 and SN74121 One Shots**
- **SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121 and SN74121 One Shots**
- **Pinout Is Identical to the SN54123, SN74123, SN54LS123, and SN74LS123**
- **Overriding Clear Terminates Output Pulse**

| TYPE | MAXIMUM OUTPUT PULSE LENGTH(S) |
|---|---|
| SN54221 | 21 |
| SN74221 | 28 |
| SN54LS221 | 49 |
| SN74LS221 | 70 |

**SN54221, SN54LS221 . . . J PACKAGE**
**SN74221 . . . N PACKAGE**
**SN74LS221 . . . D, DB, N, OR NS PACKAGE**
**(TOP VIEW)**




**SN54LS221 . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

The ’221 and ’LS221 devices are dual multivibrators with performance characteristics virtually identical to those of the ’121 devices. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP − N | Tube | SN74221N | SN74221N |
| | | | SN74LS221N | SN74LS221N |
| | SOIC − D | Tube | SN74LS221D | LS221 |
| | | Tape and reel | SN74LS221DR | |
| | SOP − NS | Tape and reel | SN74LS221NSR | 74LS221 |
| | SSOP − DB | Tape and reel | SN74LS221DBR | LS221 |
| −55°C to 125°C | CDIP − J | Tube | SNJ54221J | SNJ54221J |
| | | | SNJ54LS221J | SNJ54LS221J |
| | LCCC − FK | Tube | SNJ54LS221FK | SNJ54LS221FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description/ordering information (continued)

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition at rates as slow as 1 V/s, providing the circuit with excellent noise immunity, typically of 1.2 V. A high immunity to $V_{CC}$ noise, typically of 1.5 V, also is provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse length can be varied from 35 ns to the maximum by choosing appropriate timing components. With $R_{ext}$ = 2 kΩ and $C_{ext}$ = 0, an output pulse typically of 30 ns is achieved that can be used as a dc-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are shown as a part of the switching characteristics waveforms.

Pulse-width stability is achieved through internal compensation and is virtually independent of $V_{CC}$ and temperature. In most applications, pulse stability is limited only by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and $V_{CC}$ ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_w(out) = C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ can be used. Also, the range of jitter-free output pulse widths is extended if $V_{CC}$ is held to 5 V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended $R_T$. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the ’221 is shown in Figure 3. Variations in output pulse width versus supply voltage and temperature for the ’221 are shown in Figures 4 and 5, respectively.

Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the ’221 or ’LS221 devices can be substituted for those products in systems not using the retrigger by merely changing the value of $R_{ext}$ and/or $C_{ext}$; however, the polarity of the capacitor must be changed.

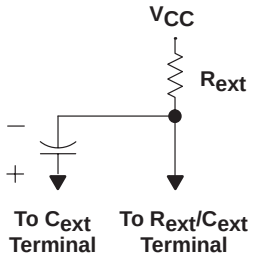
**FUNCTION TABLE**
**(each monostable multivibrator)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{CLR}$ | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍† | ⎎† |
| H | ↓ | H | ⎍† | ⎎† |
| ↑‡ | L | H | ⎍† | ⎎† |

† Pulsed-output patterns are tested during AC switching at 25°C with $R_{ext}$ = 2 kΩ, and $C_{ext}$ = 80 pF.

‡ This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to $\overline{CLR}$ going high. This latch is conditioned by taking either A high or B low while $\overline{CLR}$ is inactive (high).

## timing component connections

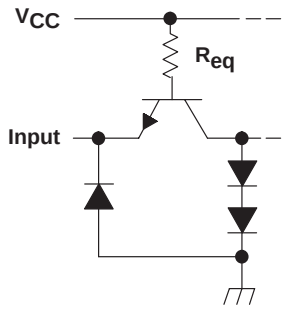



NOTE: Due to the internal circuit, the $R_{ext}/C_{ext}$ terminal never is more positive than the $C_{ext}$ terminal.

## schematics of inputs and outputs

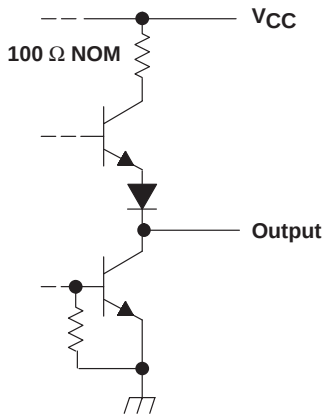
**SN54/74221**

**EQUIVALENT OF EACH INPUT**



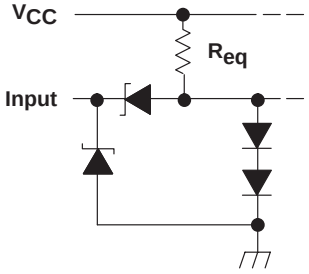

**A Input: $R_{eq}$ = 4 kΩ NOM**
**B, $\overline{CLR}$ Input: $R_{eq}$ = 2 kΩ NOM**

**TYPICAL OF ALL OUTPUTS**



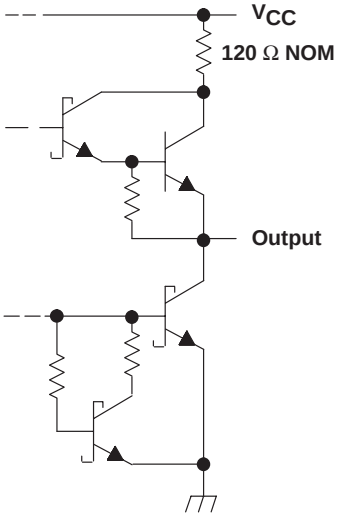

**SN54/74LS221**

**EQUIVALENT OF EACH INPUT**




**A Input: $R_{eq}$ = 25 kΩ NOM**
**B $\overline{Input}$: $R_{eq}$ = 15.4 kΩ NOM**
**$\overline{CLR}$: $R_{eq}$ = 12.5 kΩ NOM**

**TYPICAL OF ALL OUTPUTS**



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . 7 V
Input voltage range, $V_I$ (see Note 1): 'LS221 . . . . . 7 V
'221 . . . . . 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

| | | | SN54221 | | | SN74221 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | | | | −800 | | | −800 | μA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $\Delta v/\Delta t$ | Rise or fall of input pulse rate | B input | 1* | | | 1 | | | V/s |
| | | A input | 1* | | | 1 | | | V/μs |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54221 | | | SN74221 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{T+}$ | Positive-going threshold voltage, B input | $V_{CC}$ = MIN | | | 1.55 | 2* | | 1.55 | 2 | V |
| $V_{T-}$ | Negative-going threshold voltage, B input | $V_{CC}$ = MIN | | 0.8* | 1.35 | | 0.8 | 1.35 | | V |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, | $I_{OH}$ = −800 μA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, | $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | A input | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| | $\overline{CLR}$, B input | | | | | 80 | | | 80 | |
| $I_{IL}$ | A input | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| | $\overline{CLR}$, B input | | | | | −3.2 | | | −3.2 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | −20 | | −55 | −18 | | −55 | mA |
| $I_{CC}$ | Quiescent | $V_{CC}$ = MAX | | | 26 | 50* | | 26 | 50 | mA |
| | Triggered | | | | 46 | 80* | | 46 | 80 | |

∗ On products compliant to MIL-PRF-38535, this parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | | SN54221 | | SN74221 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | A or B input | 50 | | 50 | | ns |
| | | $\overline{CLR}$ | 20 | | 20 | | |
| $t_{su}$ | Setup time, inactive-state¶ | $\overline{CLR}$ | 15 | | 15 | | ns |
| $R_{ext}$ | External timing resistance | | 1.4* | 30* | 1.4 | 40 | kΩ |
| $C_{ext}$ | External timing capacitance | | 0* | 1000* | 0 | 1000 | μF |
| | Output duty cycle | $R_{ext}$ = 2 kΩ | | 67% | | 67% | |
| | | $R_{ext}$ = MAX $R_{ext}$ | | 90% | | 90% | |

∗ On products compliant to MIL-PRF-38535, this parameter is not production tested.
¶ Inactive-state setup time also is referred to as recovery time.

## switching characteristics $V_{CC}$ = 5 V, $R_L$ = 400 Ω, $T_A$ = 25°C (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54221 | | | SN74221 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Q | $C_{ext}$ = 80 pF, $R_{ext}$ = 2 kΩ | | 45 | 70 | | 45 | 70 | ns |
| | B | | | | 35 | 55 | | 35 | 55 | |
| $t_{PHL}$ | A | $\overline{Q}$ | | | 50 | 80 | | 50 | 80 | |
| | B | | | | 40 | 65 | | 40 | 65 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_{ext}$ = 80 pF, $R_{ext}$ = 2 kΩ | | | 27 | | | 27 | ns |
| $t_{PLH}$ | | $\overline{Q}$ | | | | 40 | | | 40 | |
| $t_w$ | A or B | Q or $\overline{Q}$ | $C_{ext}$ = 80 pF, $R_{ext}$ = 2 kΩ | 70 | 110 | 150 | 70 | 110 | 150 | ns |
| | | | $C_{ext}$ = 0, $R_{ext}$ = 2 kΩ | 17 | 30 | 50 | 17 | 30 | 50 | |
| | | | $C_{ext}$ = 100 pF, $R_{ext}$ = 10 kΩ | 650 | 700 | 750 | 650 | 700 | 750 | |
| | | | $C_{ext}$ = 1 µF, $R_{ext}$ = 10 kΩ | 6.5* | 7 | 7.5* | 6.5 | 7 | 7.5 | ms |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## recommended operating conditions (see Note 4)

| | | | SN54LS221 | | | SN74LS221 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | | | | −400 | | | −400 | µA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| Δv/Δt | Rise or fall of input pulse rate | B input | 1* | | | 1 | | | V/s |
| | | A input | 1* | | | 1 | | | V/µs |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS221 | | | SN74LS221 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{T+}$ | Positive-going threshold voltage, B input | $V_{CC}$ = MIN | | | 1 | 2* | | 1 | 2 | V |
| $V_{T-}$ | Negative-going threshold voltage, B input | $V_{CC}$ = MIN | | 0.7* | 0.9 | | 0.8 | 0.9 | | V |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, | $I_{OH}$ = −400 μA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | A input | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| | $\overline{CLR}$, B input | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Quiescent | $V_{CC}$ = MAX | | | 4.7 | 11 | | 4.7 | 11 | mA |
| | Triggered | | | | 19 | 27* | | 19 | 27 | |

∗ On products compliant to MIL-PRF-38535, this parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | | SN54LS221 | | SN74LS221 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | A or B | 50 | | 50 | | ns |
| | | $\overline{CLR}$ | 40 | | 40 | | |
| $t_{su}$ | Setup time, inactive state¶ | $\overline{CLR}$ | 15 | | 15 | | ns |
| $R_{ext}$ | External timing resistance | | 1.4* | 70* | 1.4 | 100 | kΩ |
| $C_{ext}$ | External timing capacitance | | 0* | 1000* | 0 | 1000 | μF |
| | Output duty cycle | $R_T$ = 2 kΩ | | 50% | | 50% | |
| | | $R_T$ = MAX $R_{ext}$ | | 90% | | 90% | |

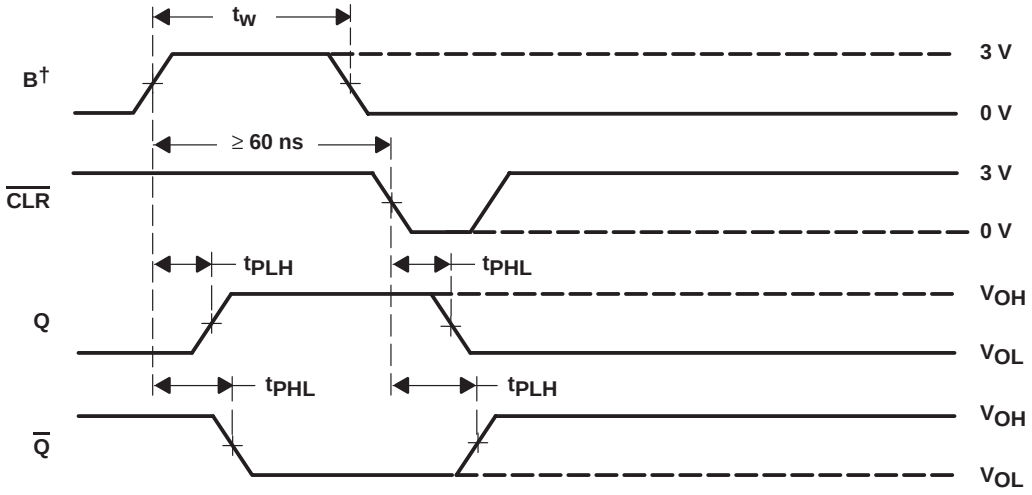
∗ On products compliant to MIL-PRF-38535, this parameter is not production tested.
¶ Inactive-state setup time also is referred to as recovery time.

## switching characteristics $V_{CC}$ = 5 V, $R_L$ = 2 kΩ, $T_A$ = 25°C (see Figures 1 and 2)

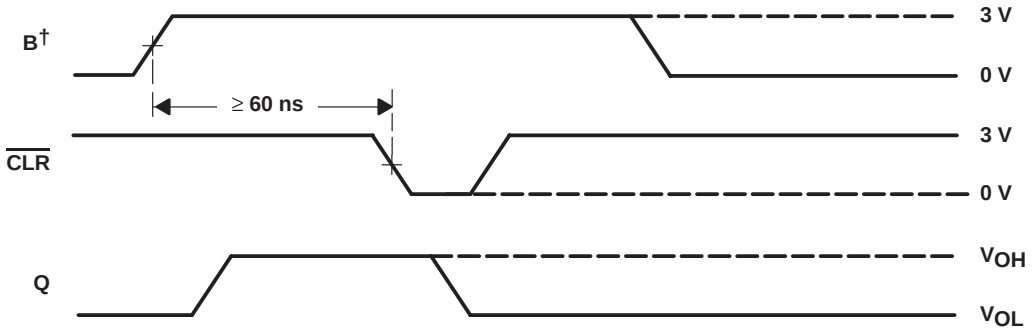
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54LS221 | | | SN74LS221 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Q | $C_{ext}$ = 80 pF, $R_{ext}$ = 2 kΩ | | 45 | 70 | | 45 | 70 | ns |
| | B | | | | 35 | 55 | | 35 | 55 | |
| $t_{PHL}$ | A | $\overline{Q}$ | | | 50 | 80 | | 50 | 80 | |
| | B | | | | 40 | 65 | | 40 | 65 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_{ext}$ = 80 pF, $R_{ext}$ = 2 kΩ | | 35 | 55 | | 35 | 55 | ns |
| $t_{PLH}$ | | $\overline{Q}$ | | | 44 | 65 | | 44 | 65 | |
| $t_w$ | A or B | Q or $\overline{Q}$ | $C_{ext}$ = 80 pF, $R_{ext}$ = 2 kΩ | 70 | 120 | 150 | 70 | 120 | 150 | ns |
| | | | $C_{ext}$ = 0, $R_{ext}$ = 2 kΩ | 20 | 47 | 70 | 20 | 47 | 70 | |
| | | | $C_{ext}$ = 100 pF, $R_{ext}$ = 10 kΩ | 670 | 740 | 810 | 670 | 740 | 810 | |
| | | | $C_{ext}$ = 1 µF, $R_{ext}$ = 10 kΩ | 6* | 6.9 | 7.5* | 6 | 6.9 | 7.5 | ms |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

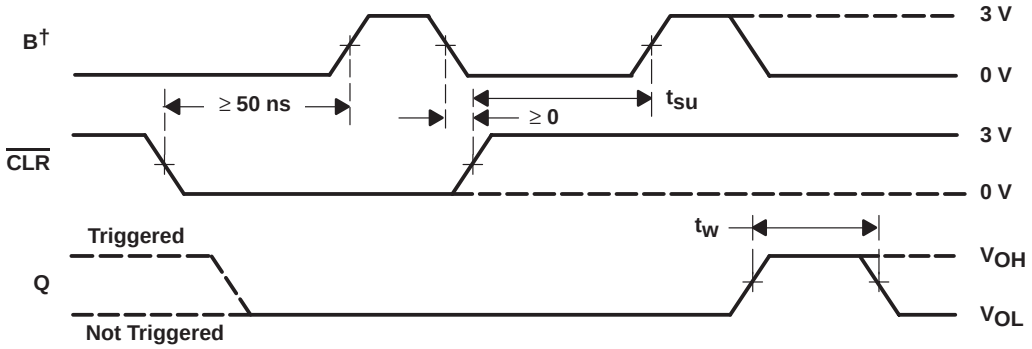
## PARAMETER MEASUREMENT INFORMATION




CONDITION 1: TRIGGER FROM B, THEN $\overline{CLR}$




CONDITION 2: TRIGGER FROM B, THEN $\overline{CLR}$

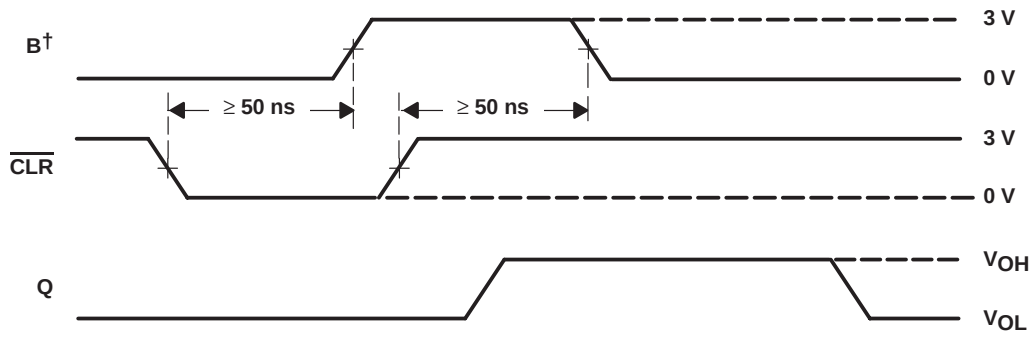



CONDITION 3: $\overline{CLR}$ OVERRIDING B, THEN TRIGGER FROM B

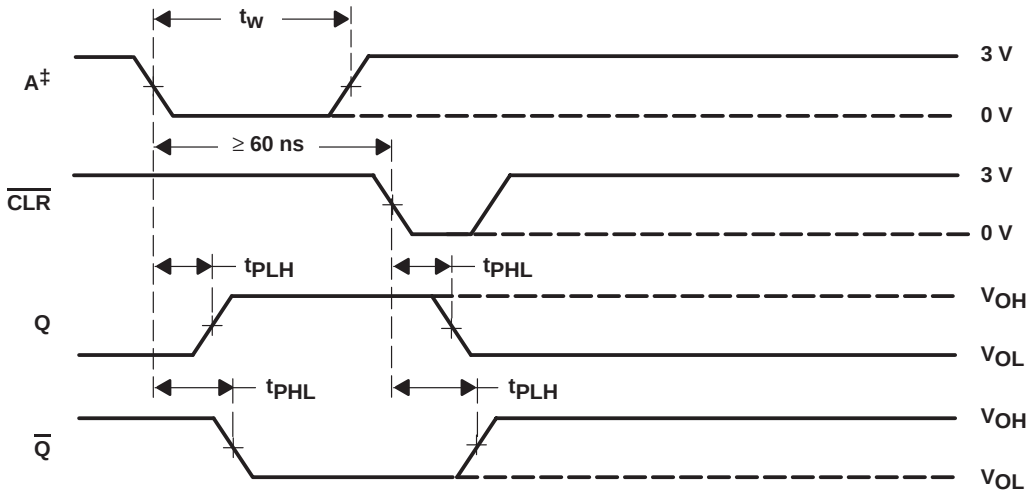
† A is low.

**Figure 1. Switching Characteristics**

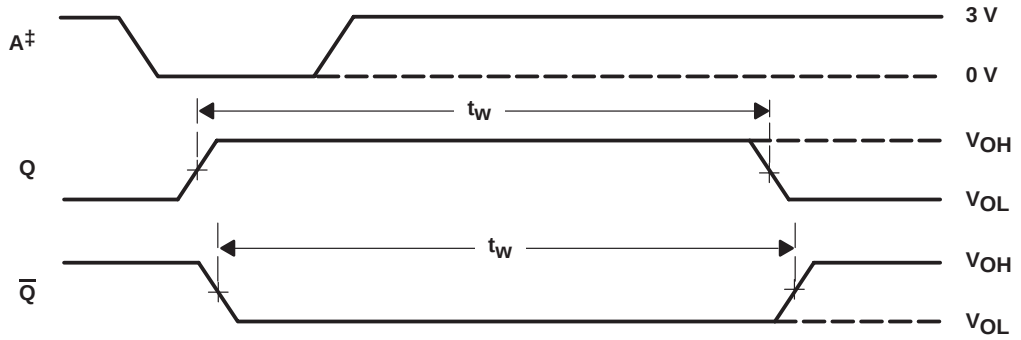
## PARAMETER MEASUREMENT INFORMATION




**CONDITION 4: TRIGGERING FROM POSITIVE TRANSITION OF $\overline{CLR}$**




**CONDITION 5: TRIGGER FROM A, THEN $\overline{CLR}$**



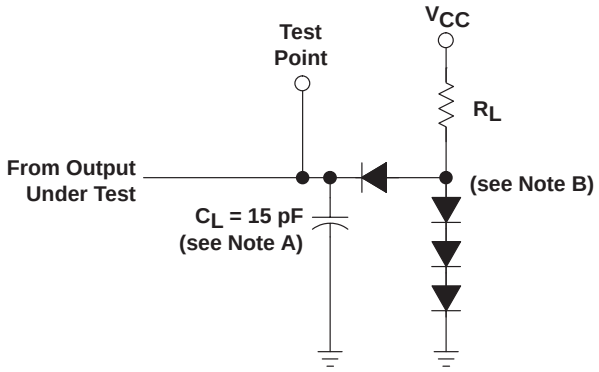

**CONDITION 6: TRIGGER FROM A**

† A is low.
‡ B and $\overline{CLR}$ are high.

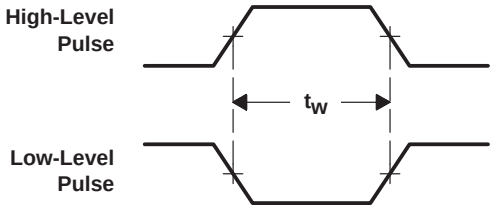
NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\Omega$; for SN54/74221, $t_r \le 7$ ns, $t_f \le 7$ ns, for SN54/74LS221, $t_r \le 15$ ns, $t_f \le 6$ ns.
B. All measurements are made between the 1.5-V points of the indicated transitions for the SN54/74221 or between the 1.3-V points for the SN54/74LS221.

**Figure 1. Switching Characteristics (Continued)**

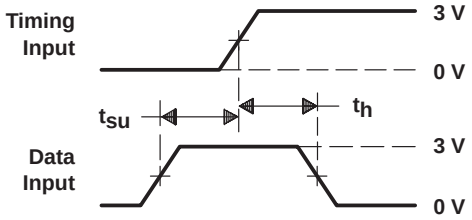
## PARAMETER MEASUREMENT INFORMATION



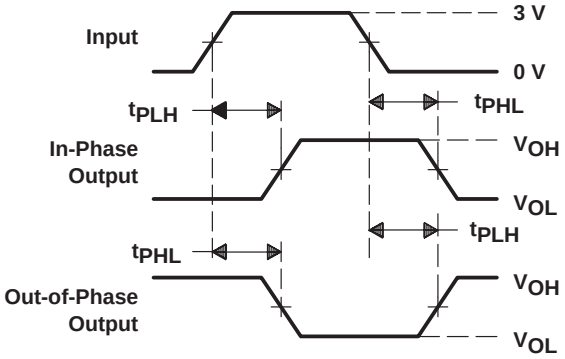

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$ and, for SN54/74221, $t_r \le 7$ ns, $t_f \le 7$ ns, for SN54/74LS221, $t_r \le 15$ ns, $t_f \le 6$ ns.
E. All measurements are made between the 1.5-V points of the indicated transitions for the SN54/74221 or between the 1.3-V points for the SN54/74LS221.

**Figure 2. Load Circuits and Voltage Waveforms**

## TYPICAL CHARACTERISTICS (SN54/74221 ONLY)†

**DISTRIBUTION OF UNITS FOR OUTPUT PULSE**

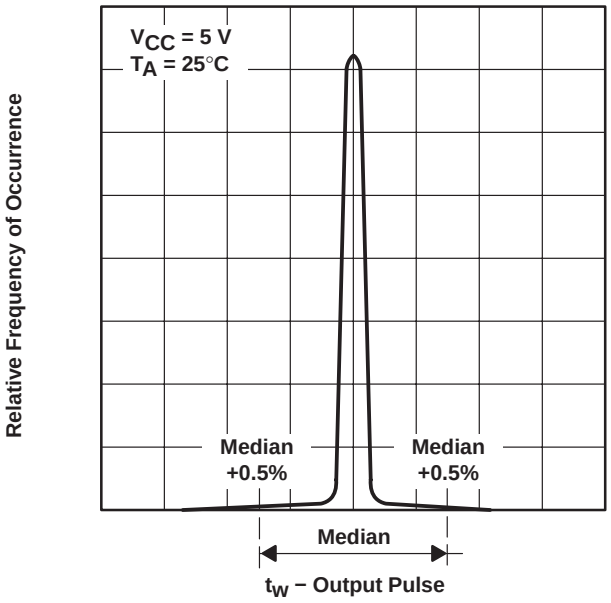



Figure 3

**VARIATION IN OUTPUT PULSE vs SUPPLY VOLTAGE**

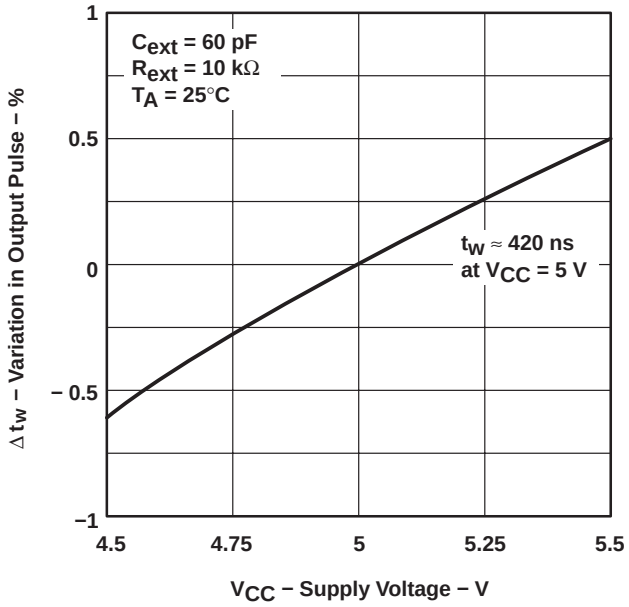



Figure 4

**VARIATION IN OUTPUT PULSE vs FREE-AIR TEMPERATURE**

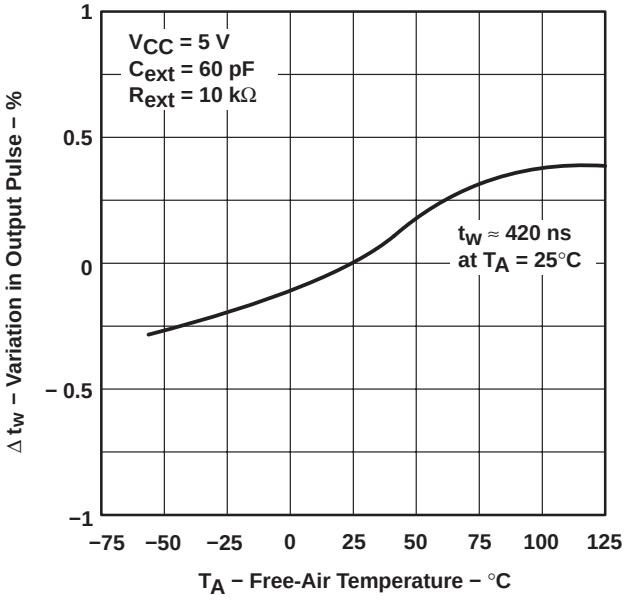



Figure 5

**OUTPUT PULSE vs TIMING RESISTOR VALUE**

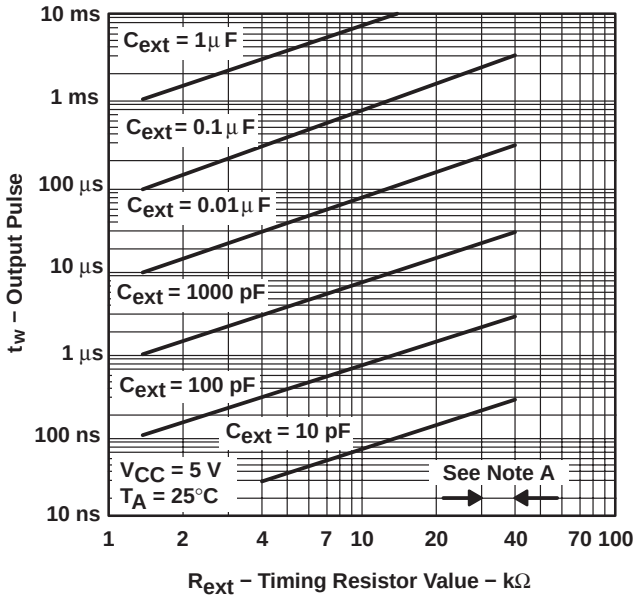



Figure 6

† Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.
NOTE A: These values of resistance exceed the maximum recommended for use over the full military temperature range of the SN54221.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8771101EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8771101EA SNJ54221J | Samples |
| 76042012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 76042012A SNJ54LS 221FK | Samples |
| 7604201EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7604201EA SNJ54LS221J | Samples |
| 7604201FA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7604201FA SNJ54LS221W | Samples |
| JM38510/31402B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31402B2A | Samples |
| JM38510/31402BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31402BEA | Samples |
| JM38510/31402BFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31402BFA | Samples |
| M38510/31402B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31402B2A | Samples |
| M38510/31402BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31402BEA | Samples |
| M38510/31402BFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31402BFA | Samples |
| SN54221J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Non-Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54221J | Samples |
| SN54LS221J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS221J | Samples |
| SN74221N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74221N | Samples |
| SN74221NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74221N | Samples |
| SN74LS221D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS221 | Samples |
| SN74LS221DBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS221 | Samples |
| SN74LS221DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS221 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS221DRE4 | ACTIVE | SOIC | D | 16 | 2500 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| SN74LS221N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS221N | Samples |
| SN74LS221NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS221N | Samples |
| SN74LS221NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS221 | Samples |
| SNJ54221J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8771101EA SNJ54221J | Samples |
| SNJ54LS221FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 76042012A SNJ54LS 221FK | Samples |
| SNJ54LS221J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7604201EA SNJ54LS221J | Samples |
| SNJ54LS221W | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7604201FA SNJ54LS221W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54221, SN54LS221, SN74221, SN74LS221 :**

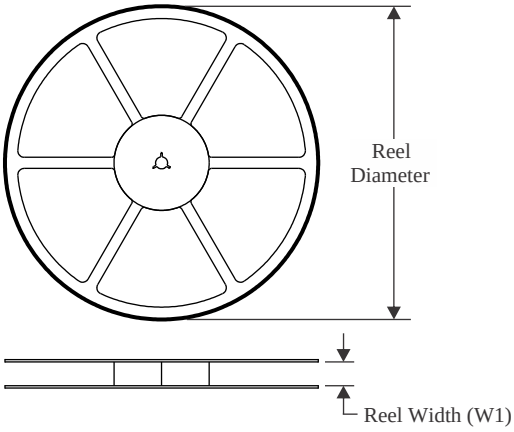
- Catalog : SN74221, SN74LS221
- Military : SN54221, SN54LS221

NOTE: Qualified Version Definitions:

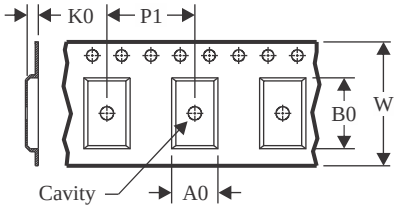
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

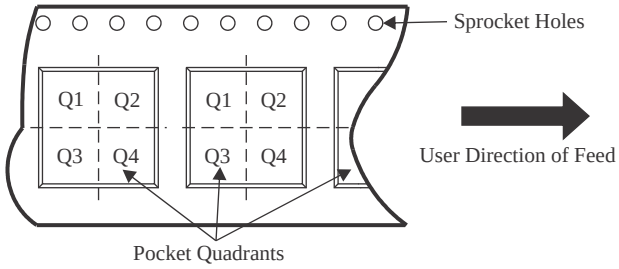



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

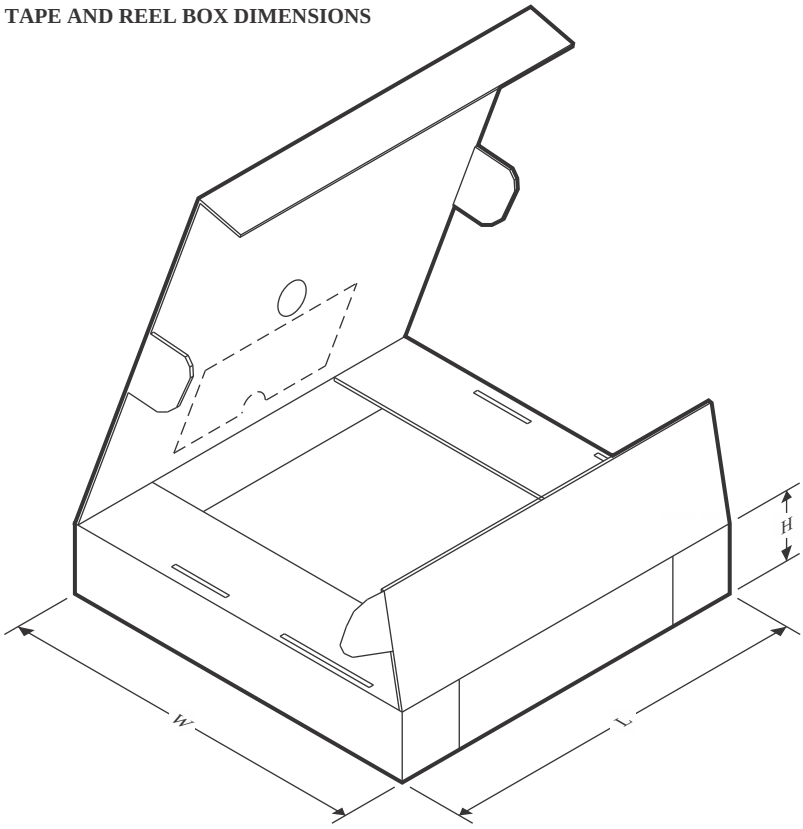
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS221DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LS221DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS221NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

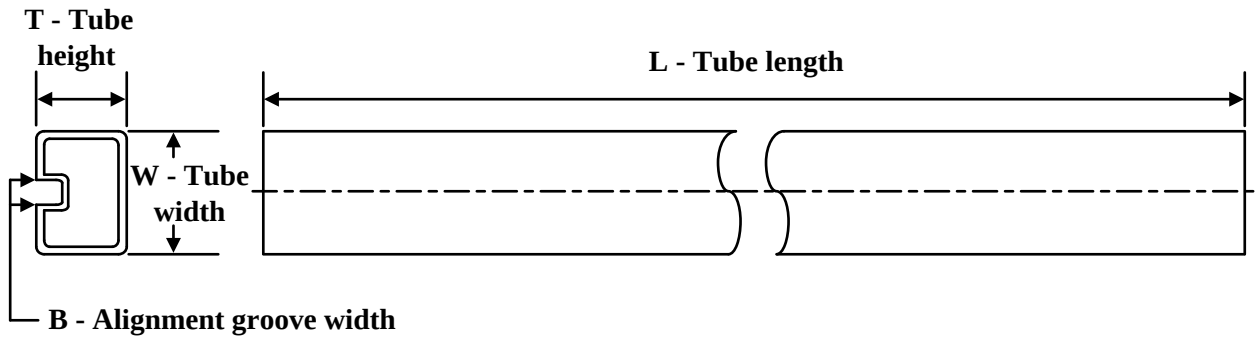
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS221DBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS221DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LS221NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |

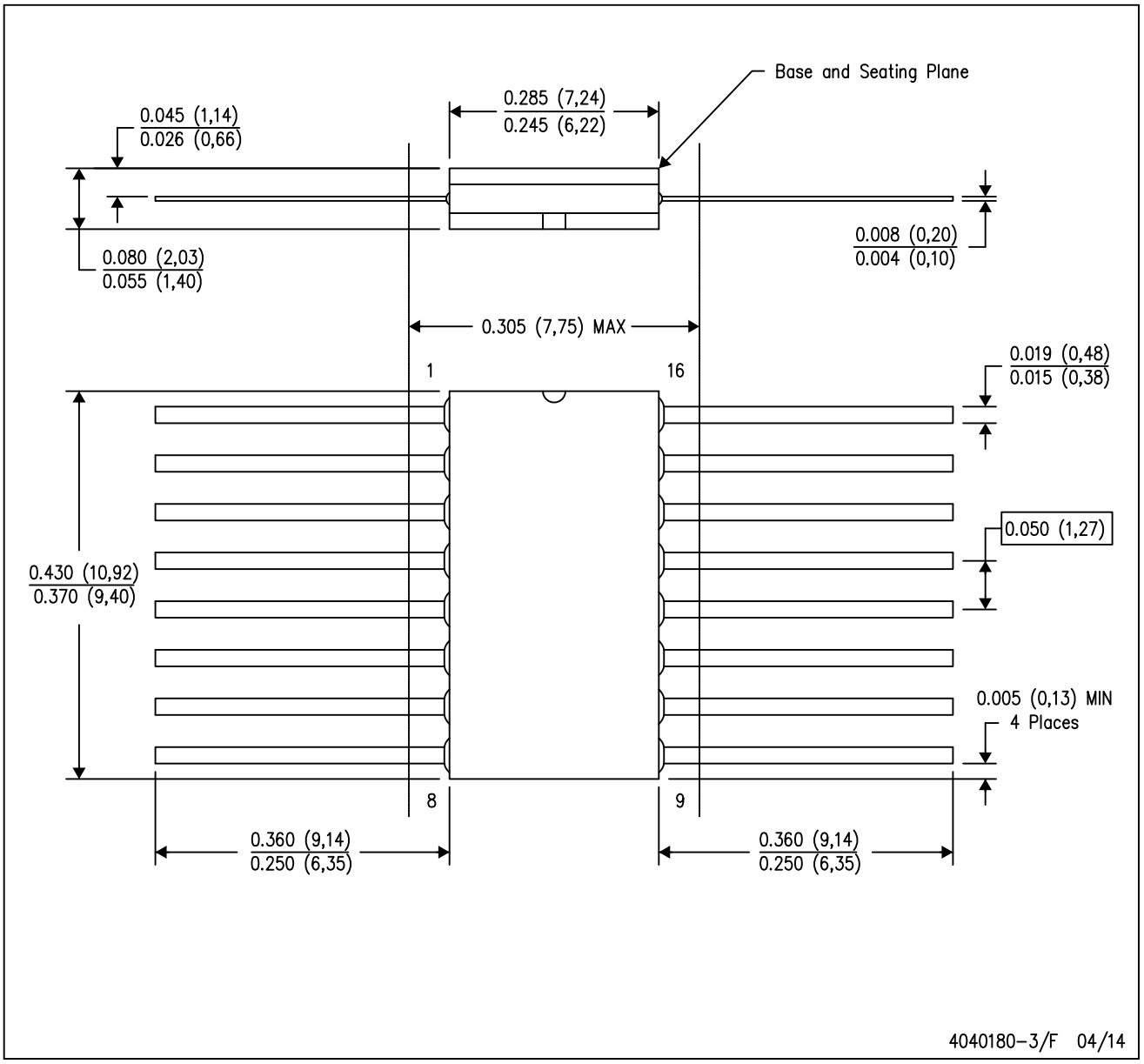
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 76042012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 7604201FA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/31402B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/31402BFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/31402B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/31402BFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74221N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74221N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74221NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74221NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS221D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LS221N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS221N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS221NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS221NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS221FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS221W | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

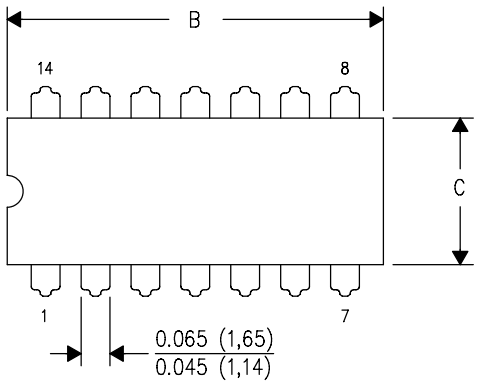



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

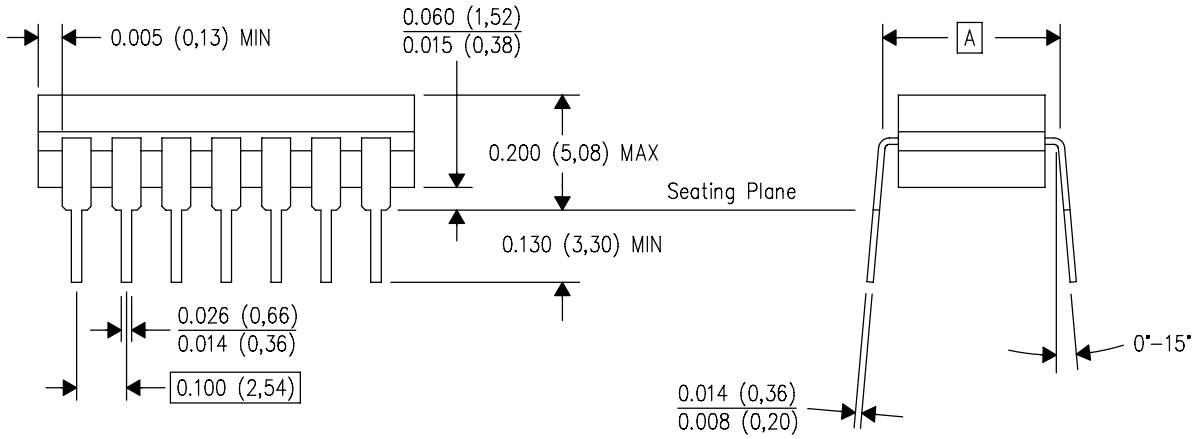
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



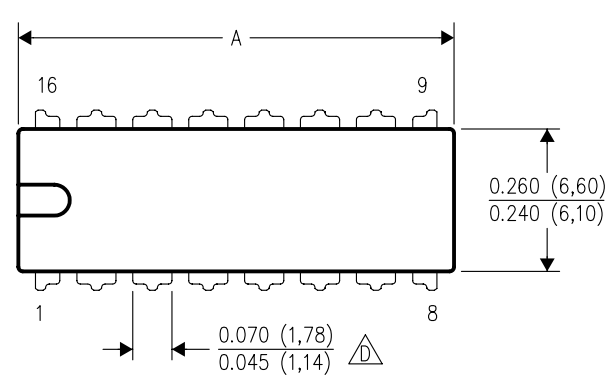

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

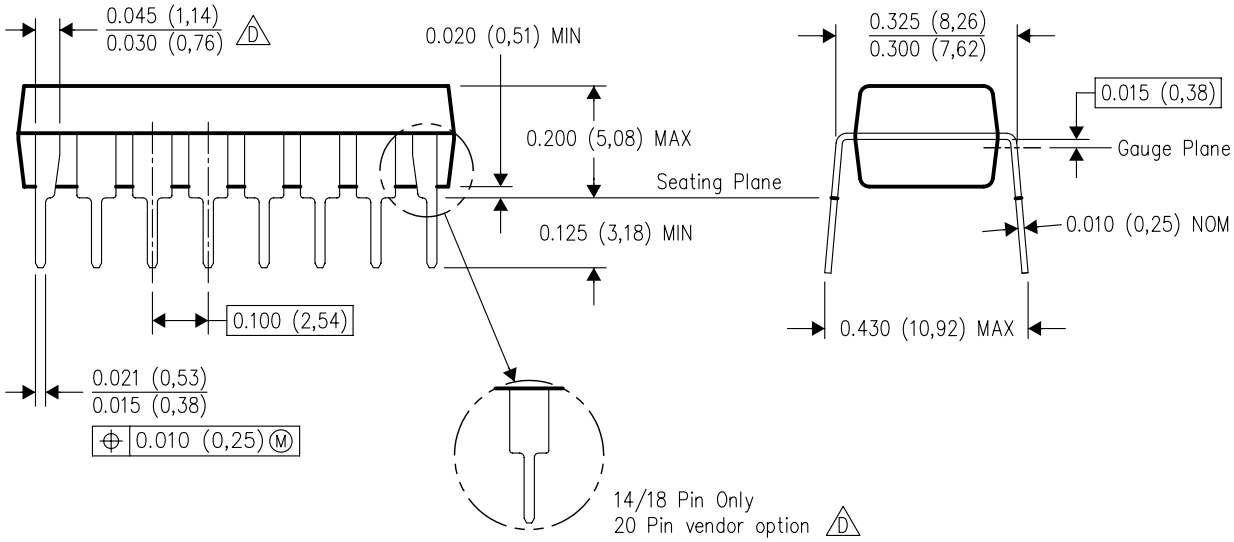
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

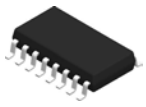



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

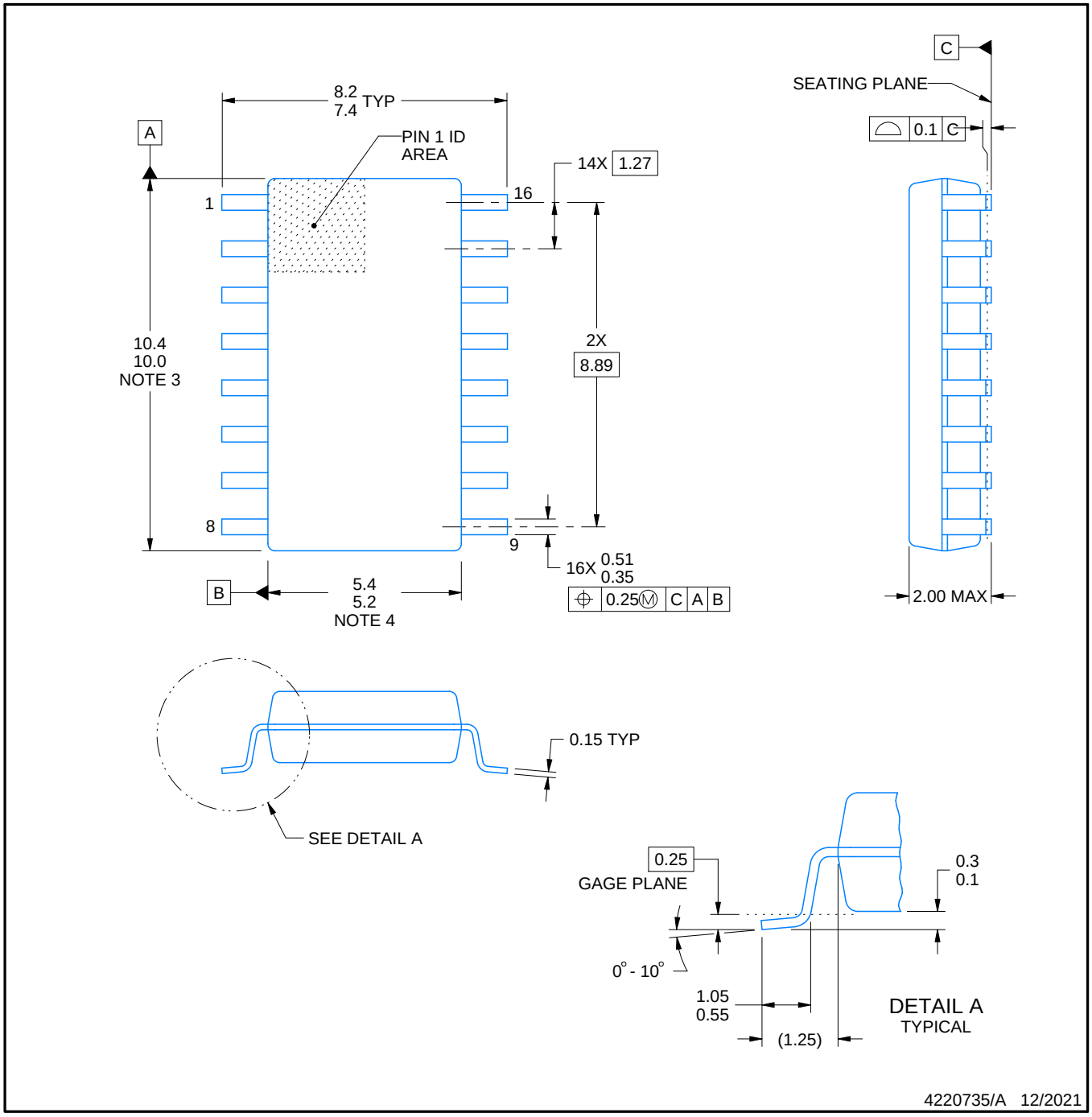


# PACKAGE OUTLINE

## NS0016A

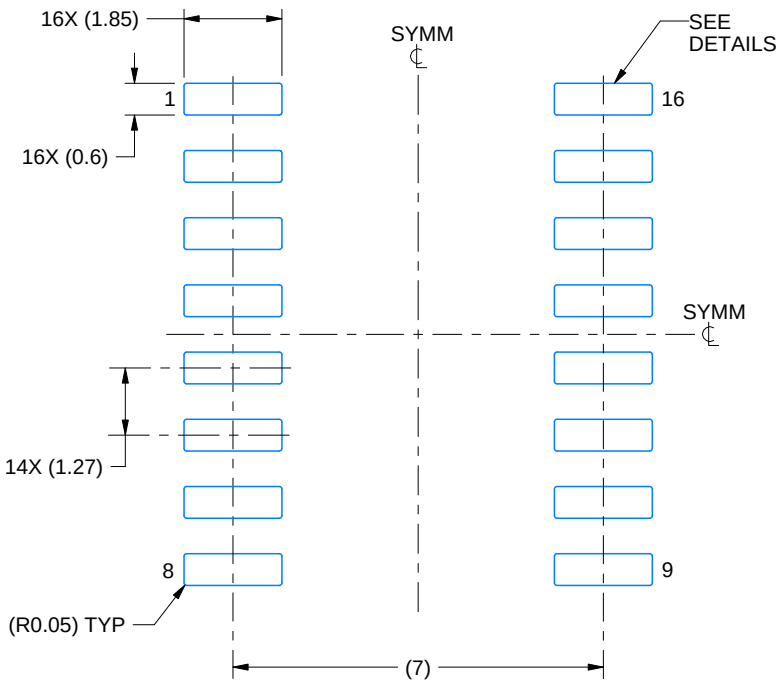
## SOP - 2.00 mm max height

SOP

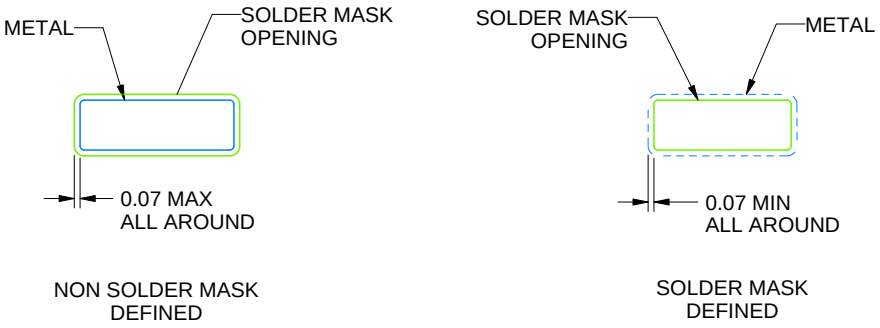



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

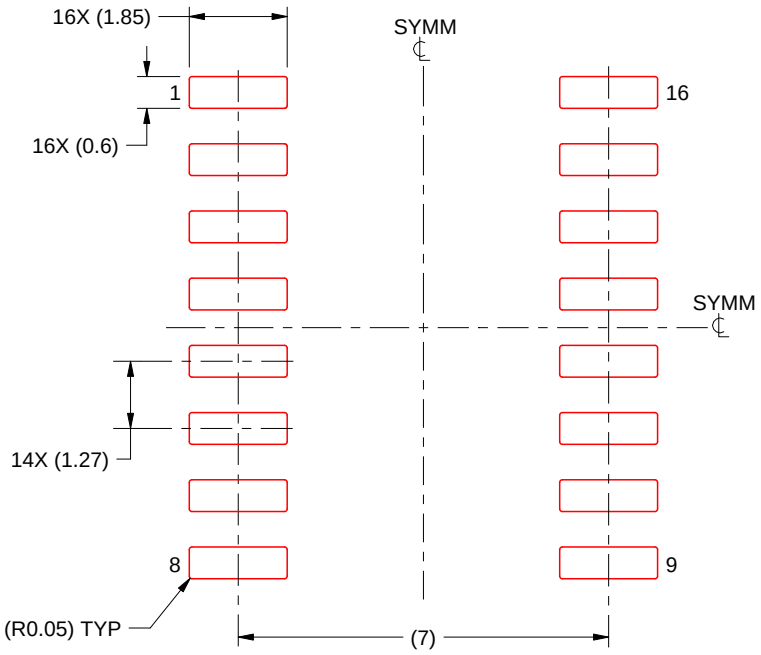
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

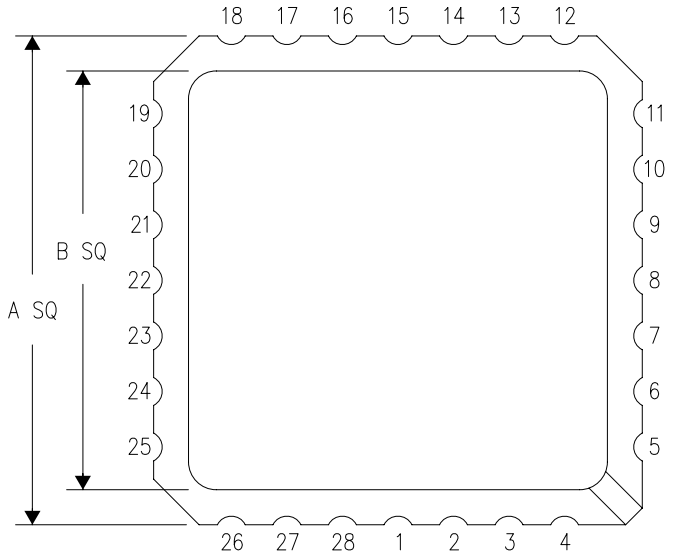
4220735/A 12/2021

NOTES: (continued)

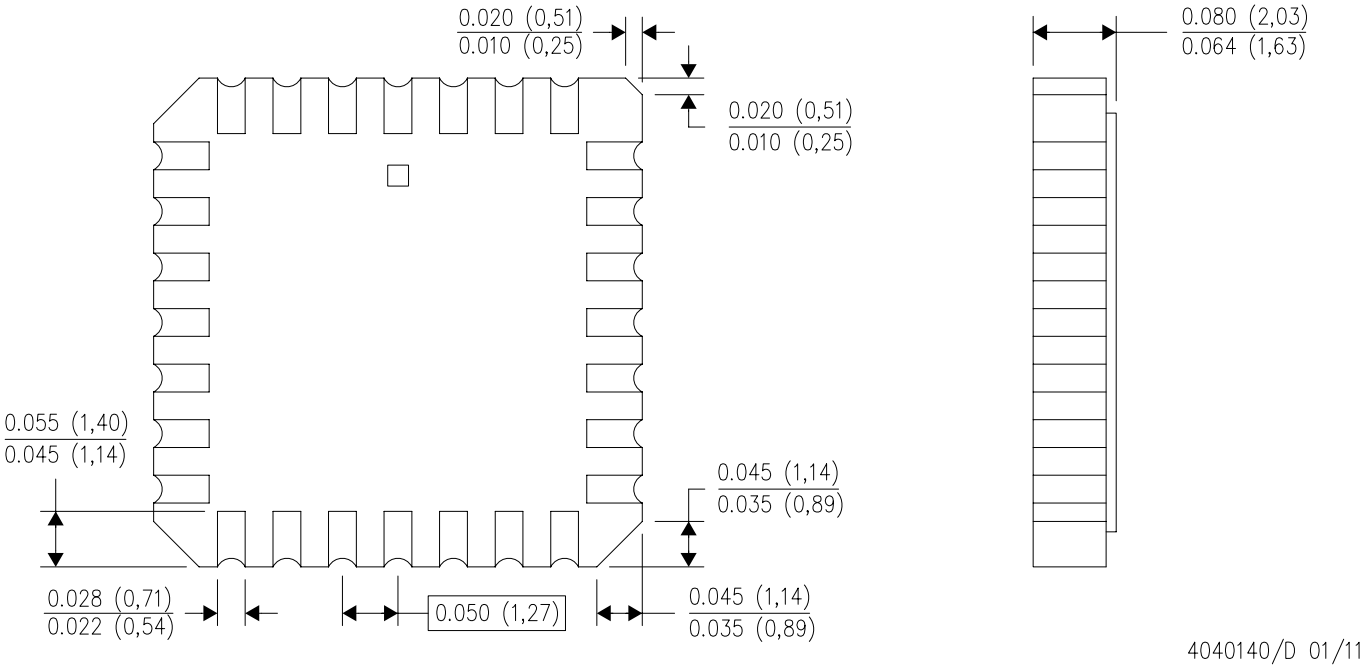
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



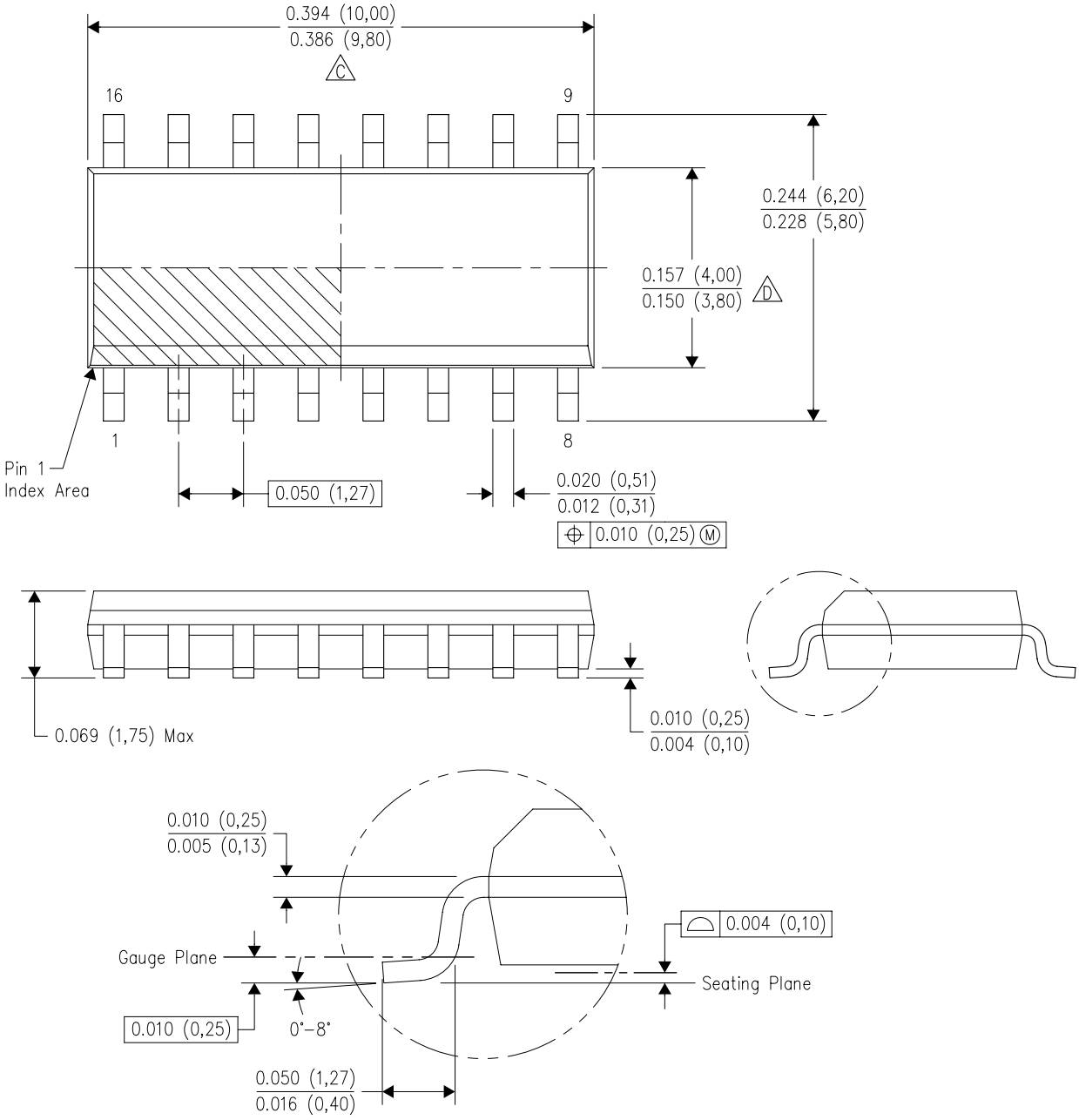

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

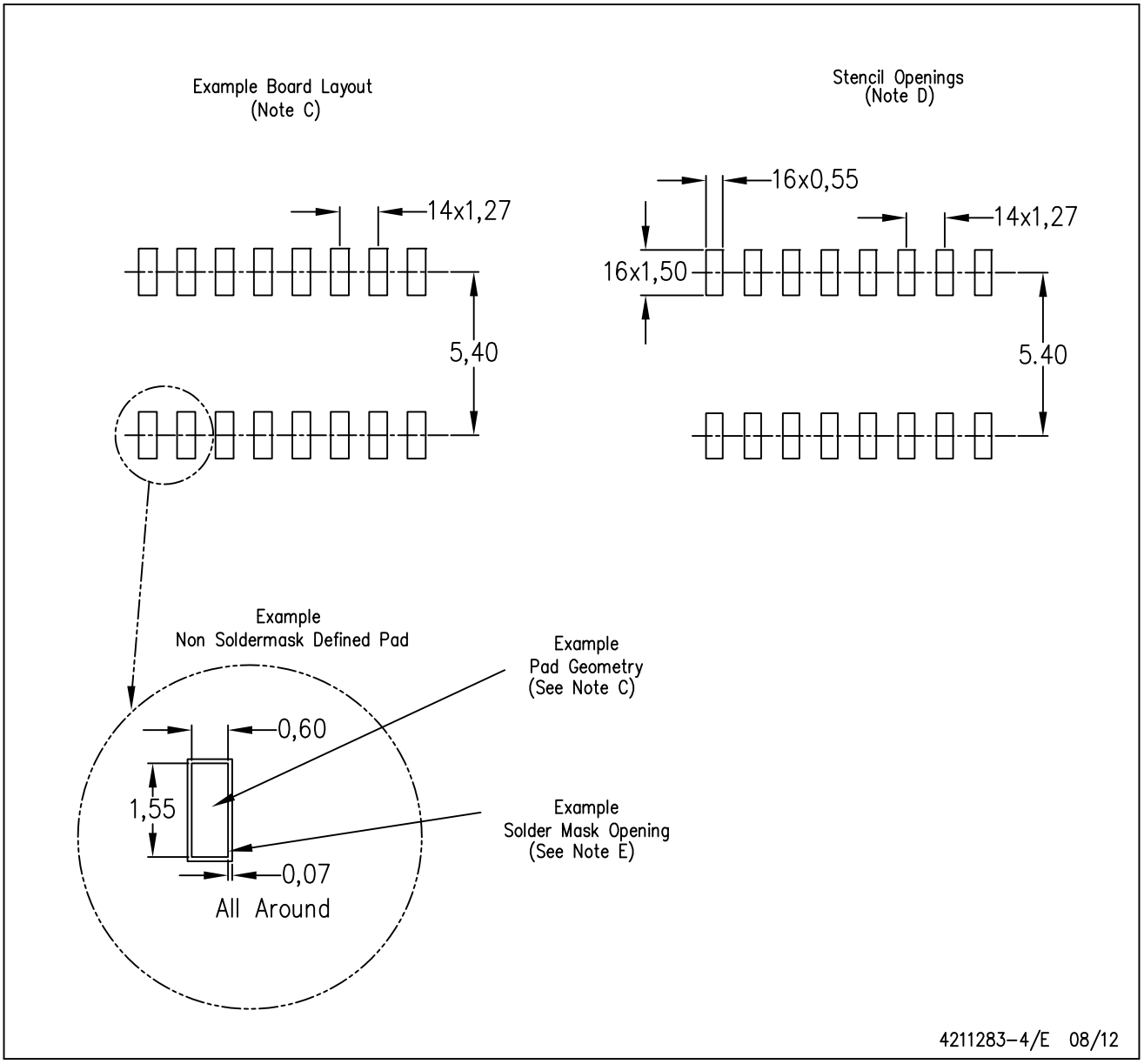
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



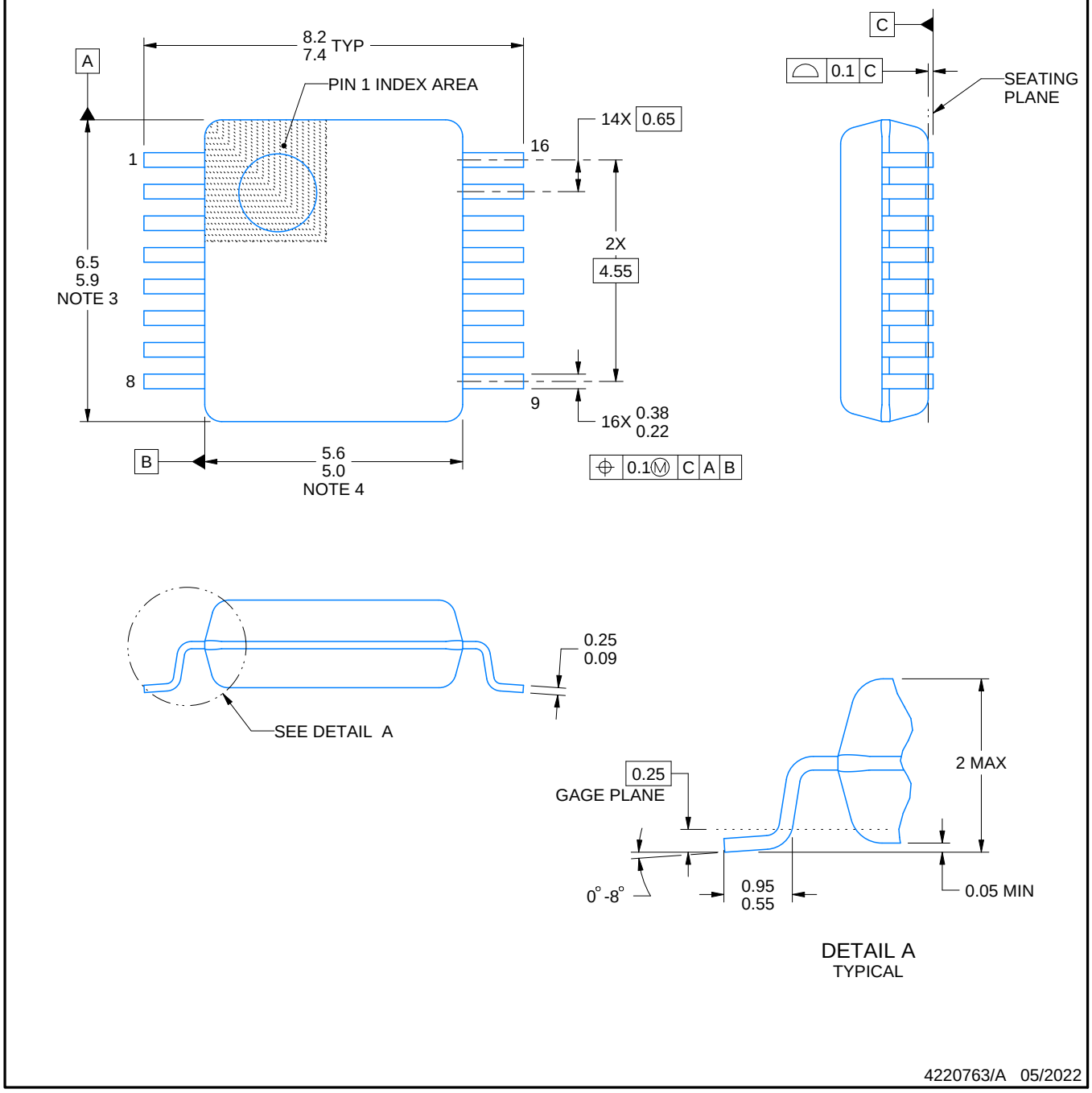

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## DB0016A

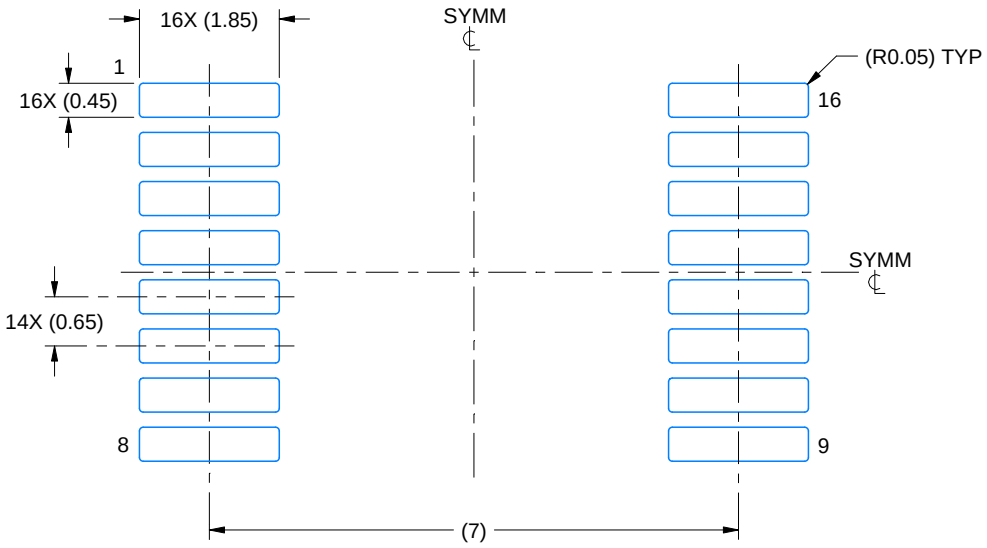
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

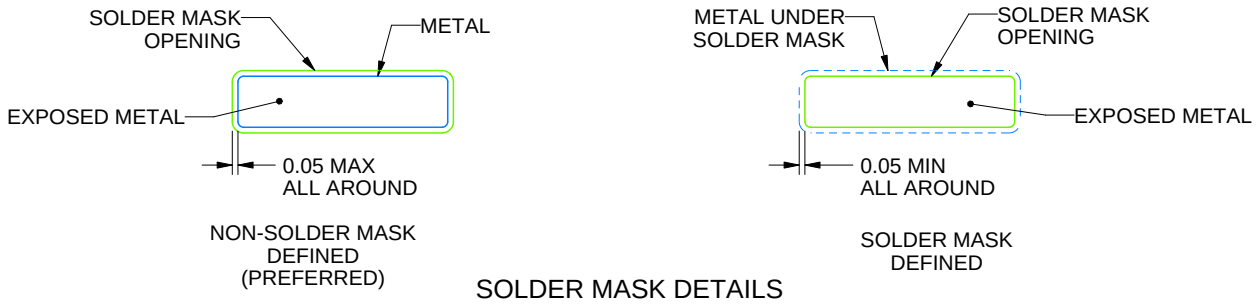



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

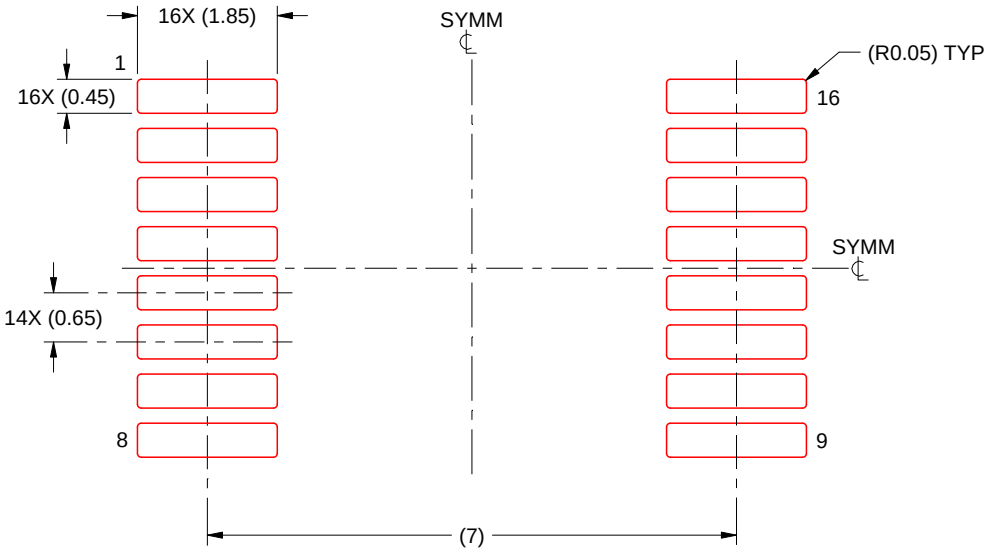



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

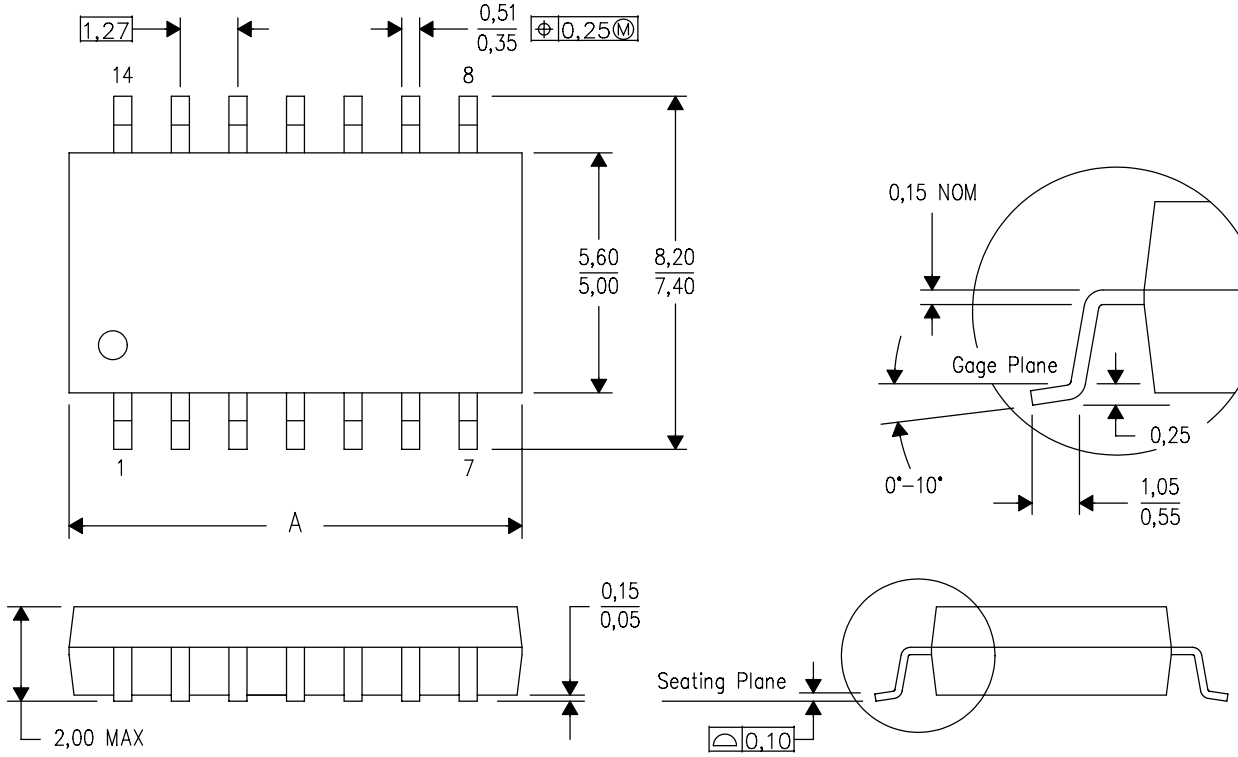
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated