SM72485 100-V, 150-mA Constant On-Time Buck Switching Regulator

1 Features

- Operating Input Voltage: 6 V to 95 V
- Integrated 100-V, N-Channel Buck Switch
- Internal Start-Up Regulator
- No Loop Compensation Required
- Ultra-Fast Transient Response
- On-time Varies Inversely With Input Voltage
- Operating Frequency Remains Constant With Varying Line Voltage and Load Current
- Adjustable Output Voltage From 2.5 V
- Highly Efficient Operation
- Precision Internal Reference
- Low Bias Current
- Intelligent Current Limit
- Thermal Shutdown
- Package
  - VSSOP (3 mm × 3 mm)
  - WSON (4 mm × 4 mm)

2 Applications

- PV Panel Smart Junction Boxes
- Nonisolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- 42-V Automotive Systems

3 Description

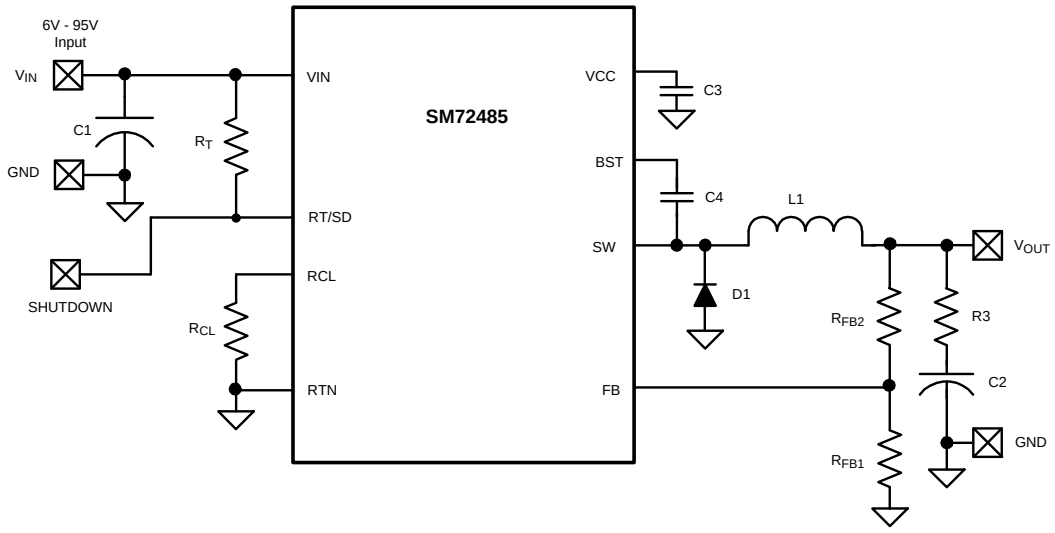
The SM72485 step-down switching regulator features all of the functions required to implement a low cost, efficient, Buck bias regulator. This high voltage regulator contains an 100-V N-channel buck switch. The device is easy to implement and is provided in the VSSOP and the thermally enhanced WSON package. The regulator is based on a control scheme using an on-time inversely proportional to V_{IN}. This feature allows the operating frequency to remain relatively constant. The control scheme requires no loop compensation. An intelligent current limit is implemented with forced off-time, which is inversely proportional to V_{OUT}. This scheme ensures short circuit control while providing minimum foldback. Other features include: Thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limiter, and a precharge switch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SM72485	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application, Basic Step-Down Regulator



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E — **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Renewable Energy Grade from *Features* ... 1
- Deleted Lead temperature (260°C maximum) from *Absolute Maximum Ratings* table ... 4
- Changed Junction to Ambient, $R_{\theta JA}$, value in *Thermal Information* table From: 200°C/W To: 139.6°C/W (VSSOP) and From: 40°C/W To: 42.3°C/W (WSON) ... 4

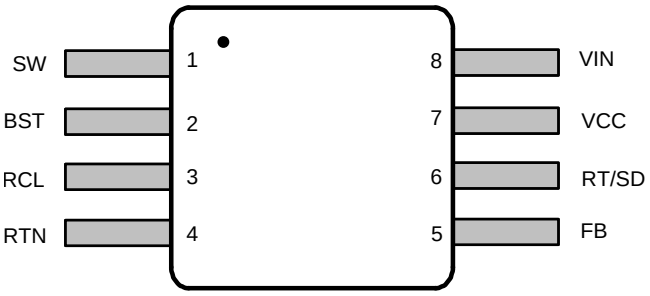
Changes from Revision C (April 2013) to Revision D — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

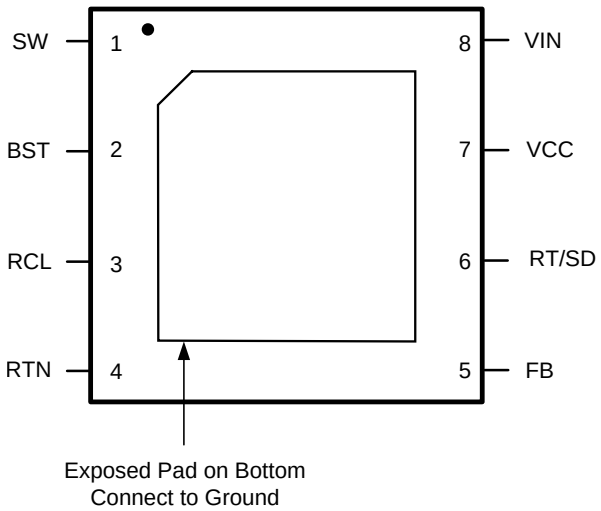
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5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



NGU Package
8-Pin WSON
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	VSSOP	WSON		
BST	2	2	I	An external capacitor is required between the BST and the SW pins. TI recommends a 0.01-µF ceramic capacitor. An internal diode charges the capacitor from VCC during each off-time.
FB	5	5	I	This pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V.
RCL	3	3	I	A resistor between this pin and RTN sets the off-time when current limit is detected. The off-time is preset to 35 µs if FB = 0 V.
RT/SD	6	6	I	A resistor between this pin and VIN sets the switch on-time as a function of V_{IN}. The minimum recommended on-time is 400 ns at the maximum input voltage. This pin can be used for remote shutdown.
RTN	4	4	G	Ground for the entire circuit.
SW	1	1	O	Power switching node. Connect to the output inductor, re-circulating diode, and bootstrap capacitor.
VCC	7	7	I	This regulated voltage provides gate drive power for the internal Buck switch. An internal diode is provided between this pin and the BST pin. A local 0.47-µF decoupling capacitor is required. The series pass regulator is current limited to 9 mA.
VIN	8	8	I	Input operating voltage: 6 V to 95 V.
Exposed Pad	—	Thermal Pad	NC	The exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance.

(1) G = Ground, I = Input, O = Output, NC = No Contact

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
V_{IN} to GND	–0.3	100	V
BST to GND	–0.3	114	V
SW to GND (steady-state)	–1		V
BST to V_{CC}		100	V
BST to SW		14	V
V_{CC} to GND		14	V
All other inputs to GND	–0.3	7	V
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For detailed information on soldering plastic VSSOP and WSON packages, see *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	6	95	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SM72485		UNIT
		DGK (VSSOP)	NGU (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.6	42.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	41.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.5	20.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

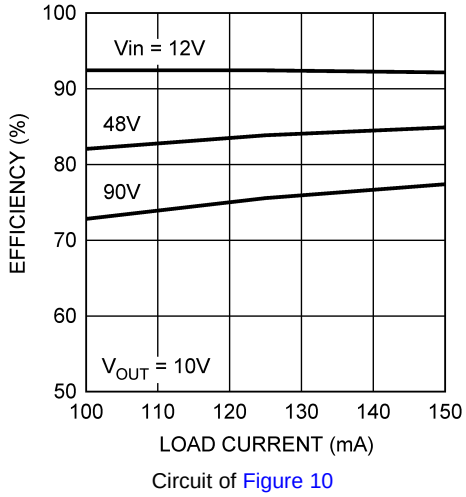
Typical values apply for $T_A = T_J = 25°C$, Minimum and Maximum limits apply for $T_A = T_J = –40°C$ to 125°C, and $V_{IN} = 48$ V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC}REG	V_{CC} regulator output	V_{IN} = 48 V	6.6	7	7.4	V
	Dropout voltage, $V_{IN} – V_{CC}$	V_{IN} = 6 V to 8.5 V		100		mV
	V_{CC} bypass threshold	V_{IN} rising		8.5		V
	V_{CC} bypass hysteresis			300		mV
	V_{CC} output impedance	V_{IN} = 6 V		100		Ω
		V_{IN} = 10 V		8.8		
		V_{IN} = 48 V		0.8		
	V_{CC} current limit	V_{IN} = 48 V		9.2		mA
	V_{CC} UVLO	V_{CC} rising		5.3		V
	V_{CC} UVLO hysteresis			190		mV
	V_{CC} UVLO filter delay			3		µs
I_{CC}	Operating current	V_{FB} = 3 V, V_{IN} = 48 V		550	750	µA
	Shutdown current	$V_{RT/SD}$ = 0 V		110	176	µA
SWITCH CHARACTERISTICS						
	Buckswitch $R_{DS(ON)}$	I_{TEST} = 200 mA		2.2	4.6	Ω
	Gate drive UVLO	$V_{BST} – V_{SW}$ rising	2.8	3.8	4.8	V
	Gate drive UVLO hysteresis			490		mV
	Precharge switch voltage	At 1 mA		0.8		V
	Precharge switch on-time			150		ns
CURRENT LIMIT						
	Current limit threshold		0.24	0.3	0.36	A
	Current limit response time	I_{SW} overdrive = 0.1 A, time to switch OFF		350		ns
t_{OFF_1}	Off-time generator	V_{FB} = 0 V, R_{CL} = 100 kΩ		35		µs
t_{OFF_2}	Off-time generator	V_{FB} = 2.3 V, R_{CL} = 100 kΩ		2.56		
ON-TIME GENERATOR						
t_{ON_1}	On-time generator	V_{IN} = 10 V, R_{ON} = 200 kΩ	2.15	2.77	3.5	µs
t_{ON_2}	On-time generator	V_{IN} = 95 V, R_{ON} = 200 kΩ	200	300	420	ns
	Remote shutdown threshold	Rising	0.4	0.7	1.05	V
	Remote shutdown hysteresis			35		mV
MINIMUM OFF-TIME						
	Minimum off-time	V_{FB} = 0 V		300		ns
REGULATION AND OV COMPARATORS						
	FB reference threshold	Internal reference, trip point for switch = ON	2.445	2.5	2.55	V
	FB overvoltage threshold	Trip point for switch = OFF		2.875		V
	FB bias current			100		nA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			25		°C

(1) All limits are ensured. All electrical characteristics having room temperature limits are tested during production with $T_A = T_J = 25°C$. All minimum and maximum limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

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6.6 Typical Characteristics



Circuit of Figure 10

Figure 1. Efficiency vs Load Current and V_{IN}

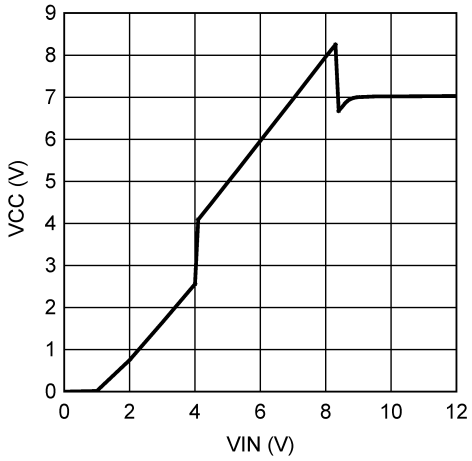


Figure 2. V_{CC} vs V_{IN}

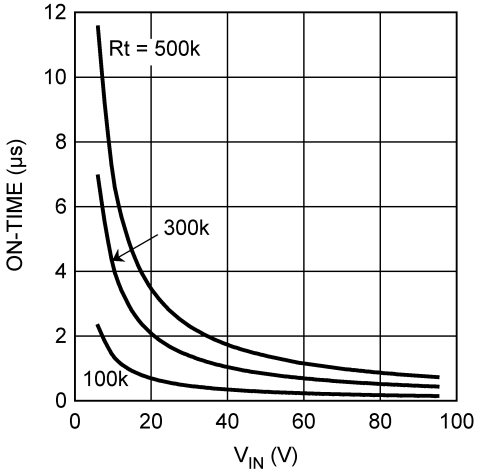


Figure 3. On-Time vs Input Voltage and R_T

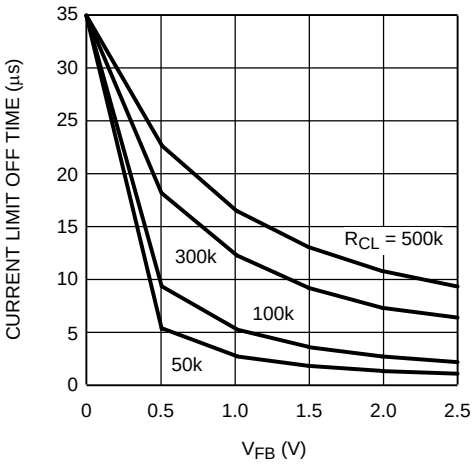


Figure 4. Current Limit OFF-Time vs V_{FB} and R_{CL}

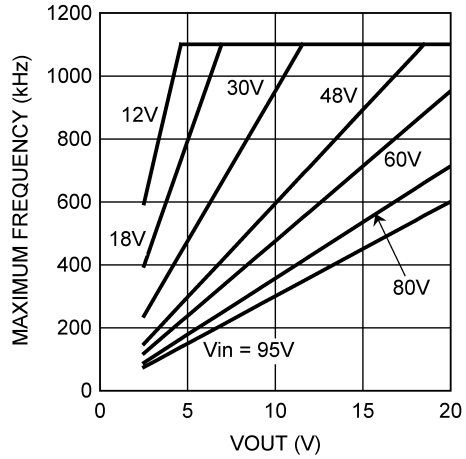


Figure 5. Maximum Frequency vs V_{OUT} and V_{IN}

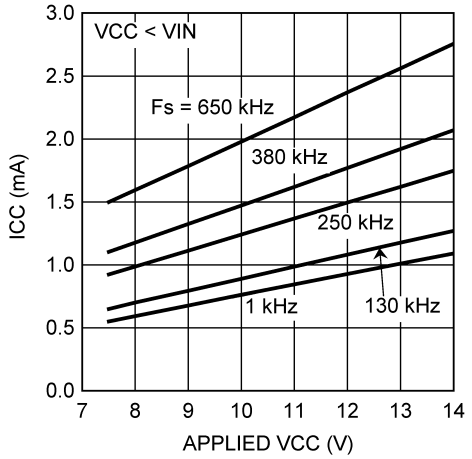


Figure 6. I_{CC} Current vs Applied V_{CC} Voltage

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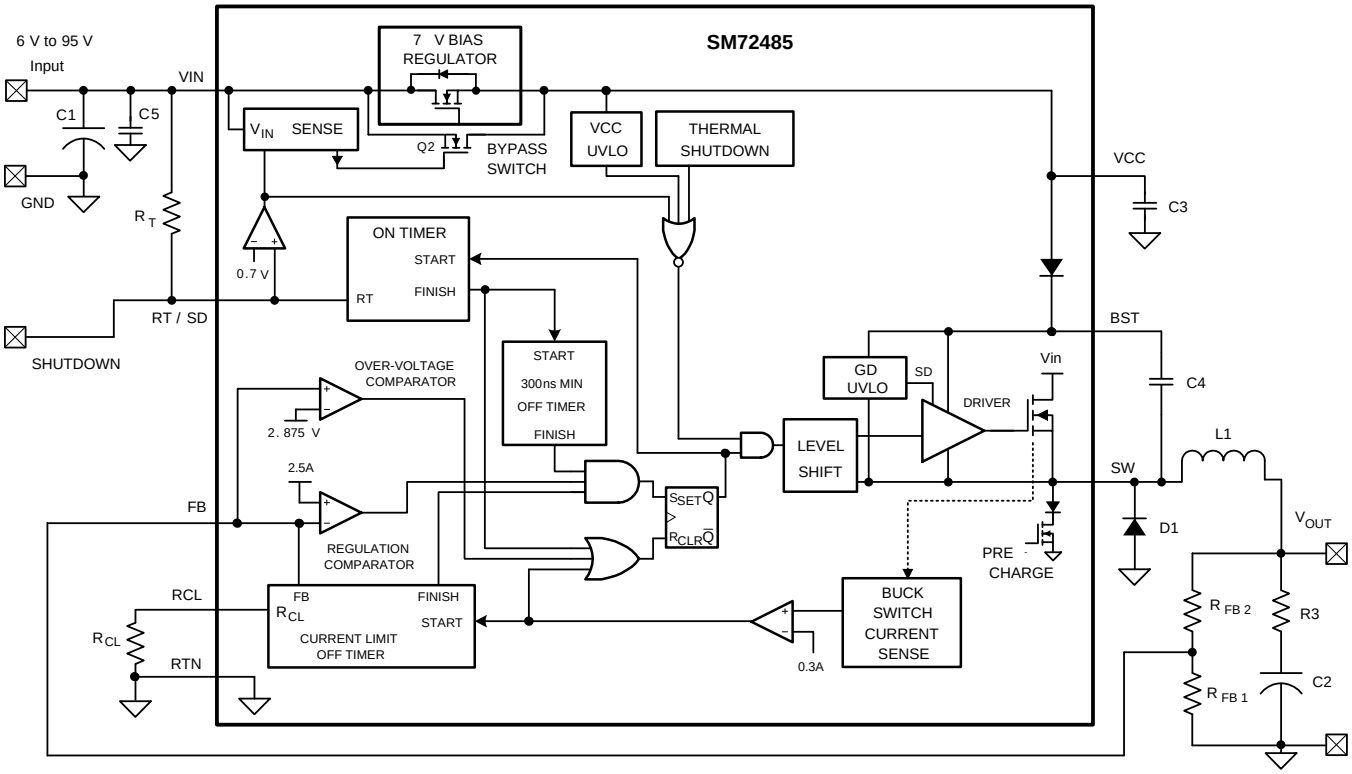
7 Detailed Description

7.1 Overview

The SM72485 step-down switching regulator features all the functions required to implement a low-cost, efficient, buck-bias power converter. This high-voltage regulator contains a 100-V, N-channel buck switch that is easy to implement and is provided in the VSSOP and the thermally enhanced WSON package. The regulator is based on a control scheme using an on-time inversely proportional to V_{IN}. The control scheme requires no loop compensation. Current limit is implemented with forced off-time, which is inversely proportional to V_{OUT}. This scheme ensures short-circuit control while providing minimum foldback.

The SM72485 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for high voltage PV panel junction boxes, 48-V telecom and the new 42-V automotive power bus ranges. Features include: thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limit timer, intelligent current limit off-timer, and a precharge switch.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Control Circuit Overview

The SM72485 is a buck DC-DC regulator that uses a control scheme in which the on-time varies inversely with line voltage (V_{IN}). Control is based on a comparator and the on-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB level is below the reference the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor (R_T). Following the ON period, the switch remains off for at least the minimum off-timer period of 300 ns. If FB is still below the reference at that time, the switch turns on again for another on-time period. This continues until regulation is achieved.

Feature Description (continued)

The SM72485 operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference, until then the inductor current remains zero. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Therefore at light loads the conversion efficiency is maintained, because the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency can be calculated in Equation 1.

$$F = \frac{V_{OUT}^2 \times L \times 1.04 \times 10^{20}}{R_L \times (R_T)^2} \quad (1)$$

where

- R_L = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated in Equation 2.

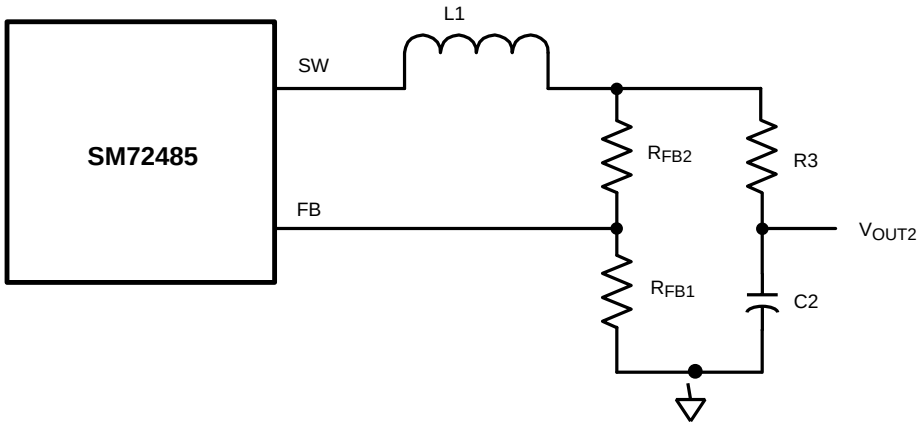
$$F = \frac{V_{OUT}}{1.385 \times 10^{-10} \times R_T} \quad (2)$$

The output voltage (V_{OUT}) is programmed by two external resistors as shown in the *Functional Block Diagram*. The regulation point can be calculated in Equation 3.

$$V_{OUT} = 2.5 \times (R_{FB1} + R_{FB2}) / R_{FB1} \quad (3)$$

The SM72485 regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. A minimum of 25 mV to 50 mV of ripple voltage at the feedback pin (FB) is required for the SM72485. In cases where the capacitor ESR is too small, additional series resistance may be required (R3 in the block diagram).

For applications where lower output voltage ripple is required the output can be taken directly from a low-ESR output capacitor, as shown in Figure 7. However, R3 slightly degrades the load regulation.



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Figure 7. Low Ripple Output Configuration

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Feature Description (continued)

7.3.2 Current Limit

The SM72485 contains an intelligent current limit off-timer. If the current in the Buck switch exceeds 0.3 A, the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by an external resistor (R_{CL}) and the FB voltage (see Figure 4). When FB = 0 V, a maximum off-time is required, and the time is preset to 35 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short-circuit operation up to the maximum input voltage of 95 V. In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time is less than 35 µs. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and the start-up time. The off-time is calculated in Equation 4.

$$t_{OFF} = 10^{-5} / (0.285 + (V_{FB} / 6.35 \times 10^{-6} \times R_{CL})) \quad (4)$$

The current-limit-sensing circuit is blanked for the first 50 ns to 70 ns of each on-time so it is not falsely tripped by the current surge which occurs at turnon. The current surge is required by the re-circulating diode (D1) for its turnoff recovery.

7.3.3 N-Channel Buck Switch and Driver

The SM72485 integrates an N-channel buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01-µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the on-time.

During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 300 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

The internal precharge switch at the SW pin is turned on for ≅150 ns during the minimum off-time period, ensuring sufficient voltage exists across the bootstrap capacitor for the on-time. This feature helps prevent operating problems which can occur during very light load conditions, involving a long off-time, during which the voltage across the bootstrap capacitor could otherwise reduce below the gate drive UVLO threshold. The precharge switch also helps prevent start-up problems which can occur if the output voltage is precharged prior to turnon. After current limit detection, the precharge switch is turned on for the entire duration of the forced off-time.

7.3.4 Thermal Protection

The SM72485 must be operated so the junction temperature does not exceed 125°C during normal operation. An internal thermal shutdown circuit is provided to shutdown the SM72485 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state by disabling the buck switch. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 140°C (typical hysteresis = 25°C) normal operation is resumed.

7.4 Device Functional Modes

7.4.1 Start-Up Regulator (V_{CC})

The high voltage bias regulator is integrated within the SM72485. The input pin (VIN) can be connected directly to line voltages between 6 V and 95 V, with transient capability to 100 V. Referring to the block diagram and the graph of V_{CC} vs V_{IN}, when V_{IN} is between 6 V and the bypass threshold (nominally 8.5 V), the bypass switch (Q2) is on, and V_{CC} tracks V_{IN} within 100 mV to 150 mV. The bypass switch on-resistance is approximately 100 Ω, with inherent current limiting at approximately 100 mA. When V_{IN} is above the bypass threshold Q2 is turned off, and V_{CC} is regulated at 7 V. The V_{CC} regulator output current is limited at approximately 9.2 mA. When the SM72485 is shutdown using the RT/SD pin, the V_{CC} bypass switch is shut off regardless of the voltage at V_{IN}.

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Device Functional Modes (continued)

When V_{IN} exceeds the bypass threshold, the time required for Q2 to shut off is approximately 2 µs to 3 µs. The capacitor at VCC (C3) must be a minimum of 0.47 µF to prevent the voltage at VCC from rising above its absolute maximum rating in response to a step input applied at V_{IN}. C3 must be placed as close as possible to the VCC and RTN pins. In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5 V and 14 V can be diode connected to the VCC pin to shut off the V_{CC} regulator, thereby reducing internal power dissipation. The current required into the VCC pin is shown in Figure 6. Internally a diode connects VCC to VIN requiring that the auxiliary voltage be less than V_{IN}.

The turnon sequence is shown in Figure 8. During the initial delay (t1) VCC ramps up at a rate determined by its current limit and C3 while internal circuitry stabilizes. When V_{CC} reaches the upper threshold of its undervoltage lockout (UVLO, typically 5.3 V) the buckswitch is enabled. The inductor current increases to the current limit threshold (I_{LIM}) and during t2 V_{OUT} increases as the output capacitor charges up. When V_{OUT} reaches the intended voltage the average inductor current decreases (t3) to the nominal load current (I_O).

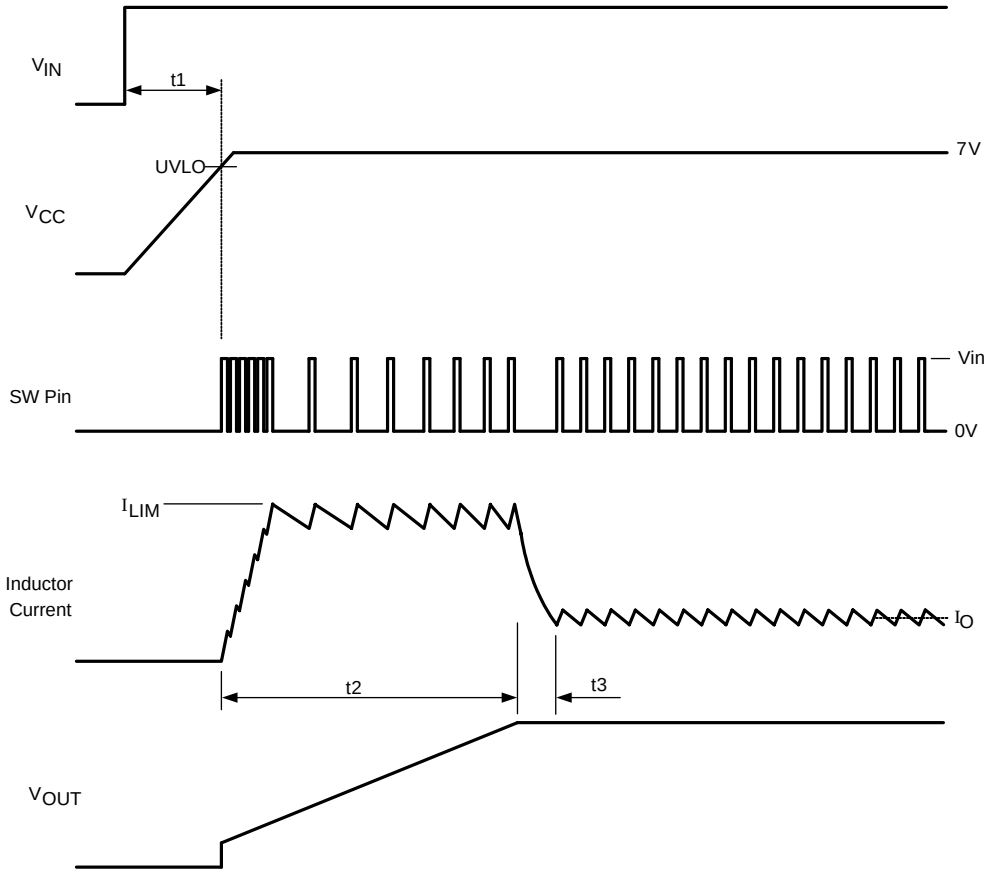


Figure 8. Start-Up Sequence

7.4.2 Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5-V reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch remains on for the on-time, causing the FB voltage to rise above 2.5 V. After the on-time period, the buck switch remains off until the FB voltage again falls below 2.5 V. During start-up, the FB voltage is below 2.5 V at the end of each on-time, resulting in the minimum off-time of 300 ns. Bias current at the FB pin is nominally 100 nA.

7.4.3 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.875-V reference. If the voltage at FB rises 2.875 V above the on-time pulse is immediately terminated. This condition can occur if the input voltage, or the output load, change suddenly. The buck switch does not turn on again until the voltage at FB falls below 2.5 V.

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Device Functional Modes (continued)

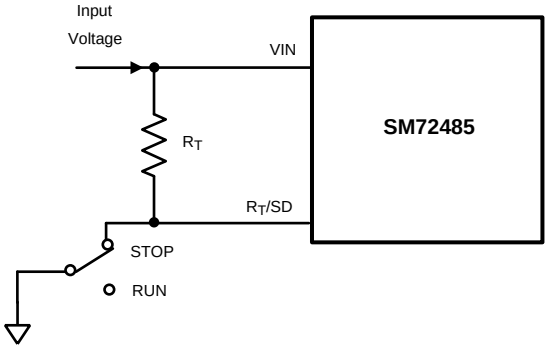
7.4.4 ON-Time Generator and Shutdown

The on-time for the SM72485 is determined by the R_T resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the SM72485 is Equation 5.

$$t_{ON} = 1.385 \times 10^{-10} \times R_T / V_{IN} \quad (5)$$

R_T must be selected for a minimum on-time (at maximum V_{IN}) greater than 400 ns, for proper current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}.

The SM72485 can be remotely disabled by taking the RT/SD pin to ground. See Figure 9. The voltage at the RT/SD pin is between 1.5 V and 3 V, depending on V_{IN} and the value of the R_T resistor.



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Figure 9. Shutdown Implementation

8 Application and Implementation

NOTE

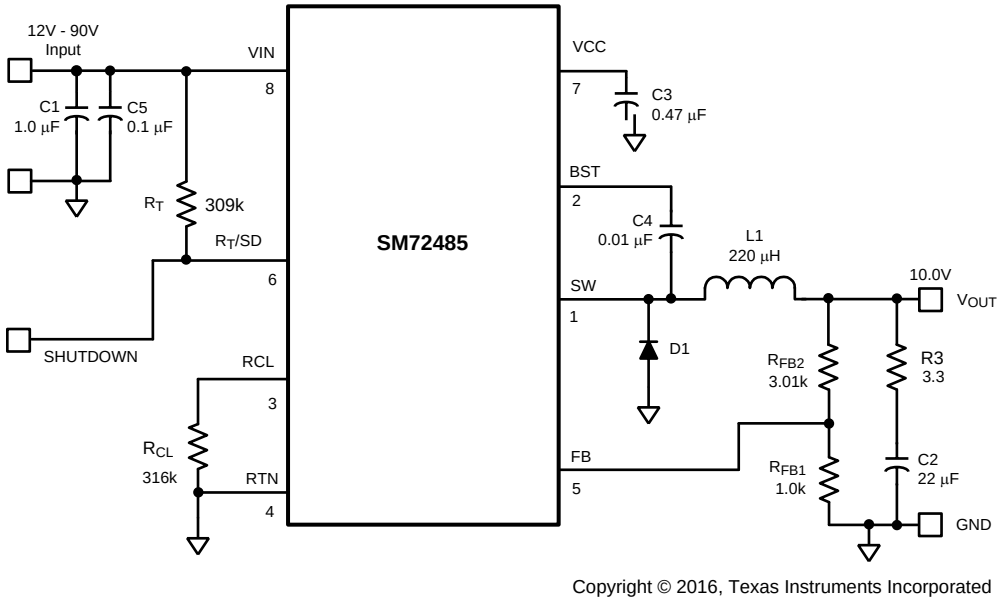
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SM72485 is a step-down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 150 mA. The following design procedure can be used to select components for the SM72485. This section presents a simplified discussion of the design process.

The final circuit is shown in Figure 10. The circuit was tested, and the resulting performance is shown in Figure 14 and Figure 15.

8.2 Typical Application



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Figure 10. SM72485 Example Circuit Diagram

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	12 V to 90 V
Output voltage	10 V
Minimum load current	100 mA
Maximum load current	150 mA
Feedback resistor ratio	3:1
Switching frequency	234 kHz
Inductor	200 µH

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8.2.2 Detailed Design Procedure

8.2.2.1 Selection of External Components

Here is a guide for determining the component values illustrated with a design example. See *Functional Block Diagram* and Table 2 for more information. The following sections configure the SM72485 for:

- Input voltage (V_{IN}): 12 V to 90 V
- Output voltage (V_{OUT1}): 10 V
- Load current (for continuous conduction mode): 100 mA to 150 mA

Table 2. Bill of Materials

ITEM	DESCRIPTION	PART NUMBER	VALUE
C1	Ceramic capacitor	TDK C4532X7R2A105M	1 µF, 100 V
C2	Ceramic capacitor	TDK C4532X7R1E226M	22 µF, 25 V
C3	Ceramic capacitor	Kemet C1206C474K5RAC	0.47 µF, 50 V
C4	Ceramic capacitor	Kemet C1206C103K5RAC	0.01 µF, 50 V
C5	Ceramic capacitor	TDK C3216X7R2A104M	0.1 µF, 100 V
D1	Schottky power diode	Diodes Inc. DFLS1100	100 V, 1 A
L1	Power inductor	COILTRONICS DR125-221-R, or	220 µH
		TDK SLF10145T-221MR65	
R_{FB2}	Resistor	Vishay CRCW12063011F	3.01 kΩ
R_{FB1}	Resistor	Vishay CRCW12061001F	1 kΩ
R3	Resistor	Vishay CRCW12063R30F	3.3 Ω
R_T	Resistor	Vishay CRCW12063093F	309 kΩ
R_{CL}	Resistor	Vishay CRCW12063163F	316 kΩ
U1	Switching regulator	Texas Instruments SM72485	—

8.2.2.1.1 R_{FB1} and R_{FB2}

$V_{OUT} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB1}$, and because V_{FB} = 2.5 V, the ratio of R_{FB2} to R_{FB1} calculates as 3:1. Standard values of 3.01 kΩ and 1 kΩ are chosen. Other values could be used as long as the 3:1 ratio is maintained.

8.2.2.1.2 F_s and R_T

The recommended operating frequency range for the SM72485 is 50 kHz to 1.1 MHz. Unless the application requires a specific frequency, the choice of frequency is generally a compromise, because it affects the size of L1 and C2, and the switching losses. The maximum allowed frequency, based on a minimum on-time of 400 ns, is calculated from Equation 6.

$$F_{MAX} = V_{OUT} / (V_{INMAX} \times 400\ ns) \quad (6)$$

For this exercise, F_{MAX} = 277 kHz. From Equation 2, R_T calculates to 260 kΩ. A standard value 309-kΩ resistor is used to allow for tolerances in Equation 2, resulting in a frequency of 234 kHz.

8.2.2.1.3 L1

The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum V_{IN}.

Minimum load current: To maintain continuous conduction at minimum Io (100 mA), the ripple amplitude (I_{OR}) must be less than 200 mA_{P-P} so the lower peak of the waveform does not reach zero. L1 is calculated using Equation 7.

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{OR} \times F_s \times V_{IN}} \quad (7)$$

At V_{IN} = 90 V, L1(min) calculates to 190 µH. The next larger standard value (220 µH) is chosen and with this value I_{OR} calculates to 173 mA_{P-P} at V_{IN} = 90 V, and 32 mA_{P-P} at V_{IN} = 12 V.

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Maximum load current: At a load current of 150 mA, the peak of the ripple waveform must not reach the minimum ensured value of the SM72485's current limit threshold (240 mA). Therefore the ripple amplitude must be less than 180 mA_{P-P}, which is already satisfied in the above calculation. With L1 = 220 µH, at maximum V_{IN} and I_O, the peak of the ripple is 236 mA. While L1 must carry this peak current without saturating or exceeding its temperature rating, it also must be capable of carrying the maximum specified value of the SM72485's current limit threshold (360 mA) without saturating, because the current limit is reached during start-up.

The DC resistance of the inductor must be as low as possible to minimize its power loss.

8.2.2.1.4 C3

The capacitor on the V_{CC} output provides not only noise filtering and stability, but its primary purpose is to prevent false triggering of the V_{CC} UVLO at the buck switch on or off transitions. C3 must be no smaller than 0.47 µF.

8.2.2.1.5 C2 and R3

When selecting the output filter capacitor C2, the items to consider are ripple voltage due to its ESR, ripple voltage due to its capacitance, and the nature of the load.

8.2.2.1.6 ESR and R3

A low ESR for C2 is generally desirable so as to minimize power losses and heating within the capacitor. However, the regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the SM72485 the minimum ripple required at pin 5 is 25 mV_{P-P}, requiring a minimum ripple at V_{OUT} of 100 mV. Because the minimum ripple current (at minimum V_{IN}) is 32 mA_{P-P}, the minimum ESR required at V_{OUT} is 100 mV / 32 mA = 3.12 Ω. Because quality capacitors for SMPS applications have an ESR considerably less than this, R3 is inserted as shown in the *Functional Block Diagram*. R3's value, along with C2's ESR, must result in at least 25-mV_{P-P} ripple at pin 5. Generally, R3 is 0.5 to 4 Ω.

8.2.2.1.7 R_{CL}

When current limit is detected, the minimum off-time set by this resistor must be greater than the maximum normal off-time, which occurs at maximum input voltage. Using Equation 5, the minimum on-time is 476 ns, yielding an off-time of 3.8 µs (at 234 kHz). Due to the 25% tolerance on the on-time, the off-time tolerance is also 25%, yielding a maximum off-time of 4.75 µs. Allowing for the response time of the current limit detection circuit (350 ns) increases the maximum off-time to 5.1 µs. This is increased an additional 25% to 6.4 µs to allow for the tolerances of Equation 4. Using Equation 4, R_{CL} calculates to 310 kΩ at V_{FB} = 2.5 V. A standard value 316-kΩ resistor is used.

8.2.2.1.8 D1

The important parameters are reverse recovery time and forward voltage. The reverse recovery time determines how long the reverse current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is only this diode's voltage which forces the inductor current to reduce during the forced off-time. For this reason, a higher voltage is better, although that affects efficiency. A good choice is a Schottky power diode, such as the DFLS1100. D1's reverse voltage rating must be at least as great as the maximum V_{IN}, and its current rating be greater than the maximum current limit threshold (360 mA).

8.2.2.1.9 C1

This capacitor's purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at V_{IN}, on the assumption that the voltage source feeding V_{IN} has an output impedance greater than zero. At maximum load current, when the buck switch turns on, the current into pin 8 suddenly increases to the lower peak of the output current waveform, ramp up to the peak value, then drop to zero at turnoff. The average input current during this on-time is the load current (150 mA). For a worst case calculation, C1 must supply this average load current during the maximum on-time. To keep the input voltage ripple to less than 2 V (for this exercise), C1 is calculated by Equation 8.

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.15\,A \times 3.57\,\mu s}{2.0\,V} = 0.268\ \mu F \tag{8}$$

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Quality ceramic capacitors in this value have a low ESR which adds only a few millivolts to the ripple. It is the capacitance which is dominant in this case. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 1-µF, 100-V, X7R capacitor is used.

8.2.2.1.10 C4

TI recommends a value of 0.01 µF for C4, as this is appropriate in the majority of applications. A high-quality ceramic capacitor, with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turnon. A low ESR also ensures a quick recharge during each off-time. At minimum V_{IN}, when the on-time is at maximum, it is possible during start-up that the C4 does not fully recharge during each 300-ns off-time. The circuit is not able to complete the start-up and achieve output regulation then. This can occur when the frequency is intended to be low (for example, R_T = 500 K). In this case, C4 must be increased so it can maintain sufficient voltage across the buck switch driver during each on-time.

8.2.2.1.11 C5

This capacitor helps avoid supply voltage transients and ringing due to long lead inductance at V_{IN}. A low ESR, 0.1-µF ceramic chip capacitor is recommended, placed close to the SM72485.

8.2.2.2 Low Output Ripple Configurations

For applications where low output ripple is required, the following sections can be used to reduce or nearly eliminate the ripple.

8.2.2.2.1 Reduced Ripple Configuration

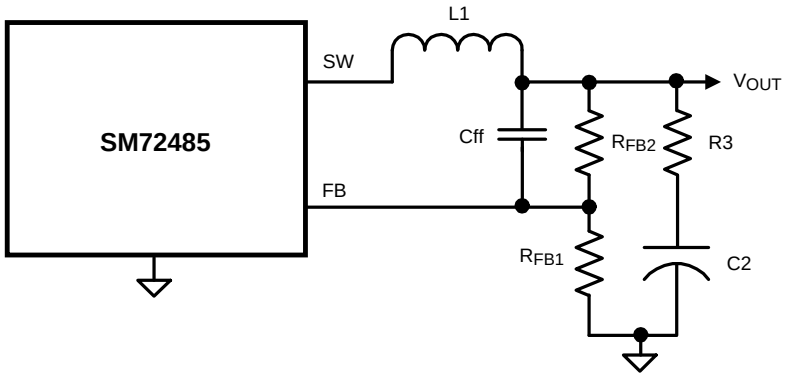
In Figure 11, Cff is added across R_{FB2} to AC-couple the ripple at V_{OUT} directly to the FB pin. This allows the ripple at V_{OUT} to be reduced to a minimum of 25 mVp–p by reducing R3, because the ripple at V_{OUT} is not attenuated by the feedback resistors. The minimum value for Cff is determined from Equation 9.

$$Cff = \frac{3 \times t_{ON(max)}}{(R_{FB1} // R_{FB2})} \quad (9)$$

where

- $t_{ON(max)}$ is the maximum on-time which occurs at $V_{IN(min)}$

The next larger standard value capacitor must be used for Cff.



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Figure 11. Reduced Ripple Configuration

8.2.2.2.2 Minimum Ripple Configuration

If the application requires a lower value of ripple (<10 mVp–p), the circuit of Figure 12 can be used. R3 is removed, and the resulting output ripple voltage is determined by the inductor's ripple current and C2's characteristics. RA and CA are chosen to generate a sawtooth waveform at their junction, and that voltage is AC-coupled to the FB pin through CB. To determine the values for RA, CA and CB, use Equation 10.

Calculate $V_A = V_{OUT} – (V_{SW} \times (1 – (V_{OUT} / V_{IN(min)})))$

where

- V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1 V) (10)

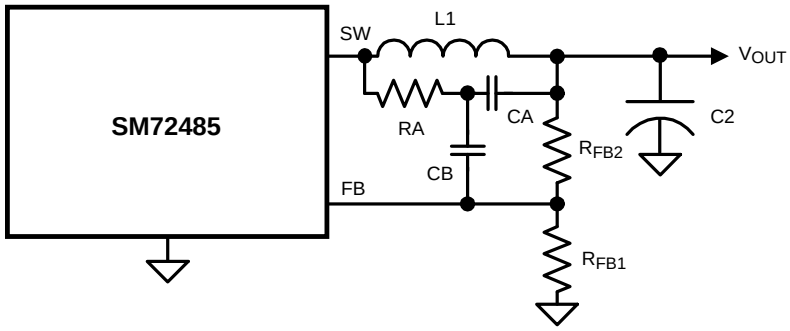
V_A is the DC voltage at the RA/CA junction, and is used in Equation 11.

Calculate $RA \times CA = (V_{IN(min)} – V_A) \times t_{ON} / \Delta V$

where

- t_{ON} is the maximum on-time (at minimum input voltage)
- ΔV is the desired ripple amplitude at the RA/CA junction (typically 40 mV to 50 mV) (11)

RA and CA are then chosen from standard value components to satisfy the above product. Typically CA is 1000 pF to 5000 pF, and RA is 10 kΩ to 300 kΩ. CB is then chosen large compared to CA, typically 0.1 µF.

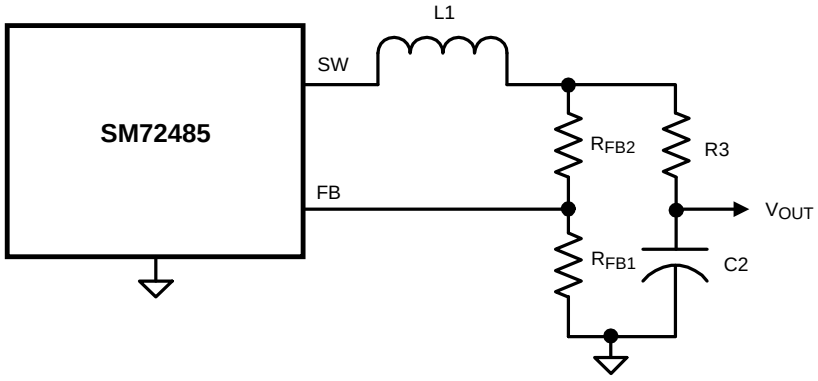


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Figure 12. Minimum Output Ripple Using Ripple Injection

8.2.2.2.3 Alternate Minimum Ripple Configuration

The circuit in Figure 13 is the same as that in the block diagram, except the output voltage is taken from the junction of R3 and C2. The ripple at V_{OUT} is determined by the inductor's ripple current and C2's characteristics. However, R3 slightly degrades the load regulation. This circuit may be suitable if the load current is fairly constant.



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Figure 13. Alternate Minimum Output Ripple

8.2.3 Application Curves

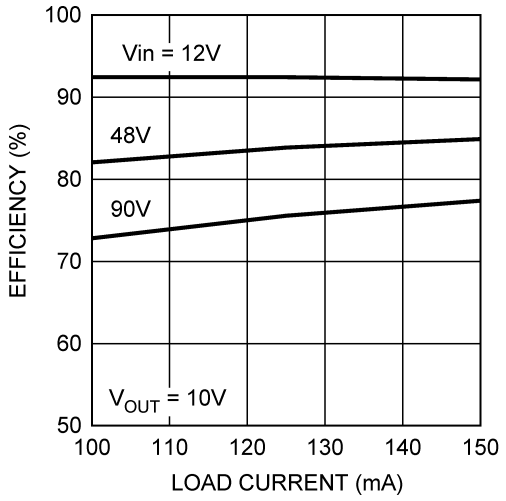


Figure 14. Efficiency vs Load Current and V_{IN}

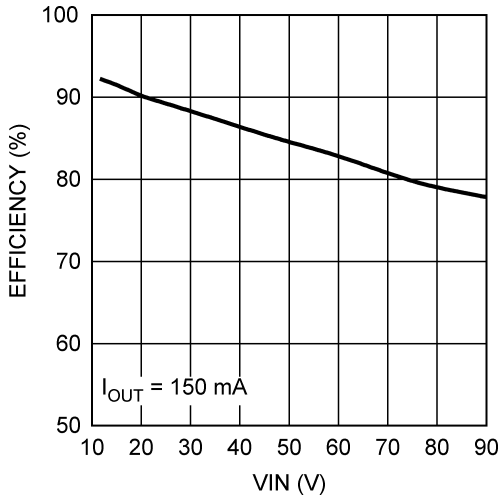


Figure 15. Efficiency vs V_{IN}

9 Power Supply Recommendations

The SM72485 is designed to operate from an input voltage supply range between 6 V and 95 V. This input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the SM72485 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is placed more than a few inches from the SM72485, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

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10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines must be observed.

1. CIN: The loop consisting of input capacitor (CIN), VIN pin, and RTN pin carries switching currents. Therefore, the input capacitor must be placed close to the IC, directly across VIN and RTN pins and the connections to these two pins must be direct to minimize the loop area. In general, it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-µF or 0.47-µF capacitor directly across the VIN and RTN pins close to the IC, and the remaining bulk capacitor as close as possible.
2. CVCC and CBST: The VCC and bootstrap (BST) bypass capacitors supply switching currents to the high- and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area must be minimized.
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of SM72485. Therefore, take care while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace must not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between VIN and GND every cycle and is therefore a possible source of noise. The SW node area must be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

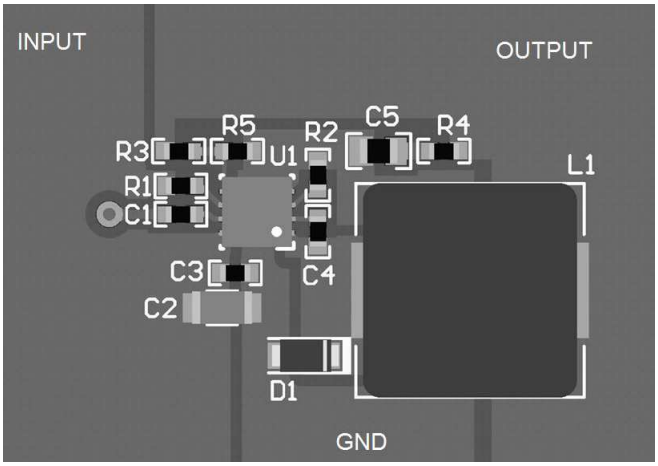


Figure 16. Layout Recommendation

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Absolute Maximum Ratings for Soldering (SNOA549)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM72485MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2485	Samples
SM72485MME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2485	Samples
SM72485MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2485	Samples
SM72485SD/NOPB	ACTIVE	WSON	NGU	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S2485	Samples
SM72485SDE/NOPB	ACTIVE	WSON	NGU	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S2485	Samples
SM72485SDX/NOPB	ACTIVE	WSON	NGU	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S2485	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

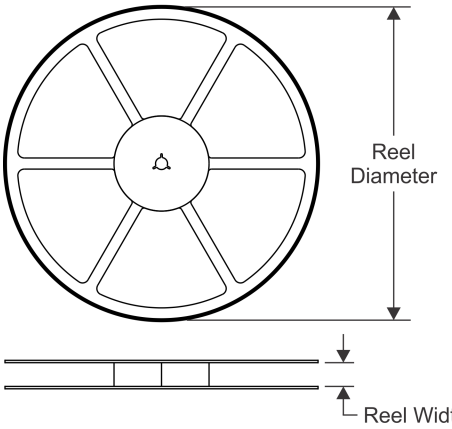
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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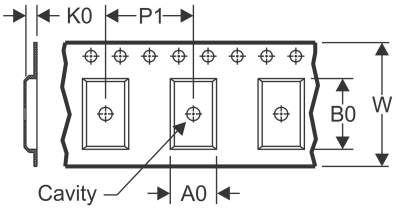
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

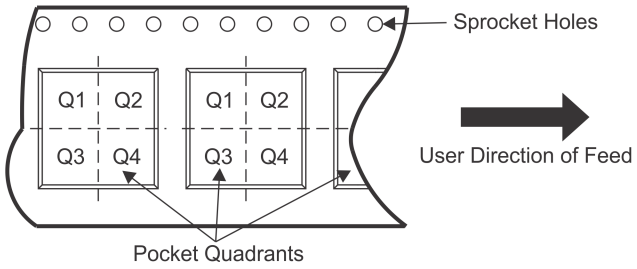


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

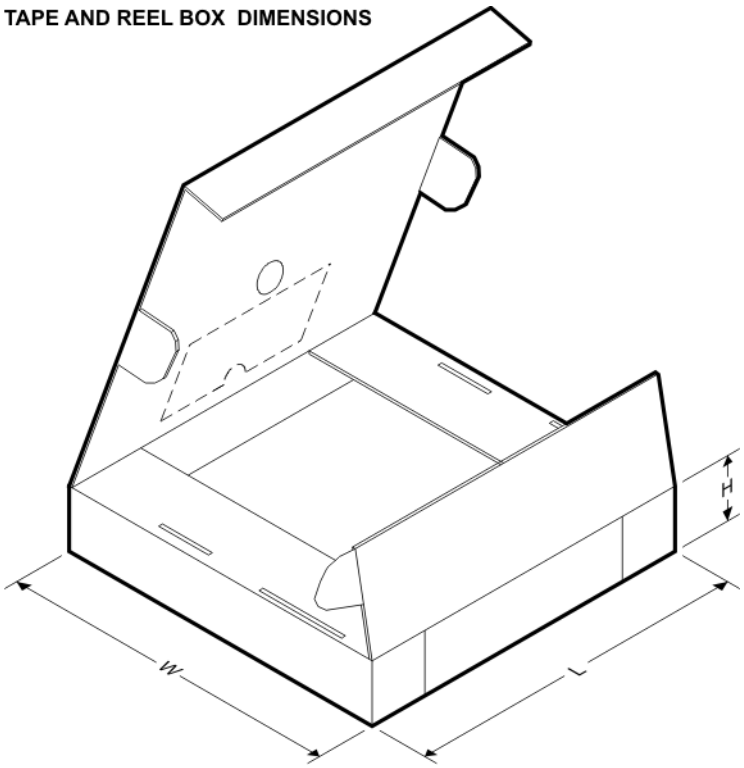
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM72485MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SM72485MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SM72485MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SM72485SD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
SM72485SDE/NOPB	WSON	NGU	8	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
SM72485SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

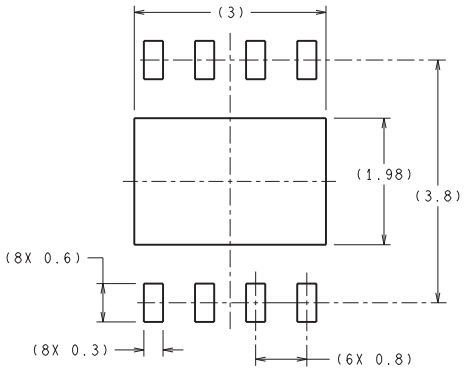
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

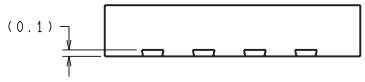
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM72485MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
SM72485MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
SM72485MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
SM72485SD/NOPB	WSON	NGU	8	1000	208.0	191.0	35.0
SM72485SDE/NOPB	WSON	NGU	8	250	208.0	191.0	35.0
SM72485SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

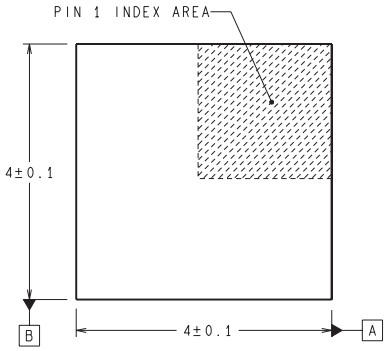
NGU0008B

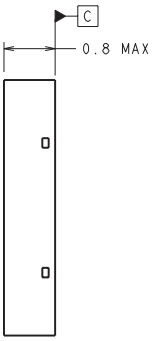


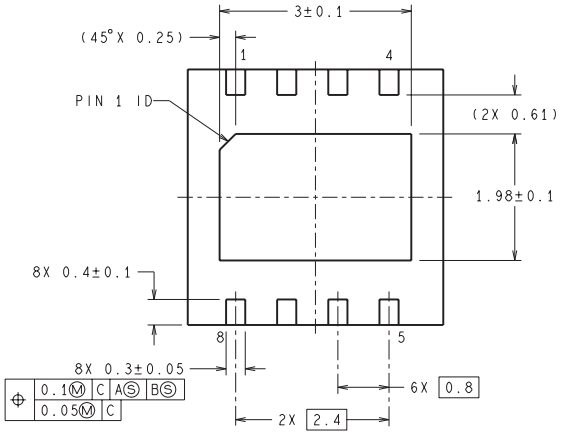
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



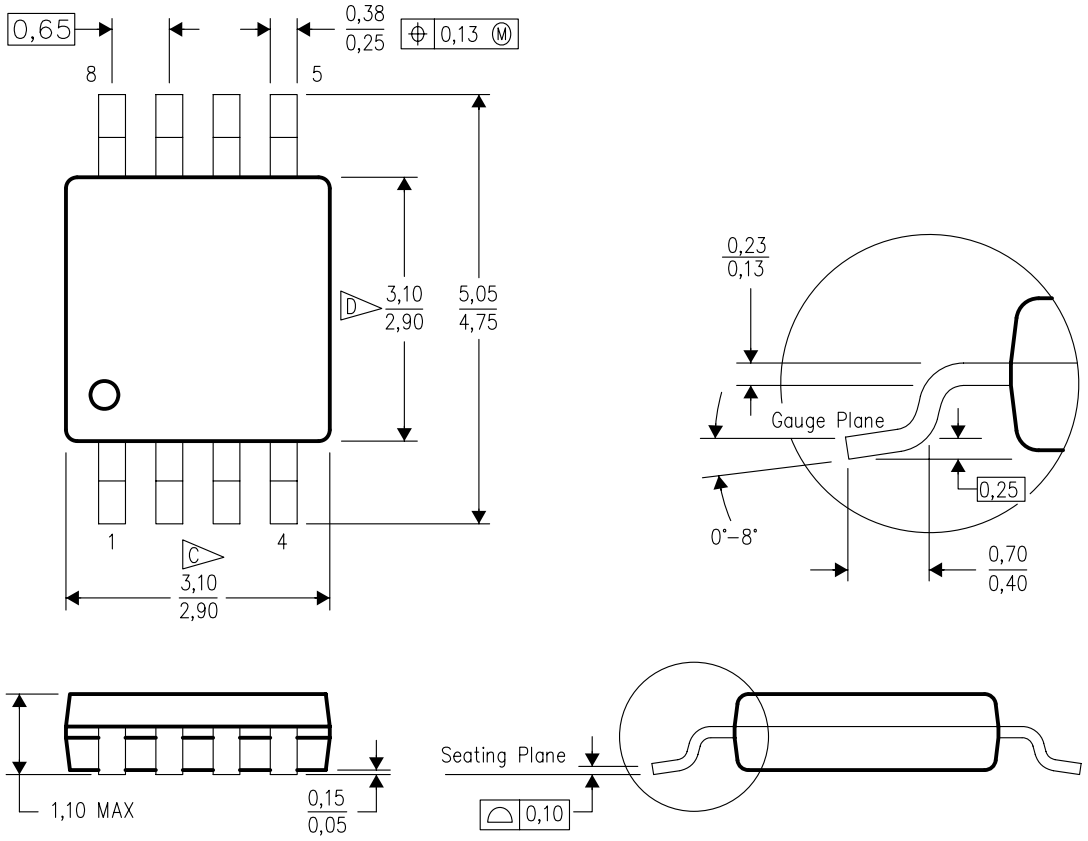






SDC08B (Rev A)

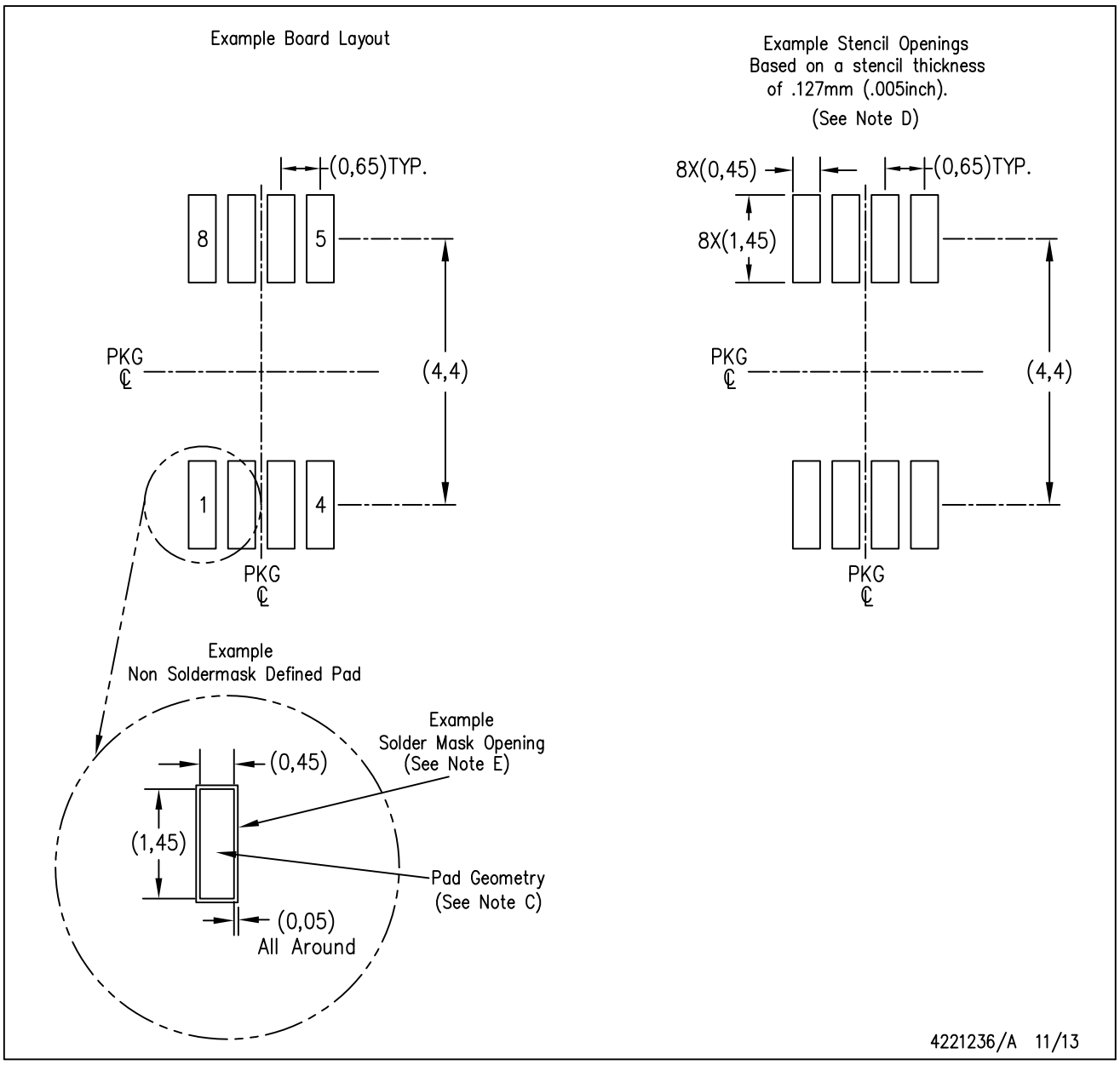
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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