SNx52x0 USB 端口瞬态抑制器

1 特性

- 旨在保护亚微米 3V 或 5V 电路免受瞬态噪声的影响
- 端口 ESD 保护功能超越了：
  - 15kV 人体放电模型
  - 2kV 机器模型
- 采用 WCSP 芯片级封装
- 关断电压：6V (最小值)
- 低电流泄漏：6V 时的最大值为 1μA
- 低电容：35pF (典型值)

2 应用

- USB 全速主机、HUB 或外设
- 端口

3 说明

SN65220 器件为双路单向瞬态电压抑制器，SN65240 和 SN75240 器件为四路单向瞬态电压抑制器 (TVS)。这些器件为通用串行总线 (USB) 低速和全速端口提供电瞬态噪声保护。35pF 的输入电容使其不适合用于高速 USB 2.0 应用。

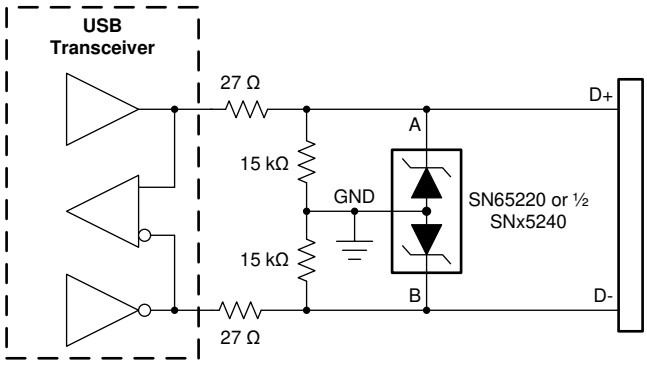
所有带线缆的 I/O 都容易遭受来自各种信号源的电瞬态噪声影响。这些瞬态噪声如果具有足够的幅度和持续时间，就有可能导致 USB 收发器或 USB ASIC 受到损坏。

SN65220、SN65240 和 SN75240 器件的 ESD 性能是在系统级别上根据 IEC61000-4-2 进行测量的；但是，系统设计会影响这些测试的结果。为了达到高符合性标准，需要周密的电路板设计和布局技术。

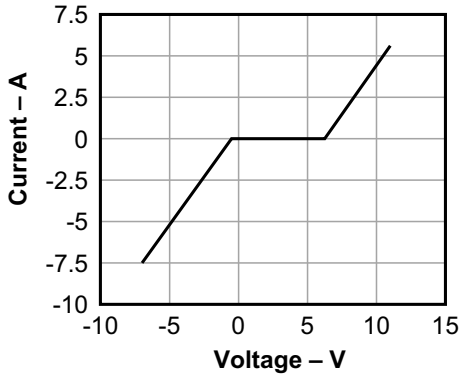
器件信息(1)

器件型号	封装	封装尺寸 (标称值)
SN65220	SOT-23 (6)	2.90mm × 1.60mm
	DSBGA (4)	0.925mm × 0.925mm
SN65240 SN75240	PDIP (8)	9.09mm × 6.35mm
	TSSOP (8)	3.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



TVS 电流与电压间的关系

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (May 2015) to Revision I (April 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将简化版原理图 图中的电阻单位从 *O* 更改为 Ω	1
• Updated the units from *O* to Ω in the *Typical Application Schematic for ESD Protection of USB Transceivers* figure	8
• Updated the units from *O* to Ω in the *Layout Example of a 4-Layer Board With SN65220* figure	10

Changes from Revision G (August 2008) to Revision H (May 2015)	Page
• 添加了 *引脚配置和功能* 部分、*ESD* 表、*热性能信息* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1

5 Device Comparison Table

PRODUCT	SUPPRESSORS	T_A - RANGE	PACKAGE
SN65220	1	–40°C to 85°C	WCSP-4
			SOT23-6
SN65240	2	–40°C to 85°C	DIP-8
			TSSOP-8
SN75240	2	0°C to 70°C	DIP-8
			TSSOP-8

6 Pin Configuration and Functions

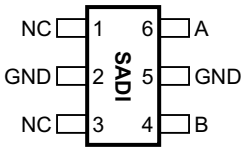


图 6-1. DBV Package 6-Pin SOT-23 Top View

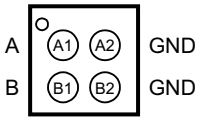


图 6-2. YZB Package 4-Pin DSBGA Top View

图 6-3. P, PW Packages 8-Pin PDIP, TSSOP Top View

表 6-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DBV	YZB	P, PW		
A	6	A1	8	Analog input	Transient suppressor input – Line 1
B	4	B2	6	Analog input	Transient suppressor input – Line 2
C	—	—	2	Analog input	Transient suppressor input – Line 3
D	—	—	4	Analog input	Transient suppressor input – Line 4
GND	2, 5	A2, B2	1, 3, 5, 7	Power	Local device ground
NC	1, 3	—	—	—	Internally not connected

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$P_{D(peak)}$	Peak power dissipation		60	W
I_{FSM}	Peak forward surge current		3	A
I_{RSM}	Peak reverse surge current		–9	A
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 7.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±15000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
T_A	Ambient temperature	SN75240	0	70	°C
		SN65220, SN65240	–40	85	

7.4 Thermal Information

THERMAL METRIC(1)		SN65220		SN65240, SN75240		UNIT
		DBV (SOT-23)	YZB (DSBGA)	P (PDIP)	PW (TSSOP)	
		6 PINS	4 BALLS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	199.5	170	67.5	185.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	159.7	1.8	57.9	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.1	43.5	44.5	114.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41	9.2	36.2	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.5	43.5	44.5	112.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current	V_I = 6 V at A, B, C, or D terminals			1	μA
$V_{(BR)}$	Breakdown voltage	V_I = 1 mA at A, B, C, or D terminals	6.5	7	8	V
C_{IN}	Input capacitance to ground	V_I = 0.4 sin (4E6 π t) + 0.5 V		35		pF

7.6 Typical Characteristics

T_A = 25°C unless otherwise noted.

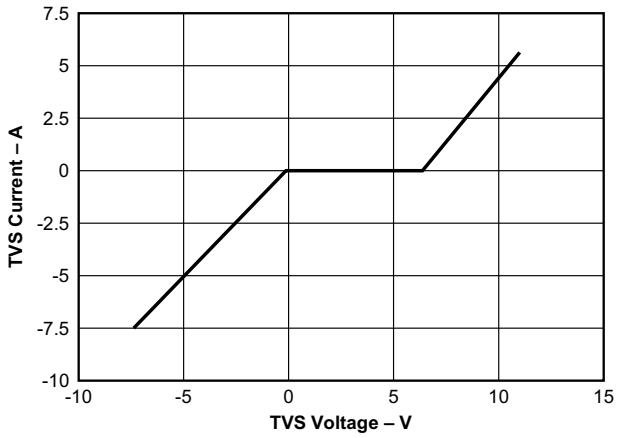


图 7-1. Transient-Voltage-Suppressor Current vs Voltage

8 Parameter Measurement Information

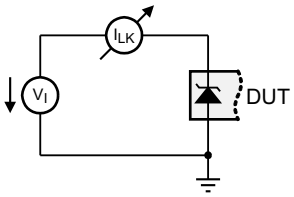


图 8-1. Measurement of Leakage Current

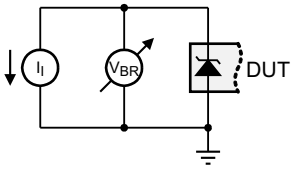


图 8-2. Measurement of Breakdown Voltage

9 Detailed Description

9.1 Overview

The SN65220, SN65240, and SN75240 devices integrate multiple unidirectional transient voltage suppressors (TVS). 图 9-1 shows the equivalent circuit diagram of a single TVS diode.

For positive transient voltages, only the Q1 transistor determines the switching characteristic. When the input voltage reaches the Zener voltage, V_Z, Zener diode D1 conducts; therefore, allowing for the base-emitter voltage, V_{BE}, to increase. At $V_{IN} = V_Z + V_{BE}$, the transistor starts conducting. From then on, its on-resistance decreases linearly with increasing input voltage.

For negative transient voltages, only diode D2 determines the switching characteristic. Here, switching occurs when the input voltage exceeds the diode forward voltage, V_{FW}.

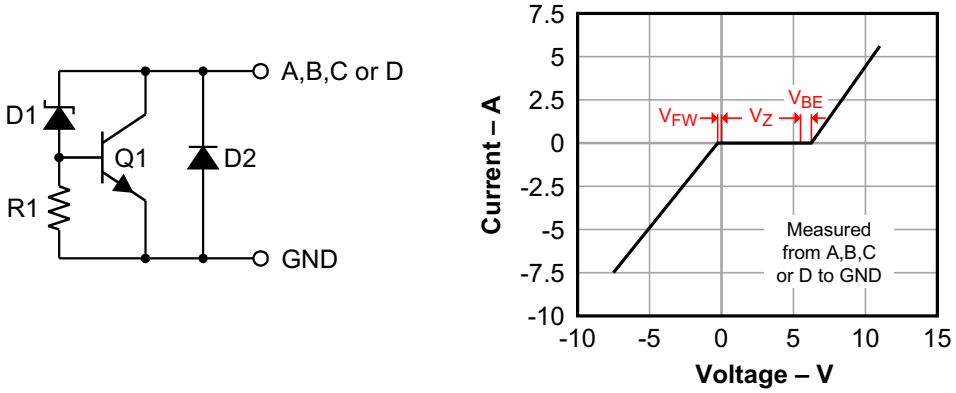
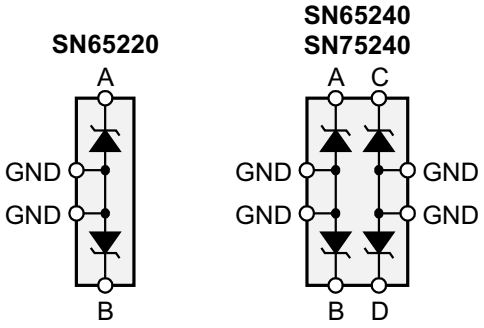


图 9-1. TVS Structure and Current — Voltage Characteristic

9.2 Functional Block Diagram



9.3 Feature Description

The SN65220, SN65240, and SN75240 family of unidirectional transient voltage suppressors provide transient protection to Universal Serial Bus low and full−speed ports. These TVS diodes provide a minimum breakdown voltage of 6.5V to protect USB transceivers and USB ASICs typically implemented in 3-V or 5-V digital CMOS technology.

9.4 Device Functional Modes

TVS diodes possess two functional modes, a high-impedance and a conducting mode.

During normal operating conditions, that is in the absence of high voltage transients, the breakdown voltage of TVS diodes is not exceeded and the devices remain high-impedance.

In the presence of high-voltage transients the breakdown voltage is exceeded. The TVS diodes then conduct and become low-impedance. In this mode excessive transient energy is shunted directly to local circuit ground, preventing USB transceivers from electrical damage.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The universal serial bus (USB) has become a popular solution to connect PC peripherals. USB allows devices to be hot-plugged in and out of the existing PC system without rebooting or turning off the PC. Because frequent human interaction with the USB system occurs as a result of its attractive hot-plugging ability, there is the possibility for large ESD strikes and damage to crucial system elements. The ESD protection included on the existing hardware is typically in the 2-kV to 4-kV range for the human body model (HBD) and 200-V to 300-V for the machine model (MM). The ESD voltage levels found in a normal USB operating environment can exceed these levels. The SN75240, SN65240, and SN65220 devices will increase the robustness of the existing USB hardware to ESD strikes common to the environment in which USB is likely to be used.

10.2 Typical Application

图 10-1 illustrates a typical USB system and application of the SN75240, SN65240, and SN65220 devices. Connections to pin A from the D+ data line, pin B from the D – data line, and the device grounds from the GND line that already exists are necessary to increase the amount of ESD protection provided to the USB port.

The design of the suppressor gives it very low maximum current leakage of 1 μA, a very low typical capacitance of 35 pF, and a standoff voltage minimum of 6 V. Because of these levels, the SN75240, SN65240, and SN65220 devices will provide added protection to the USB system hardware during ESD events without introducing the high capacitance and current leakage levels typical of external transient voltage suppressors. The addition of an SN75240, SN65240, or SN65220 device is beneficial to both full-speed and low-speed USB 1.1 bandwidth standards.

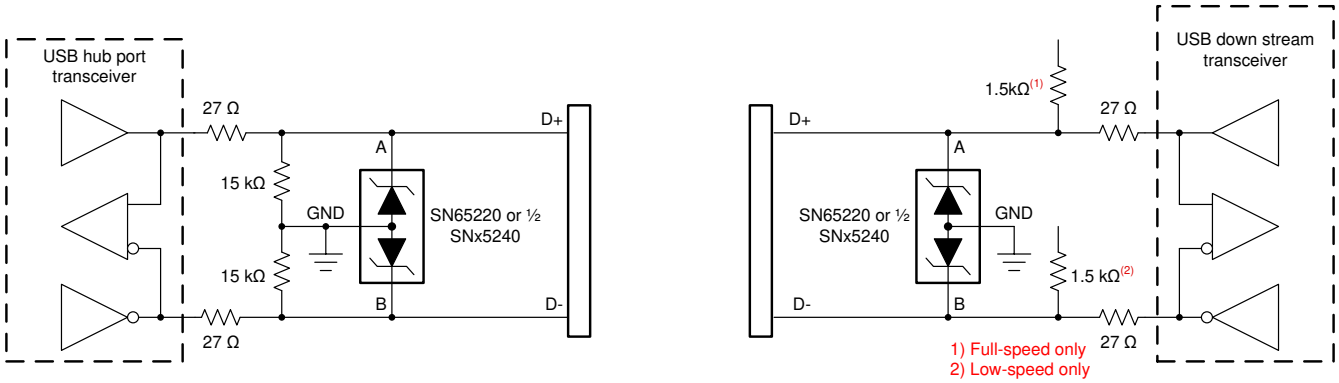


图 10-1. Typical Application Schematic for ESD Protection of USB Transceivers

10.2.1 Design Requirements

For this design example, use the parameters listed in 表 10-1 as design parameters.

表 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum breakdown voltage (TVS)	6.5 V
Maximum supply voltage (USB transceiver)	5.5 V
Typical junction capacitance (TVS)	35 pF
Maximum data rate (USB transceiver)	12 Mbps

10.2.2 Detailed Design Procedure

To effectively protect USB transceivers, use TVS diodes with breakdown voltages close to 6 V, such as the SN65220, SN65240, or SN75220 devices.

Because of the TVS junction capacitance of 35 pF, apply these TVS diodes only to USB transceivers with full-speed capability that is 12 Mbps maximum.

Place the TVS diodes as close to the board connector as possible to prevent transient energies from entering further board space.

Connect the TVS diode between the data lines (D+, D –) and local circuit ground (GND).

Because noise transient represents high-speed frequencies, ensure low-inductance return paths for the transient currents by providing a solid ground plane and using two VIAs connecting the TVS terminals to ground.

10.2.3 Application Curve

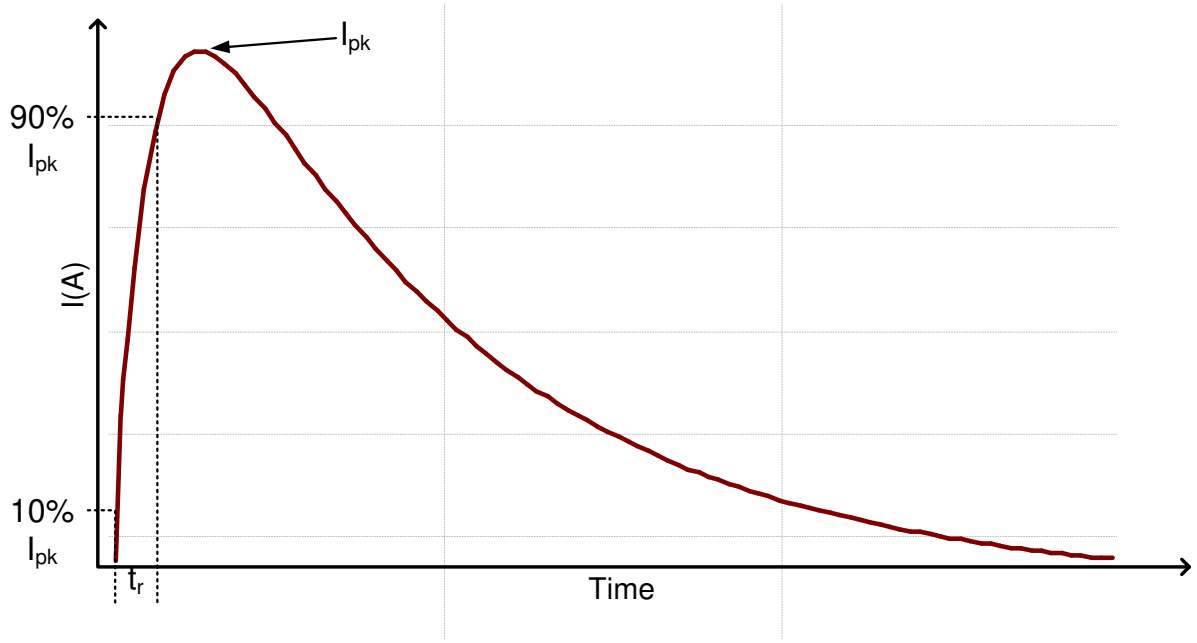


图 10-2. HBM Curve

11 Power Supply Recommendations

Unlike other semiconductor components that require a supply voltage to operate, the SN65220, SN65240, and SN75240 transient suppressors are combinations of multiple p-n diodes, activated by transient voltages. Therefore, these transient suppressors do not require external voltage supplies.

12 Layout

12.1 Layout Guidelines

The multiple ground pins provided lower the connection resistance to ground. In order to improve circuit operation, a connection to all ground pins must be provided on the system printed circuit board. Without proper device connection to ground, the speed and protection capability of the device will be degraded.

- The ground termination pads should be connected directly to a ground plane on the board for optimum performance. A single trace ground conductor will not provide an effective path for fast rise-time transient events including ESD due to parasitic inductance.
- Nominal inductive values of a PCB trace are approximately 20 nH/cm. This value may seem small, but an apparent *short length* of trace may be sufficient to produce significant L(di/dt) effects with fast rise-time ESD spikes.
- Mount the TVS as close as possible to the I/O socket to reduce radiation originating from the transient as it is routed to ground.

Note

Direct connective paths of the traces are taken to the suppressor mounting pads to minimize parasitic inductance in the surge-current conductive path, thus minimizing L(di/dt) effects.

12.2 Layout Example

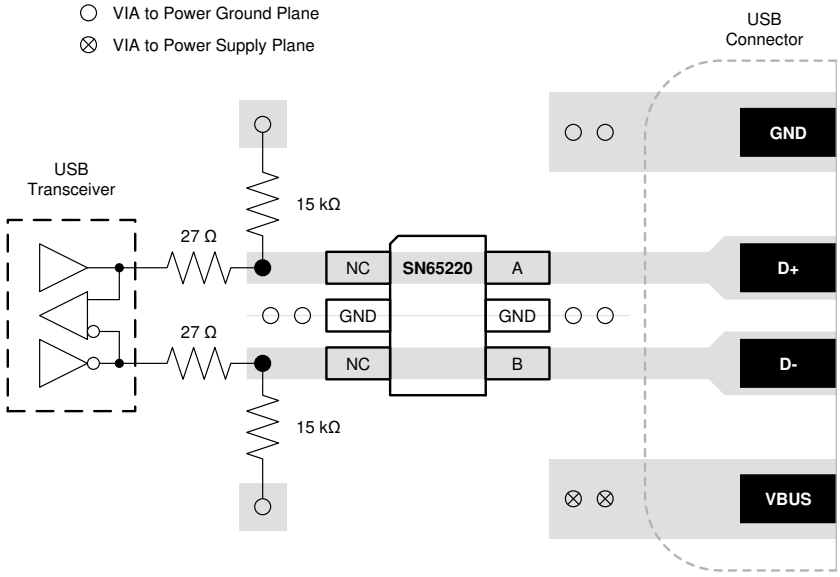


图 12-1. Layout Example of a 4-Layer Board With SN65220

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 13-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65220	Click here	Click here	Click here	Click here	Click here
SN65240	Click here	Click here	Click here	Click here	Click here
SN75240	Click here	Click here	Click here	Click here	Click here

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65220DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	Samples
SN65220DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	Samples
SN65220DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	Samples
SN65220DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	Samples
SN65240P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65240P	Samples
SN65240PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65240P	Samples
SN65240PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	Samples
SN65240PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	Samples
SN65240PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	Samples
SN65240PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	Samples
SN75240P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75240P	Samples
SN75240PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	Samples
SN75240PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	Samples
SN75240PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	Samples
SN75240PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65220 :

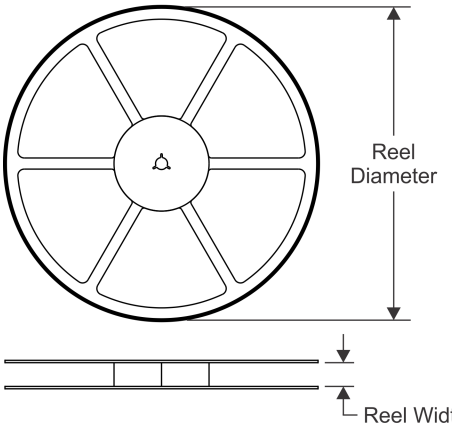
- Automotive : SN65220-Q1

NOTE: Qualified Version Definitions:

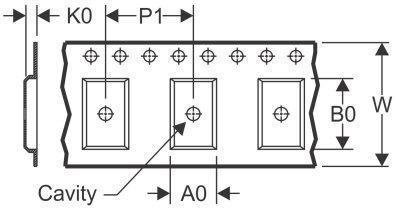
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

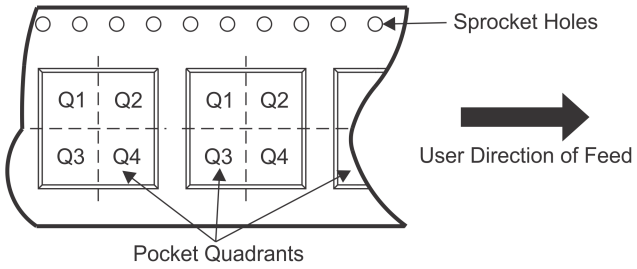


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

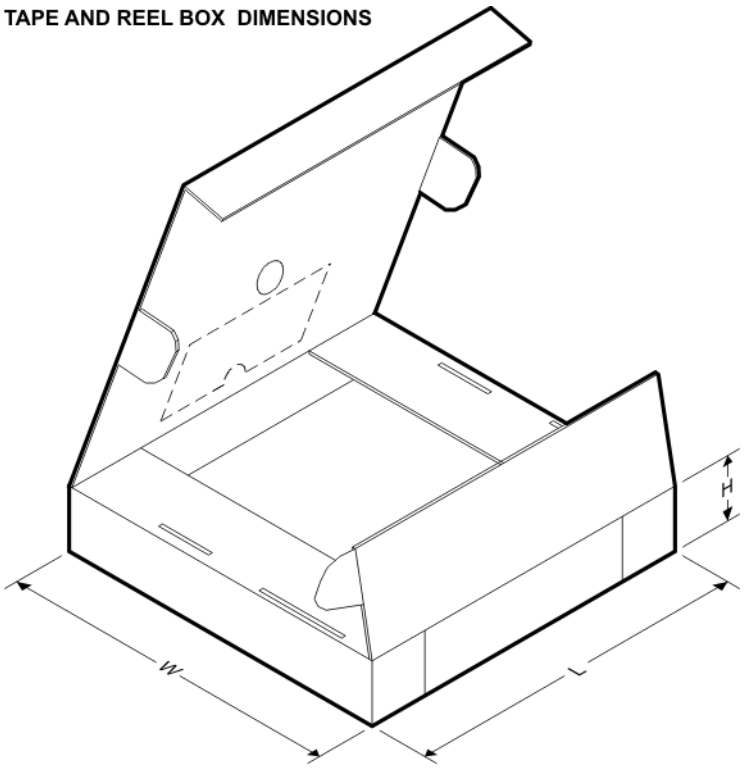
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65220DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN65220DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN65240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN75240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

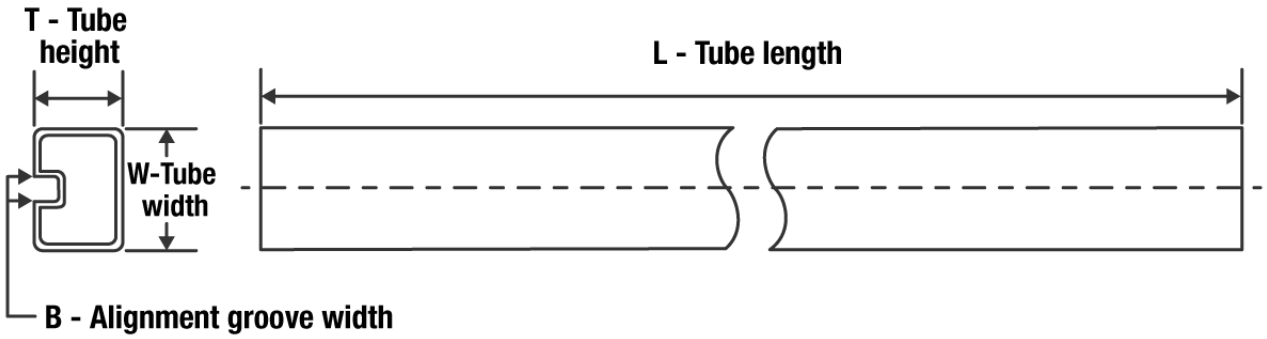
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65220DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN65220DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN65240PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
SN75240PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

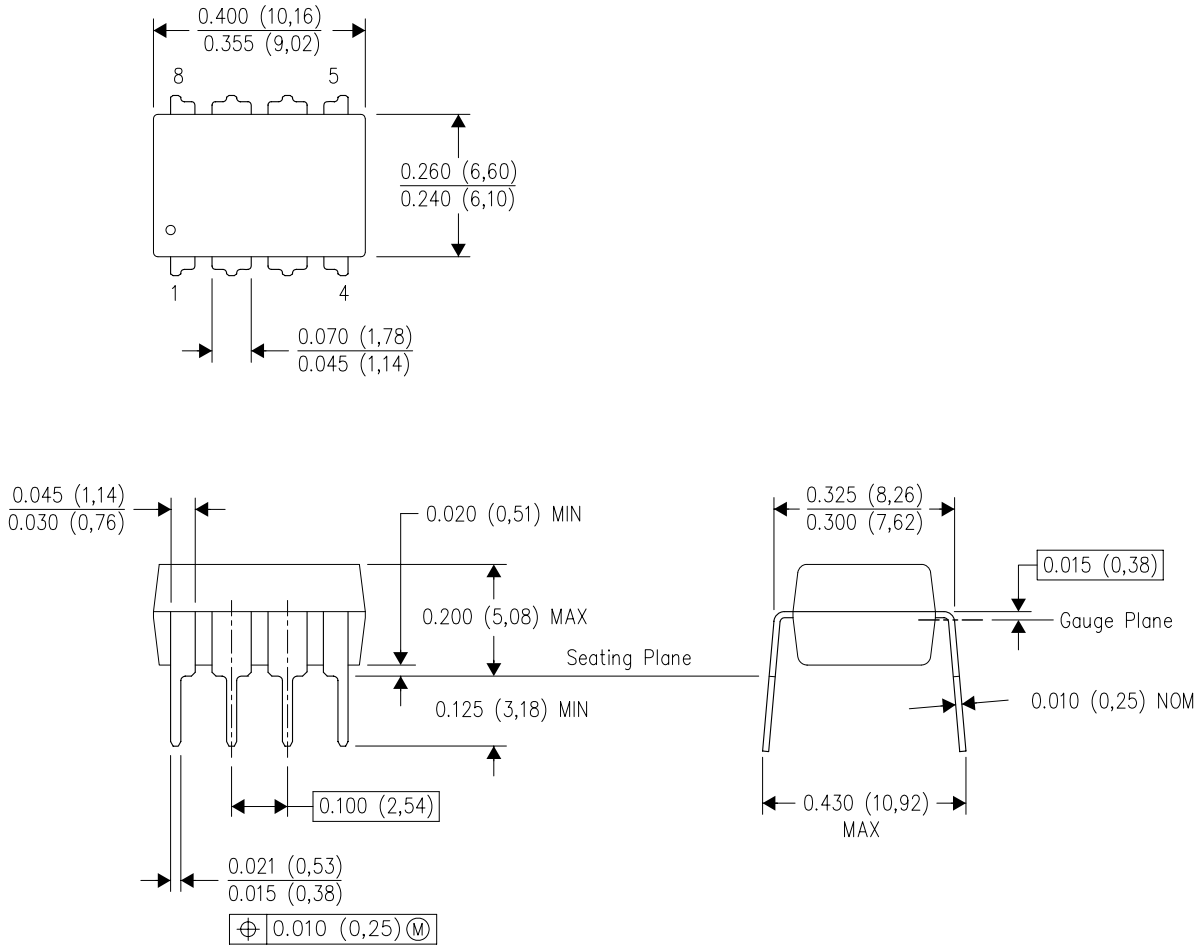
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65240P	P	PDIP	8	50	506	13.97	11230	4.32
SN65240PE4	P	PDIP	8	50	506	13.97	11230	4.32
SN65240PW	PW	TSSOP	8	150	530	10.2	3600	3.5
SN65240PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5
SN75240P	P	PDIP	8	50	506	13.97	11230	4.32
SN75240PW	PW	TSSOP	8	150	530	10.2	3600	3.5
SN75240PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



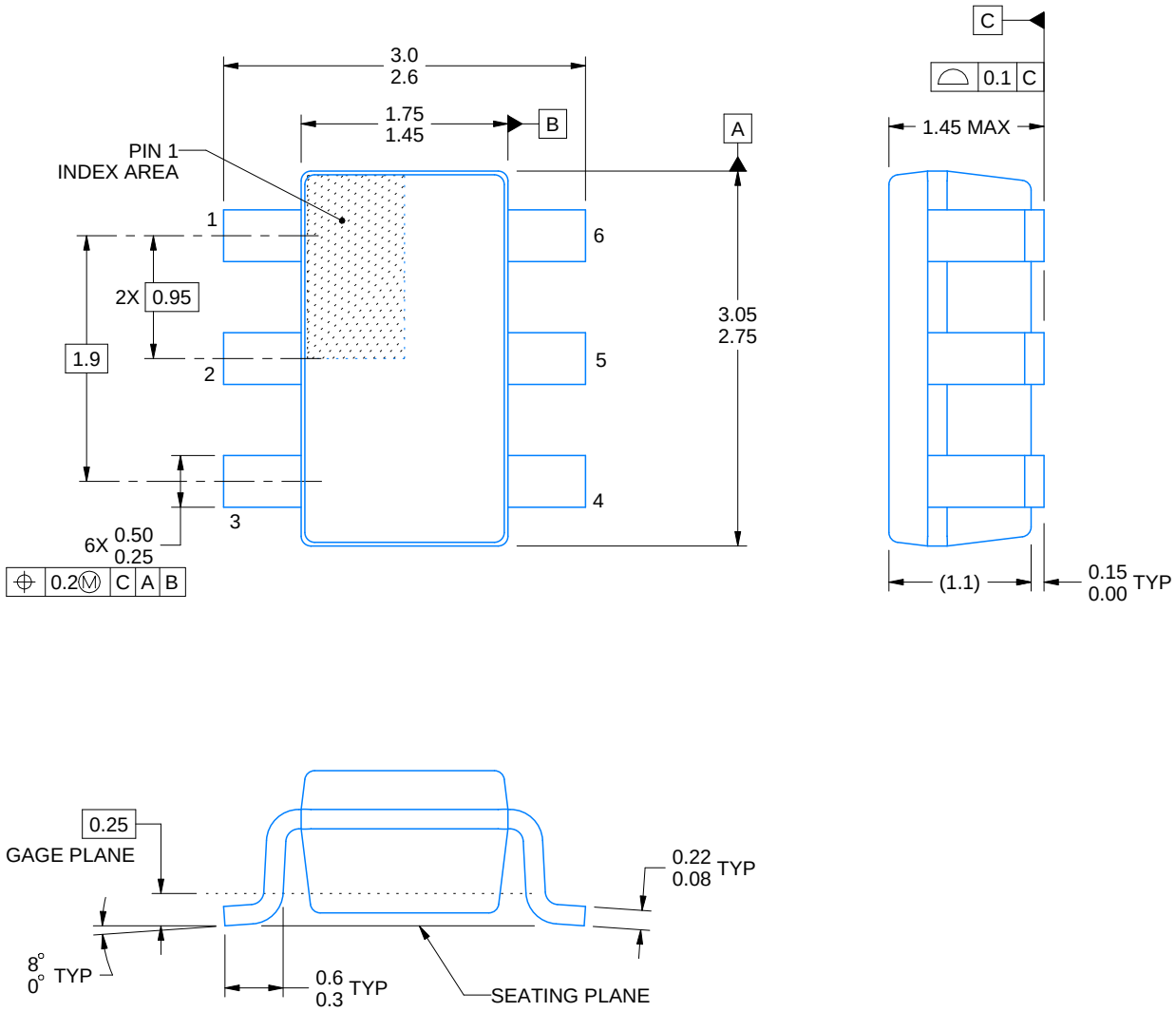
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

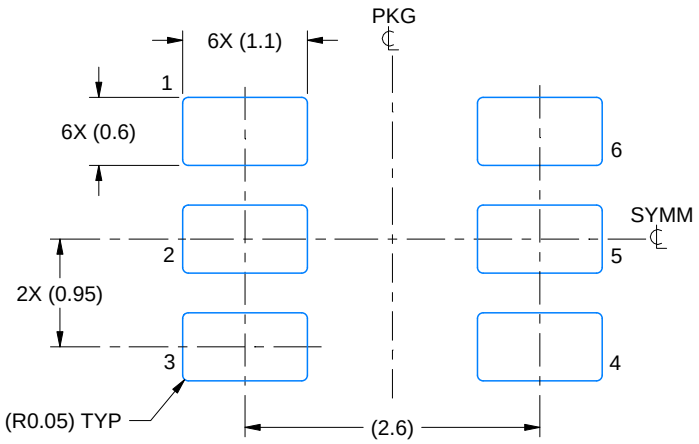
SMALL OUTLINE TRANSISTOR



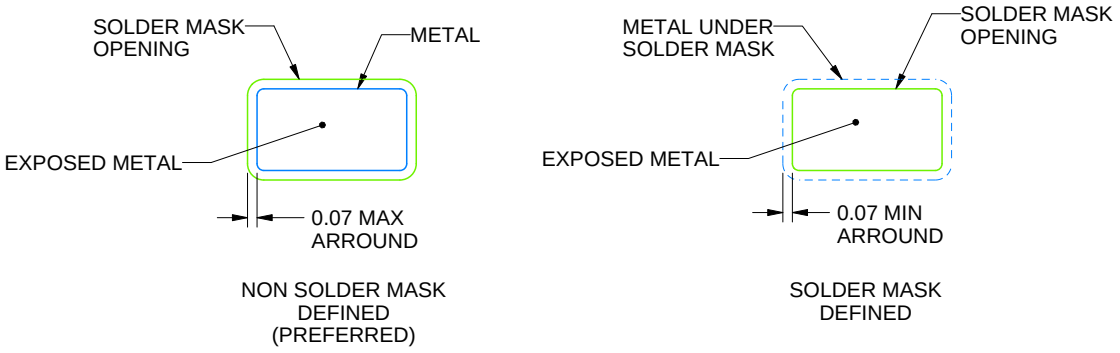
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

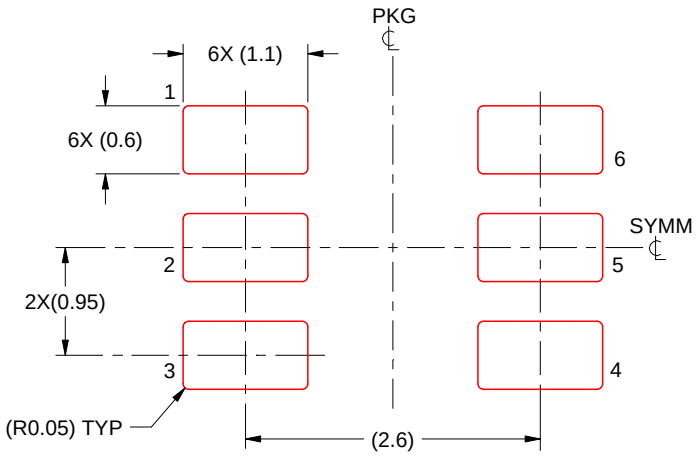


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

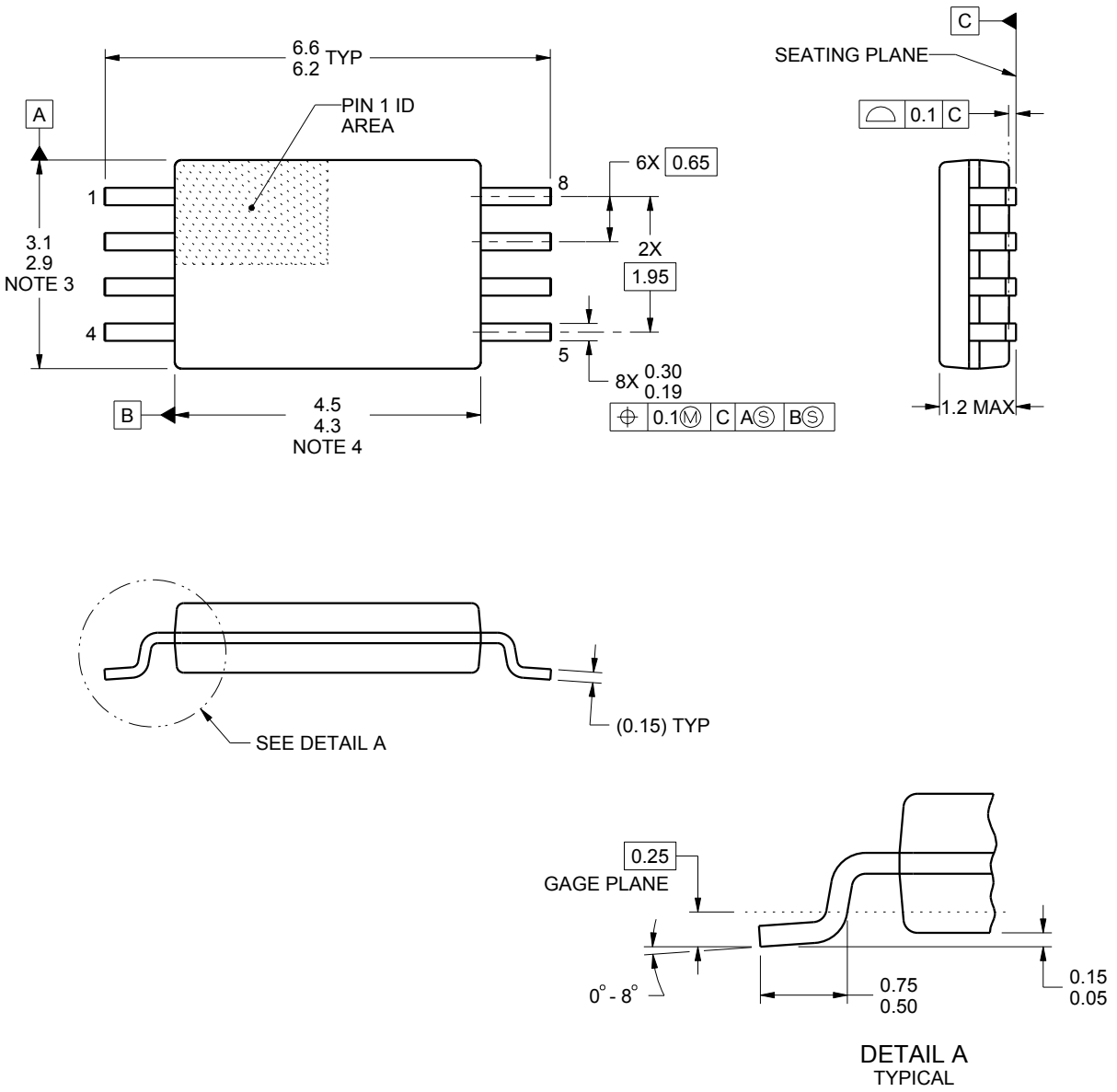
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

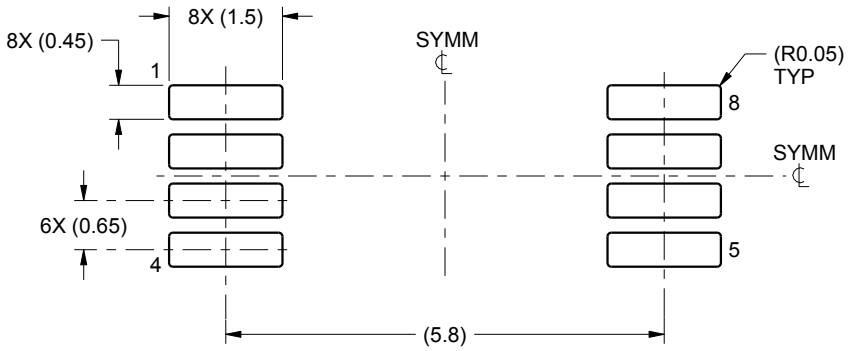
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

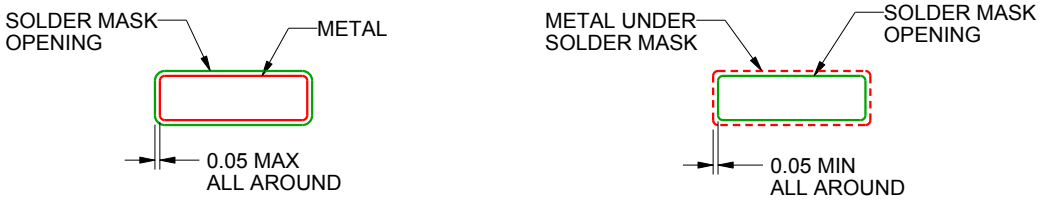


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

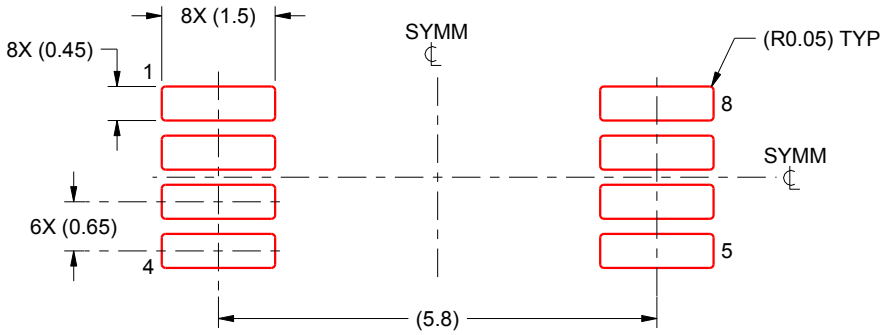


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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