

# 适用于隔离电源的 SN6505x-Q1 低噪声 1A 变压器驱动器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 (1 级)
  - 器件温度等级 1:  $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$ ,  $T_A$
- 用于变压器的推挽式驱动器
- 宽输入电压范围: 2.25V 至 5.5V
- 高输出驱动: 5V 电源时为 1A
- 低  $R_{\text{ON}}$ , 4.5V 电源时的最大值为  $0.25\Omega$
- 降低了传导和辐射 EMI
- 扩频时钟
- 精密内部振荡器选项: 160kHz (SN6505A-Q1) 和 420kHz (SN6505B-Q1 和 SN6505D-Q1)
- 通过外部时钟输入同步多个器件
- 转换率控制
- 1.7A 限流
- 低关断电流:  $< 1\mu\text{A}$
- 热关断
- 小型 6 引脚 SOT23 (DBV) 封装
- 启用软启动 (SN6505A-Q1 和 SN6505B-Q1) 可减小浪涌电流, 禁用软启动 (SN6505D-Q1) 可实现快速启动

## 2 应用

- 用于以下应用的隔离式电源:
  - 牵引逆变器和电机控制
  - 直流/直流转换器
  - 电池管理系统 (BMS)
  - 车载充电器 (OBC)

## 3 说明

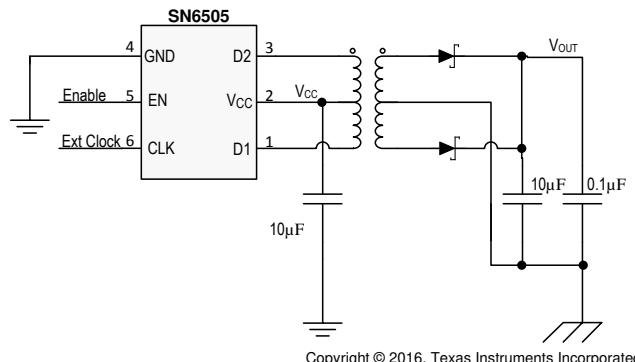
SN6505x-Q1 是一款低噪声、低 EMI 的推挽式变压器驱动器, 专为小型隔离式电源而设计。该器件通过 2.25V 至 5V 的直流电源来驱动薄型、中间抽头的变压器。通过输出开关电压的转换速率控制和扩频时钟 (SSC) 可实现非常低的噪声和 EMI。SN6505x-Q1 包含一个振荡器, 然后是一个栅极驱动器电路, 此电路提供补偿输出信号以驱动接地参考 N 通道电源开关。该器件包含两个 1A 电源 MOSFET 开关, 确保在重负载条件下正常启动。开关时钟也可由外部提供, 这样可确保准确定位开关谐波或者与多个互感器驱动器搭配使用。内部保护功能包括一个 1.7A 的电流限制、欠压锁定、热关断且先断后通型电路。SN6505A-Q1 和 SN6505B-Q1 具有软启动功能, 可防止大负载电容器在上电过程中出现高浪涌电流。对于要求快速输出启动的应用, 已禁用 SN6505D-Q1 中的软启动功能。SN6505A-Q1 具有一个 160kHz 的内部振荡器, 适用于要求大幅降低辐射的应用, 而 SN6505B-Q1 和 SN6505D-Q1 具有一个 420kHz 的内部振荡器, 适用于要求更高效率和更小变压器尺寸的应用。SN6505x-Q1 采用小型 6 引脚 SOT23/DBV 封装。该器件的运行温度范围为  $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$ 。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
SN6505A-Q1		
SN6505B-Q1	SOT23 (6 引脚)	2.90mm × 1.60mm
SN6505D-Q1		

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

### 简化原理图



本文档旨在为方便起见, 提供有关 TI 产品中文版本的信息, 以确认产品的概要。有关适用的官方英文版本的最新信息, 请访问 [www.ti.com](http://www.ti.com), 其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前, 请务必参考最新版本的英文版本。

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## 4 修订历史记录

### Changes from Revision B (July 2019) to Revision C

Page

•	Added UNIT V to EN, CLK Voltage specification in <b>Absolute Maximum Ratings</b> table	4
•	Changed '<' or 'less than' sign to ' $\leq$ ' or 'less than or equal' sign in $V_{CC}$ range description at multiple location for better clarity	5
•	Added <b>Revision History</b> comments for data sheet Revision B	6
•	Added 'Power up time' or $t_{PWRUP}$ specification for two $V_{CC}$ TEST CONDITIONS	6

### Changes from Revision A (April 2019) to Revision B

Page

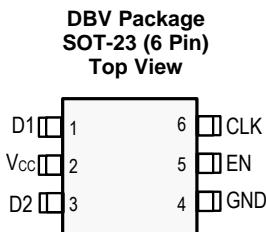
•	Split 'Soft-start time' or $t_{SS}$ specification for SN6505A-Q1 and SN6505B-Q1	6
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### Changes from Original (November 2018) to Revision A

Page

•	已更改 将器件状态更改为“生产数据”	1
•	已添加 DA2303-AL transformer to 表 3 table	24
•	已添加 DA2304-AL transformer to 表 3 table	24

## 5 Pin Configuration and Functions



### Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
D1	1	O	Open drain output of the first power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
V <sub>CC</sub>	2	P	This is the device supply pin. It should be bypassed with a 4.7 $\mu$ F or greater, low ESR capacitor. When $V_{CC} \leq 2.25$ V, an internal undervoltage lockout circuit trips and turns both outputs off.
D2	3	O	Open drain output of the second power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
GND	4	P	GND is connected to the source of the power MOSFET switches via an internal sense circuit. Because large currents flow through it, the GND terminals must be connected to a low-inductance quality ground plane.
EN	5	I	The EN pin turns the device on or off. Grounding or leaving this pin floating disables all internal circuitry. If unused this pin should be tied directly to V <sub>CC</sub> .
CLK	6	I	This pin is used to run the device with external clock. Internally it is pulled down to GND. If valid clock is not detected on this pin, the device shifts automatically to internal clock.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ .

		MIN	MAX	UNIT
Supply voltage <sup>(2)</sup>	$V_{CC}$	-0.5	6	V
Voltage	EN, CLK	-0.5	$V_{CC} + 0.5$ <sup>(3)</sup>	V
Output switch voltage	D1, D2		16	V
Peak output switch current	$I_{(D1)PK}, I_{(D2)PK}$		2.4	A
Junction temperature, $T_J$		-40	150	$^\circ\text{C}$
Storage temperature range, $T_{stg}$		-65	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under Absolute Maximum Ratings cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND) and are peak voltage values.
- (3) Maximum voltage must not exceed 6V. A strongly driven EN or CLK input signal can weakly power the floating  $V_{CC}$  via an internal protection diode and cause undetermined output.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 3A	$\pm 6000$
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	$\pm 1500$

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
$V_{CC}$	Supply voltage	2.25	5.5		V
$I_{D1}, I_{D2}$	Output switch current - Primary side	2.25 V $\leq V_{CC} \leq$ 2.8 V		0.75	A
		2.8 V $< V_{CC} \leq$ 5.5 V		1	
$T_A$	Ambient temperature	-40		125	$^\circ\text{C}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN6505x-Q1	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{iJA}$	Junction-to-ambient thermal resistance	137.7	$^\circ\text{C/W}$
$R_{iJC(\text{top})}$	Junction-to-case (top) thermal resistance	57.7	$^\circ\text{C/W}$
$R_{iJB}$	Junction-to-board thermal resistance	46.0	$^\circ\text{C/W}$
$\psi_{JT}$	Junction-to-top characterization parameter	13.4	$^\circ\text{C/W}$
$\psi_{JB}$	Junction-to-board characterization parameter	44.9	$^\circ\text{C/W}$
$R_{iJC(\text{bottom})}$	Junction-to-case(bottom) thermal resistance	N/A	$^\circ\text{C/W}$

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

over full-range of recommended operating conditions, unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VOLTAGE SUPPLY</b>					
$I_{(V_{CC})}$	Supply Current (2.8 V $\leq V_{CC} \leq$ 5.5 V) (SN6505A-Q1)	$R_L = 50\ \Omega$	1	1.4	mA
	Supply Current (2.8 V $\leq V_{CC} \leq$ 5.5 V) (SN6505B-Q1 and SN6505D-Q1)	$R_L = 50\ \Omega$	1.56	2.3	mA
$I_{IH}$	Leakage Current on EN and CLK pin	$EN / CLK = V_{CC}$	10	20	$\mu\text{A}$
$I_{DIS}$	$V_{CC}$ current for EN = 0		0.1		$\mu\text{A}$
$I_{LKG(D1)}$ $I_{LKG(D2)}$	Leakage Current on D1, D2 for EN=0	Voltage of D1, D2 = $V_{CC}$	0.1		$\mu\text{A}$
$V_{CC+}$ (UVLO)	Positive-going UVLO threshold		2.25		V
$V_{CC-}$ (UVLO)	Negative-going UVLO threshold		1.7		V
$V_{HYS}$ (UVLO1)	UVLO threshold hysteresis		0.3		V
$V_{IN(ON)}$	EN, CLK pin logic high threshold		0.7		$V_{CC}$
$V_{IN(OFF)}$	EN, CLK pin logic low threshold		0.3		$V_{CC}$
$V_{IN(HYS)}$	EN, CLK pin threshold hysteresis		0.2		$V_{CC}$
<b>CLK</b>					
$F_{SW}$	D1, D2 average switching Frequency (SN6505A-Q1)	$R_L = 50\ \Omega$ to $V_{CC}$ ; Refer to <a href="#">图 36</a>	138	160	203
	D1, D2 average switching Frequency (SN6505B-Q1 and SN6505D-Q1)	$R_L = 50\ \Omega$ to $V_{CC}$ ; Refer to <a href="#">图 36</a> .	363	424	517
$F_{(EXT)}$	External clock frequency on CLK pin (SN6505A-Q1)		100	600	kHz
	External clock frequency on CLK pin (SN6505B-Q1 and SN6505D-Q1)		100	1600	kHz
<b>OUTPUT STAGE</b>					
DMM	Average ON time mismatch between D1 and D2	$R_L = 50\ \Omega$	0%		
$R_{(ON)}$	Output switch on resistance	$V_{CC} = 4.5\text{ V}$ , $I_{D1}, I_{D2} = 1\text{ A}$	0.16	0.25	$\Omega$
		$V_{CC} = 2.8\text{ V}$ , $I_{D1}, I_{D2} = 1\text{ A}$	0.19	0.31	$\Omega$
		$V_{CC} = 2.25\text{ V}$ , $I_{D1}, I_{D2} = 0.5\text{ A}$	0.21	0.45	$\Omega$
$V_{(SLEW)}$	Voltage slew rates on D1 and D2 for SN6505A-Q1	$R_L = 50\ \Omega$ to $V_{CC}$ ; Refer to <a href="#">图 36</a>	48		$\text{V}/\mu\text{s}$
$I_{(SLEW)}$	Current slew rates at D1 and D2 for SN6505A-Q1	$R_L = 5\ \Omega$ through transformer; Refer to <a href="#">图 37</a>	11		$\text{A}/\mu\text{s}$
$V_{(SLEWHF)}$	Voltage slew rates on D1 and D2 for SN6505B-Q1 and SN6505D-Q1	$R_L = 50\ \Omega$ to $V_{CC}$ ; Refer to <a href="#">图 36</a>	152		$\text{V}/\mu\text{s}$
$I_{(SLEWHF)}$	Current slew rates at D1 and D2 for SN6505B-Q1 and SN6505D-Q1	$R_L = 5\ \Omega$ through transformer; Refer to <a href="#">图 37</a>	41		$\text{A}/\mu\text{s}$
$I_{LIM}$	Current clamp limit (2.8 V $< V_{CC} \leq$ 5.5V )		1.42	1.75	2.15
	Current clamp limit (2.25 V $\leq V_{CC} \leq$ 2.8 V)		0.65	1.85	A
<b>THERMAL SHUT DOWN</b>					
$T_{SD+}$	$T_{SD}$ turn on temperature		154	168	181
$T_{SD-}$	$T_{SD}$ turn off temperature		135	150	166
$T_{SD-}$	$T_{SD}$ hysteresis		13	17	$^\circ\text{C}$

## 6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
<b>CLK</b>						
$t_{CLKTIMER}$	Duration after which device switches to internal clock in case of invalid external clock		10	25		μs
<b>OUTPUT STAGE</b>						
$t_{BBM}$	Break-before-make time(SN6505A-Q1)	Measured as voltage with $R_L = 50 \Omega$ to $V_{CC}$ , Refer to <a href="#">图 36</a>		115		ns
	Break-before-make time (SN6505B-Q1 and SN6505D-Q1)	Measured as voltage with $R_L = 50 \Omega$ to $V_{CC}$ , Refer to <a href="#">图 36</a>		90		ns
<b>SOFT-START ENABLED (SN6505A-Q1 AND SN6505B-Q1)</b>						
$t_{SS}$	Soft-start time (SN6505A-Q1)	10% to 90% transition time on $V_{OUT}$ With transformer $C_{LOAD} = 40 \mu F$ $R_L = 5 \Omega$	1	2.2	8	ms
	Soft-start time (SN6505B-Q1)	10% to 90% transition time on $V_{OUT}$ With transformer $C_{LOAD} = 40 \mu F$ $R_L = 5 \Omega$	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on $V_{OUT}$ With transformer $C_{LOAD} = 40 \mu F$ $R_L = 5 \Omega$	3.5	8.5	18	ms
<b>SOFT-START DISABLED (SN6505D-Q1)</b>						
$t_{PWRUP}$	Power up time	From $EN=1$ to full drive-current available at D1 and D2; $2.25 V \leq V_{CC} < 3 V$		75	160	μs
		From $EN=1$ to full drive-current available at D1 and D2; $3 V \leq V_{CC} \leq 5.5 V$		60	100	μs
$t_{PWRDN}$	Power down time	From $EN=0$ to output MOSFETs off (no current on D1 and D2)		1	5	μs

## 6.7 Typical Characteristics, SN6505A-Q1

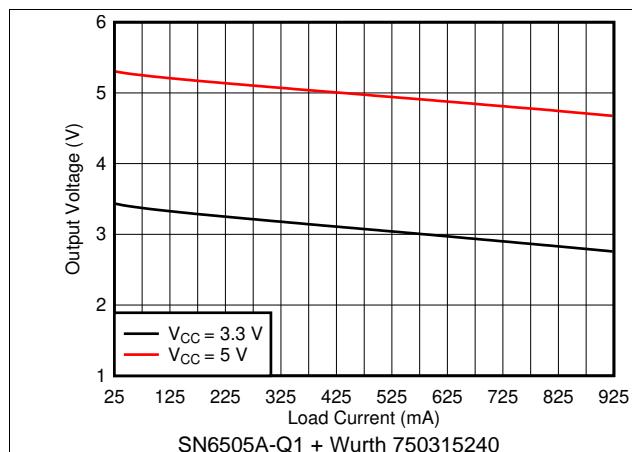


图 1. Output Voltage vs Load Current

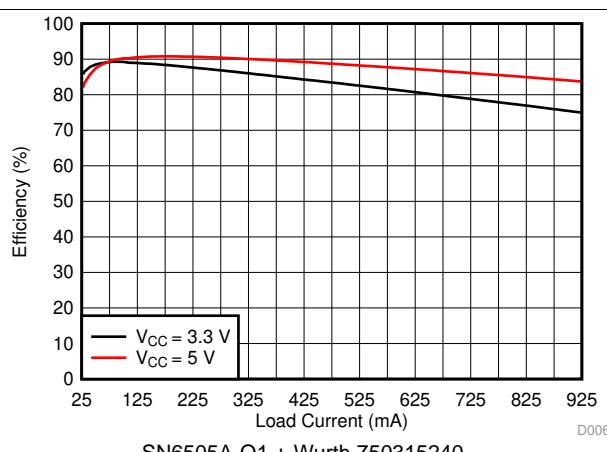


图 2. Efficiency vs Load Current

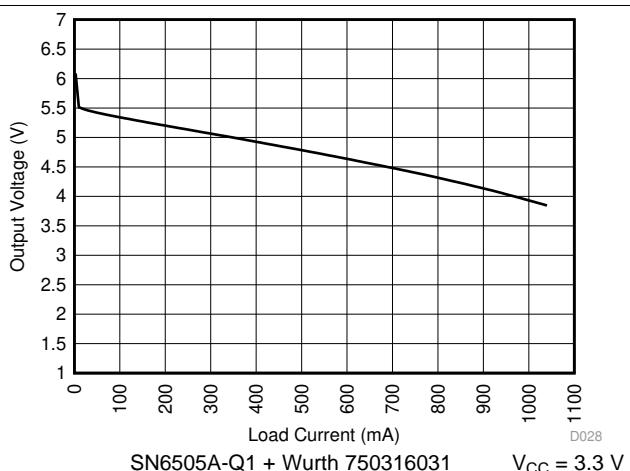


图 3. Output Voltage vs Load Current

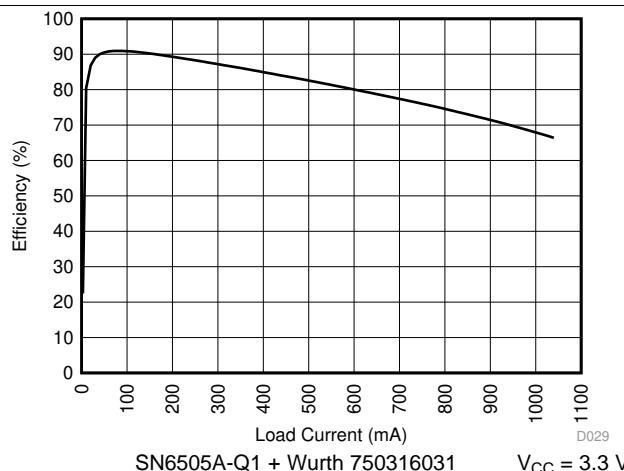


图 4. Efficiency vs Load Current

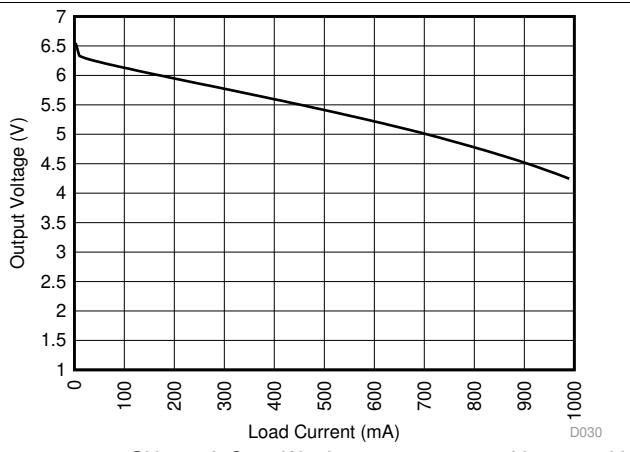


图 5. Output Voltage vs Load Current

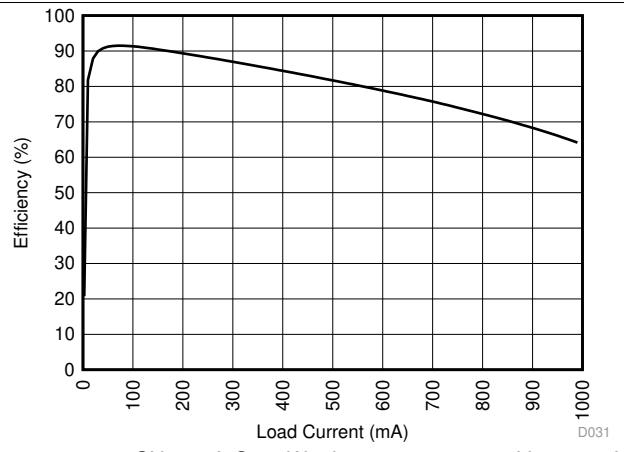
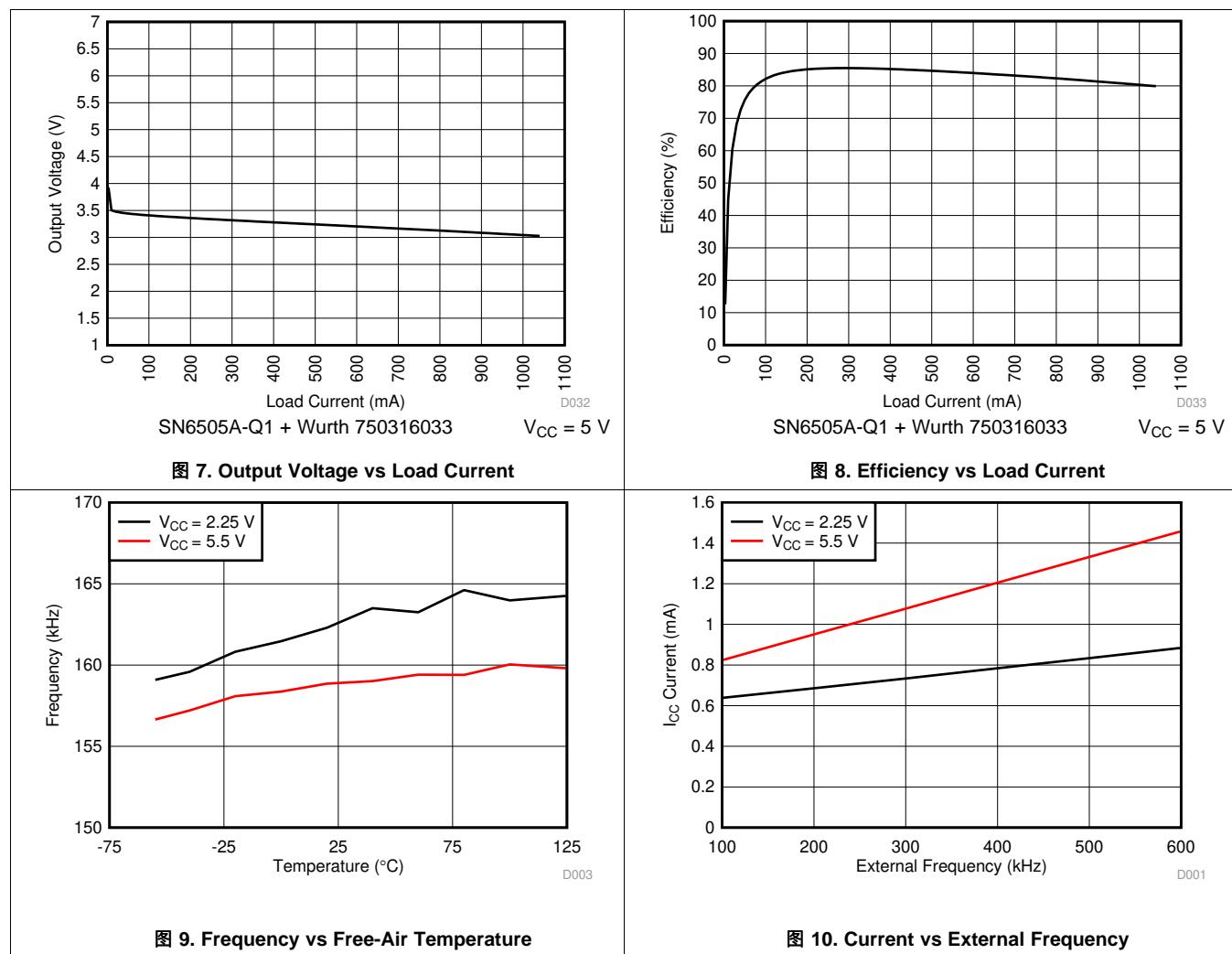


图 6. Efficiency vs Load Current

**Typical Characteristics, SN6505A-Q1 (接下页)**


## 6.8 Typical Characteristics, SN6505B-Q1 or SN6505D-Q1

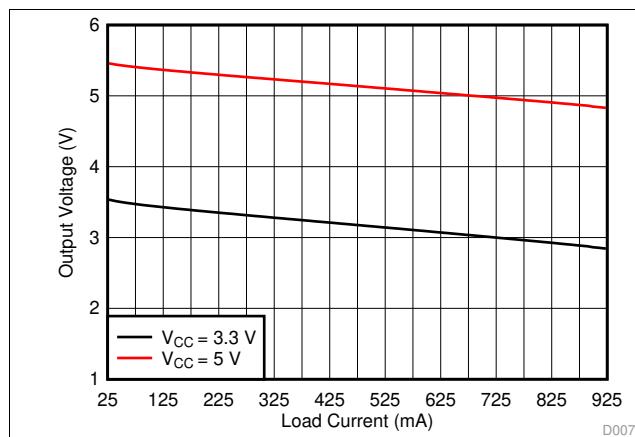


图 11. Output Voltage vs Load Current

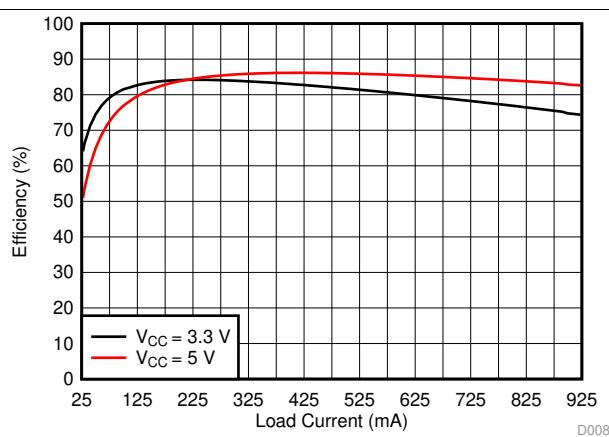


图 12. Efficiency vs Load Current

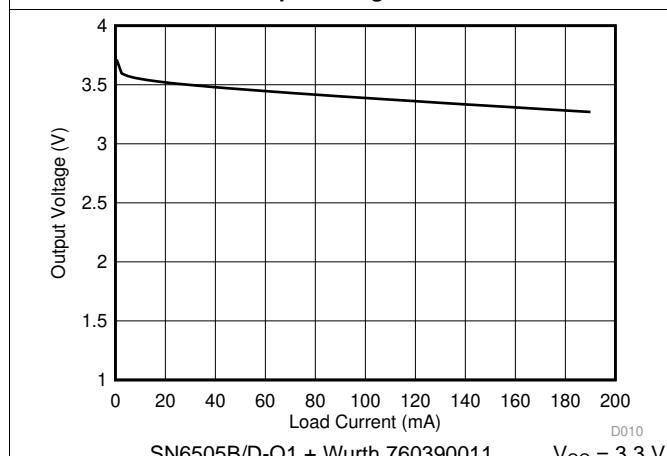


图 13. Output Voltage vs Load Current

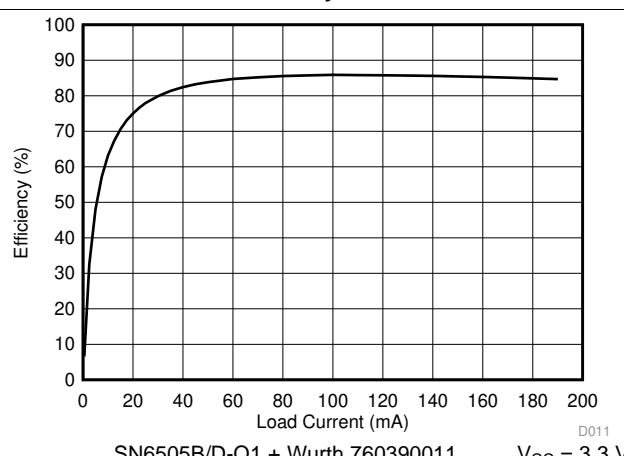


图 14. Efficiency vs Load Current

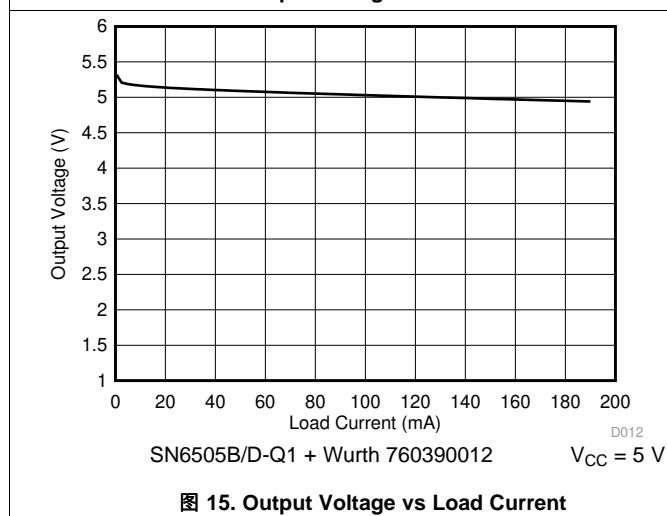


图 15. Output Voltage vs Load Current

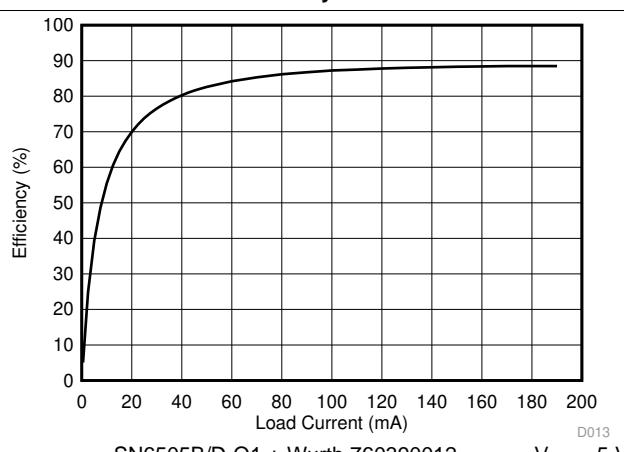
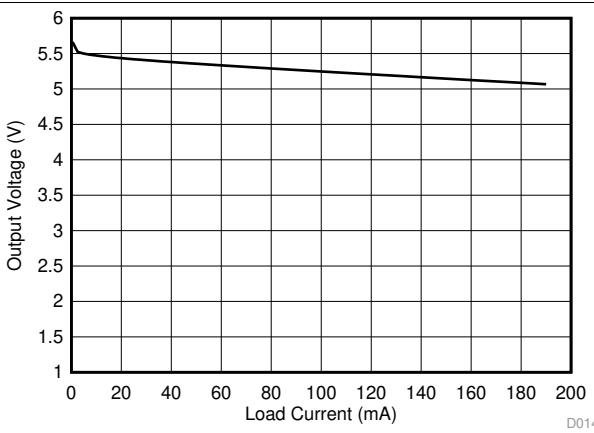
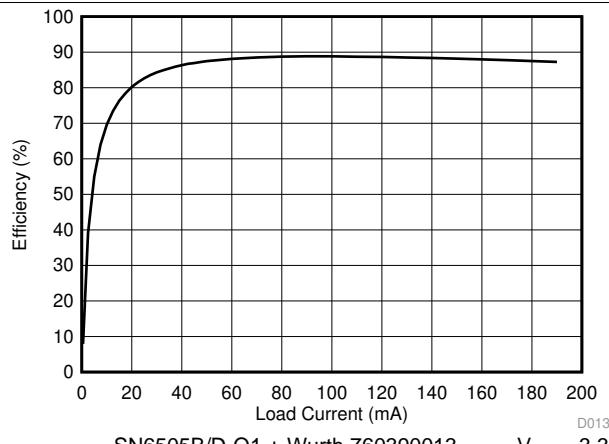
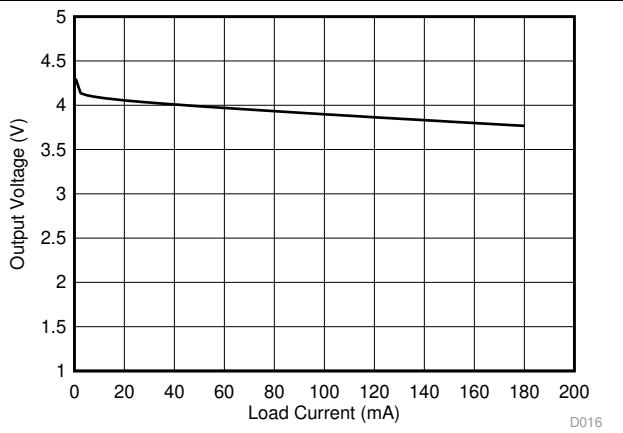
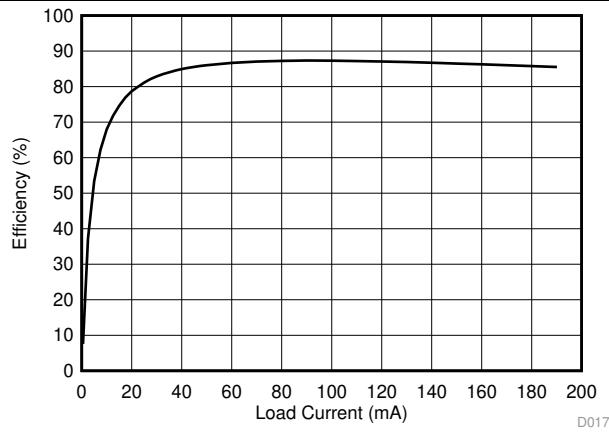
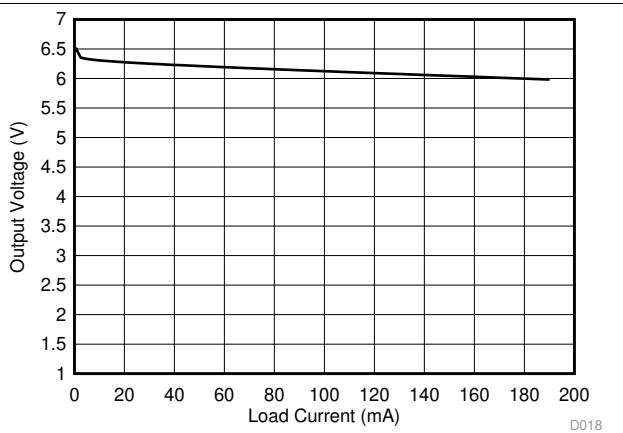
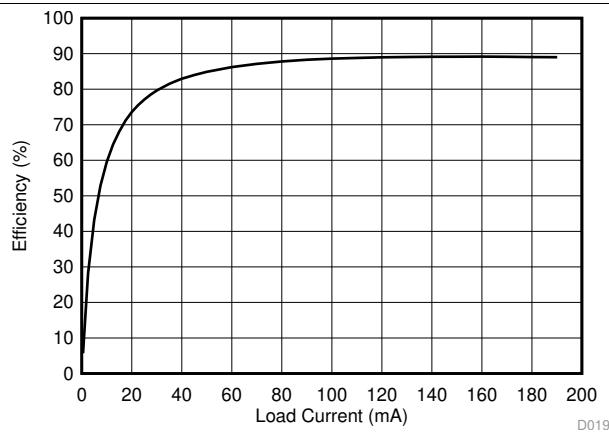
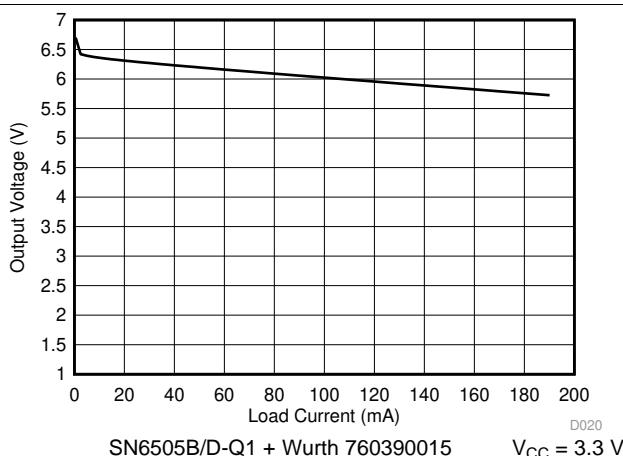
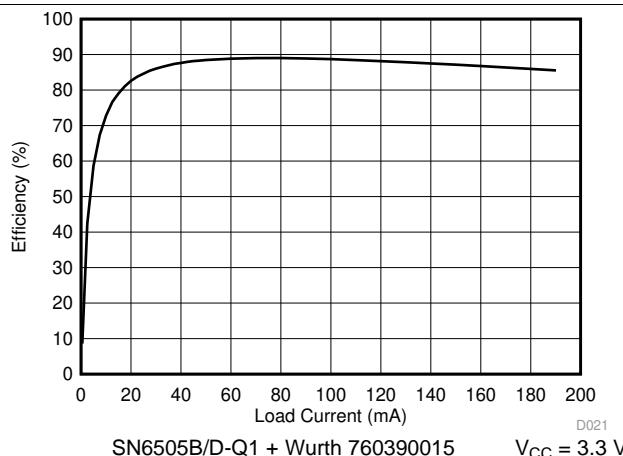
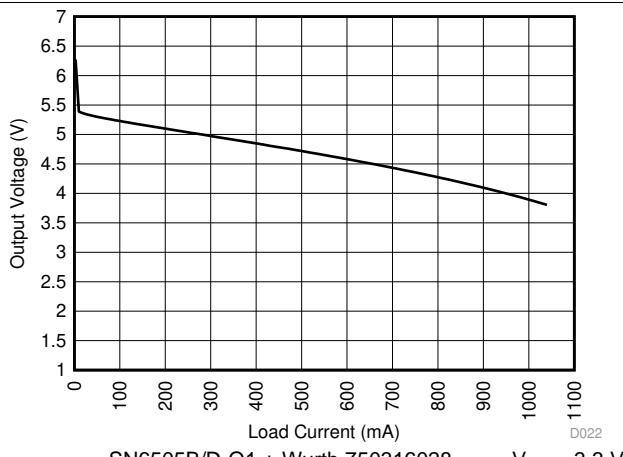
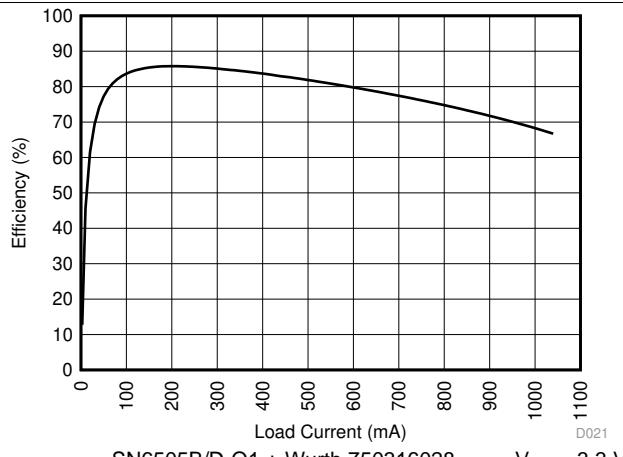
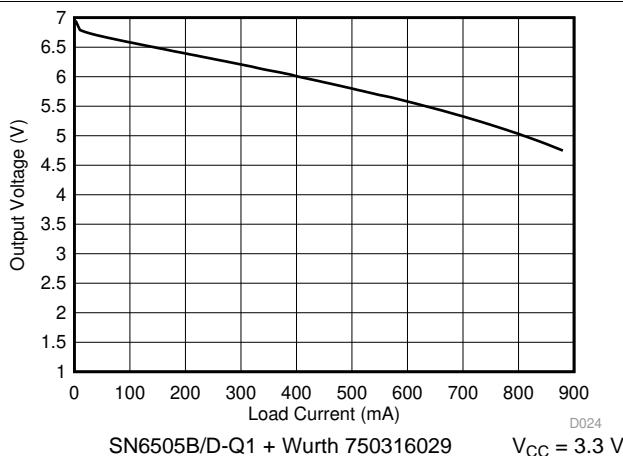
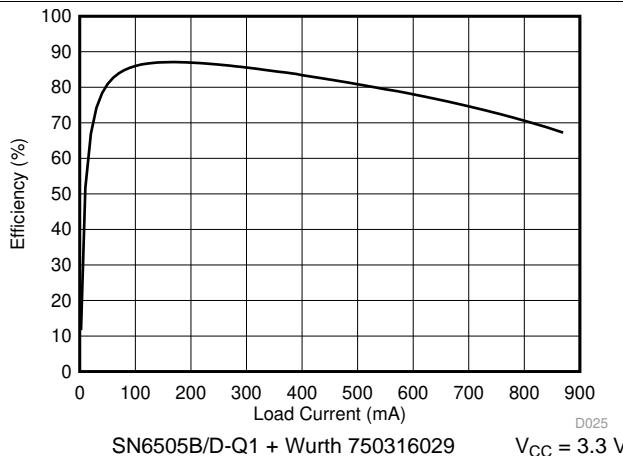
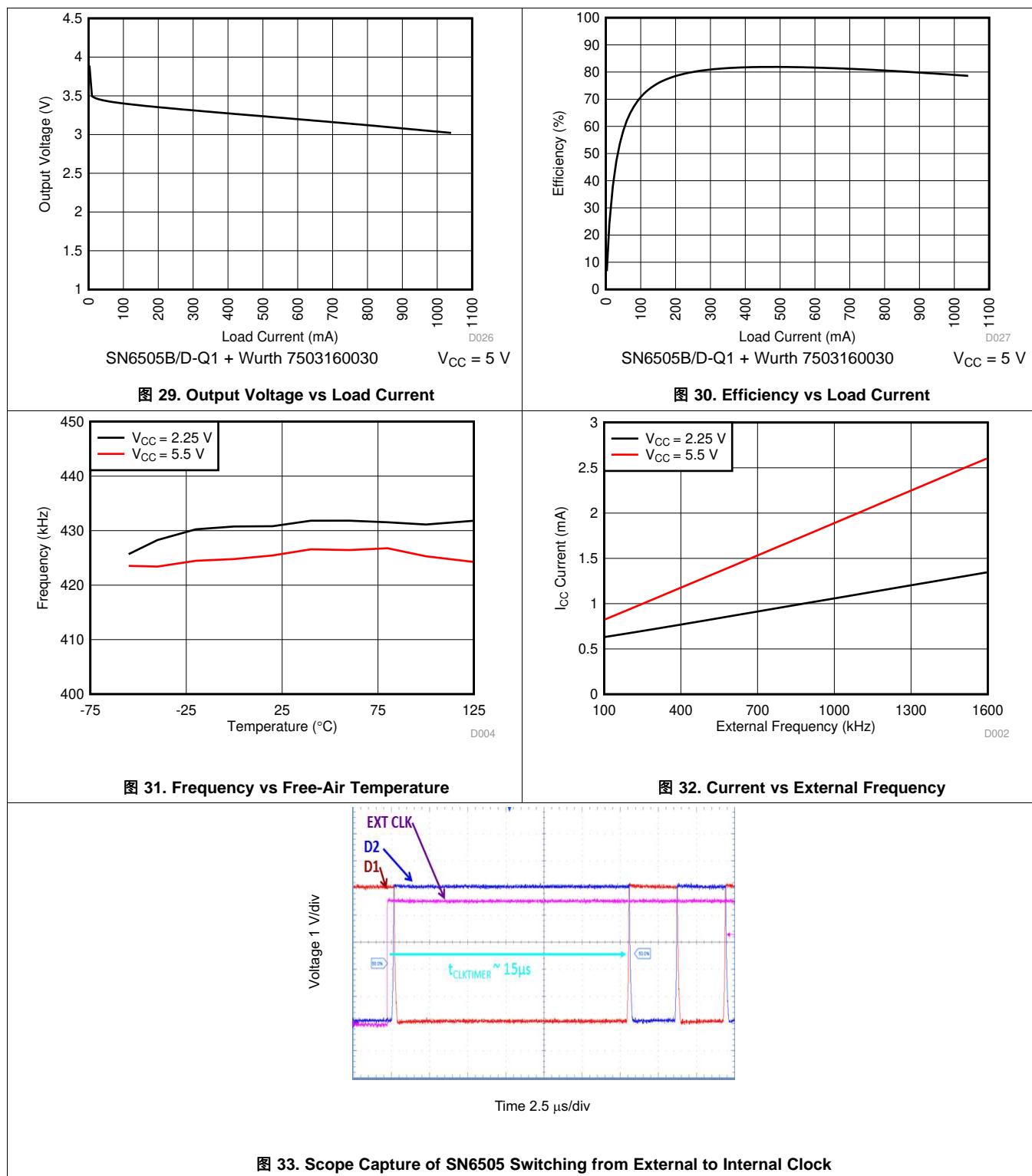


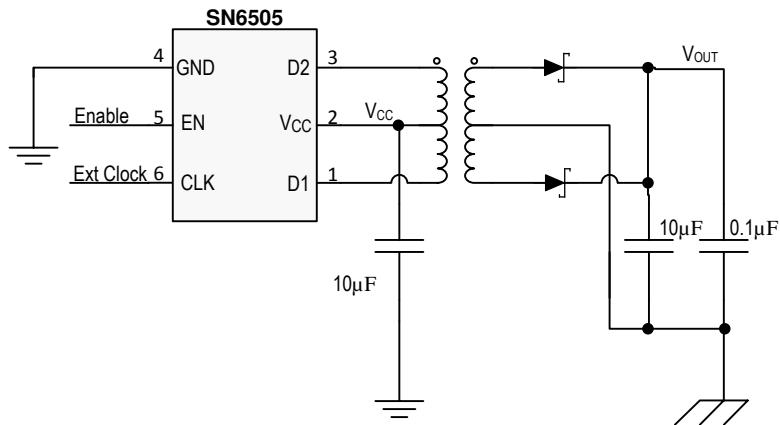
图 16. Efficiency vs Load Current

**Typical Characteristics, SN6505B-Q1 or SN6505D-Q1 (接下页)**

**图 17. Output Voltage vs Load Current**

**图 18. Efficiency vs Load Current**

**图 19. Output Voltage vs Load Current**

**图 20. Efficiency vs Load Current**

**图 21. Output Voltage vs Load Current**

**图 22. Efficiency vs Load Current**

**Typical Characteristics, SN6505B-Q1 or SN6505D-Q1 (接下页)**

**图 23. Output Voltage vs Load Current**

**图 24. Efficiency vs Load Current**

**图 25. Output Voltage vs Load Current**

**图 26. Efficiency vs Load Current**

**图 27. Output Voltage vs Load Current**

**图 28. Efficiency vs Load Current**

**Typical Characteristics, SN6505B-Q1 or SN6505D-Q1 (接下页)**


## 7 Parameter Measurement Information



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图 34. Measurement Circuit for Unregulated Output (TP1)

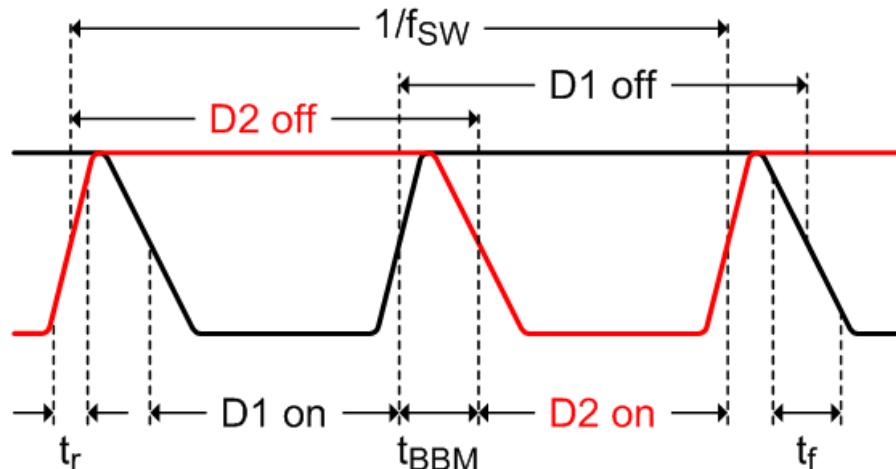
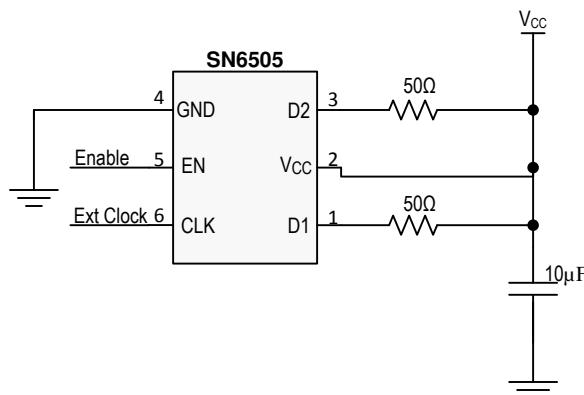


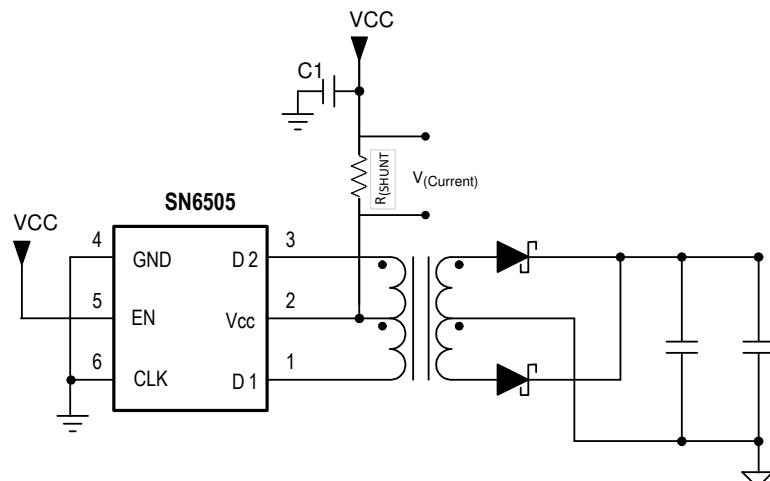
图 35. Timing Diagram



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图 36. Test Circuit for  $f_{SW}$ ,  $V_{(slew)}$ ,  $t_{BBM}$

## Parameter Measurement Information (接下页)



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图 37.  $I_{(slew)}$  Test Setup

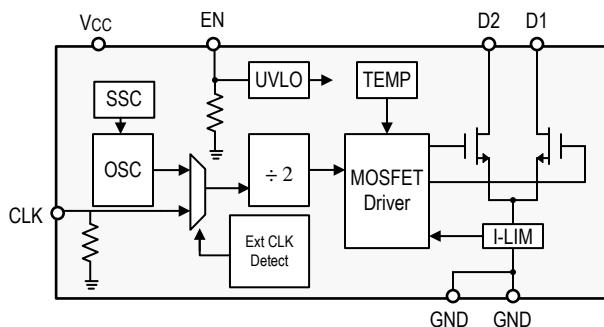
## 8 Detailed Description

### 8.1 Overview

The SN6505x-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

The output frequency of the oscillator is divided down by two. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. Before either one of the gates can assume logic high, the BBM logic ensures a short time period during which both signals are low and both transistors are high-impedance. This short period, is required to avoid shorting out both ends of the primary. The resulting output signals, present the gate-drive signals for the output transistors.

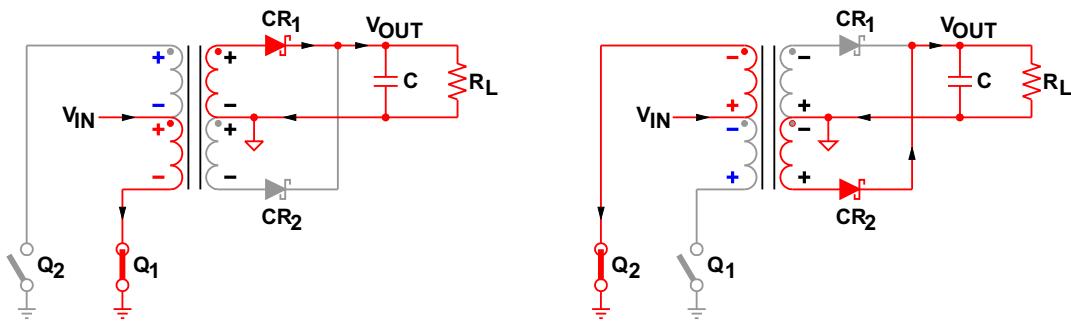
### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see [图 38](#)).



**图 38. Switching Cycles of a Push-Pull Converter**

When  $Q_1$  conducts,  $V_{IN}$  drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the  $V_{IN}$  potential at the center-tap.

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through  $Q_2$ , which now has turned high-impedance. The two voltage sources, each of which equaling  $V_{IN}$ , appear in series and cause a voltage potential at the open end of the primary of  $2 \times V_{IN}$  with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode  $CR_1$ . The secondary current starting from the upper secondary end flows through  $CR_1$ , charges capacitor  $C$ , and returns through the load impedance  $R_L$  back to the center-tap.

## Feature Description (接下页)

When  $Q_2$  conducts,  $Q_1$  goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a  $2 \times V_{IN}$  potential against ground. In this case  $CR_2$  is forward biased while  $CR_1$  is reverse biased and current flows from the lower secondary end through  $CR_2$ , charging the capacitor and returning through the load to the center-tap.

### 8.3.2 Core Magnetization

图 39 shows the ideal magnetizing curve for a push-pull converter with  $B$  as the magnetic flux density and  $H$  as the magnetic field strength. When  $Q_1$  conducts the magnetic flux is pushed from  $A$  to  $A'$ , and when  $Q_2$  conducts the flux is pulled back from  $A'$  to  $A$ . The difference in flux and thus in flux density is proportional to the product of the primary voltage,  $V_P$ , and the time,  $t_{ON}$ , it is applied to the primary:  $B \approx V_P \times t_{ON}$ .

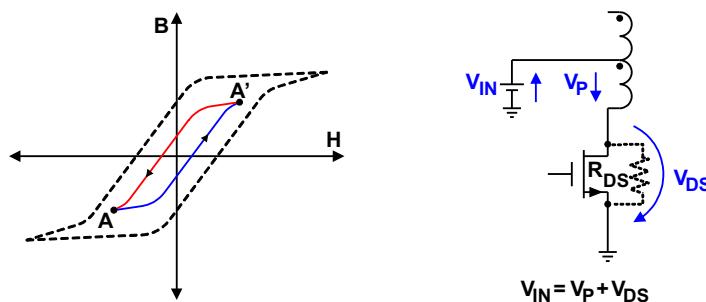


图 39. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of  $R_{DS(on)}$

This volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

## 8.4 Device Functional Modes

The functional modes of the device are divided into start-up, operating, and off-mode.

### 8.4.1 Start-Up Mode

When the supply voltage at  $V_{CC}$  ramps up to 2.25 V, the internal oscillator starts operating. The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached its full maximum yet.

#### 8.4.1.1 Soft-Start

SN6505A-Q1 and SN6505B-Q1 devices support soft-start feature. Upon power up or when EN pin transitions from Low to High, the gate drive of the output power-MOSFET is gradually increased over a period of time from 0 V to  $V_{CC}$ . Soft-start prevents high inrush current from  $V_{CC}$  while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up. For applications that need quick power-up, the SN6505D-Q1, that has soft-start disabled, can be used.

### 8.4.2 Operating Mode

When the device supply has reached its nominal value  $\pm 10\%$  the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2.

### 8.4.3 Shutdown-Mode

The device has a dedicated enable pin to put the device in very low power mode to save power when not in use. Enable pin has an internal pull down resistor which keeps device disabled when not driven. When disabled or when  $V_{CC}$  is  $< 1.7$  V, both drain outputs, D1 and D2, are tri-stated.

### 8.4.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. SN6505 addresses this by modulating its internal clock in such a way that the emitting energy is spread over multiple frequency bins. This Spread Spectrum clocking feature greatly improves the emissions performance of the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

### 8.4.5 External Clock Mode

The SN6505x-Q1 has a CLK pin which can be used to synchronize the device with system clock and in turn with other SN6505x-Q1 devices so that the system can control the exact switching frequency of the device. The Rising edge of the CLK is used to divide a clock by two and used to drive the gates. [图 41](#) shows the timing diagram for the same. The device also has external clock fail safe feature which automatically switches the device to the internal clock if a valid input clock is not present for long ( $t_{CLKTIMER}$ ). The in-built emissions reduction scheme of Spread Spectrum clocking is disabled when external clock is present.

## 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN6505x-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters using the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

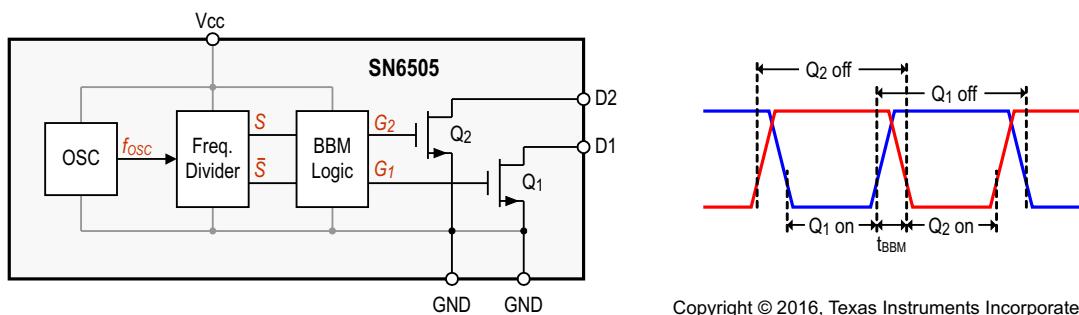


图 40. Block Diagram and Output Timing With Break-Before-Make Action

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and  $\bar{S}$ , with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals,  $G_1$  and  $G_2$ , present the gate-drive signals for the output transistors  $Q_1$  and  $Q_2$ . As shown in [图 41](#), before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

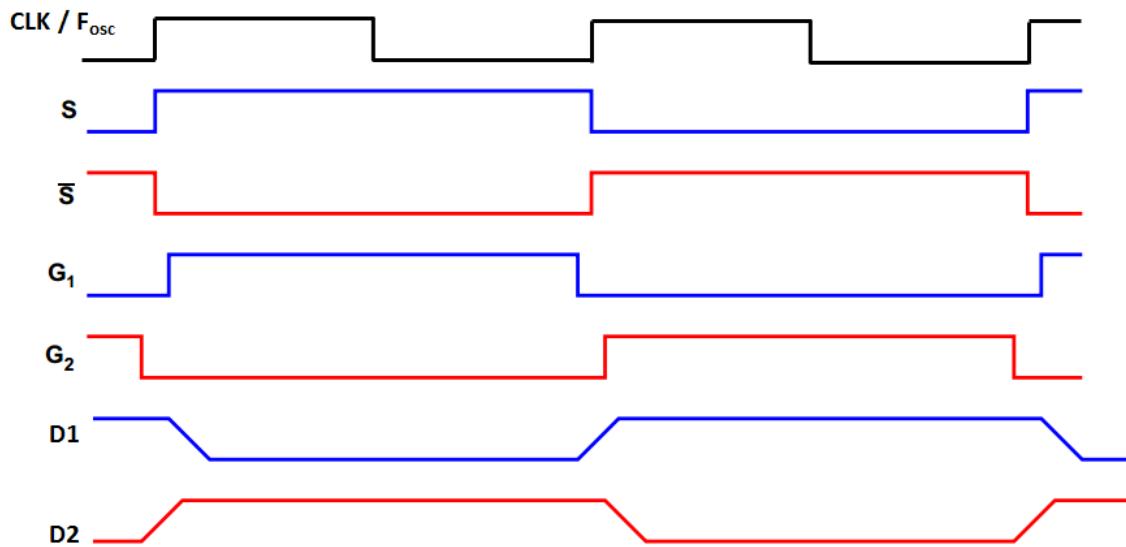
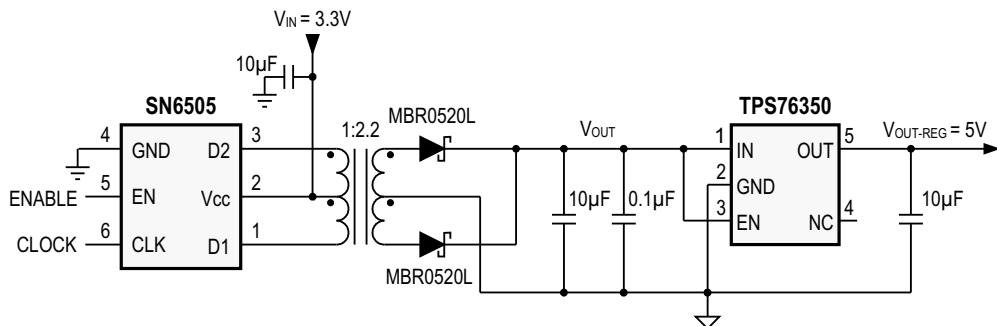


图 41. Detailed Output Signal Waveforms

## 9.2 Typical Application



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图 42. Typical Application Schematic

### 9.2.1 Design Requirements

For this design example, use the parameters listed in [表 1](#) as design parameters.

表 1. Design Parameters

Design Parameter	Example Value
Input voltage range	3.3 V ± 3%
Output voltage	5 V
Maximum load current	100 mA

### 9.2.2 Detailed Design Procedure

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, the output voltage of the unregulated converter output drops significantly over a wide range in load current. The characteristic curve in [图 1](#) and [图 11](#) for example, shows that the difference between  $V_{OUT}$  at minimum load and  $V_{OUT}$  at maximum load exceeds a transceiver's supply range. Therefore, in order to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

The final converter circuit is shown in [图 47](#). The measured  $V_{OUT}$  and efficiency characteristics for the regulated and unregulated outputs are shown in [图 2](#) and [图 12](#).

### 9.2.2.1 Drive Capability

The transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 2.25 V to 5.5 V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios don't lead to primary currents that exceed the specified current limits of the device.

### 9.2.2.2 LDO Selection

The minimum requirements for a suitable low dropout regulator are:

- Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 600 mA, choose a 600 mA to 750 mA LDO. While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.
- The internal dropout voltage,  $V_{DO}$ , at the specified load current should be as low as possible to maintain efficiency. For a low-cost 750 mA LDO, a  $V_{DO}$  of 600 mV at 750 mA is common. Be aware; however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I-min} = V_{DO-max} + V_{O-max} \quad (1)$$

This means in order to determine  $V_I$  for worst-case condition, the user must take the maximum values for  $V_{po}$  and  $V_O$  specified in the LDO data sheet for rated output current (that is, 600 mA) and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than  $V_{I-min}$ . If it is not, the LDO will lose line-regulation and any variations at the input passes straight through to the output. Hence, below  $V_{I-min}$  the output voltage follows the input and the regulator behaves like a simple conductor.

- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across  $R_{DS-on}$  negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches its maximum voltage of

$$V_{S-max} = V_{IN-max} \times n \quad (2)$$

with  $V_{IN-max}$  as the maximum converter input voltage and  $n$  as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than  $V_{S-max}$ . 表 2 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

**表 2. Required Maximum LDO Input Voltages for Various Push-Pull Configurations**

PUSH-PULL CONVERTER			LDO	
CONFIGURATION	$V_{IN-max}$ [V]	TURNS-RATIO	$V_{S-max}$ [V]	$V_{I-max}$ [V]
3.3 $V_{IN}$ to 3.3 $V_{OUT}$	3.6	$1.5 \pm 3\%$	5.6	6 to 10
3.3 $V_{IN}$ to 5 $V_{OUT}$	3.6	$2.2 \pm 3\%$	8.2	10
5 $V_{IN}$ to 5 $V_{OUT}$	5.5	$1.5 \pm 3\%$	8.5	10

### 9.2.2.3 Diode Selection

A rectifier diode should always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the SN6505x-Q1 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275 mV at 100-mA forward current. For higher output voltages such as ±10 V and above use the MBR0530 which provides a higher DC blocking voltage of 30 V.

Lab measurements have shown that at temperatures higher than 100°C the leakage currents of the above Schottky diodes increase significantly. This can cause thermal runaway leading to the collapse of the rectifier output voltage. Therefore, for ambient temperatures higher than 85°C use low-leakage Schottky diodes, such as RB168MM-40.

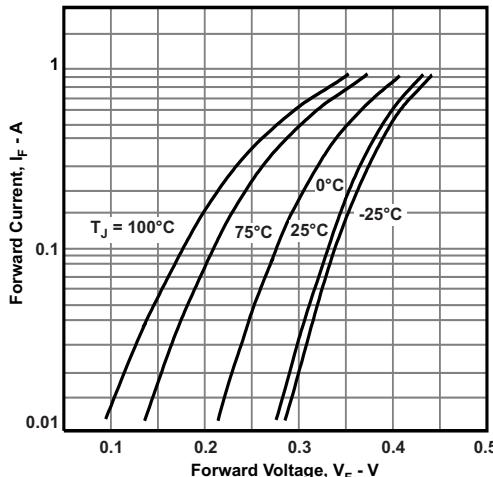


图 43. Diode Forward Characteristics for MBR0520L

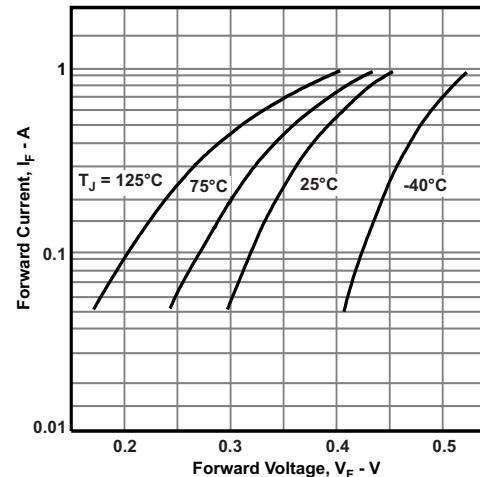


图 44. Diode Forward Characteristics MBR0530

### 9.2.2.4 Capacitor Selection

The capacitors in the converter circuit in [图 47](#) are multi-layer ceramic chip (MLCC) capacitors.

As with all high speed CMOS ICs, the device requires a bypass capacitor in the range of 10 nF to 100 nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1  $\mu$ F to 10  $\mu$ F. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and  $V_{IN}$ , the capacitor can be placed at the supply entrance of the board. To ensure low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 1  $\mu$ F to 10  $\mu$ F.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47 nF to 100 nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7  $\mu$ F to 10  $\mu$ F will satisfy these requirements.

### 9.2.2.5 Transformer Selection

#### 9.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by the device. The maximum voltage delivered by the device is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through:

$$Vt_{min} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \quad (3)$$

Taking an example of  $f_{min}$  as 138 kHz for SN6505A-Q1 and 363 kHz for SN6505B-Q1 or SN6505D-Q1 with a 5 V supply, [公式 3](#) yields the minimum V-t products of:

$$Vt_{min} \geq \frac{5.5 \text{ V}}{2 \times 138 \text{ kHz}} = 20 \text{ V}\mu\text{s} \quad \text{for SN6505A-Q1, and}$$

$$Vt_{min} \geq \frac{5.5 \text{ V}}{2 \times 363 \text{ kHz}} = 7.6 \text{ V}\mu\text{s} \quad \text{for SN6505B/D-Q1 applications.} \quad (4)$$

Common V-t values for low-power center-tapped transformers range from 22 V $\mu$ s to 150 V $\mu$ s with typical footprints of 10 mm x 12 mm. However, transformers specifically designed for PCMCIA applications provide as little as 11 V $\mu$ s and come with a significantly reduced footprint of 6 mm x 6 mm only.

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

#### 9.2.2.5.2 Turns Ratio Estimate

Assume the rectifier diodes and linear regulator has been selected. Also, it has been determined that the transformer chosen must have a V-t product of at least 11 V $\mu$ s. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typical efficiency of 97% into account:

$$V_{P-min} = V_{IN-min} - V_{DS-max} \quad (5)$$

$V_{S-min}$  must be large enough to allow for a maximum voltage drop,  $V_{F-max}$ , across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the [LDO Selection](#) section, this minimum input voltage is known and by adding  $V_{F-max}$  gives the minimum secondary voltage with:

$$V_{S-min} = V_{F-max} + V_{DO-max} + V_{O-max} \quad (6)$$

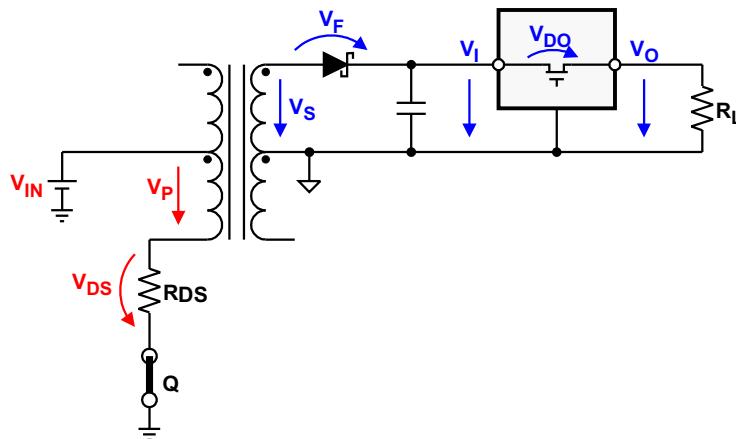


图 45. Establishing the Required Minimum Turns Ratio Through  $N_{\min} = 1.031 \times V_{S-\min} / V_{P-\min}$

Then calculating the available minimum primary voltage,  $V_{P-\min}$ , involves subtracting the maximum possible drain-source voltage of the device,  $V_{DS-\max}$ , from the minimum converter input voltage  $V_{IN-\min}$ :

$$V_{P-\min} = V_{IN-\min} - V_{DS-\max} \quad (7)$$

$V_{DS-\max}$  however, is the product of the maximum  $R_{DS(\text{on})}$  and  $I_D$  values for a given supply specified in the data sheet:

$$V_{DS-\max} = R_{DS-\max} \times I_{D\max} \quad (8)$$

Then inserting 公式 8 into 公式 7 yields:

$$V_{P-\min} = V_{IN-\min} - R_{DS-\max} \times I_{D\max} \quad (9)$$

and inserting 公式 9 and 公式 6 into 公式 5 provides the minimum turns ration with:

$$n_{\min} = 1.031 \times \frac{V_{F-\max} + V_{DO-\max} + V_{O-\max}}{V_{IN-\min} - R_{DS-\max} \times I_{D\max}} \quad (10)$$

### Example:

For a 3.3 V<sub>IN</sub> to 5 V<sub>OUT</sub> converter using the rectifier diode MBR0520L and the 5 V LDO, the data sheet values taken for a load current of 600 mA and a maximum temperature of 85°C are  $V_{F-\max} = 0.2$  V,  $V_{DO-\max} = 0.5$  V, and  $V_{O-\max} = 5.1$  V.

Then assuming that the converter input voltage is taken from a 3.3 V controller supply with a maximum  $\pm 2\%$  accuracy makes  $V_{IN-\min} = 3.234$  V. Finally the maximum values for drain-source resistance and drain current at 3.3 V are taken from the data sheet with  $R_{DS-\max} = 0.31$  Ω and  $I_{D\max} = 1$  A.

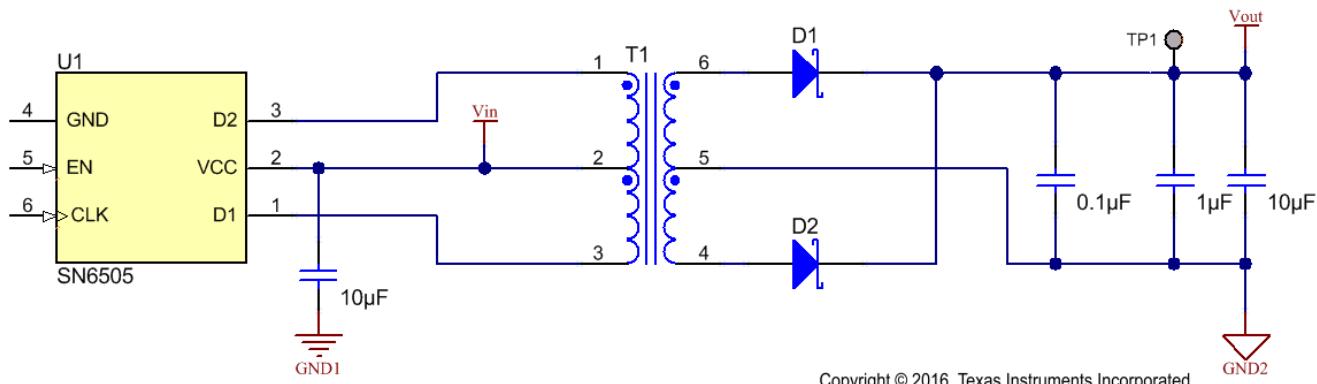
Inserting the values above into 公式 10 yields a minimum turns ratio of:

$$n_{\min} = 1.031 \times \frac{0.2 \text{ V} + 0.5 \text{ V} + 5.1 \text{ V}}{3.234 \text{ V} - 0.31 \Omega \times 1 \text{ A}} = 2.05 \quad (11)$$

Most commercially available transformers for 3-to-5 V push-pull converters offer turns ratios between 2.0 and 2.3 with a common tolerance of  $\pm 3\%$ .

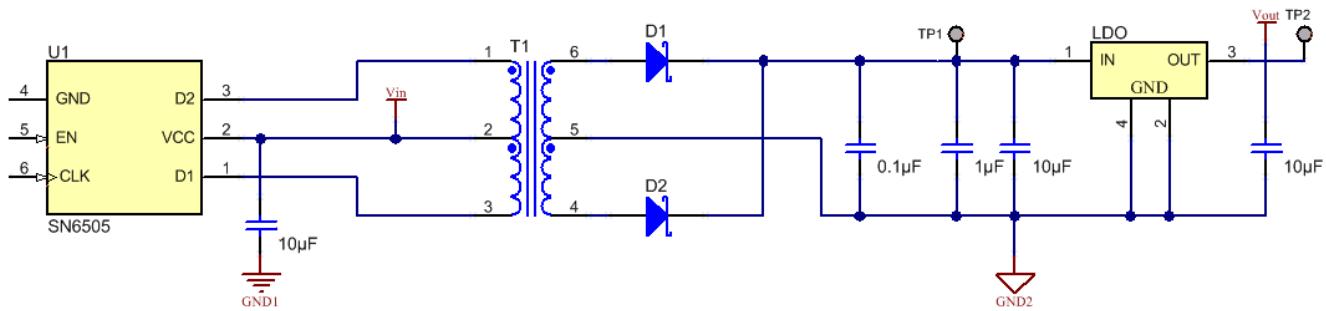
### 9.2.2.5.3 Recommended Transformers

Depending on the application, use the minimum configuration in [图 46](#) or standard configuration in [图 47](#).



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**图 46. Unregulated Output for Low-Current Loads With Wide Supply Range**



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**图 47. Regulated Output for Stable Supplies and High Current Loads**

The Wurth Electronics Midcom isolation transformers in [表 3](#) are optimized designs for the device, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

**表 3. Recommended Isolation Transformers Optimized for the Device**

TURNS RATIO	V × T (V $\mu$ s)	ISOLATION (V <sub>RMS</sub> )	DIMENSIONS (mm)	APPLICATION	LDO <sup>(1)</sup>	ORDER NO.	MANUFACTURER
1:1.1 ±2%	7	11	6.73 x 10.05 x 4.19 2500	3.3 V → 3.3 V, 100mA, SN6505B/D-Q1 Refer to <a href="#">图 13</a> and <a href="#">图 14</a>	No	760390011	Wurth Electronics / Midcom
1:1.1 ±2%				5 V → 5 V, 100mA, SN6505B/D-Q1 Refer to <a href="#">图 15</a> and <a href="#">图 16</a>		760390012	
1:1.7 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1 Refer to <a href="#">图 17</a> and <a href="#">图 18</a>		760390013	
1:1.3 ±2%				3.3 V → 3.3 V, 100mA, SN6505B/D-Q1 Refer to <a href="#">图 19</a> and <a href="#">图 20</a>	Yes	760390014	
1:1.3 ±2%				5 V → 5 V, 100mA, SN6505B/D-Q1 Refer to <a href="#">图 21</a> and <a href="#">图 22</a>		760390014	
1:2.1 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1 Refer to <a href="#">图 23</a> and <a href="#">图 24</a>		760390015	
1.23:1 ±2%				5 V → 3.3 V, 100mA, SN6505B/D-Q1		750313710	
1:1.7 ±2%	8.9			3.3 V → 3.3 V, 1A, SN6505B/D-Q1 Refer to <a href="#">图 25</a> and <a href="#">图 26</a>		750316028	
1:2.1 ±2%				3.3 V → 5 V, 1A, SN6505B/D-Q1 Refer to <a href="#">图 27</a> and <a href="#">图 28</a>	No	750316029	
1.3:1 ±2%	10.8			5 V → 3.3 V, 1A, SN6505B/D-Q1 Refer to <a href="#">图 29</a> and <a href="#">图 30</a>		750316030	
1:1.1 ±2%	8.6			3.3 V → 3.3 V, 1A, SN6505B/D-Q1 5 V → 5 V, 1A, SN6505B/D-Q1 Refer to <a href="#">图 11</a> and <a href="#">图 12</a>		750315371	
1:1.1 ±2%	11	5000	9.14 x 12.7 x 7.37	3.3 V → 3.3 V, 100mA, SN6505B/D-Q1	Yes	750313734	Wurth Electronics / Midcom
1:1.1 ±2%				5 V → 5 V, 100mA, SN6505B/D-Q1		750313734	
1:1.7 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1		750313769	
1:1.3 ±2%				3.3 V → 3.3 V, 100mA, SN6505B/D-Q1 5 V → 5 V, 100mA, SN6505B/D-Q1		750313638	
1:2.1 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1	No	750313626	
1.3:1 ±2%				5 V → 3.3 V, 100mA, SN6505B/D-Q1		750313638	
1:1.75 ±2%	41	12.32 x 15.41 x 11.05	3.3 V → 3.3 V, 1A, SN6505A-Q1 Refer to <a href="#">图 3</a> and <a href="#">图 4</a>	Yes	750316031	Wurth Electronics / Midcom	
1:2 ±2%				3.3 V → 5 V, 1A, SN6505A-Q1 Refer to <a href="#">图 5</a> and <a href="#">图 6</a>	No	750316032	
1.3:1 ±2%				5.0 V → 3.3 V, 1A, SN6505A-Q1 Refer to <a href="#">图 7</a> and <a href="#">图 8</a>		750316033	
1:1.1 ±2%				3.3 V → 3.3 V, 1A, SN6505A-Q1 5 V → 5 V, 1A, SN6505A-Q1 Refer to <a href="#">图 1</a> and <a href="#">图 2</a>	Yes	750315240	
1:1.3 ±3%	11	5000	10.4 x 12.2 x 6.1	3.3 V → 3.3 V, 300mA, SN6505B/D-Q1 5 V → 5 V, 300mA, SN6505B/D-Q1	No	HCT-SM-1.3-8-2	Bourns
1:1.5 ±3%	34.4	2500	10 x 12.07 x 5.97	3.3 V → 3.3 V, 1A, SN6505A/B/D-Q1 5 V → 5 V, 1A, SN6505A/B/D-Q1	Yes	DA2303-AL	Coilcraft
1:2.2 ±3%	21.5	2500	10 x 12.07 x 5.97	3.3 V → 5 V, 1A, SN6505A/B/D-Q1		DA2304-AL	

(1) For configurations with LDO, a higher voltage than the required output voltage is generated, to allow for LDO drop-out. Figures show the voltage and efficiency at the LDO input.

### 9.2.3 Application Curves

See the [Typical Characteristics, SN6505A-Q1](#) and [Typical Characteristics, SN6505B-Q1 or SN6505D-Q1](#) for application curves with transformers optimized for the device, providing high efficiency and small form factor at low-cost.

## 9.2.4 System Examples

### 9.2.4.1 Higher Output Voltage Designs

The device can drive push-pull converters that provide high output voltages of up to 30 V, or bipolar outputs of up to  $\pm 15$  V. Using commercially available center-tapped transformers, with their rather low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. 图 48 to 图 50 show some of these topologies together with their respective open-circuit output voltages.

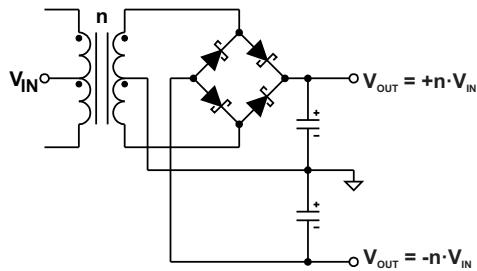


图 48. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

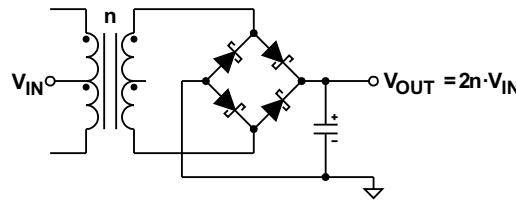


图 49. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling

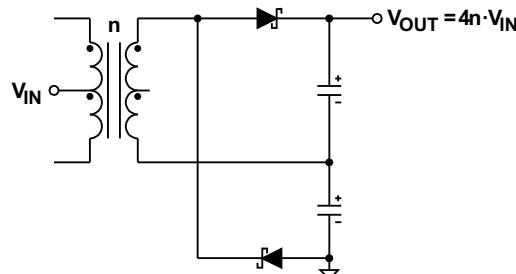


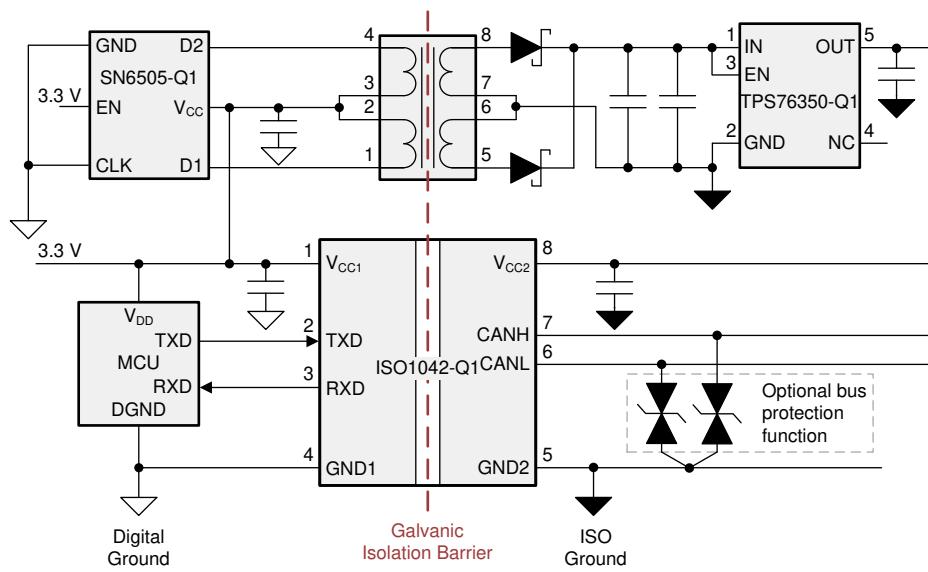
图 50. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V\_IN

### 9.2.4.2 Application Circuits

The following application circuits are shown for a 3.3 V input supply commonly taken from the local, regulated microcontroller supply. For 5 V input voltages requiring different turn ratios refer to the transformer manufacturers and their web sites listed in 表 4.

表 4. Transformer Manufacturers

MANUFACTURER	MORE INFORMATION
Coilcraft Inc.	<a href="http://www.coilcraft.com">http://www.coilcraft.com</a>
Halo-Electronics Inc.	<a href="http://www.haloelectronics.com">http://www.haloelectronics.com</a>
Murata Power Solutions	<a href="http://www.murata-ps.com">http://www.murata-ps.com</a>
Wurth Electronics Midcom Inc	<a href="http://www.midcom-inc.com">http://www.midcom-inc.com</a>


**图 51. Isolated CAN Interface**

## 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5 V nominal. This input supply must be regulated within  $\pm 10\%$ . If the input supply is located more than a few inches from the device, a  $0.1 \mu\text{F}$  by-pass capacitor should be connected as close as possible to the device  $V_{\text{CC}}$  pin and a  $10 \mu\text{F}$  capacitor should be connected close to the transformer center-tap pin.

## 11 Layout

### 11.1 Layout Guidelines

- The  $V_{\text{IN}}$  pin must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from  $1 \mu\text{F}$  to  $10 \mu\text{F}$ . The capacitor must have a voltage rating of 10 V minimum and a X5R or X7R dielectric.
- The optimum placement is closest to the  $V_{\text{IN}}$  and GND pins at the board entrance to minimize the loop area formed by the bypass-capacitor connection, the  $V_{\text{IN}}$  terminal, and the GND pin. See [图 52](#) for a PCB layout example.
- The connections between the device D1 and D2 pins and the transformer primary endings, and the connection of the device  $V_{\text{CC}}$  pin and the transformer center-tap must be as close as possible for minimum trace inductance.
- The connection of the device  $V_{\text{CC}}$  pin and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from  $1 \mu\text{F}$  to  $10 \mu\text{F}$ . The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.
- The device GND pins must be tied to the PCB ground plane using two vias for minimum inductance.
- The ground connections of the capacitors and the ground plane should use two vias for minimum inductance.
- The rectifier diodes should be Schottky diodes with low forward voltage in the 10 mA to 100 mA current range to maximize efficiency.
- The  $V_{\text{OUT}}$  pin must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from  $1 \mu\text{F}$  to  $10 \mu\text{F}$ . The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.

### 11.2 Layout Example

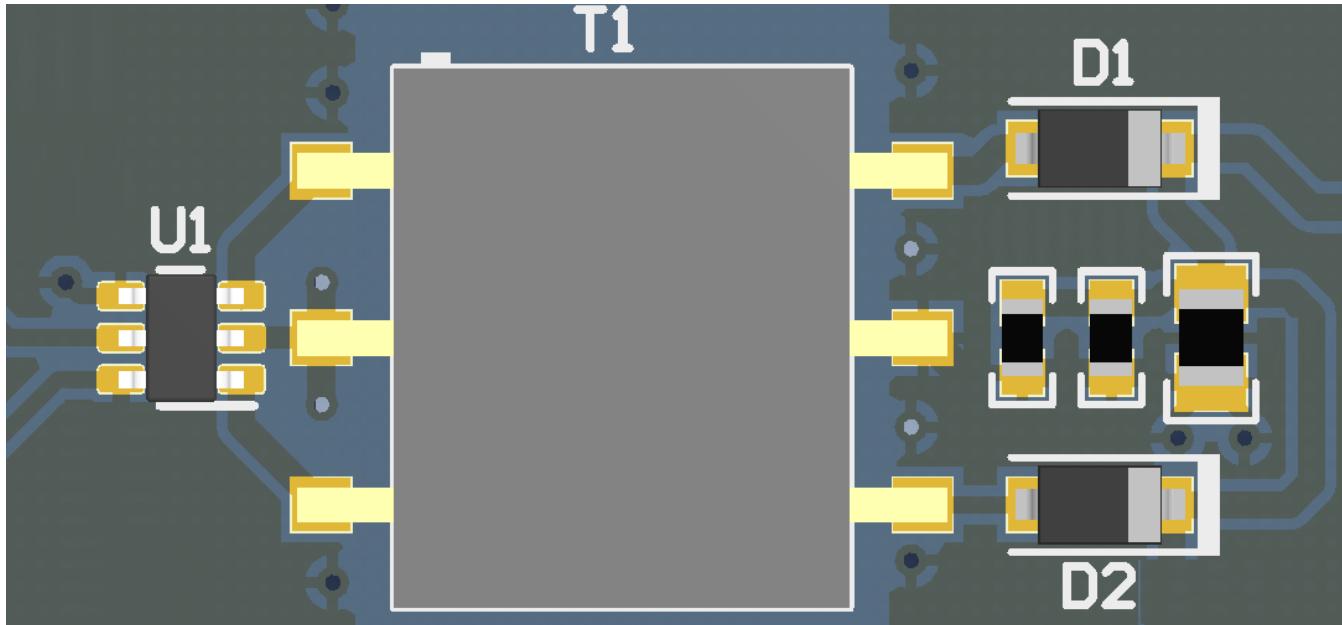


图 52. Layout Example of a 2-Layer Board

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 第三方产品免责声明

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### 12.2 文档支持

#### 12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI), [《数字隔离器设计指南》](#)
- 德州仪器 (TI), [《隔离相关术语》](#)
- 德州仪器 (TI), [如何在隔离式 CAN 系统中隔离信号和电源 TI 技术手册](#)
- 德州仪器 (TI), [《适用于三相逆变器的小型增强型隔离式 IGBT 栅极驱动参考设计》TI 设计](#)

### 12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 5. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
SN6505A-Q1	<a href="#">单击此处</a>				
SN6505B-Q1	<a href="#">单击此处</a>				
SN6505D-Q1	<a href="#">单击此处</a>				

### 12.4 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.6 商标

E2E is a trademark of Texas Instruments.

### 12.7 静电放电警告

 ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

 ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能导致器件与其发布的规格不相符。

### 12.8 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN6505AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65AQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN6505AQDBVTQ1	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65AQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN6505BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65BQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN6505BQDBVTQ1	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65BQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN6505DQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65DQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN6505DQDBVTQ1	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65DQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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## PACKAGE OPTION ADDENDUM

10-Dec-2020

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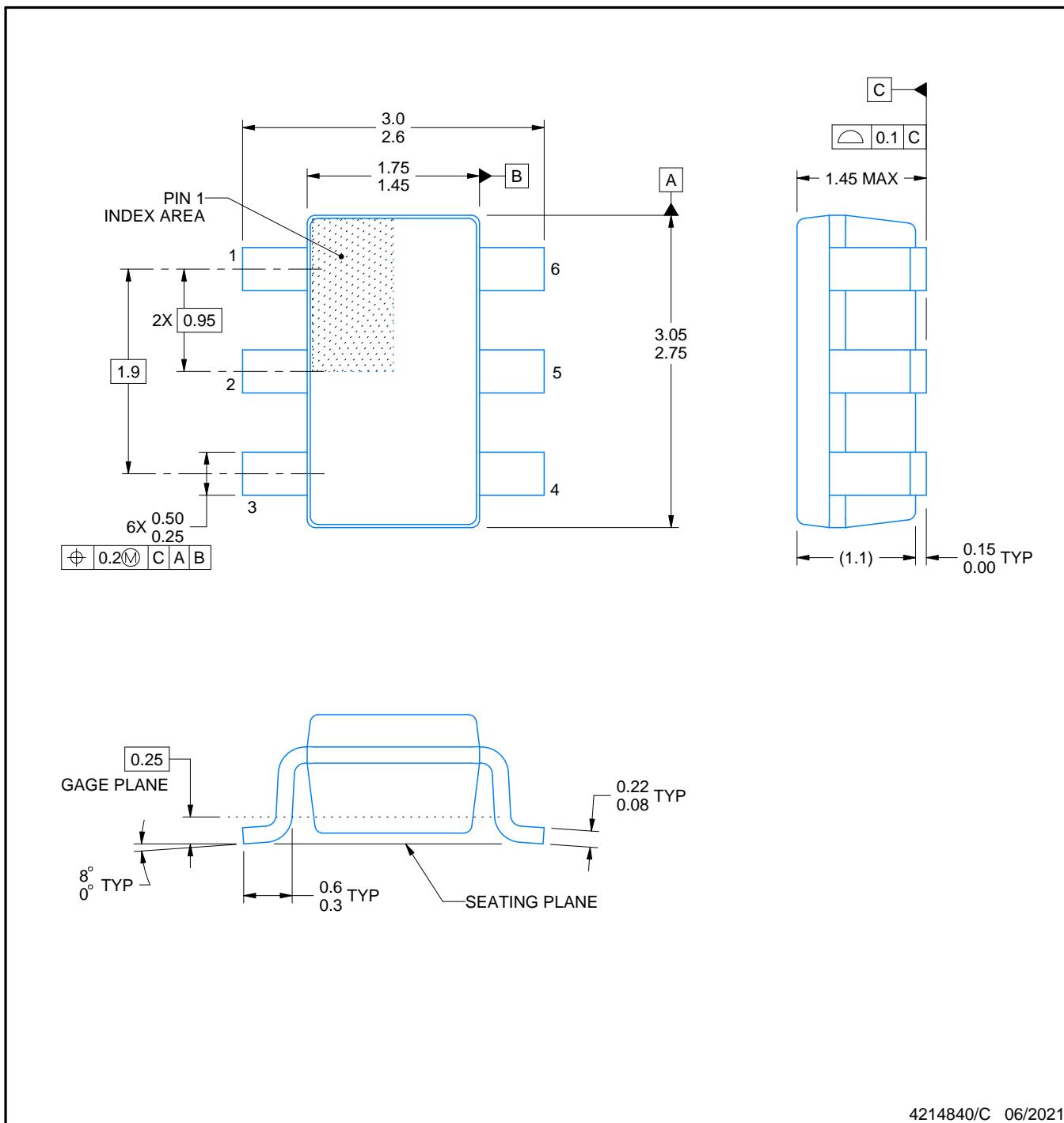
# PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

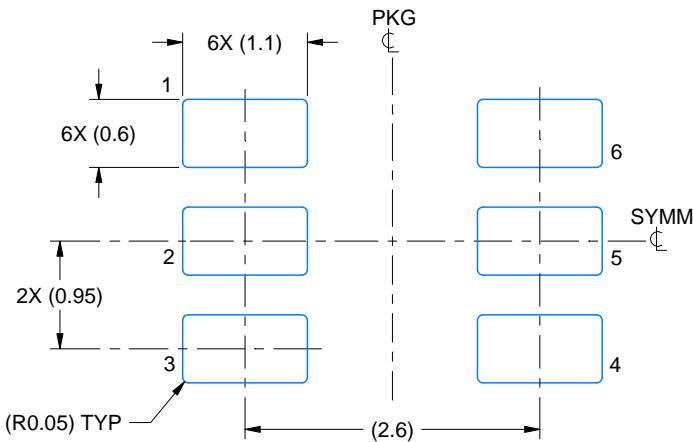
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

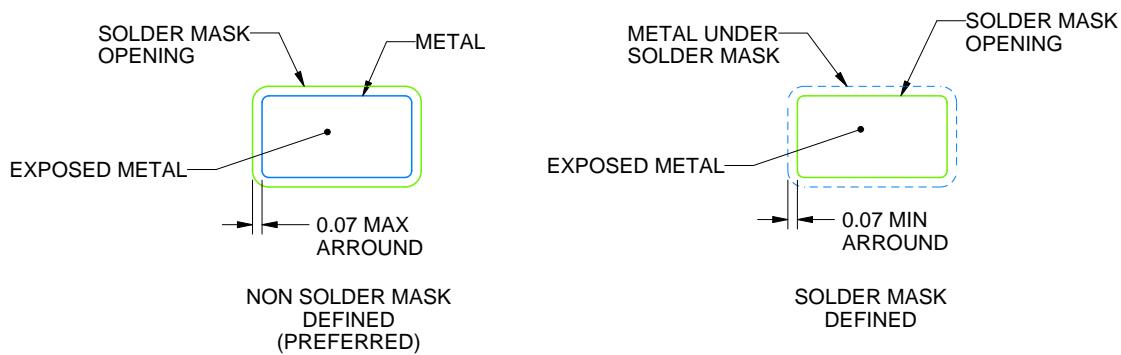
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

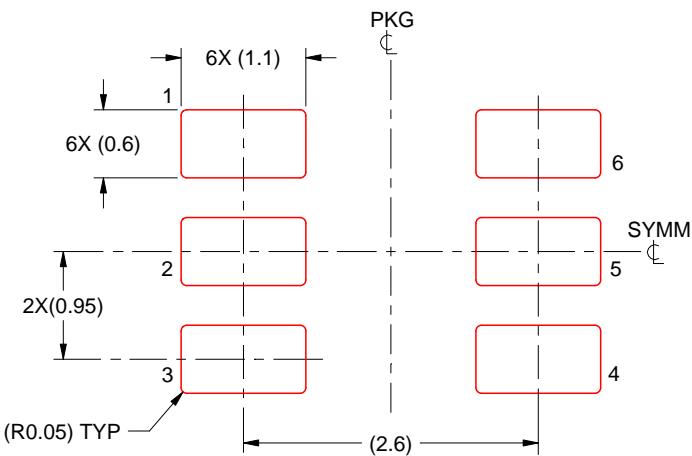
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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