

5-V PECL/ECL 1:2 Fanout Buffer

FEATURES

- 1:2 PECL/ECL Fanout Buffer
- Operating Range
 - PECL: $V_{CC} = 4.2\text{ V to }5.7\text{ V}$ With $V_{EE} = 0\text{ V}$
 - NECL: $V_{CC} = 0\text{ V}$ With $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
- 5-ps Skew Between Outputs
- Support for Clock Frequencies $>2.5\text{ GHz}$
- 265-ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions
- Drop-In Compatible With MC10EL11, MC100EL11
- Built-In Input Pulldown Resistors
- Built-In Temperature Compensation

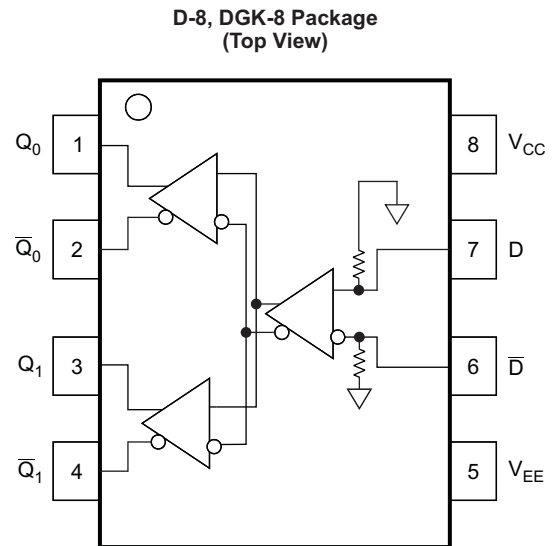
APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

DESCRIPTION

The SN65EL11 is a differential 1:2 PECL/ECL fanout buffer. The device includes circuitry to maintain a known logic level when inputs are in an open condition. The SN65EL11 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 package.

PINOUT ASSIGNMENT



P0065-02

Table 1. Pin Description

| PIN | FUNCTION |
|----------------------------------|----------------------|
| D, \bar{D} | PECL/ECL data inputs |
| $Q_0, \bar{Q}_0, Q_1, \bar{Q}_1$ | PECL/ECL outputs |
| V_{CC} | Positive supply |
| V_{EE} | Negative supply |

ORDERING INFORMATION⁽¹⁾

| PART NUMBER | PART MARKING | PACKAGE | LEAD FINISH |
|-------------|--------------|------------|-------------|
| SN65EL11D | SN65EL11 | SOIC | NiPdAu |
| SN65EL11DGK | SN65EL11 | SOIC-TSSOP | NiPdAu |

(1) Leaded device options not initially available; contact a sales representative for further details.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| PARAMETER | CONDITIONS | VALUE | UNIT |
|---|--|------------|------|
| Absolute PECL-mode supply voltage, V_{CC} | $V_{EE} = 0\text{ V}$ | 6 | V |
| Absolute NECL-mode supply voltage, V_{EE} | $V_{CC} = 0\text{ V}$ | -6 | V |
| PECL-mode input voltage | $V_{EE} = 0\text{ V}; V_I \leq V_{CC}$ | 6 | V |
| NECL-mode input voltage | $V_{CC} = 0\text{ V}; V_I \geq V_{EE}$ | -6 | V |
| Output current | Continuous | 50 | mA |
| | Surge | 100 | mA |
| Operating temperature range | | -40 to 85 | °C |
| Storage temperature range | | -65 to 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | POWER RATING $T_A < 25^\circ\text{C}$ (mW) | THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW | DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C) | POWER RATING $T_A = 85^\circ\text{C}$ (mW) |
|------------|---------------------|---|---|--|--|
| SOIC | Low-K | 719 | 139 | 7 | 288 |
| | High-K | 840 | 119 | 8 | 336 |
| SOIC-TSSOP | Low-K | 469 | 213 | 5 | 188 |
| | High-K | 527 | 189 | 5 | 211 |

THERMAL CHARACTERISTICS

| PARAMETER | | PACKAGE | VALUE | UNIT |
|---------------|--------------------------------------|------------|-------|------|
| θ_{JB} | Junction-to-board thermal resistance | SOIC | 79 | °C/W |
| | | SOIC-TSSOP | 120 | |
| θ_{JC} | Junction-to-case thermal resistance | SOIC | 98 | °C/W |
| | | SOIC-TSSOP | 74 | |

KEY ATTRIBUTES

| CHARACTERISTICS | VALUE |
|---|-----------------------|
| Internal input pulldown resistor | 75 k Ω |
| Moisture sensitivity level | Level 1 |
| Flammability rating (oxygen index: 28 to 34) | UL 94 V-0 at 0.125 in |
| ESD-HBM | 4 kV |
| ESD-machine model | 200 V |
| Meets or exceeds JEDEC Spec EIA/JESD78 latchup test | |

PECL DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 5\text{ V}$; $V_{EE} = 0\text{ V}$)⁽²⁾

| PARAMETER | –40°C | | | 25°C | | | 85°C | | | UNIT |
|---|-------|-----|------|------|------|------|------|-----|------|------|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{CC} Power-supply current | | 18 | 26 | | 21 | 26 | | 23 | 26 | mA |
| V_{OH} Output HIGH voltage ⁽³⁾ | 3915 | | 4120 | 3915 | 4000 | 4120 | 3915 | | 4120 | mV |
| V_{OL} Output LOW voltage ⁽³⁾ | 3170 | | 3380 | 3170 | 3288 | 3380 | 3170 | | 3380 | mV |
| V_{IH} Input HIGH voltage (single-ended) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| V_{IL} Input LOW voltage (single-ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| V_{IHCMR} Input HIGH voltage, common-mode range (differential) ⁽⁴⁾ | 2.5 | | 4.6 | 2.5 | | 4.6 | 2.5 | | 4.6 | V |
| I_{IH} Input HIGH current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} Input LOW current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

(2) Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / –0.5 V.

(3) Outputs are terminated through a 50-Ω resistor to $V_{CC} - 2\text{ V}$.

(4) V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the more-positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min and 1 V.

NECL DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 0\text{ V}$; $V_{EE} = 5\text{ V}$)⁽²⁾

| PARAMETER | –40°C | | | 25°C | | | 85°C | | | UNIT |
|---|-------|-----|-------|-------|-------|-------|-------|-----|-------|------|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{EE} Power-supply current | | 19 | 26 | | 21 | 26 | | 23 | 26 | mA |
| V_{OH} Output HIGH voltage ⁽³⁾ | –1085 | | –880 | –1025 | –995 | –880 | –1025 | | –880 | mV |
| V_{OL} Output LOW voltage ⁽³⁾ | –1830 | | –1620 | –1810 | –1712 | –1620 | –1810 | | –1620 | mV |
| V_{IH} Input HIGH voltage (single-ended) | –1165 | | –880 | –1165 | | –880 | –1165 | | –880 | mV |
| V_{IL} Input LOW voltage (single-ended) | –1810 | | –1475 | –1810 | | –1475 | –1810 | | –1475 | mV |
| V_{IHCMR} Input HIGH voltage, common-mode range (differential) ⁽⁴⁾ | –2.5 | | –0.4 | –2.5 | | –0.4 | –2.5 | | –0.4 | V |
| I_{IH} Input HIGH current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} Input LOW current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

(2) Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / –0.5 V.

(3) Outputs are terminated through a 50-Ω resistor to $V_{CC} - 2\text{ V}$.

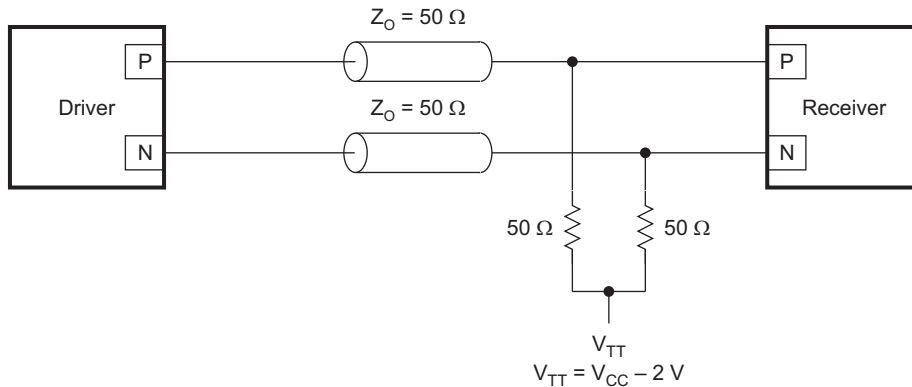
(4) V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the more-positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min and 1 V.

AC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 5\text{ V}$; $V_{EE} = 0\text{ V}$ or $V_{CC} = 0\text{ V}$; $V_{EE} = -5\text{ V}$)⁽²⁾

| PARAMETER | | -40°C | | | 25°C | | | 85°C | | | UNIT |
|-------------------|---|-------|-----|------|------|-----|------|------|-----|------|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{MAX} | Maximum switching frequency ⁽³⁾ (see Figure 6) | 3.5 | | | 3.4 | | | 3.1 | | | GHz |
| t_{PLH}/t_{PHL} | Propagation delay to output (see Figure 2) | 200 | | 300 | 200 | | 300 | 200 | | 300 | ps |
| t_{SKEW} | Device skew ⁽⁴⁾ (see Figure 5) | 7 15 | | | 7 15 | | | 7 15 | | | ps |
| | Duty cycle skew ⁽⁵⁾ | 5 15 | | | 5 15 | | | 5 15 | | | |
| t_{JITTER} | Random clock jitter (RMS) | 0.2 | | | 0.2 | | | 0.2 | | | ps |
| V_{PP} | Input swing ⁽⁶⁾ (see Figure 3) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t_r/t_f | Q-output rise/fall times (20%–80%) (see Figure 4) | 150 | | 250 | 150 | | 250 | 150 | | 250 | ps |

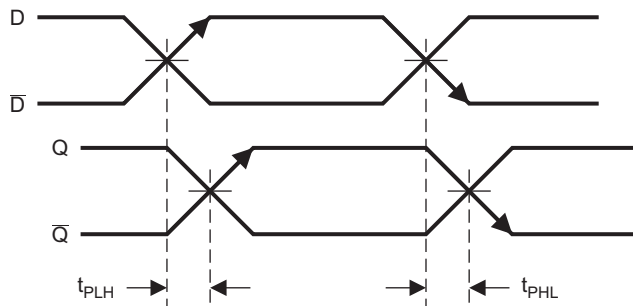
- (1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / -0.5 V.
- (3) Maximum switching frequency is measured at an output amplitude of 300 mVpp.
- (4) Within-device skew defined as identical transitions on similar paths through a device.
- (5) Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- (6) $V_{PP(min)}$ is the minimum input swing for which ac parameters are assured.

Typical Termination for Output Driver



S0078-02

Figure 1. Typical Termination for Output Driver



T0400-01

Figure 2. Propagation Delay

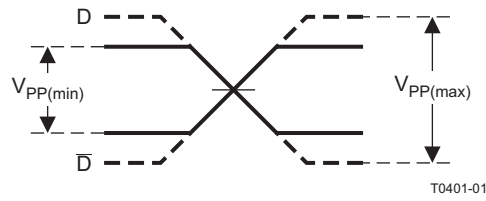


Figure 3. Input Voltage Swing

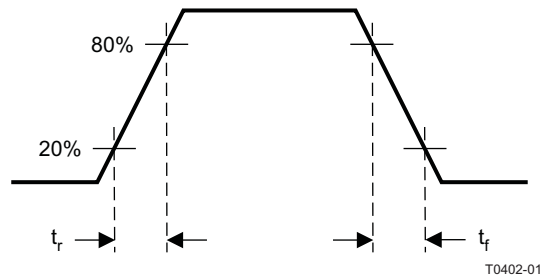
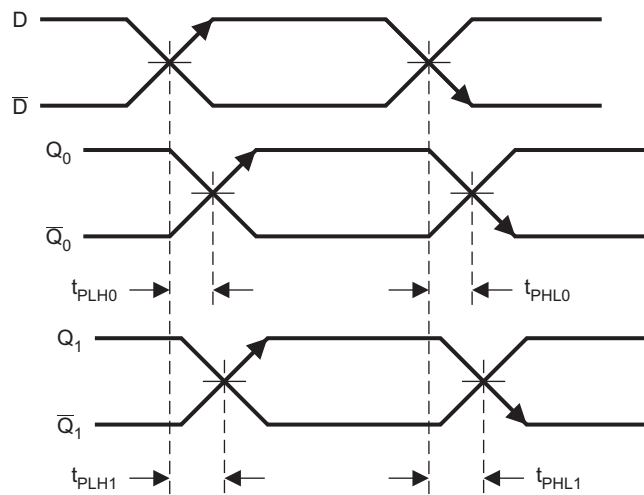


Figure 4. Output Rise and Fall Times



$$\text{Device Skew} = [(t_{PLH1} - t_{PLH0}), (t_{PHL1} - t_{PHL0})]$$

T0403-01

Figure 5. Device Skew

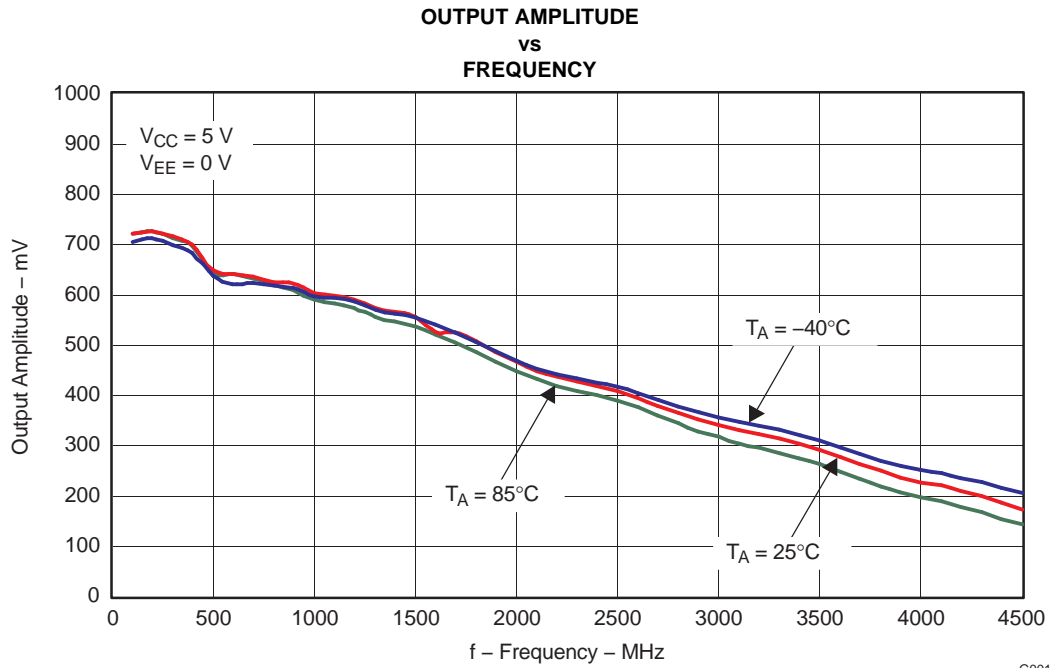


Figure 6.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65EL11D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EL11 | Samples |
| SN65EL11DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SILI | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65EL11D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| SN65EL11DGK | DGK | VSSOP | 8 | 80 | 330.2 | 6.6 | 3005 | 1.88 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

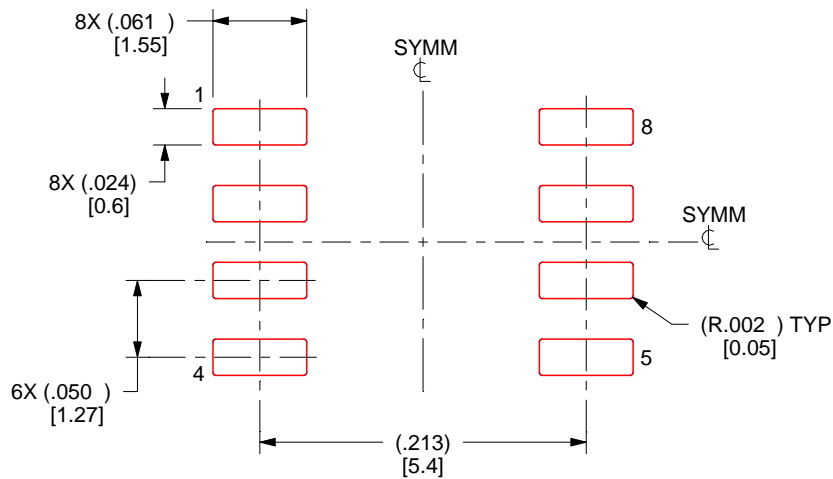
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

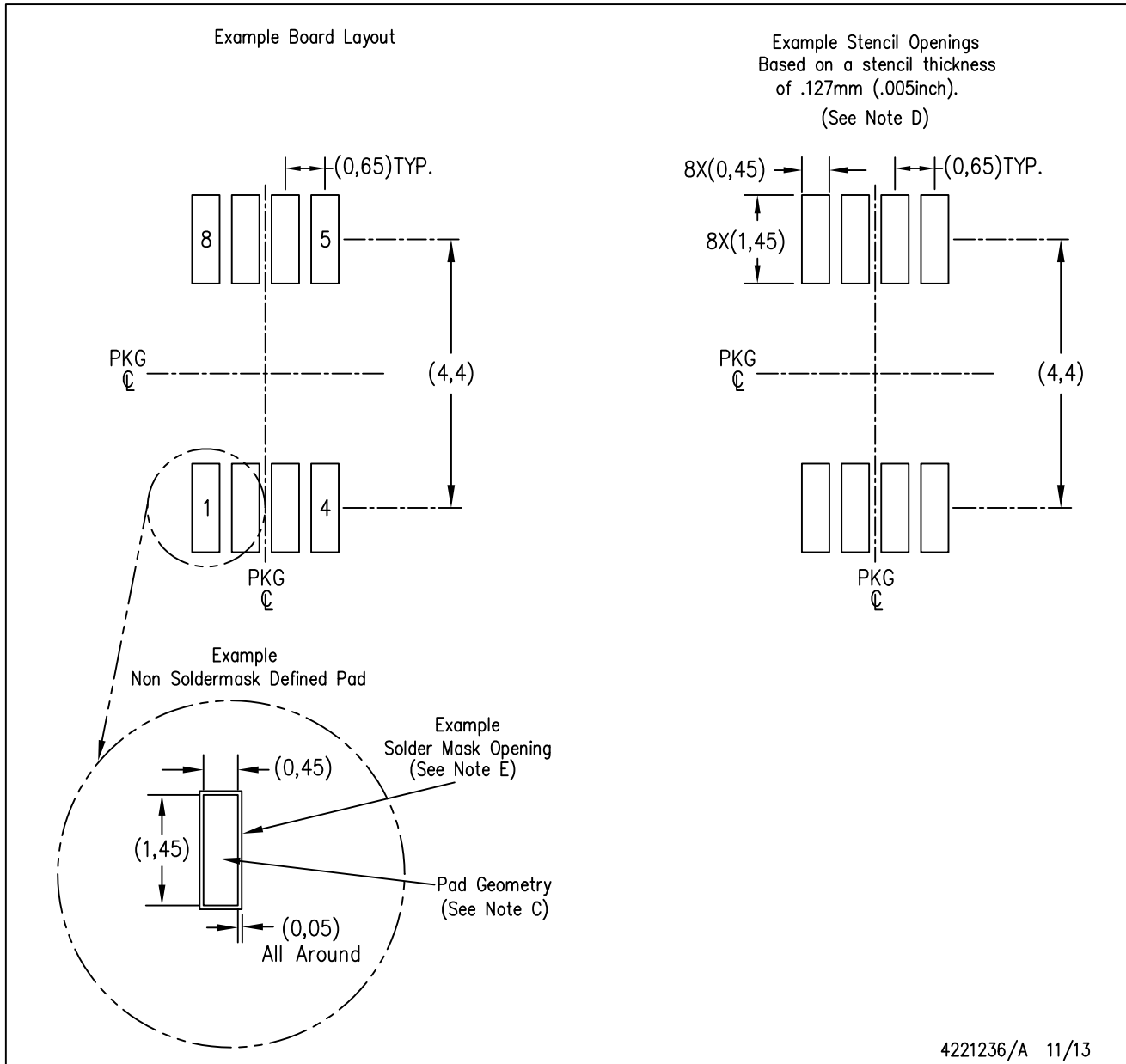


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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