

SN65HVD3x 3.3-V Full-Duplex RS-485 Drivers and Receivers

1 Features

- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Bus-Pin ESD Protection Exceeds 15-kV HBM
- Optional Driver Output Transition Times for Signaling Rates of 1 Mbps, 5 Mbps and 26 Mbps
 - Line Signaling Rate is the Number of Voltage Transitions Made per Second Expressed in Units of bps (bits per second)
- Low-Current Standby Mode: $<1\ \mu\text{A}$
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- 5-V Tolerant Inputs
- Bus Idle, Open, and Short-Circuit Failsafe
- Driver Current Limiting and Thermal Shutdown
- Designed for RS-422 and RS-485 Networks
- 5-V Devices Available, SN65HVD50-55

2 Applications

- Utility Meters
- DTE and DCE Interfaces
- Industrial, Process, and Building Automation
- Point-of-Sale (POS) Pins and Networks

3 Description

The SN65HVD3x devices are 3-state differential line drivers and differential-input line receivers that operate with 3.3-V power supply.

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for RS-422 and RS-485 data transmission over cable lengths of up to 1500 meters.

The SN65HVD30, SN65HVD31, and SN65HVD32 devices are fully enabled with no external enabling pins.

The SN65HVD33, SN65HVD34, and SN65HVD35 devices have active-high driver enables and active-low receiver enables. A low, less than $1\ \mu\text{A}$, standby current can be achieved by disabling both the driver and receiver.

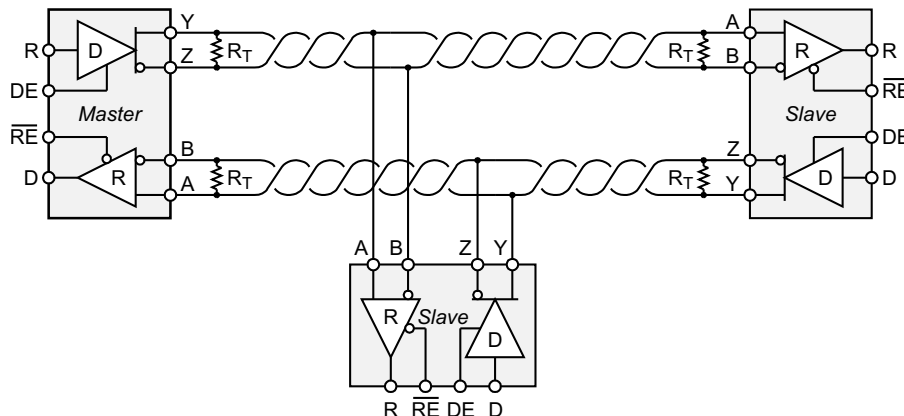
All devices are characterized for ambient temperatures from -40°C to 85°C . Low power dissipation allows operation at temperatures up to 105°C or 125°C , depending on package option.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD30	SOIC (8)	4.90 mm × 3.91 mm
SN65HVD31		
SN65HVD32		
SN65HVD33	SOIC (14)	8.65 mm × 3.91 mm
	VQFN (20)	4.50 mm × 3.50 mm
SN65HVD34	SOIC (14)	8.65 mm × 3.91 mm
SN65HVD35		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (October 2015) to Revision L	Page
• Changed text From: "defaults to Y high and Z low" To: "defaults to Y low and Z high" in the <i>Low-Power Standby Mode</i> section	20

Changes from Revision J (July 2015) to Revision K	Page
• Changed device listing in the Device Information table to match the <i>Package Option Addendum</i> listing.	1
• Changed device listing in the <i>Pinout Configuration</i> section to match the <i>Package Option Addendum</i> listing.	5
• Changed device listing in the Thermal Information table to match the <i>Package Option Addendum</i> listing.	7

Changes from Revision I (April 2010) to Revision J	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision H (May 2009) to Revision I	Page
• Changed wording of 3rd sentence of <i>Description</i>	1
• Changed the labels in the <i>SN65HVD3x Drivers Operate Correctly After Bus Contention Faults</i> image	23

Changes from Revision G (December 2008) to Revision H	Page
• Added explanatory notes for pin 6 and pin 13 to the 14-Pin SOIC	5
• Added explanatory notes for pin 1 and pin 10 to the 20-Pin VQFN	5
• Added Supply current typical value of 3.8 mA for SN65HVD31, SN65HVD3 in the <i>Supply Current Characteristics</i> table .	10
• Changed characteristic graph for Figure 6	12
• Changed characteristic graph for Figure 7	12
• Added subsection <i>Safe Operation With Bus Contention</i>	22

Changes from Revision F (July 2008) to Revision G	Page
• Changed From: 5-V Devices Available, SN65HVD50-59 To: 5-V Devices Available, SN65HVD50-55 in the <i>Features</i>	1
• Deleted SN65HVD36 and SN65HVD37 from the <i>Description</i>	1
• Deleted SN65HVD38 and SN65HVD39 from the <i>Description</i>	1
• Deleted last 2 paragraphs of <i>Description</i>	1
• Deleted SN65HVD36, SN65HVD37 from the 8-Pin SOIC	5
• Deleted SN65HVD36, SN65HVD37 from the the 14-Pin SOIC	5
• Deleted devices SN65HVD36, SN65HVD38 from the <i>Recommended Operating Conditions</i>	7
• Deleted devices SN65HVD37, SN65HVD39 from the <i>Recommended Operating Conditions</i>	7
• Deleted all HVD36, HVD38, HVD37, HVD39 from the <i>Electrical Characteristics: Driver</i> table	8
• Added added last sentence to note 4 in the <i>Electrical Characteristics: Driver</i> table	8
• Deleted all HVD36, HVD38, HVD37, HVD39 from the <i>Electrical Characteristics: Receiver</i> table	9
• Deleted all HVD36, HVD38, HVD37, HVD39 rows from the <i>Supply Current Characteristics</i> table	10
• Deleted all HVD36, HVD38, HVD37, HVD39 from the <i>Switching Characteristics: Driver</i> table	10
• Deleted HVD36, HVD38, HVD37, and HVD39 from the <i>Switching Characteristics: Receiver</i> table	11
• Deleted <i>Receiver Equalization Characteristics</i> table	12
• Added subsection <i>Driver Output Current Limiting</i>	21
• Added subsection <i>Hot-Plugging</i>	21
• Added subsection <i>Receiver Failsafe</i>	22
• Deleted SN65HVD38 and SN65HVD39 from Table 3 title	24
• Deleted SN65HVD38 and SN65HVD39 from Table 4 title	24
• Deleted SN65HVD36 and SN65HVD37 from Table 5 title	24
• Deleted SN65HVD36 and SN65HVD37 from Table 6 title	24
• Deleted SN65HVD36 and SN65HVD37 from first row of Table 7	25
• Deleted SN65HVD37, SN65HVD38 and SN65HVD39 from second row of Table 7	25

Changes from Revision E (March 2008) to Revision F	Page
• Changed From: Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A and RS-422 Compatible To: Designed for RS-422 and RS-485 Networks in the <i>Features</i>	1
• Added Table Note 4 in the <i>Electrical Characteristics: Driver</i> table	8

Changes from Revision D (January 2008) to Revision E	Page
• Changed spelling From: termperatures To: temperatures	1

5 Device Comparison

Table 1. Device Features

BASE PART NUMBER	SIGNALING RATE	UNIT LOADS	ENABLES
SN65HVD30	26 Mbps	1/2	No
SN65HVD31	5 Mbps	1/8	No
SN65HVD32	1 Mbps	1/8	No
SN65HVD33	26 Mbps	1/2	Yes
SN65HVD34	5 Mbps	1/8	Yes
SN65HVD35	1 Mbps	1/8	Yes

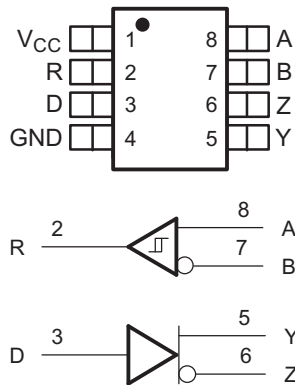
Table 2. Improved Replacement for Devices

PART NUMBER	REPLACE WITH	BENEFITS
MAX3491 MAX3490	SN65HVD33 SN65HVD30	Better ESD protection (15 kV versus 2 kV, or not specified) Higher Signaling Rate (26 Mbps versus 10 Mbps) Fractional Unit Load (64 Nodes versus 32)
MAX3491E MAX3490E	SN65HVD33 SN65HVD30	Higher Signaling Rate (26 Mbps versus 12 Mbps) Fractional Unit Load (64 Nodes versus 32)
MAX3076E MAX3077E	SN65HVD33 SN65HVD30	Higher Signaling Rate (26 Mbps versus 16 Mbps) Lower Standby Current (1 μ A versus 10 μ A)
MAX3073E MAX3074E	SN65HVD34 SN65HVD31	Higher Signaling Rate (5 Mbps versus 500 kbps) Lower Standby Current (1 μ A versus 10 μ A)
MAX3070E MAX3071E	SN65HVD35 SN65HVD32	Higher Signaling Rate (1 Mbps versus 250 kbps) Lower Standby Current (1 μ A versus 10 μ A)

6 Pin Configuration and Functions

SN65HVD30, SN65HVD31, SN65HVD32, D Package

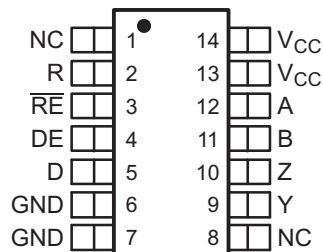
**8-Pin SOIC
Top View**



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SN65HVD33, SN65HVD34, SN65HVD35 D Package

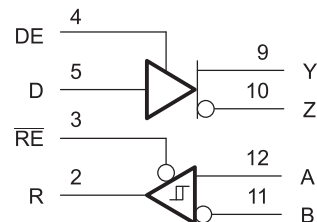
**14-Pin SOIC
Top View**



NC - No internal connection

Pins 6 and 7 are connected together internally

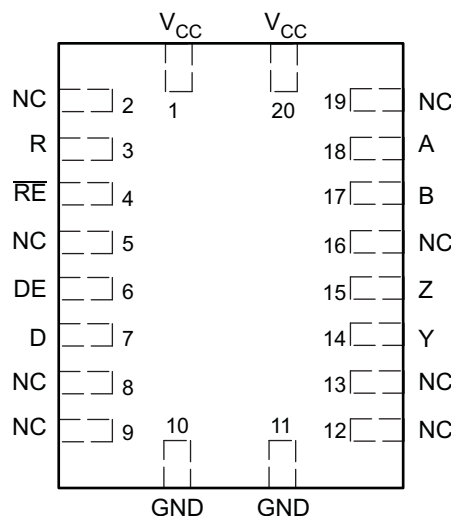
Pins 13 and 14 are connected together internally



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SN65HVD33 RHL Package

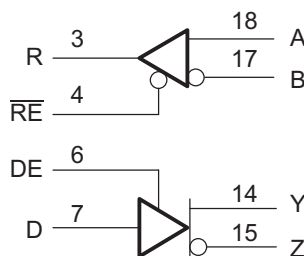
**20-Pin VQFN
Top View**



NC - No internal connection

Pins 10 and 11 are connected together internally

Pins 1 and 20 are connected together internally



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Pin Functions

PIN				TYPE	DESCRIPTION
NAME	D (8-Pins)	D (14-Pins)	RHL (20-Pins)		
A	8	12	18	Bus input	Receiver input (complementary to B)
B	7	11	17	Bus input	Receiver input (complementary to A)
D	3	5	7	Digital input	Driver data input
DE	—	4	6	Digital input	Driver enable, active high
GND	4	6, 7	10, 11	Reference potential	Local device ground
NC	—	1, 8	2, 5, 8, 9, 12, 13, 16, 19	No connect	No connect; must be left floating
R	2	2	3	Digital output	Receive data output
$\overline{RE}$	—	3	4	Digital output	Receiver enable, active low
V _{CC}	1	13, 14	1, 20	Supply	3-V to 3.6-V supply
Y	5	9	14	Bus output	Driver output (complementary to Z)
Z	6	10	15	Bus output	Driver output (complementary to Y)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
V _{CC} Supply voltage	−0.3	6	V
V _(A) , V _(B) , V _(Y) , V _(Z) Voltage at any bus terminal (A, B, Y, Z)	−9	14	V
V _(TRANS) Voltage input, transient pulse through 100 Ω. See Figure 28 (A, B, Y, Z) ⁽³⁾	−50	50	V
V _I Input voltage (D, DE, $\overline{RE}$)	−0.5	7	V
I _O Output current (receiver output only, R)		11	mA
T _{stg} Storage Temperature		125	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) This tests survivability only and the output state of the receiver is not specified.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Bus pins and GND	±16000
		All pins	±4000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3		3.6	V
V _I or V _{IC}	Voltage at any bus pin (separately or common mode)		–7 ⁽¹⁾		12	V
1/t _{UI}	Signaling rate	SN65HVD30, SN65HVD33			26	Mbps
		SN65HVD31, SN65HVD34			5	
		SN65HVD32, SN65HVD35			1	
R _L	Differential load resistance		54	60		Ω
V _{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V _{CC}	V
V _{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V _{ID}	Differential input voltage		–12		12	V
I _{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I _{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T _J	Junction temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65HVD30, SN65HVD31, SN65HVD32	SN65HVD33, SN65HVD34, SN65HVD35	SN65HVD33	UNIT
		D (SOIC)	D (SOIC)	RHL (VQFN)	
		8 PINS	14 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	135	92	73	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43	59	14	°C/W
R _{θJB}	Junction-to-board thermal resistance	44	61	13.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	12.1	5.7	0.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	49.7	30.7	13.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics: Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$V_{I(K)}$	Input clamp voltage	$I_I = -18$ mA	-1.5			V
$ V_{OD(SS)} $	Steady-state differential output voltage	$I_O = 0$	2.5		V_{CC}	V
		$R_L = 54 \Omega$, See Figure 17 (RS-485)	1.5	2		
		$R_L = 100 \Omega$, See Figure 17 , ⁽²⁾ (RS-422)	2	2.3		
		$V_{test} = -7$ V to 12 V, See Figure 18	1.5			
$\Delta V_{OD(SS)} $	Change in magnitude of steady-state differential output voltage between states	$R_L = 54 \Omega$, See Figure 17 and Figure 18	-0.2		0.2	V
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot	$R_L = 54 \Omega$, $C_L = 50$ pF, See Figure 21 and Figure 19			10% ⁽³⁾	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	SN65HVD30, SN65HVD33	See Figure 20		0.5	V
		SN65HVD31, SN65HVD34, SN65HVD32, SN65HVD35	See Figure 20		0.25	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 20	1.6		2.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See Figure 20	-0.05		0.05	V
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	SN65HVD30, SN65HVD31, SN65HVD32	$V_{CC} = 0$ V, V_Z or $V_Y = 12$ V, Other input at 0 V		90	μ A
			$V_{CC} = 0$ V, V_Z or $V_Y = -7$ V, Other input at 0 V		-10	
		SN65HVD33, SN65HVD34, SN65HVD35	$V_{CC} = 3$ V or 0 V, DE = 0 V V_Z or $V_Y = 12$ V Other input at 0 V		90	
			$V_{CC} = 3$ V or 0 V, DE = 0 V V_Z or $V_Y = -7$ V Other input at 0 V		-10	
$I_{Z(S)}$ or $I_{Y(S)}$	Short Circuit output current ⁽⁴⁾		V_Z or $V_Y = -7$ V Other input at 0 V		-250	mA
			V_Z or $V_Y = 12$ V Other input at 0 V		250	
I_I	Input current	D, DE	0		100	μ A
$C_{(OD)}$	Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V		16		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) V_{CC} is 3.3 V_{DC} ± 5%.

(3) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485.

(4) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure can affect device reliability. This applies to the SN65HVD30, SN65HVD31, SN65HVD33, and SN65HVD34.

7.6 Electrical Characteristics: Receiver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IT+}	Positive-going differential input threshold voltage	I _O = −8 mA			−0.02	V	
V _{IT−}	Negative-going differential input threshold voltage	I _O = 8 mA	−0.20			V	
V _{hys}	Hysteresis voltage (V _{IT+} − V _{IT−})			50		mV	
V _{IK}	Enable-input clamp voltage	I _I = −18 mA	−1.5			V	
V _O	Output voltage	V _{ID} = 200 mV, I _O = −8 mA, See Figure 24	2.4			V	
		V _{ID} = −200 mV, I _O = 8 mA, See Figure 24			0.4		
I _{O(Z)}	High-impedance-state output current	V _O = 0 or V _{CC} , $\overline{RE}$ at V _{CC}	−1		1	μA	
I _A or I _B	Bus input current	SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35	V _A or V _B = 12 V Other input at 0 V		0.05	0.1	mA
			V _A or V _B = 12 V, V _{CC} = 0 V Other input at 0 V		0.06	0.1	
			V _A or V _B = −7 V Other input at 0 V		−0.10	−0.04	
			V _A or V _B = −7 V, V _{CC} = 0 V Other input at 0 V		−0.10	−0.03	
	SN65HVD30, SN65HVD33	V _A or V _B = 12 V Other input at 0 V		0.20	0.35	mA	
		V _A or V _B = 12 V, V _{CC} = 0 V Other input at 0 V		0.24	0.4		
		V _A or V _B = −7 V Other input at 0 V		−0.35	−0.18		
		V _A or V _B = −7 V, V _{CC} = 0 V Other input at 0 V		−0.25	−0.13		
I _{IH}	Input current, $\overline{RE}$	V _{IH} = 0.8 V or 2 V	−60			μA	
C _{ID}	Differential input capacitance	V _{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		15		pF	

(1) All typical values are at 25°C and with a 3.3-V supply.

7.7 Device Power Dissipation – P_D

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Power Dissipation (worst case) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: SN65HVD30, SN65HVD33 at 25 Mbps, SN65HVD31, SN65HVD34 at 5 Mbps, SN65HVD32, SN65HVD35 at 1 Mbps	SN65HVD30, SN65HVD33 $V_{CC} = 3.6$ V, $T_J = 140^\circ\text{C}$, $R_L = 54 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver)			197	mW
		SN65HVD31, SN65HVD34 $V_{CC} = 3.6$ V, $T_J = 140^\circ\text{C}$, $R_L = 54 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver)			213	
		SN65HVD32, SN65HVD35 $V_{CC} = 3.6$ V, $T_J = 140^\circ\text{C}$, $R_L = 54 \Omega$, $C_L = 50$ pF (driver), $C_L = 15$ pF (receiver)			248	
T_{SD}	Thermal Shut-down Junction Temperature			170		$^\circ\text{C}$

7.8 Supply Current Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{CC} Supply current	SN65HVD30	D at 0 V or V _{CC} and No Load			2.1	mA
	SN65HVD31, SN65HVD32			3.8	6.4	
	SN65HVD33	RE at 0 V, D at 0 V or V _{CC} , DE at 0 V, No load (Receiver enabled and driver disabled)			1.8	mA
	SN65HVD34, SN65HVD35			2.2		
	SN65HVD33, SN65HVD34, SN65HVD35	RE at V _{CC} , D at V _{CC} , DE at 0 V, No load (Receiver disabled and driver disabled)		0.022	1	μA
	SN65HVD33	RE at 0 V, D at 0 V or V _{CC} , DE at V _{CC} , No load (Receiver enabled and driver enabled)			2.1	mA
	SN65HVD34, SN65HVD35			6.5		
	SN65HVD33	RE at V _{CC} , D at 0 V or V _{CC} , DE at V _{CC} No load (Receiver disabled and driver enabled)			1.8	mA
	SN65HVD34, SN65HVD35			6.2		

(1) All typical values are at 25°C and with a 3.3-V supply.

7.9 Switching Characteristics: Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	SN65HVD30, SN65HVD33	4	10	18	ns
		SN65HVD31, SN65HVD34	25	38	65	
		SN65HVD32, SN65HVD35	120	175	305	
t _{PHL}	Propagation delay time, high-to-low-level output	SN65HVD30, SN65HVD33	4	9	18	ns
		SN65HVD31, SN65HVD34	25	38	65	
		SN65HVD32, SN65HVD35	120	175	305	
t _r	Differential output signal rise time	SN65HVD30, SN65HVD33	2.5	5	12	ns
		SN65HVD31, SN65HVD34	20	37	60	
		SN65HVD32, SN65HVD35	120	185	300	
t _f	Differential output signal fall time	SN65HVD30, SN65HVD33	2.5	5	12	ns
		SN65HVD31, SN65HVD34	20	35	60	
		SN65HVD32, SN65HVD35	120	180	300	
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})	SN65HVD30, SN65HVD33	0.6			ns
		SN65HVD31, SN65HVD34	2.0			
		SN65HVD32, SN65HVD35	5.1			

R_L = 54 Ω, C_L = 50 pF,
See [Figure 21](#)

(1) All typical values are at 25°C and with a 3.3-V supply.

Switching Characteristics: Driver (continued)

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	SN65HVD33			45	ns
		SN65HVD34			235	
		SN65HVD35			490	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	SN65HVD33			25	ns
		SN65HVD34			65	
		SN65HVD35			165	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	SN65HVD33			35	ns
		SN65HVD34			190	
		SN65HVD35			490	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	SN65HVD33			30	ns
		SN65HVD34			120	
		SN65HVD35			290	
t_{PZH1}, t_{PZL1}	Driver enable delay with bus voltage offset	$V_O = 2\text{ V (Typ)}$		500	900	ns
t_{PZH2}	Propagation delay time, standby-to-high-level output	$R_L = 110\ \Omega, \overline{RE}$ at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See Figure 22			4000	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output	$R_L = 110\ \Omega, \overline{RE}$ at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See Figure 23			4000	ns

7.10 Switching Characteristics: Receiver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	SN65HVD30, SN65HVD33		26	45	ns
		SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35		47	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output	SN65HVD30, SN65HVD33		29	45	ns
		SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35		49	70	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)	SN65HVD30, SN65HVD33			7	ns
		SN65HVD31, SN65HVD34, SN65HVD32, SN65HVD35			10	ns
t_r	Output signal rise time				5	ns
t_f	Output signal fall time				6	ns
t_{PHZ}	Output disable time from high level	DE at 3 V			20	ns
t_{PZH1}	Output enable time to high level	DE at 3 V			20	ns
t_{PZH2}	Propagation delay time, standby-to-high-level output	DE at 0 V			4000	ns
t_{PLZ}	Output disable time from low level	DE at 3 V			20	ns
t_{PZL1}	Output enable time to low level	DE at 3 V			20	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output	DE at 0 V			4000	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

7.11 Dissipation Ratings

PACKAGE	JEDEC THERMAL MODEL	$T_A < 25^\circ\text{C}$ RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ RATING	$T_A = 105^\circ\text{C}$ RATING	$T_A = 125^\circ\text{C}$ RATING
8-pin D (SOIC)	Low k	625 mW	5 mW/ $^\circ\text{C}$	325 mW		
	High k	1000 mW	8 mW/ $^\circ\text{C}$	520 mW	360 mW	
14-pin D (SOIC)	Low k	765 mW	6.1 mW/ $^\circ\text{C}$	400 mW	275 mW	
	High k	1350 mW	10.8 mW/ $^\circ\text{C}$	705 mW	485 mW	270 mW
20-pin RHL (VQFN)	High k	1710 mW	13.7 mW/ $^\circ\text{C}$	890 mW	6150 mW	340 mW

7.12 Typical Characteristics

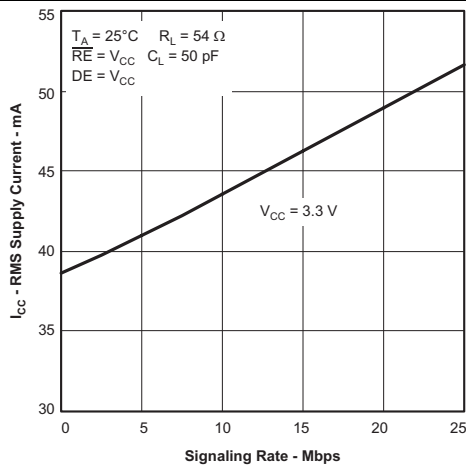


Figure 1. SN65HVD30, SN65HVD33
RMS Supply Current vs Signaling Rate

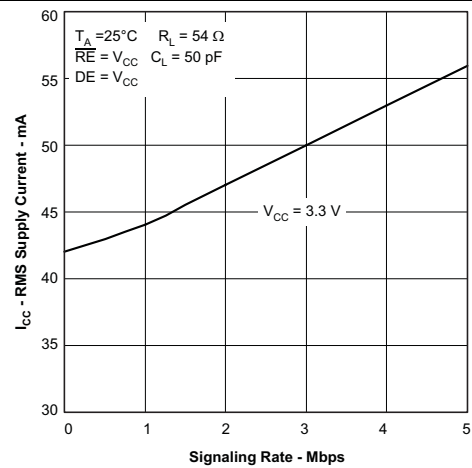


Figure 2. SN65HVD31, SN65HVD34
RMS Supply Current vs Signaling Rate

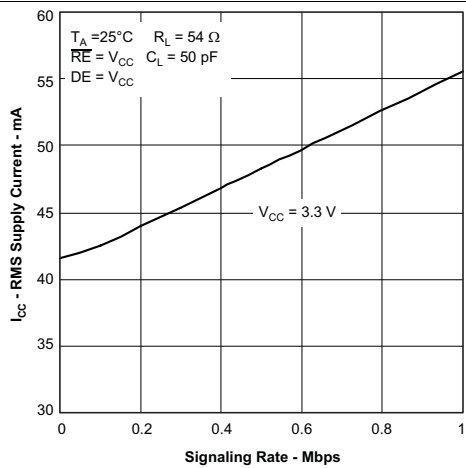


Figure 3. SN65HVD32, SN65HVD35
RMS Supply Current vs Signaling Rate

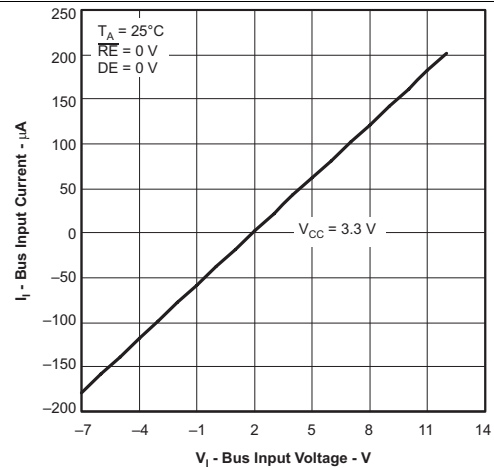
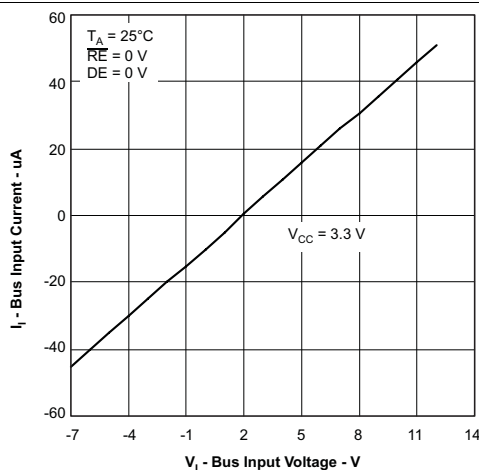


Figure 4. SN65HVD30, SN65HVD33
Bus Input Current vs Input Voltage

Typical Characteristics (continued)



**Figure 5. SN65HVD31, SN65HVD32, SN65HVD34,
SN65HVD35**
Bus Input Current vs Input Voltage

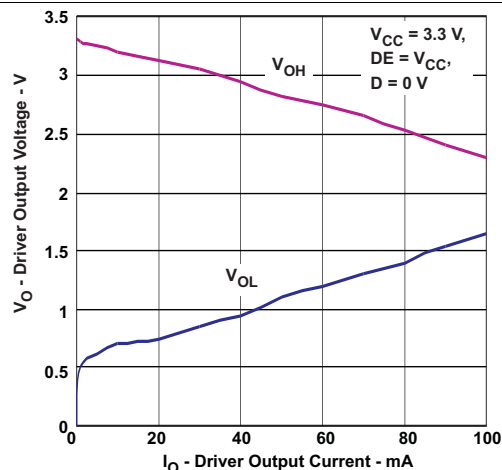
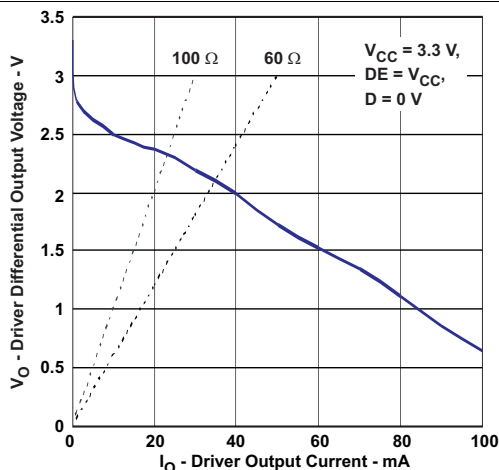
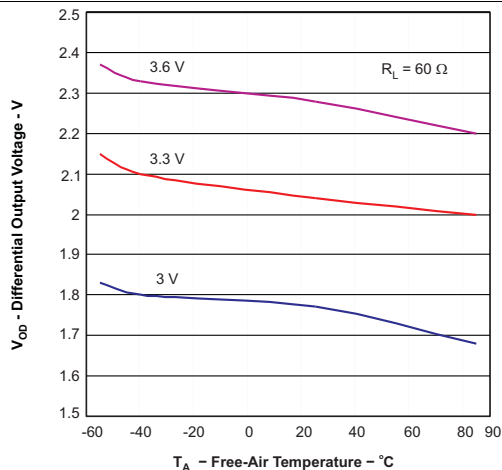


Figure 6. Driver Output Voltage vs Driver Output Current



**Figure 7. Driver Differential Output Voltage
vs Driver Output Current**



**Figure 8. Driver Differential Output Voltage
vs Free-Air Temperature**

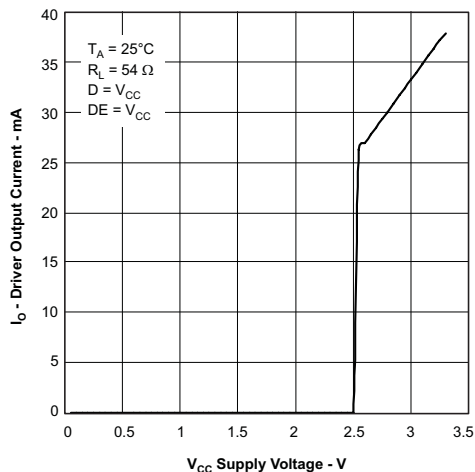


Figure 9. Driver Output Current vs Supply Voltage

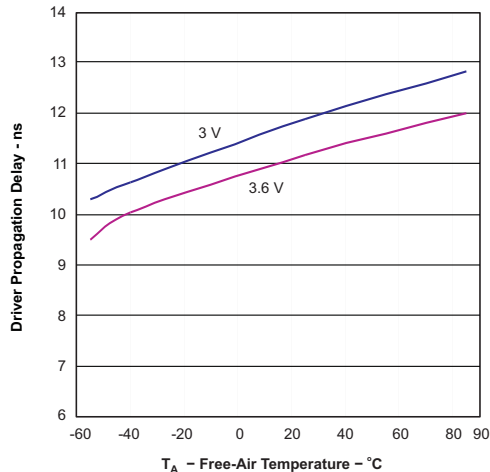


Figure 10. SN65HVD30, SN65HVD33
Driver Propagation Delay vs Free-Air Temperature

Typical Characteristics (continued)

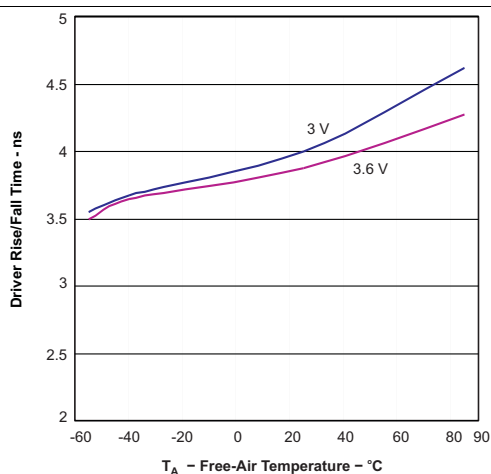


Figure 11. SN65HVD30, SN65HVD33
Driver Rise and Fall Time vs Free-Air Temperature

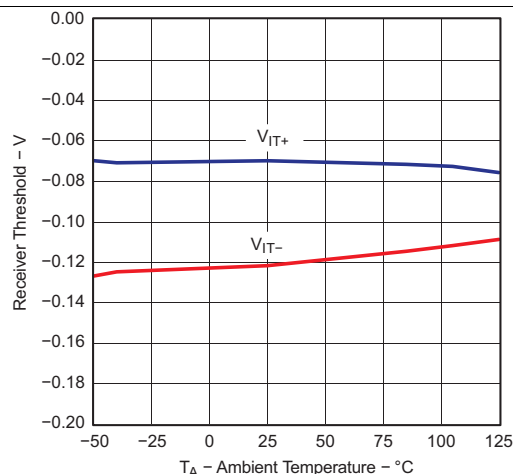


Figure 12. Receiver Threshold vs Ambient Temperature

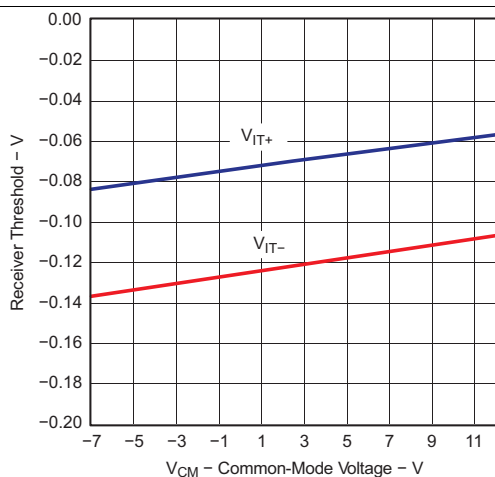


Figure 13. Receiver Threshold vs Common-Mode Voltage

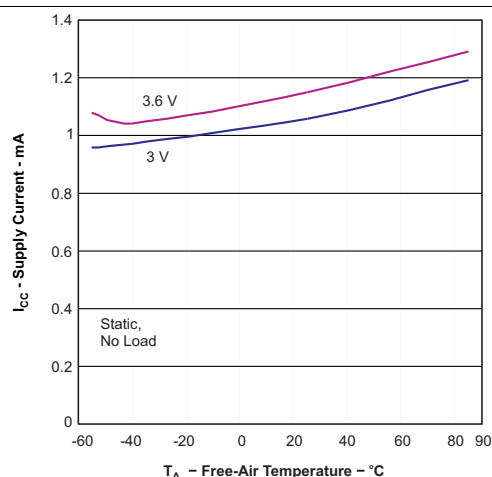


Figure 14. Supply Current vs Free-Air Temperature

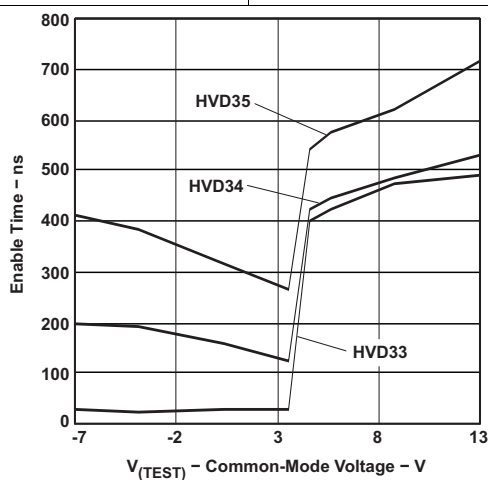
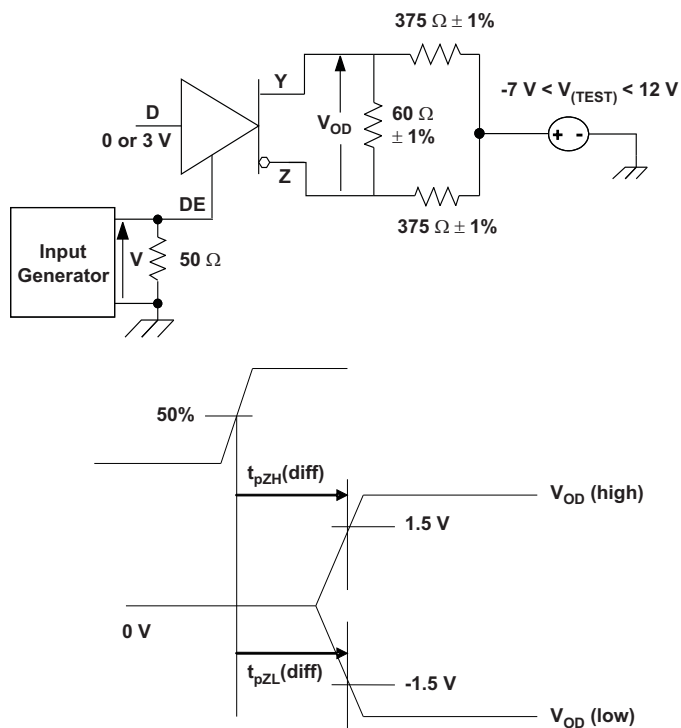


Figure 15. Enable Time vs Common-Mode Voltage
(see Figure 16)

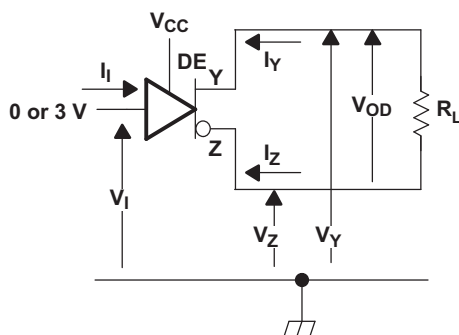
8 Parameter Measurement Information



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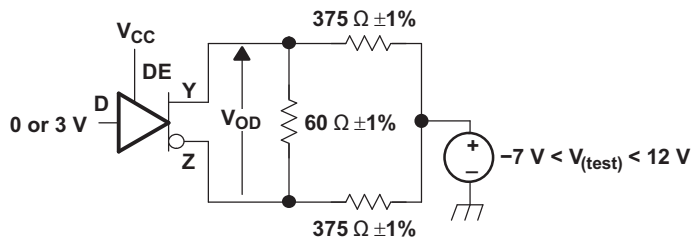
The time $t_{pZL(x)}$ is the measure from DE to $V_{OD(x)}$. V_{OD} is valid when it is greater than 1.5 V.

Figure 16. Driver Enable Time From DE to V_{OD}



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Figure 17. Driver V_{OD} Test Circuit and Voltage and Current Definitions



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Figure 18. Driver V_{OD} With Common-Mode Loading Test Circuit

Parameter Measurement Information (continued)

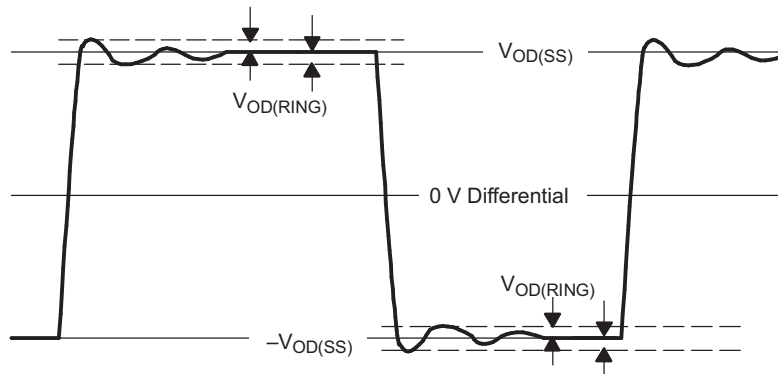
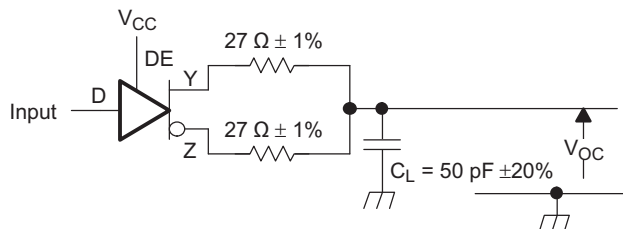


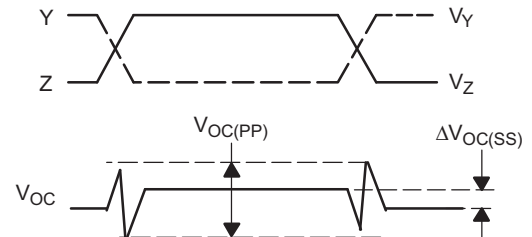
Figure 19. $V_{OD(RING)}$ Waveform and Definitions

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.



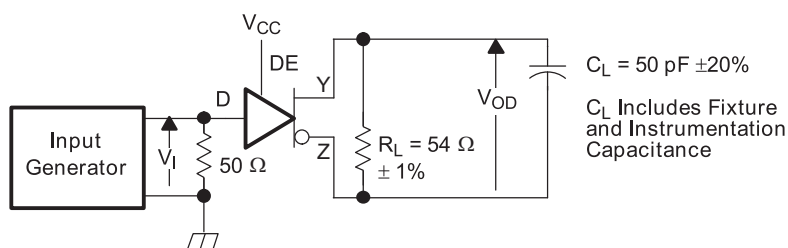
C_L Includes Fixture and Instrumentation Capacitance

Input: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6\text{ ns}$, $t_f < 6\text{ ns}$, $Z_O = 50\ \Omega$

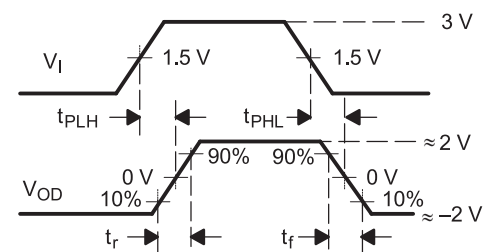


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Figure 20. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6\text{ ns}$, $t_f < 6\text{ ns}$, $Z_O = 50\ \Omega$



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Figure 21. Driver Switching Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

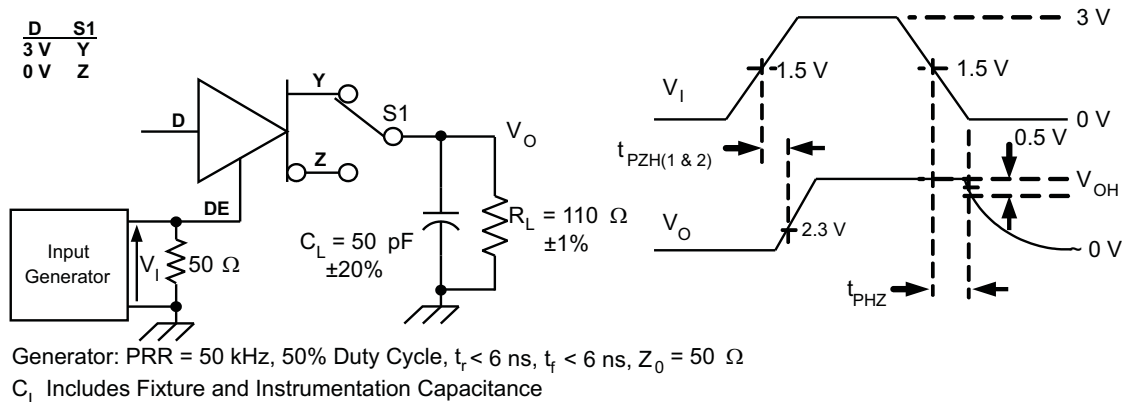
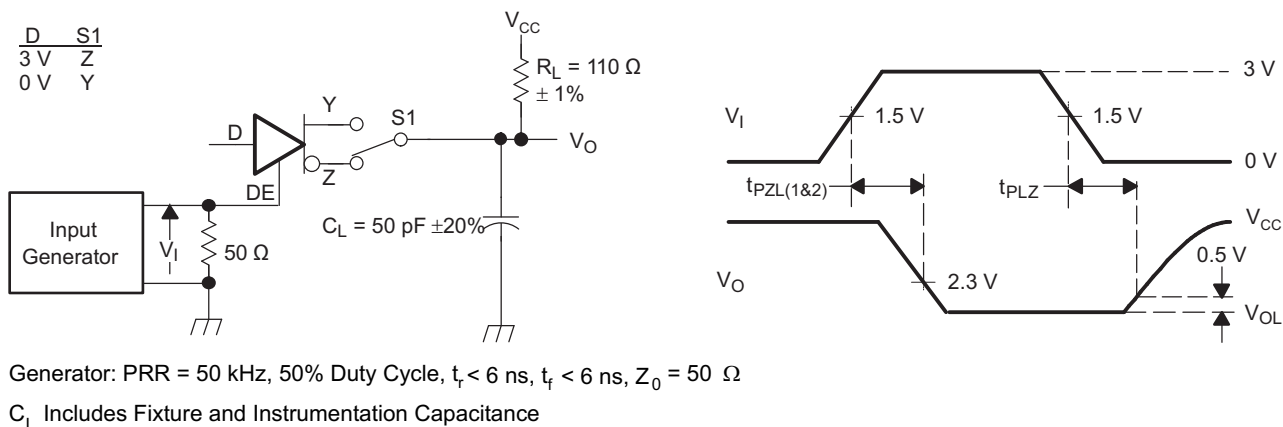
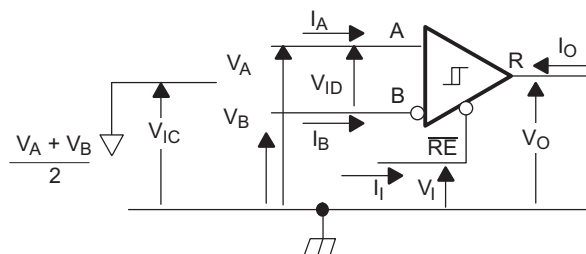


Figure 22. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



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Figure 23. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



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Figure 24. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)

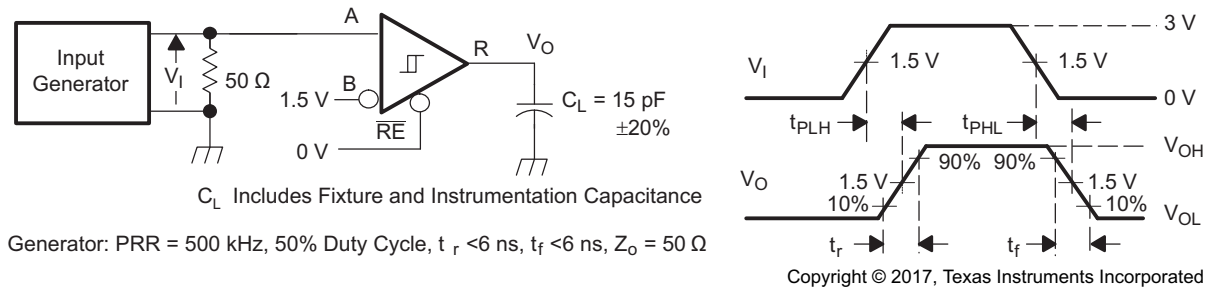


Figure 25. Receiver Switching Test Circuit and Voltage Waveforms

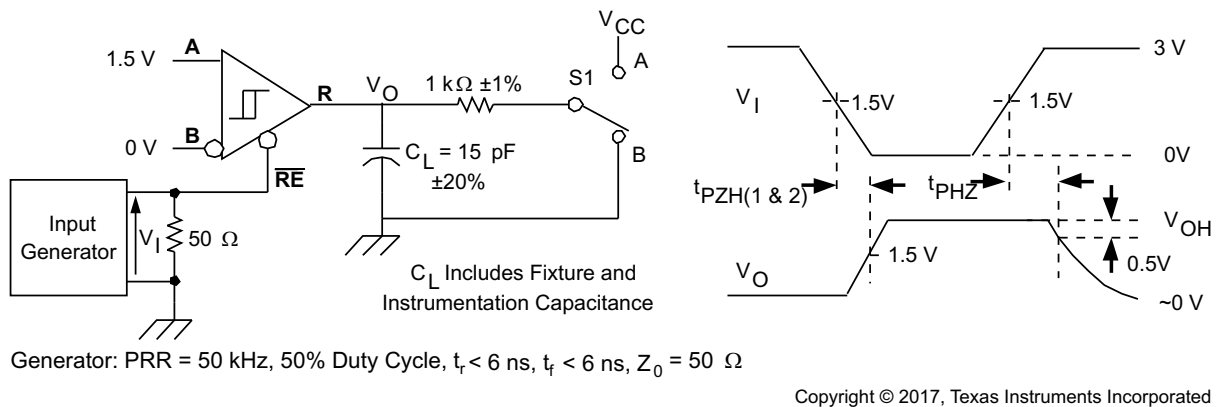


Figure 26. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

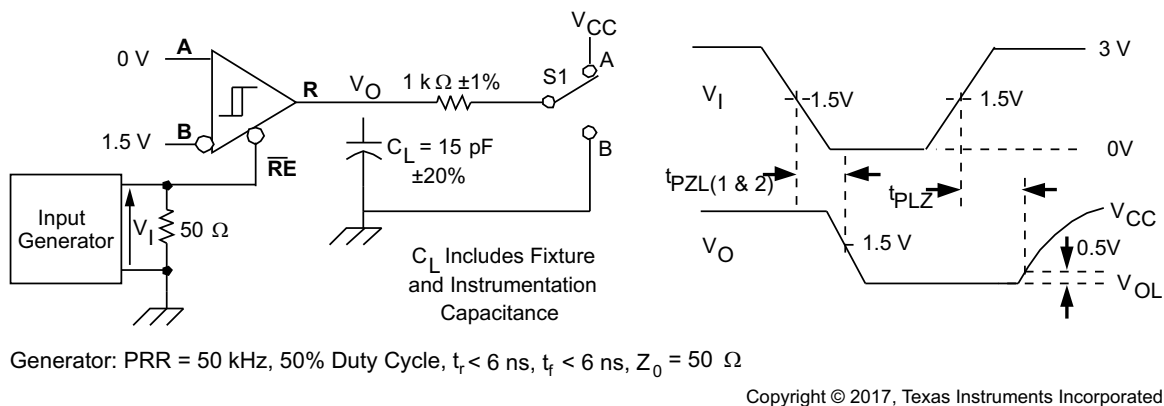
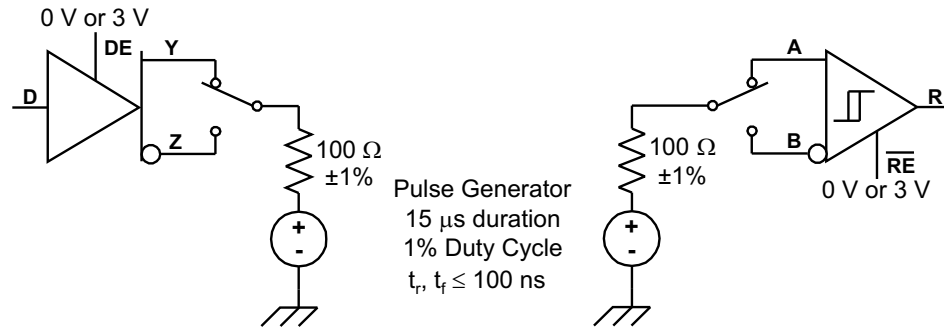


Figure 27. Receiver Enable Time From Standby (Driver Disabled)

Parameter Measurement Information (continued)



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Figure 28. Test Circuit, Transient Over Voltage Test

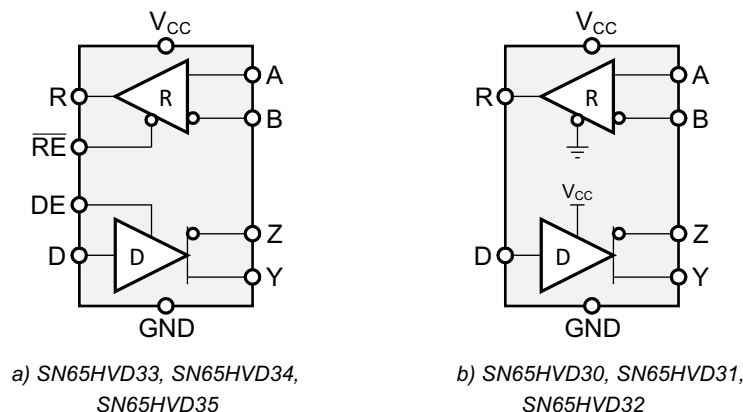
9 Detailed Description

9.1 Overview

The SN65HVD3x devices are low-power, full-duplex RS-485 transceivers available in three speed grades suitable for data transmission of 1 Mbps, 5 Mbps, and 50 Mbps.

The SN65HVD30, SN65HVD31, and SN65HVD32 devices are fully enabled with no external enabling pins. The SN65HVD33, SN65HVD34, and SN65HVD35 devices have active-high driver enables and active-low receiver enables. A standby current of less than 1 μ A can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram

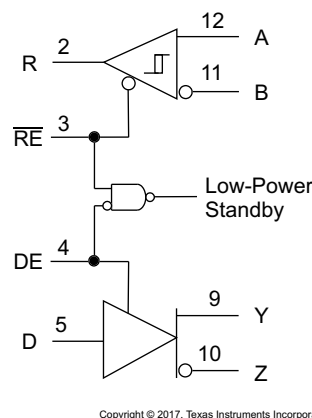


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9.3 Feature Description

9.3.1 Low-Power Standby Mode

When both the driver and receiver are disabled (DE is low and $\overline{RE}$ is high), the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver or receiver enabling. The device in standby mode only when the enable inputs are held in this state for 300 ns or more. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.



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Figure 29. Low-Power Standby Logic Diagram

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver output defaults to Y low and Z high, in accordance with the driver-failsafe feature.

Feature Description (continued)

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

9.3.2 Driver Output Current Limiting

The RS-485 standard (ANSI/TIA/EIA-485-A or equivalently ISO 8482) specifies a 250-mA driver output current limit to prevent damage caused by data contention on the bus. That applies in the event that two or more transceivers drive the bus to opposing states at the same time. The SN65HVD3x family of devices includes current-limiting circuitry that prevents damage under these conditions.

NOTE

This current limit prevents damage during the bus contention, but the logic state of the bus can be indeterminate as specified by the standard, so communication errors can occur.

In a specific combination of circumstances, a condition can occur in which current through the bus pin exceeds the 250-mA limit. This combination of conditions is not normally included in RS-485 applications:

- Loading capacitance on the pin is less than 500 pF
- The bus pin is directly connected to a voltage more negative than –1 V
- The device is supplied with V_{CC} equal to or greater than 3.3 V
- The driver is enabled
- The bus pin is driving to the logic high state

In these specific conditions, the normal current-limit circuitry and thermal-shutdown circuitry does not limit or shutdown the current flow. If the current is allowed to continue, the device heats up in a localized area near the driver outputs, and the device can be damaged.

Typical RS-485 twisted-pair cable has a capacitance of approximately 50 pF/meter. Therefore, it is expected that 10 meters of cable can provide sufficient capacitance to prevent this latch-up condition.

The –7 to +12-V common mode range specified by RS-485 is intended to allow communication between transceivers separated by significant distances when ground offsets may occur due to temporary current surges, electrical noise, and so on. Under those circumstances, the inherent cable needed to connect separated transceivers ensures that the conditions previously listed do not occur. For a transceiver separated by only a short cable length or backplane applications, it is unusual for there to be a steady-state negative common-mode voltage. It is possible for a negative power supply to be shorted to the bus lines due to miswiring or cable damage; however, this is a different root cause fault, and robust devices such as the SN65HVD178x family should be used for surviving power supply or miswiring faults.

The 250-mA current limit in the RS-485 standard is intended to prevent damage caused by data contention on the bus; that is, in the event that two or more transceivers drive the bus to different states at the same time. These devices are not damaged under these conditions because all RS-485 drivers have output impedance sufficient to prevent the direct connection condition stated previously. Typical RS-485 driver output impedance is on the order of 10 Ω to 30 Ω .

9.3.3 Hot-Plugging

These devices are designed to operate in *hot swap* or *hot pluggable* applications. Key features for hot-pluggable applications are:

- Power-up
- Power-down glitch-free operation
- Default disabled input/output pins
- Receiver failsafe

Feature Description (continued)

As shown in [Figure 9](#), an internal power-on reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device reliably operates. This ensures that no spurious bits are transmitted on the bus pin outputs as the power supply turns on or turns off.

As shown in the [Device Functional Modes](#), the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device neither drives the bus nor reports data on the R pin until the associated controller actively drives the enable pins.

9.3.4 Receiver Failsafe

The differential receivers of the SN65HVD3x family are failsafe to invalid bus states caused by:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} , V_{IT-} , and V_{HYS} (the separation between V_{IT+} and V_{IT-}). As shown in the [Electrical Characteristics](#) table, differential signals more negative than –200 mV always cause a low receiver output, and differential signals more positive than 200 mV always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{IT+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value (V_{HYS}) as well as the value of V_{IT+} .

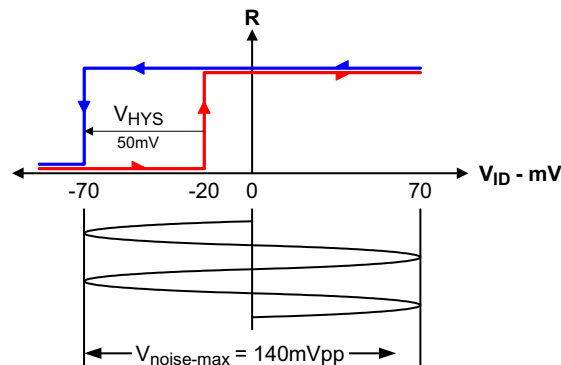


Figure 30. SN65HVD30-35 Noise Immunity Under Bus Fault Conditions

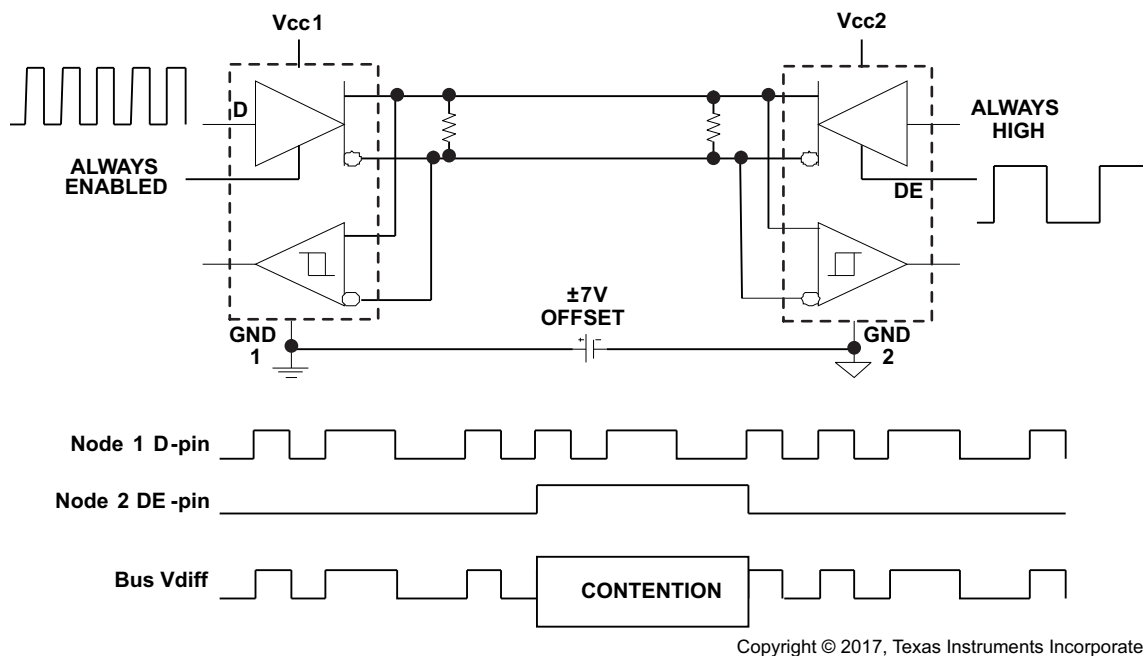
9.3.5 Safe Operation With Bus Contention

These devices incorporate a driver current limit of 250 mA across the RS-485 common-mode range of –7 V to +12 V. As stated in the *Application Guidelines for TIA/EIA-485-A* ⁽¹⁾, this sets a practical limitation to prevent damage during bus contention events. Contention can occur during system initialization, during system faults, or whenever two or more drivers are active at the same time.

(1) TIA/EIA Telecommunications System Bulletin TSB89, *Application Guidelines for TIA/EIA-485-A*

Feature Description (continued)

Figure 31 shows a 2-node system to demonstrate bus contention by forcing both drivers to be active in opposing states.



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Figure 31. Bus Contention Example

Figure 32 shows typical operation in a bus contention event. The bottom trace illustrates how the SN65HVD33 device at Node 1 continues normal operation after a contention event between the two drivers with a –7-V ground offset on Node 2. This illustrates how the SN65HVD3x family of devices operates robustly in spite of bus contention faults, even with large common-mode offsets.

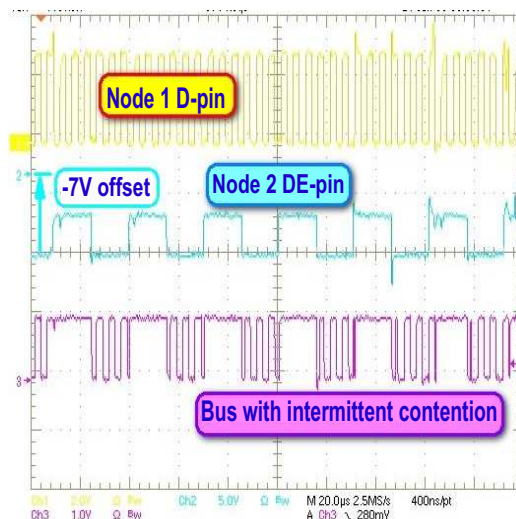


Figure 32. SN65HVD3x Drivers Operate Correctly After Bus Contention Faults

9.4 Device Functional Modes

Table 3. SN65HVD33, SN65HVD34, SN65HVD35 Driver

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

Table 4. SN65HVD33, SN65HVD34, SN65HVD35 Receiver

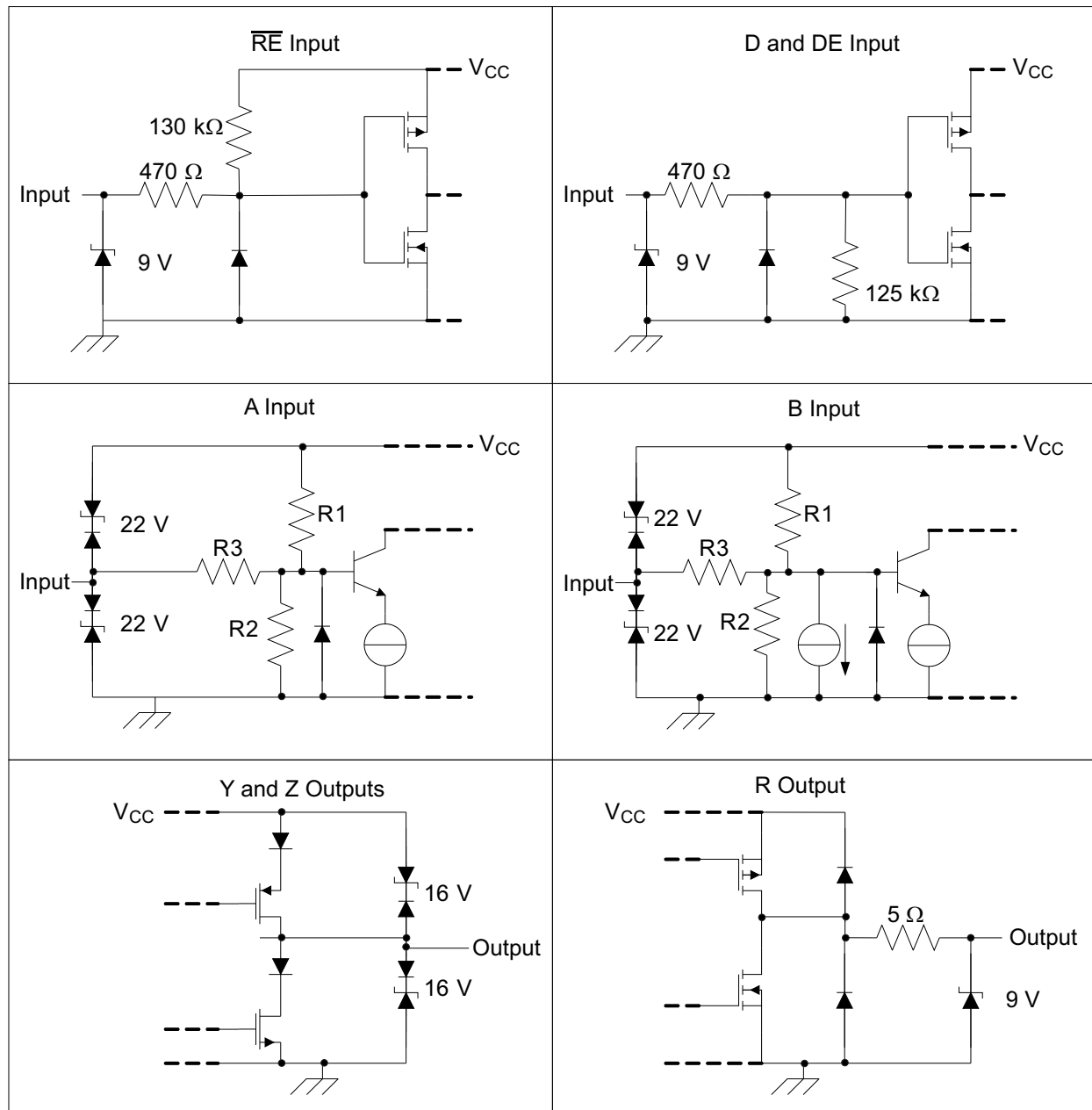
DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE RE	OUTPUT R
$V_{ID} \leq -0.2 \text{ V}$	L	L
$-0.2 \text{ V} < V_{ID} < -0.02 \text{ V}$	L	?
$-0.02 \text{ V} \leq V_{ID}$	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_{(A)} = V_{(B)}$	L	H

Table 5. SN65HVD30, SN65HVD31, SN65HVD32 Driver

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

Table 6. SN65HVD30, SN65HVD31, SN65HVD32 Receiver

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.2 \text{ V}$	L
$-0.2 \text{ V} < V_{ID} < -0.02 \text{ V}$	?
$-0.02 \text{ V} \leq V_{ID}$	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_{(A)} = V_{(B)}$	H



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Figure 33. Equivalent Input and Output Schematic Diagrams

Table 7. Input Attenuator Resistance Values

PART NUMBER	R1, R2	R3
SN65HVD30, SN65HVD33	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35	36 kΩ	180 kΩ

10 Application and Implementation

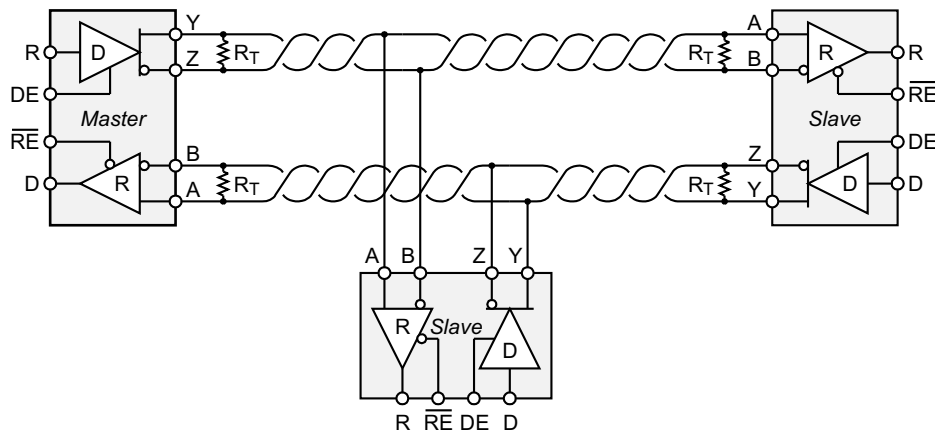
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD3x family consists of full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.



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Figure 34. Typical RS-485 Network With Full-Duplex Transceivers

10.2 Typical Application

A full-duplex RS-485 network consists of multiple transceivers connecting in parallel to two bus cables. On one signal pair, a master driver transmits data to multiple slave receivers. The master driver and slave receivers can remain fully enabled at all times. On the other signal pair, multiple slave drivers transmit data to the master receiver. To avoid bus contention, the slave drivers must be intermittently enabled and disabled such that only one driver is enabled at any time, as in half-duplex communication. The master receiver can remain fully enabled at all times.

Because the driver cannot be disabled, only connect one driver to the bus when using the SN65HVD30, SN65HVD31, or SN65HVD32 devices.

Typical Application (continued)

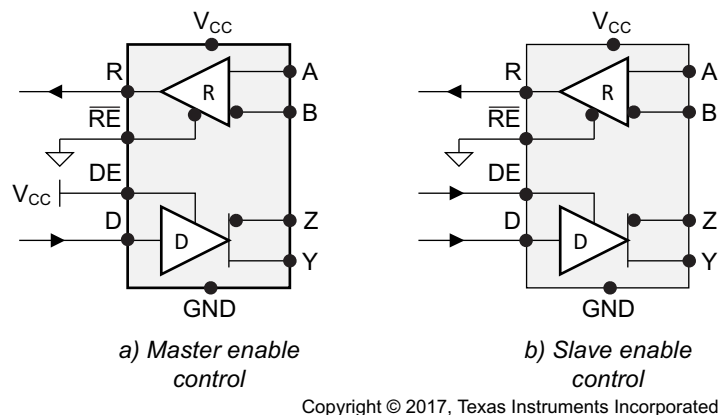


Figure 35. Full-Duplex Transceiver Configurations

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable can be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

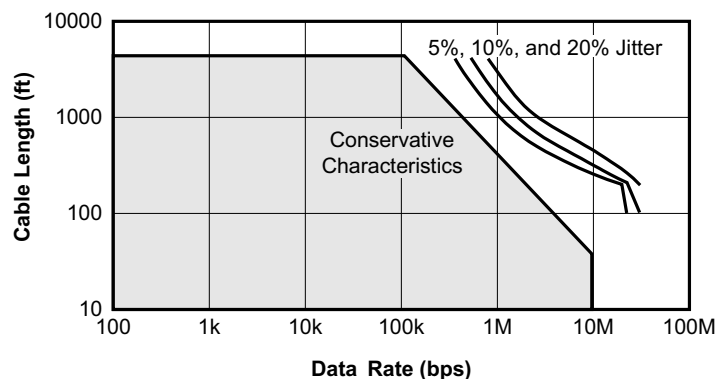


Figure 36. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (such as 26 Mbps for the SN65HVD30 and SN65HVD33 devices) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

Typical Application (continued)

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in [Equation 1](#).

$$L_{\text{stub}} \leq 0.1 \times t_r \times v \times c$$

where:

- t_r is the 10/90 rise time of the driver
 - c is the speed of light (3×10^8 m/s)
 - v is the signal velocity of the cable or trace as a factor of c
- (1)

Per [Equation 1](#), [Table 8](#) shows the maximum cable-stub lengths for the minimum driver output rise times of the SN65HVD3x full-duplex family of transceivers for a signal velocity of 78%.

Table 8. Maximum Stub Length

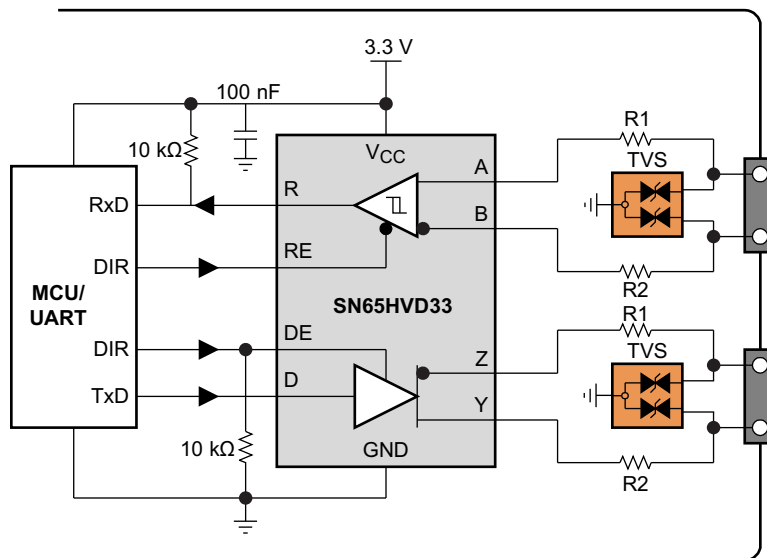
DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD30	4	0.1	0.3
SN65HVD31	25	0.6	1.9
SN65HVD32	120	2.8	9.2
SN65HVD33	4	0.1	0.3
SN65HVD34	25	0.6	1.9
SN65HVD35	120	2.8	9.2

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD30 and SN65HVD33 devices are 1/2 UL transceivers, it is possible to connect up to 64 receivers to the bus. Likewise, the SN65HVD31, SN65HVD32, SN65HVD34, and SN65HVD35 devices are 1/8 UL transceivers that can support up to 256 receivers.

10.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary (see Figure 37).



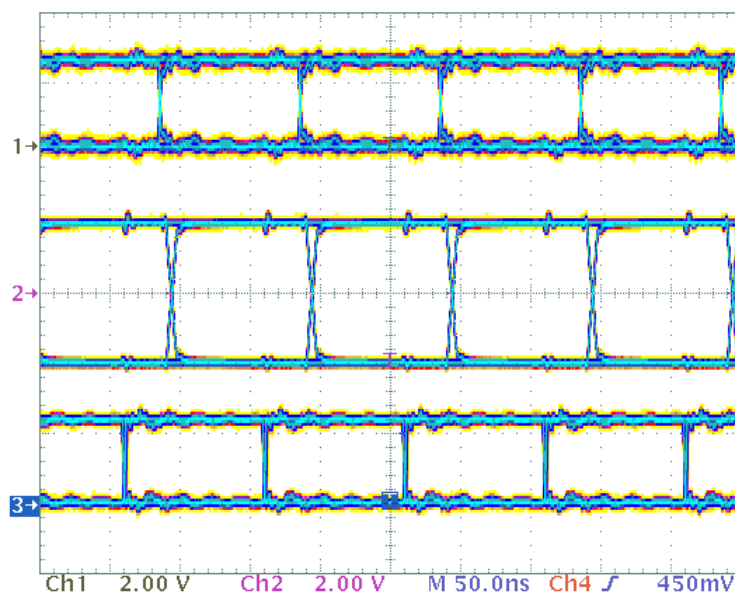
Copyright © 2017, Texas Instruments Incorporated

Figure 37. Transient Protection Against ESD, EFT, and Surge Transients

Table 9. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V Full-Duplex RS-485 Transceiver	SN65HVD33	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW060310RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns

10.2.3 Application Curve



Signals from top to bottom: D, Y, Z, VOD

Figure 38. SN65HVD33 Transient Waveform

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps compensate for the resistance and inductance of the PCB power planes.

12 Layout

12.1 Layout Guidelines

Robust and reliable bus-node design often requires the use of external transient protection devices to protect against EFT and surge transients that can occur in industrial environments. Because these transients have a wide frequency bandwidth (from approximately 3 MHz to 3 GHz), high-frequency layout techniques must be applied during PCB design.

- Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
- Use 1-k Ω to 10-k Ω pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs), which reduces the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to 200 mA.

12.2 Layout Example

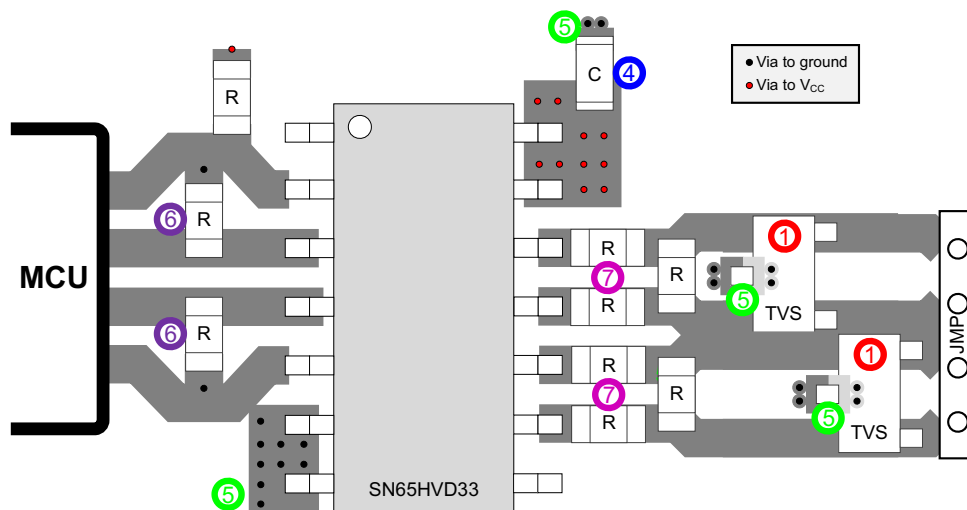


Figure 39. SN65HVD33 Layout Example

13 Device and Documentation Support

13.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD30	Click here	Click here	Click here	Click here	Click here
SN65HVD31	Click here	Click here	Click here	Click here	Click here
SN65HVD32	Click here	Click here	Click here	Click here	Click here
SN65HVD33	Click here	Click here	Click here	Click here	Click here
SN65HVD34	Click here	Click here	Click here	Click here	Click here
SN65HVD35	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
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13.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD30D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD30DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD30DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD30DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD31D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP31	Samples
SN65HVD31DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP31	Samples
SN65HVD31DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP31	Samples
SN65HVD32D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP32	Samples
SN65HVD32DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP32	Samples
SN65HVD32DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP32	Samples
SN65HVD33D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33RHLR	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33	Samples
SN65HVD33RHLT	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33	Samples
SN65HVD34D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD34DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD34DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD35D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD35DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples
SN65HVD35DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples
SN65HVD35DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65HVD30, SN65HVD33 :

- Enhanced Product : [SN65HVD30-EP](#), [SN65HVD33-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD31DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD32DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD33DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD33RHRLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN65HVD33RHRLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN65HVD34DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD35DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

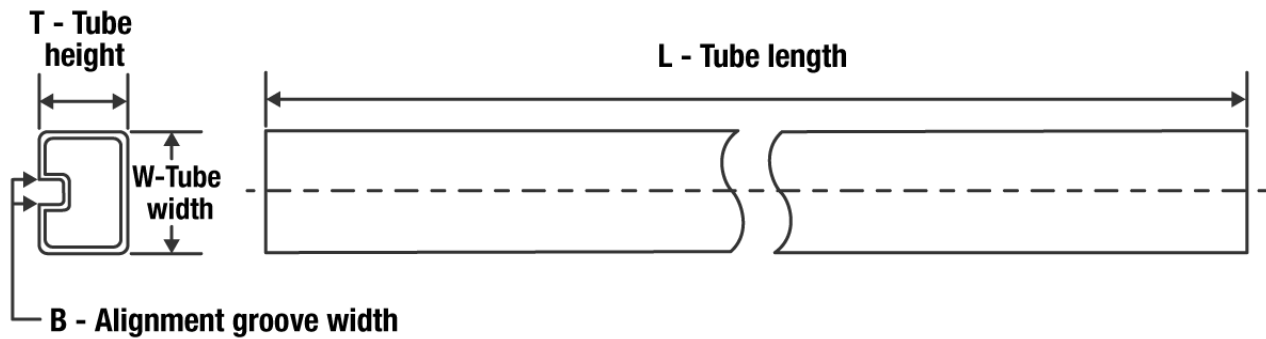
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD30DR	SOIC	D	8	2500	853.0	449.0	35.0
SN65HVD31DR	SOIC	D	8	2500	853.0	449.0	35.0
SN65HVD32DR	SOIC	D	8	2500	853.0	449.0	35.0
SN65HVD33DR	SOIC	D	14	2500	853.0	449.0	35.0
SN65HVD33RHRLR	VQFN	RHL	20	3000	853.0	449.0	35.0
SN65HVD33RHRLT	VQFN	RHL	20	250	210.0	185.0	35.0
SN65HVD34DR	SOIC	D	14	2500	350.0	350.0	43.0
SN65HVD35DR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65HVD30D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD30DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD31D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD31DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD32D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD32DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD33D	D	SOIC	14	50	505.46	6.76	3810	4
SN65HVD33D	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD33DG4	D	SOIC	14	50	505.46	6.76	3810	4
SN65HVD33DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD34D	D	SOIC	14	50	505.46	6.76	3810	4
SN65HVD34DG4	D	SOIC	14	50	505.46	6.76	3810	4
SN65HVD35D	D	SOIC	14	50	505.46	6.76	3810	4
SN65HVD35DG4	D	SOIC	14	50	505.46	6.76	3810	4

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

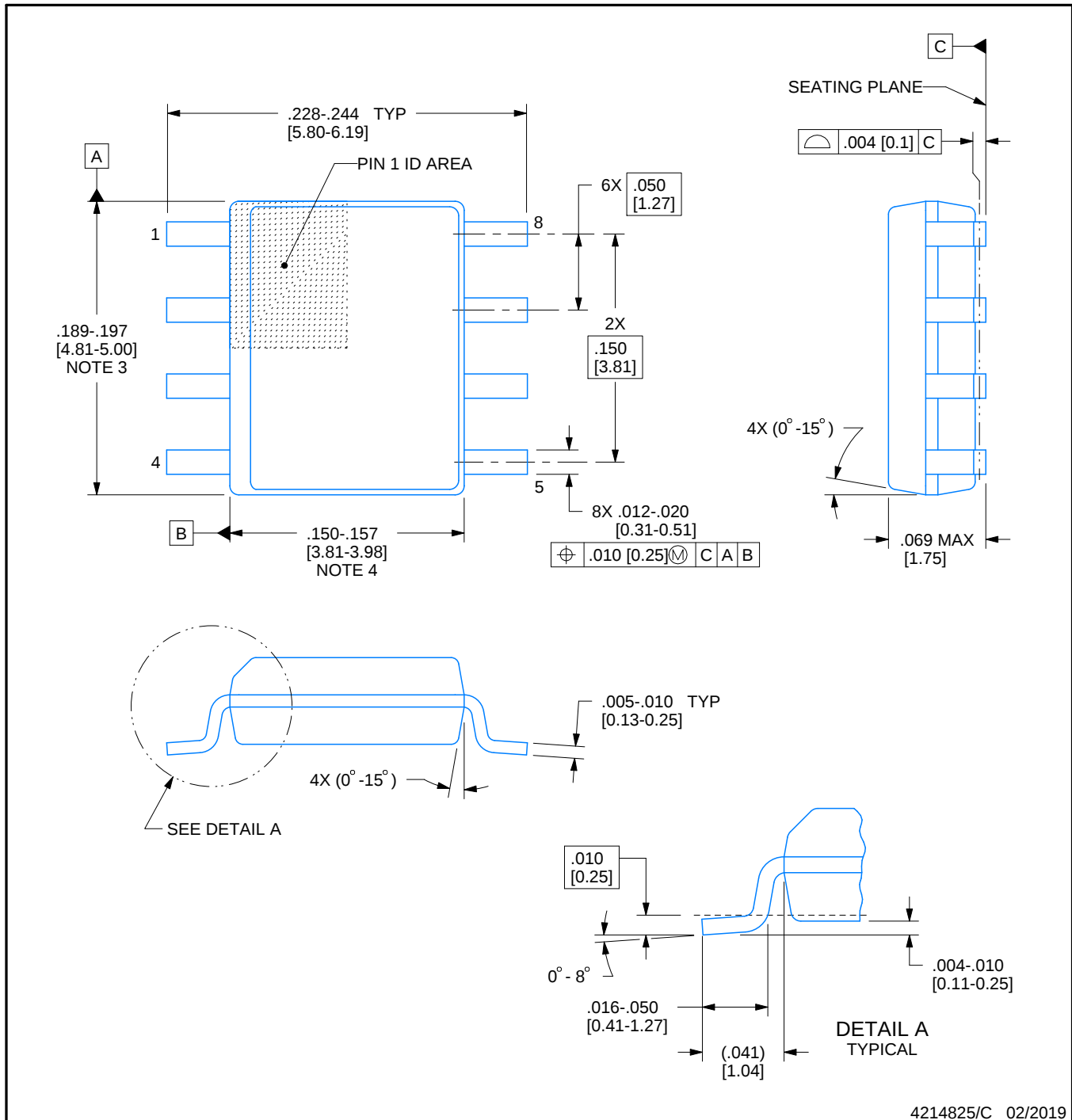


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

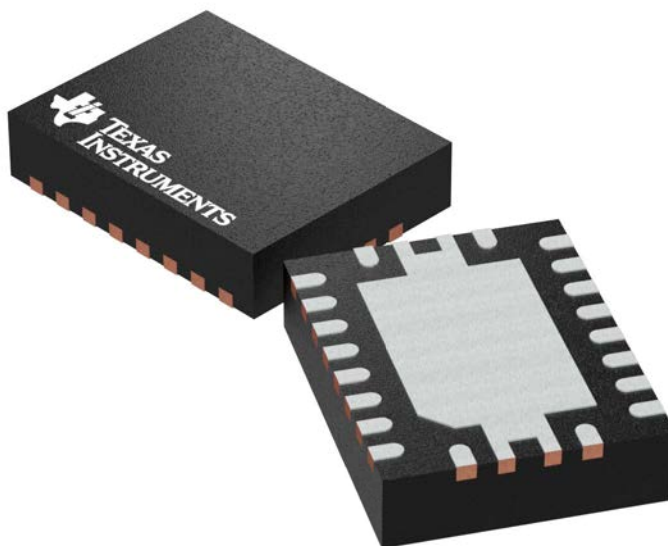
GENERIC PACKAGE VIEW

RHL 20

VQFN - 1 mm max height

3.5 x 4.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205346/L

VQFN - 1 mm max height

[illegible]

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

VQFN - 1 mm max height

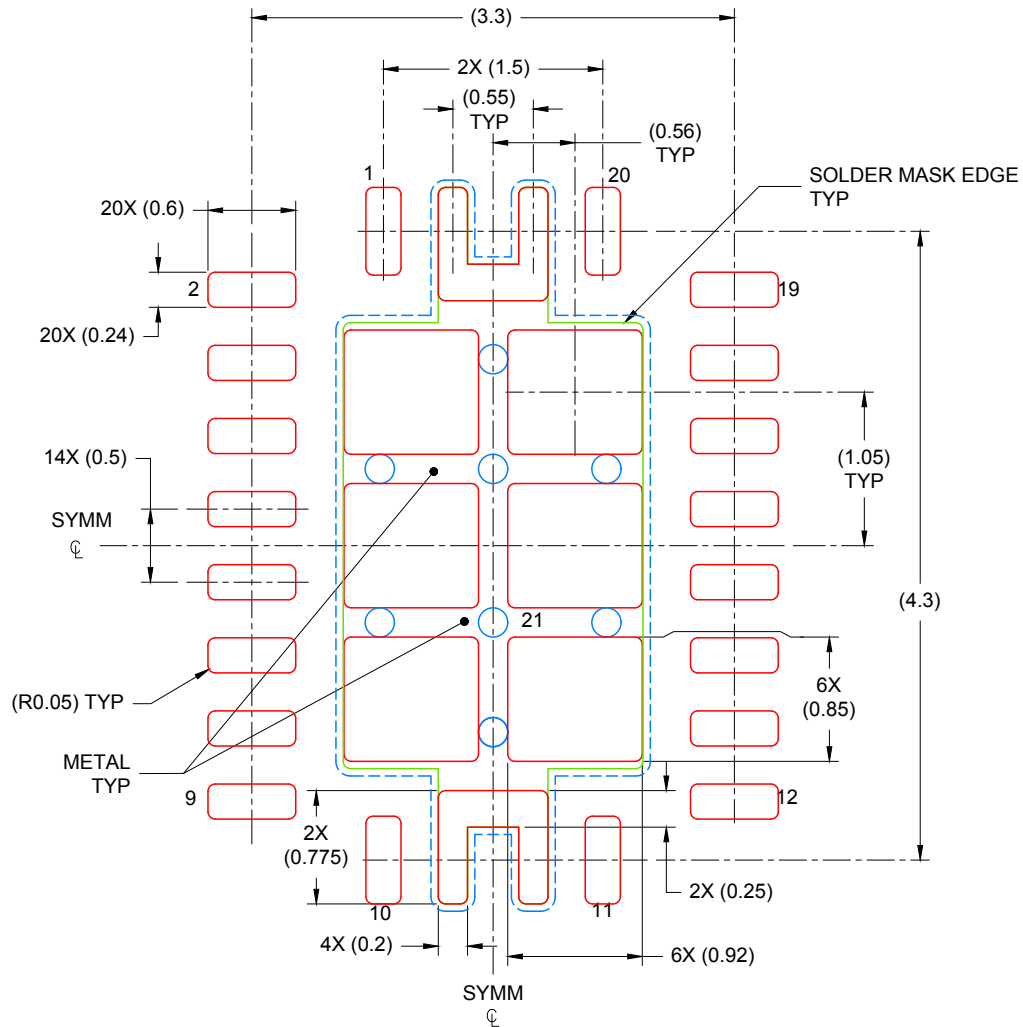
[illegible]

The diagram illustrates two PCB manufacturing methods:

- NON SOLDER MASK DEFINED (PREFERRED):** This method shows a central black dot representing the **EXPOSED METAL**. It is surrounded by a blue rectangular outline labeled **METAL**. The entire assembly is enclosed within a green rounded rectangle labeled **SOLDER MASK OPENING**. A dimension line indicates a gap of **0.07 MAX ALL AROUND** between the metal and the solder mask opening.
- SOLDER MASK DEFINED:** This method shows a central black dot representing the **EXPOSED METAL**. It is surrounded by a blue dashed rectangular outline labeled **METAL UNDER SOLDER MASK**. The entire assembly is enclosed within a green rounded rectangle labeled **SOLDER MASK OPENING**. A dimension line indicates a gap of **0.07 MIN ALL AROUND** between the metal and the solder mask opening.

4219071 / A 05/2017

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
 75% PRINTED COVERAGE BY AREA
 SCALE: 20X

4219071 / A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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