INDUSTRIAL 8-DIGITAL-INPUT SERIALIZER WITH DIAGNOSTICS

FEATURES

- **Eight Inputs**
  - **High Input Voltage – up to 34 V**
  - **Selectable Debounce Filters – 0 ms to 3 ms**
  - **Flexible Input Current Limit: 0.2 to 5.2 mA**
  - **Field Pins Protected to 15-kV HBM ESD**
- **Diagnostics:**
  - **Parity Check**
  - **Undervoltage Indication**
  - **Overtemperature Indication**
- **Output Drivers for External Status LEDs**
- **Cascadable in Multiples of Eight Inputs**
- **SPI-Compatible Interface**
- **Regulated 5-V Output for External Isolator**

APPLICATIONS

- **Sensor Inputs for Industrial Automation and Process Control**
- **High Channel Count Digital Input Modules for PC and PLC Systems**
- **Decentralized I/O Modules**
- **Motion Control Systems**

DESCRIPTION

The SN65HVS881 is an eight channel, digital-input serializer for high-channel density digital input modules in industrial automation. In combination with galvanic isolators the device completes the interface between the high voltage signals on the field-side and the low-voltage signals on the controller side. Input signals are current-limited and then validated by internal debounce filters.

With the addition of a few external components, the input switching characteristics can be configured in accordance with IEC61131-2 for Type 1, 2 and 3 sensor switches.

Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially.

Cascading of multiple devices is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Multiple devices can be cascaded through a single serial port, reducing both the isolation channels and controller inputs required.

Input status can be visually indicated via constant current LED outputs. The current limit on the inputs is set by a single external precision resistor. An integrated voltage regulator provides a 5V output to supply low-power isolators. An on-chip temperature sensor provides diagnostic information for graceful shutdown and system safety. An internal parity check for odd parity ensures trustworthy transmission of serial data to the system controller.

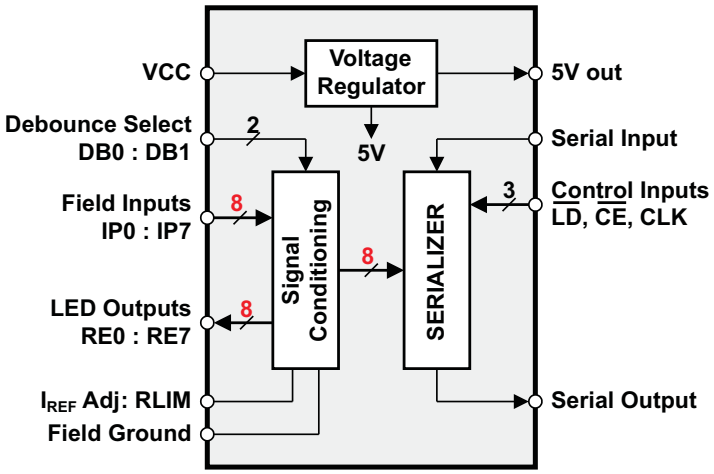
The SN65HVS881 is available in a 28-pin PWP PowerPAD™ package, allowing for efficient heat dissipation. The device is characterized for operation at temperatures from –40°C to 125°C

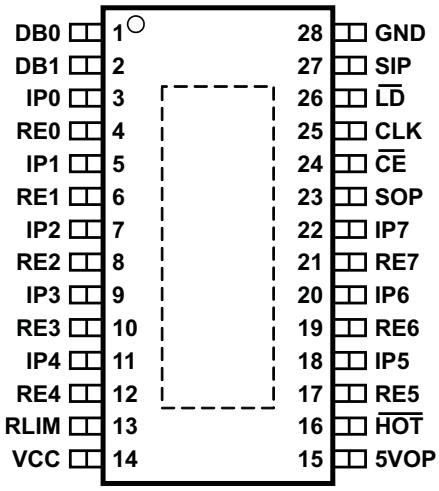
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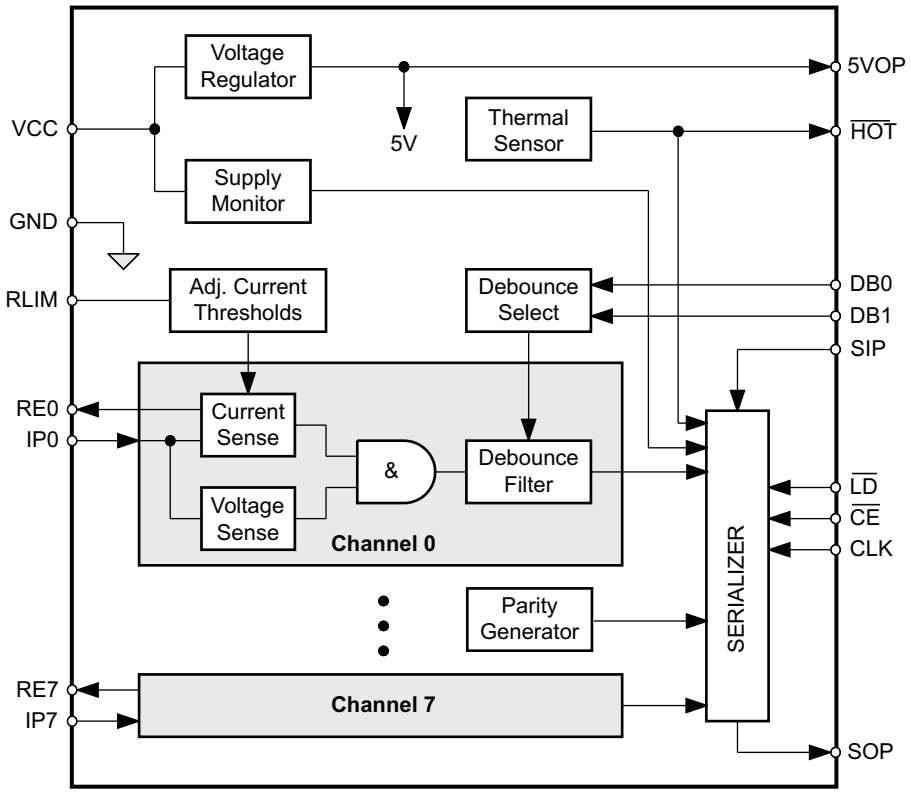
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FUNCTIONAL BLOCK DIAGRAM



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TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
PIN NO.	NAME	
1, 2	DB0, DB1	Debounce select inputs
3, 5, 7, 9, 11, 18, 20, 22	IPx	Input channel x
4, 6, 8, 10, 12, 17, 19, 21	REx	Return path x (LED drive)
13	RLIM	Current limiting resistor
14	V_{CC}	Field supply voltage
15	5VOP	5-V output to supply low-power isolators
16	$\overline{HOT}$	Active low over-temperature indication
23	SOP	Serial data output
24	$\overline{CE}$	Clock enable input
25	CLK	Serial clock input
26	$\overline{LD}$	Load pulse input
27	SIP	Serial data input
28	GND	Field ground

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
V_{CC}	Field power input			–0.3 to 36	V
V_{IPx}	Field digital inputs		IPx	–0.5 to 36	V
V_{ID}	Voltage at any logic input		DB0, DB1, CLK, SIP, $\overline{CE}$, $\overline{LD}$	–0.5 to 6	V
I_O	Output current		$\overline{HOT}$, SOP	±8	mA
V_{ESD}	Electrostatic discharge	Human-Body Model(2)	All pins	±4	kV
			IPx, V_{CC}	±15	
		Charged-Device Model(3)	All pins	±1	kV
		Machine Model(4)	All pins	±100	V
P_{TOT}	Continuous total power dissipation	See *Thermal Characteristics Table*			
T_J	Junction temperature			170	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) JEDEC Standard 22, Method A114-A.
(3) JEDEC Standard 22, Method C101
(4) JEDEC Standard 22, Method A115-A

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	High-K JEDEC thermal resistance model			35		°C/W
θ_{JB}	Junction-to-board thermal resistance				15		°C/W
θ_{JC}	Junction-to-case thermal resistance				4.27		°C/W
P_D	Device power dissipation	I_{CC} and I_{IP-LIM} = worst case with R_{LIM} = 25 kΩ, I_{LOAD} = 50 mA on 5VOP, RE0-RE7 = GND, f_{IP} = 100 MHz	IP0-IP7 = V_{CC} = 34 V			2970	mW
			IP0-IP7 = V_{CC} = 30 V			2600	
			IP0-IP7 = V_{CC} = 24 V			2020	
			IP0-IP7 = V_{CC} = 12 V			890	

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Field supply voltage		10		34	V
V_{IPL}	Field input low-state input voltage		0		4	V
V_{IPH}	Field input high-state input voltage		5.5		34	V
V_{IL}	Logic low-state input voltage		0		0.8	V
V_{IH}	Logic high-state input voltage		2.0		5.5	V
R_{LIM}	Current limiter resistor		17	25	500	kΩ
f_{IP}(1)	Input data rate (each field input)		0		1	Mbps
T_A	Free-air temperature, see *Thermal Characteristics*	V_{CC} ≤ 34 V	–40		85	°C
		V_{CC} ≤ 27 V	–40		105	
		V_{CC} ≤ 18 V	–40		125	
T_J	Junction temperature				150	°C

(1) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = GND), and R_{IN} = 0 Ω

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ELECTRICAL CHARACTERISTICS

Over full-range of recommended operating conditions, unless otherwise noted

PARAMETER		TERMINAL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FIELD INPUTS							
$V_{TH–(IP)}$	Low-level device input threshold voltage	IP0–IP7	R_{LIM} = 25 kΩ	4.0	4.3		V
$V_{TH+(IP)}$	High-level device input threshold voltage				5.2	5.5	
$V_{HYS(IP)}$	Device input hysteresis				0.9		
$V_{TH–(IN)}$	Low-level field input threshold voltage	Measured at field side of R_{IN}	18 V < V_{CC} <30 V, R_{IN} = 1.2 kΩ ± 5%, R_{LIM} = 25 kΩ, T_A ≤ 85 °C	6	8.4		V
$V_{TH+(IN)}$	High-level field input threshold voltage				9.4	10	
$V_{HYS(IN)}$	Field input hysteresis				1		
$V_{TH– (VCC)}$	Low-level V_{CC}-monitor threshold voltage	V_{CC}		15	16.05		V
$V_{TH+ (VCC)}$	High-level V_{CC}-monitor threshold voltage				16.8	18	
$V_{HYS (VCC)}$	V_{CC}-monitor hysteresis				0.75		
R_{IP}	Input resistance	IP0–IP7	3 V < V_{IPx} < 6 V, R_{LIM} = 25 k	0.2	0.63	1.1	kΩ
I_{IP-LIM}	Input current limit	IP0–IP7	R_{LIM} = 25 kΩ	3.15	3.6	4	mA
t_{DB}	Debounce times of input channels	IP0–IP7	DB0 = open, DB1 = GND		0		ms
			DB0 = GND, DB1 = open		1		
			DB0 = DB1 = open		3		
I_{RE-on}	RE on-state current	RE0–RE7	R_{LIM} = 25 kΩ, RE_x = GND	2.8	3.15	3.5	mA
FIELD SUPPLY							
$ICC_{(VCC)}$	Supply current, no load	V_{CC}	IP0 to IP7 = V_{CC}, 5VOP = open, RE_X = GND, All logic inputs open			8.7	mA
5V REGULATED OUTPUT							
$V_{O(5V)}$	Linear regulator output voltage	5VOP	10V < V_{CC} < 34V, no load	4.5	5	5.5	V
			10V < V_{CC} < 34V, I_L = 5mA	4.5	5	5.5	
			10V < V_{CC} < 34V, I_L = 20mA, T_A ≤ 105°C	4.5	5	5.5	
			10V < V_{CC} < 34V, I_L = 50 mA, T_A ≤ 85°C	4.5	5	5.5	
$I_{LIM(5V)}$	Linear regulator output current limit				115		mA
$\Delta V_5/\Delta V_{CC}$	Linear regulation	5VOP, V_{CC}	10V < V_{CC} < 34V, I_L = 5 mA			2	mV/V
LOGIC INPUT AND OUTPUTS							
V_{OL}	Logic low-level output voltage	SOP, $\overline{HOT}$	I_{OL} = 20 µA			0.4	V
V_{OH}	Logic high-level output voltage		I_{OH} = –20 µA	4			V
I_{IL}	Logic input leakage current	DB0, DB1, $\overline{SIP}$, $\overline{LD}$, $\overline{CE}$, CLK		–50		50	µA
T_{OVER}	Over-temperature indication (internal)	$\overline{HOT}$			150		°C
T_{SHDN}	Shutdown temperature (internal)				170		°C

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TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t_{W1}	CLK pulse duration	See Figure 6	4			ns
t_{W2}	$\overline{LD}$ pulse duration	See Figure 4	6			ns
t_{SU1}	SIP to CLK setup time	See Figure 7	4			ns
t_{H1}	SIP to CLK hold time	See Figure 7	2			ns
t_{SU2}	Falling edge to rising edge ($\overline{CE}$ to CLK) setup time	See Figure 8	4			ns
t_{REC}	$\overline{LD}$ to CLK recovery time	See Figure 5	2			ns
f_{CLK}	Clock pulse frequency	See Figure 6	DC		100	MHz

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}, t_{PHL1}	CLK to SOP	C_L = 15 pF, see Figure 6			10	ns
t_{PLH2}, t_{PHL2}	$\overline{LD}$ to SOP	C_L = 15 pF, see Figure 4			14	ns
t_r, t_f	Rise and fall times	C_L = 15 pF, see Figure 6			5	ns

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INPUT CHARACTERISTICS

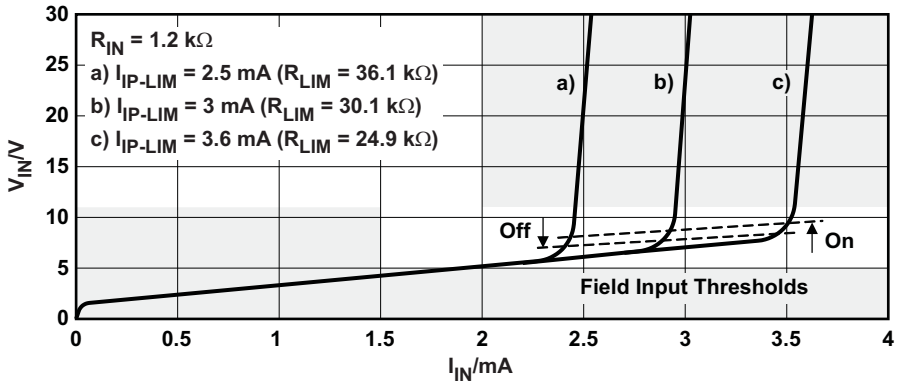


Figure 1. Typical Input Characteristic

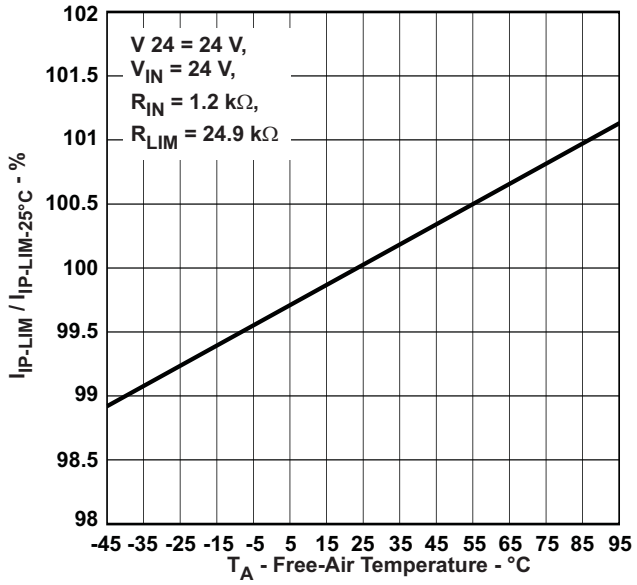


Figure 2. Typical Current Limiter Variation vs Ambient Temperature

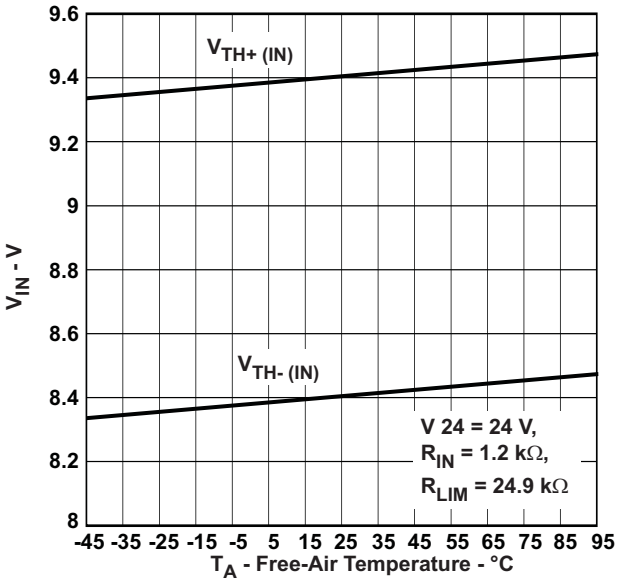


Figure 3. Typical Limiter Input Threshold Voltage Variation vs Ambient Temperature

PARAMETER MEASUREMENT INFORMATION

Waveforms

For the complete serial interface timing, refer to Figure 21.

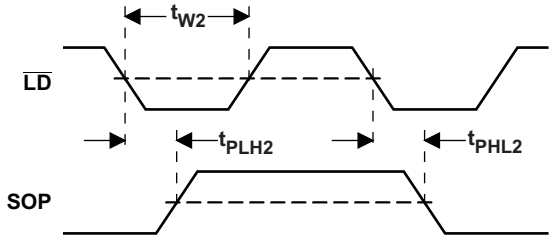


Figure 4. Parallel – Load Mode

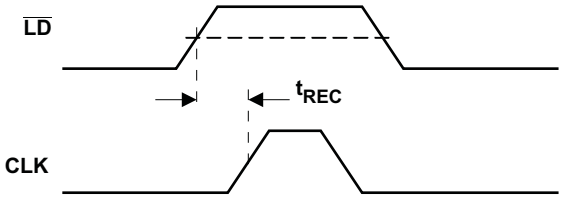


Figure 5. Serial – Shift Mode

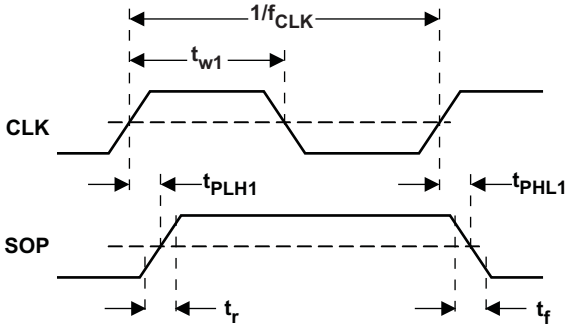


Figure 6. Serial – Shift Mode

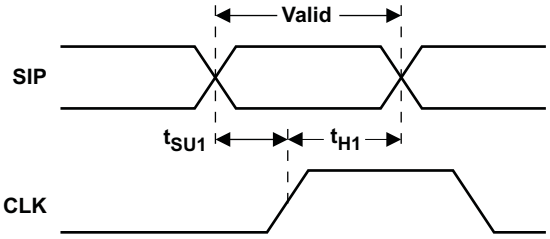


Figure 7. Serial – Shift Mode

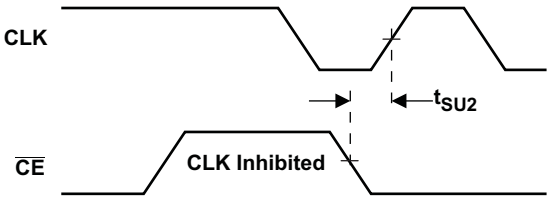


Figure 8. Serial – Shift Clock Inhibit Mode

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VOLTAGE REGULATOR PERFORMANCE CHARACTERISTICS

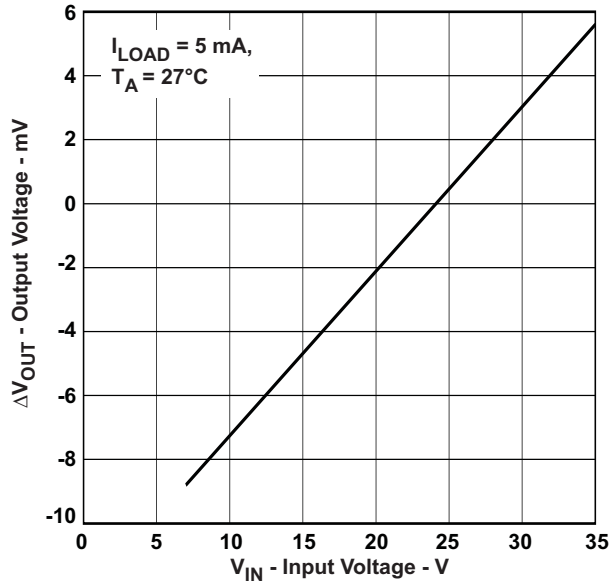


Figure 9. Line Regulation

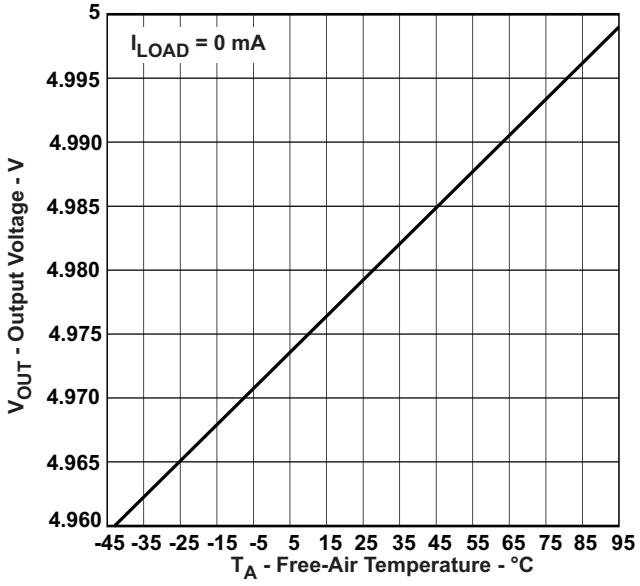


Figure 10. Output Voltage vs Ambient Temperature

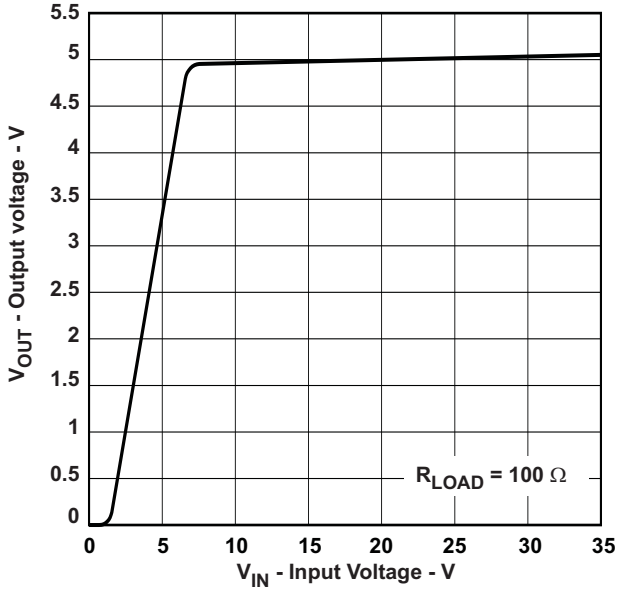


Figure 11. Output Voltage vs Input Voltage

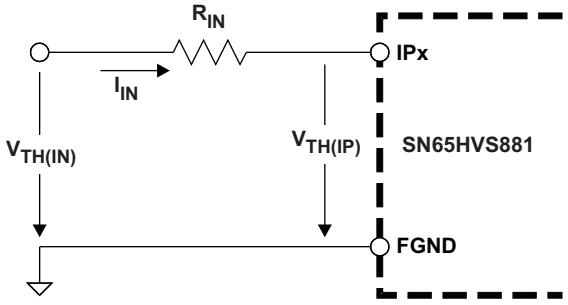


Figure 12. On/Off Threshold Voltage Measurements

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DEVICE INFORMATION

Digital Inputs

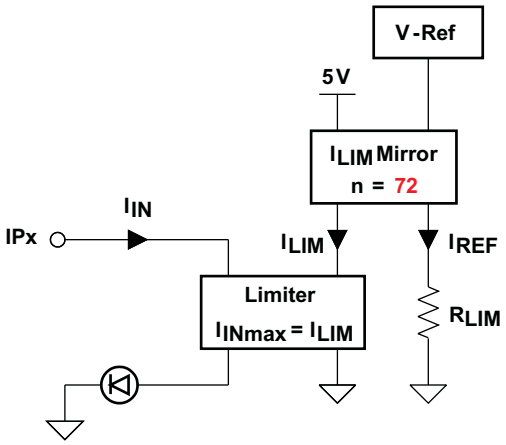


Figure 13. Digital Input Stage

Each digital input operates as a controlled current sink limiting the input current to a maximum value of I_{LIM}. The current limit is derived from the reference current via $I_{LIM} = n \times I_{REF}$, and I_{REF} is determined by $I_{REF} = V_{REF}/R_{LIM}$. Thus, changing the current limit requires the change of R_{LIM} to a different value via: $R_{LIM} = n \times V_{REF}/I_{LIM}$.

While the device is specified for a current limit of 3.6 mA, (via R_{LIM} = 25 kΩ), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of 2.5 mA simply calculate:

$$R_{LIM} = \frac{90}{I_{LIM}} = \frac{90}{2.5\ mA} = 36\ k\Omega$$

Debounce Filter

The HVS881 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table

Table 1. Debounce Times

DB1	DB0	FUNCTION
Open	Open	3 ms delay
Open	GND	1 ms delay
GND	Open	0 ms delay (filter bypassed)
GND	GND	Reserved

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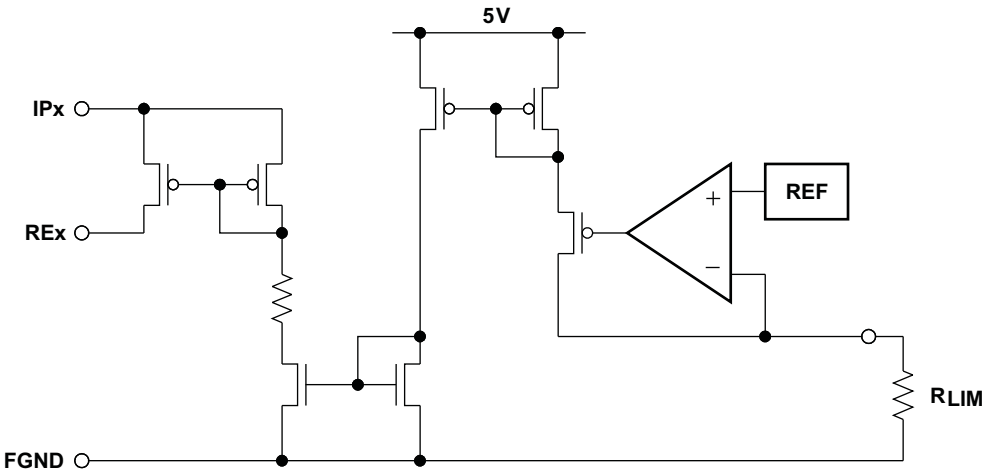


Figure 14. Equivalent Input Diagram

Shift Register

The conversion from parallel input- to serial output data is performed by an eight channel parallel-in serial-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7 that are enabled by a low level at the load input ($\overline{LD}$). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{LD}$ is held high and the clock enable ($\overline{CE}$) input is held low. Parallel loading is inhibited when /LD is held high. The parallel inputs to the register are enabled while $\overline{LD}$ is low independently of the levels of the CLK, $\overline{CE}$, or serial (SIP) inputs.

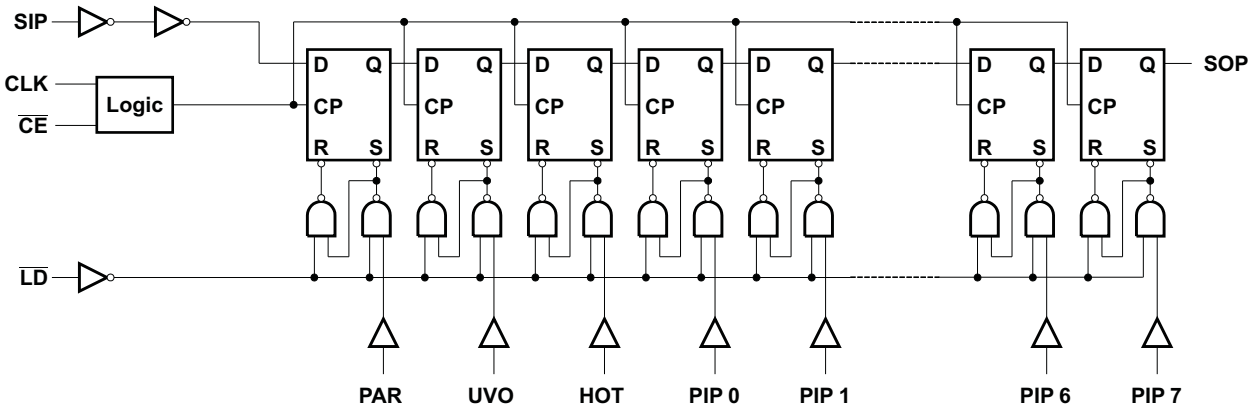


Figure 15. Shift Register Logic Structure

Table 2. Function Table

INPUTS			FUNCTION
$\overline{LD}$	CLK	$\overline{CE}$	
L	X	X	Parallel load
H	X	H	No change
H	↑	L	Shift(1)

(1) Shift = content of each internal register shifts towards serial outputs. Data at SIP is shifted into first register.

Voltage Regulator

The on-chip linear voltage regulator provides a 5V supply to the internal- and external-circuitry, such as digital isolators, with an output drive capability of 50 mA and a typical current limit of 115 mA. The regulator accepts input voltages from 30V down to 10V. Because the regulator output is intended to supply external digital isolator circuits proper output voltage decoupling is required. For best results connect a 1µF and a 0.1µF ceramic capacitor as close as possible to the 5VOP-output. For longer traces between the SN65HVS881 and isolators of the ISO72xx family use additional 0.1µF and 10pF capacitors next to the isolator supply pins. Make sure, however, that the total load capacitance does not exceed 4.7µF.

For good stability the voltage regulator requires a minimum load current, $I_{L\text{-}MIN}$. Ensure that under any operating condition the ratio of the minimum load current in mA to the total load capacitance in µF is larger than 1:

$$\frac{I_{L\text{-}MIN}}{C_L} > \frac{1\ mA}{1\ \mu F}$$

Temperature Sensor

An on-chip temperature sensor monitors the device temperature and signals a fault condition if the internal temperature reaches 150°C. If the internal temperature exceeds this trip point, the $\overline{HOT}$ output switches to an active low state. If the internal temperature continues to rise, passing a second trip point at 170°C, all device outputs are put in a high-impedance state.

A special condition occurs, however, when the chip temperature exceeds the second temperature trip point due to an output short. Then the output buffer becomes 3-state, thus separating the buffer from the external circuitry. An internal 100-kΩ pull-down resistor, connecting the $\overline{HOT}$ pin to ground, is used as a *cooling down* resistor, which continues to provide a logic low level to the external circuitry.

Parity Generator

A parity bit is generated when one or more of the following conditions occur:

- a change in input status
- a change in Undervoltage status
- a change in Overtemperature status

Upon the application of a load pulse the input status (IP0–IP7) and the diagnostic bits (HOT, UVO, and PAR) are loaded parallel into the serializer assuming the following format:

Bit 11										Bit 1
PAR	UVO	HOT	PIP0	PIP1	PIP2	PIP3	PIP4	PIP5	PIP6	PIP7

Figure 16. Sequence of Status Bits in Serializer

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APPLICATION INFORMATION

System-Level EMC

The SN65HVS881 is designed to operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards. In addition to the device internal ESD structures, external protection circuitry, as shown in Figure 17, can be used to absorb as much energy from burst- and surge-transients as possible.

R_1	56 Ω, 1/3 W MELF Resistor
D_1	33 V – 36 V fast Zener Diode, Z2SMB36
C_1	10 µF, 60 V Ceramic Capacitor
R_{IN}	1.2 kΩ, 1/4 W MELF Resistor
C_{IN}	22 nF, 60 V Ceramic Capacitor
C_S	4.7 nF, 2 kV Polypropylene Capacitor
D_S	39V Transient Voltage Suppressor: SM15T39CA
D_2	Super Rectifier: BYM10-1000, or General Purpose rectifier: 1N4007

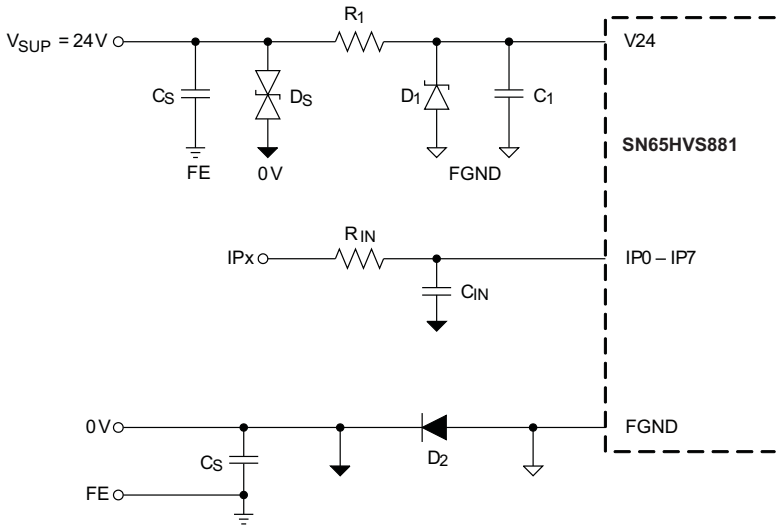


Figure 17. Typical EMC Protection Circuitry for Supply and Signal Inputs

Input Channel Switching for IEC61131-2 PLC Applications

The input stage of the SN65HVS881 is designed so that with a 24-V supply on V_{CC} and an input resistor R_{IN} = 1.2 kΩ, the trip point for signaling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 type-1 and type-3 switches.

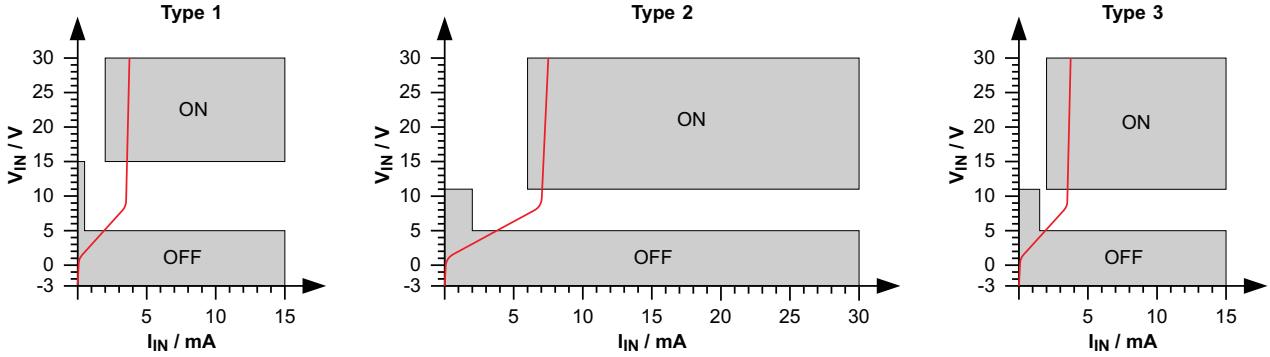


Figure 18. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 Proximity Switches

For a type-2 switch application two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (GND).

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

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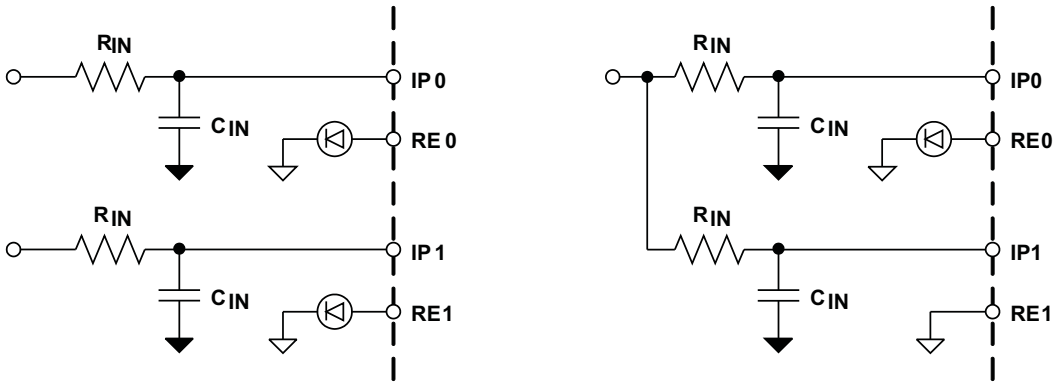


Figure 19. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input

Digital Interface Timing

The digital interface of the SN65HVS881 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard microcontrollers.

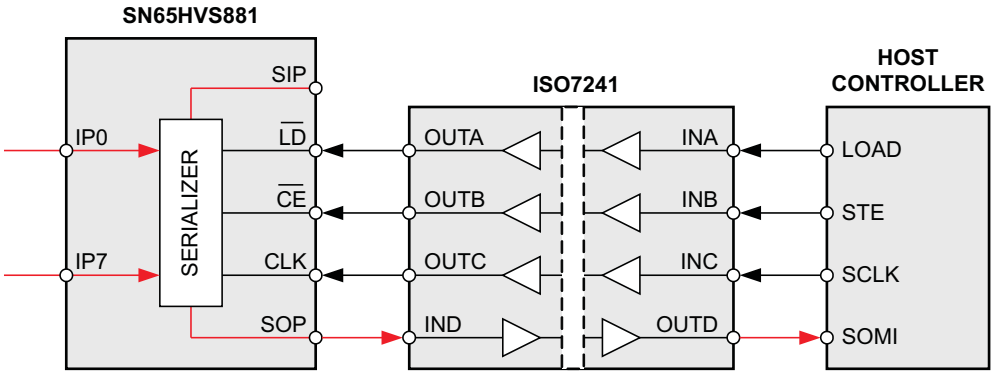


Figure 20. Simple Isolation of the Shift Register Interface

Upon a low-level at the load input, /LD, the information of the field inputs and the diagnostic bits are latched into the shift register. Taking $\overline{LD}$ high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, $\overline{CE}$, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus after eleven consecutive clock cycles all data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

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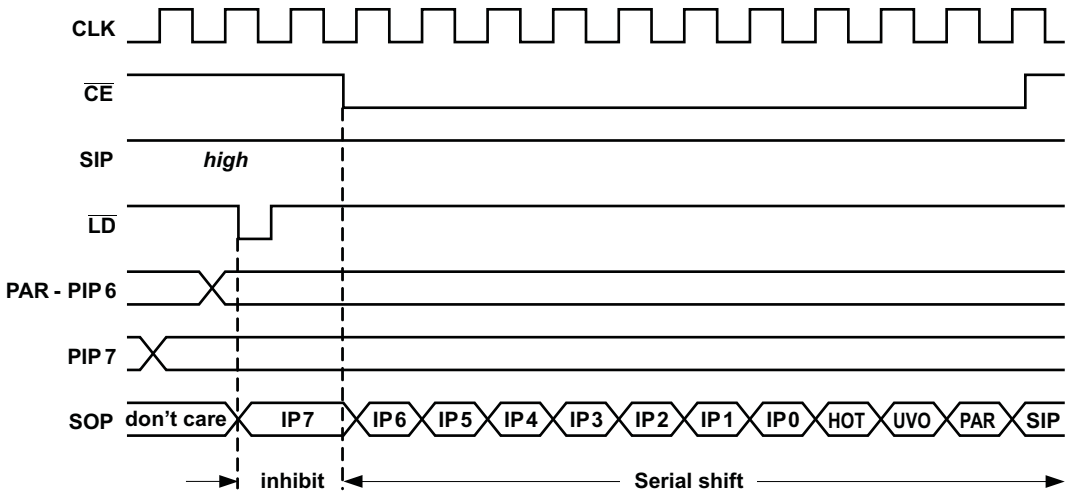


Figure 21. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register

Cascading for High Channel Count Input Modules

Designing high-channel count modules requires cascading multiple SN65HVS881 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

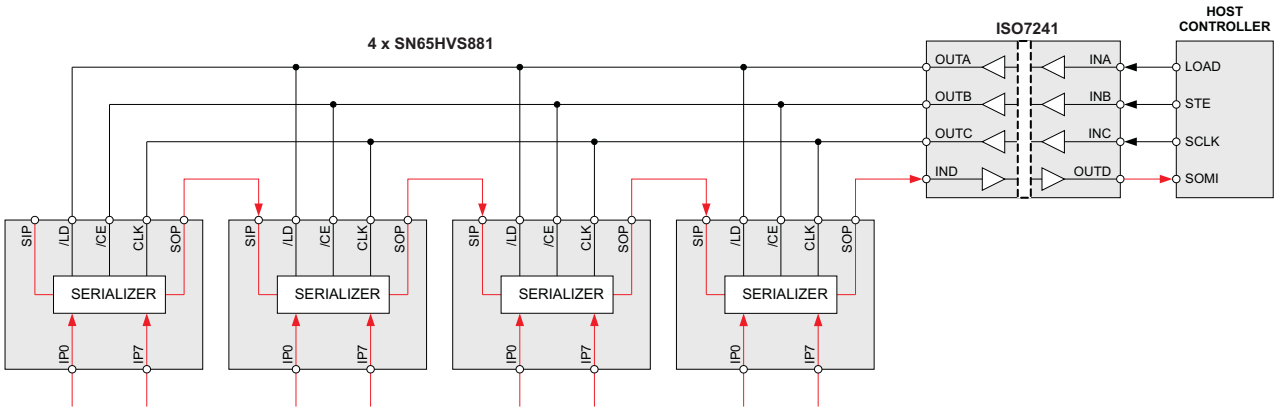


Figure 22. Cascading Four SN65HVS881 for a 32-Channel Input Module

Typical Digital Input Module Application

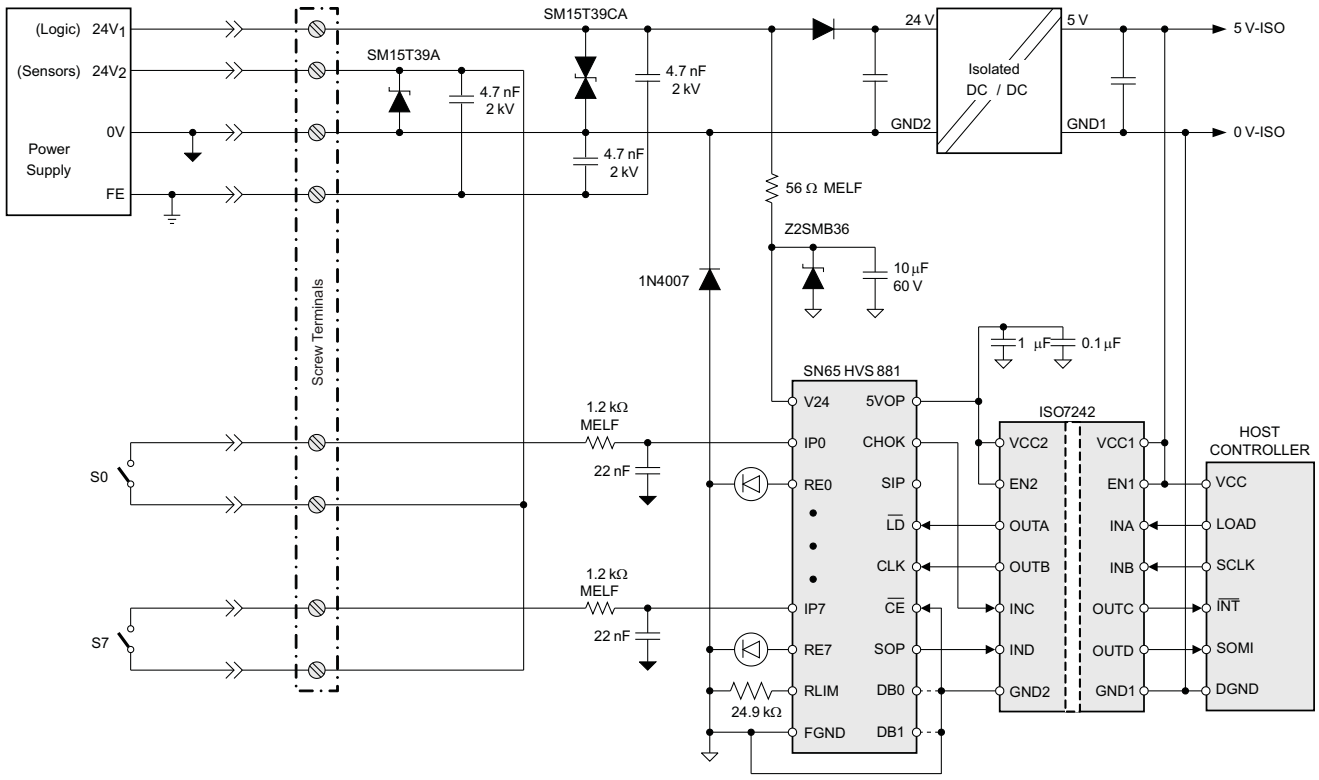
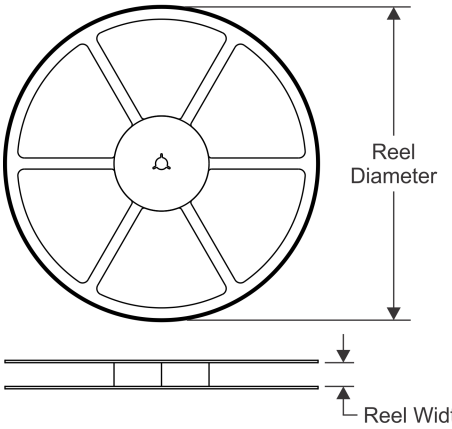


Figure 23. Typical Digital Input Module Application

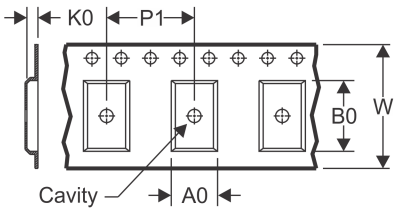
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

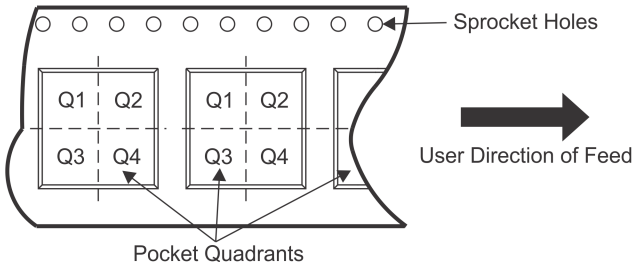


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

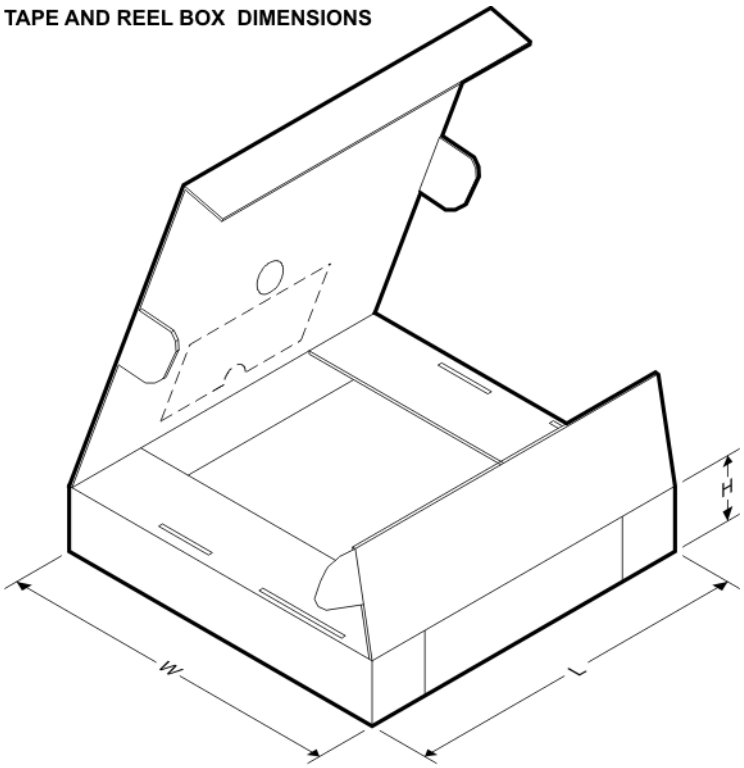
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVS881PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

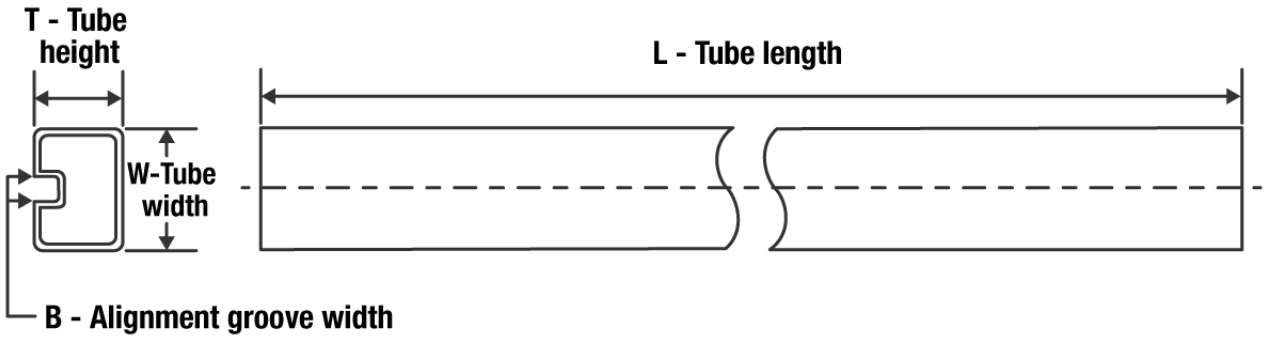
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVS881PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVS881PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

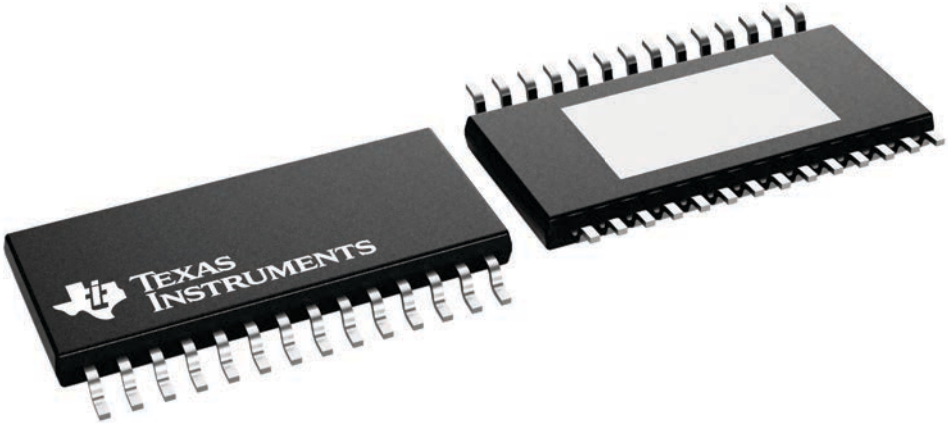
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

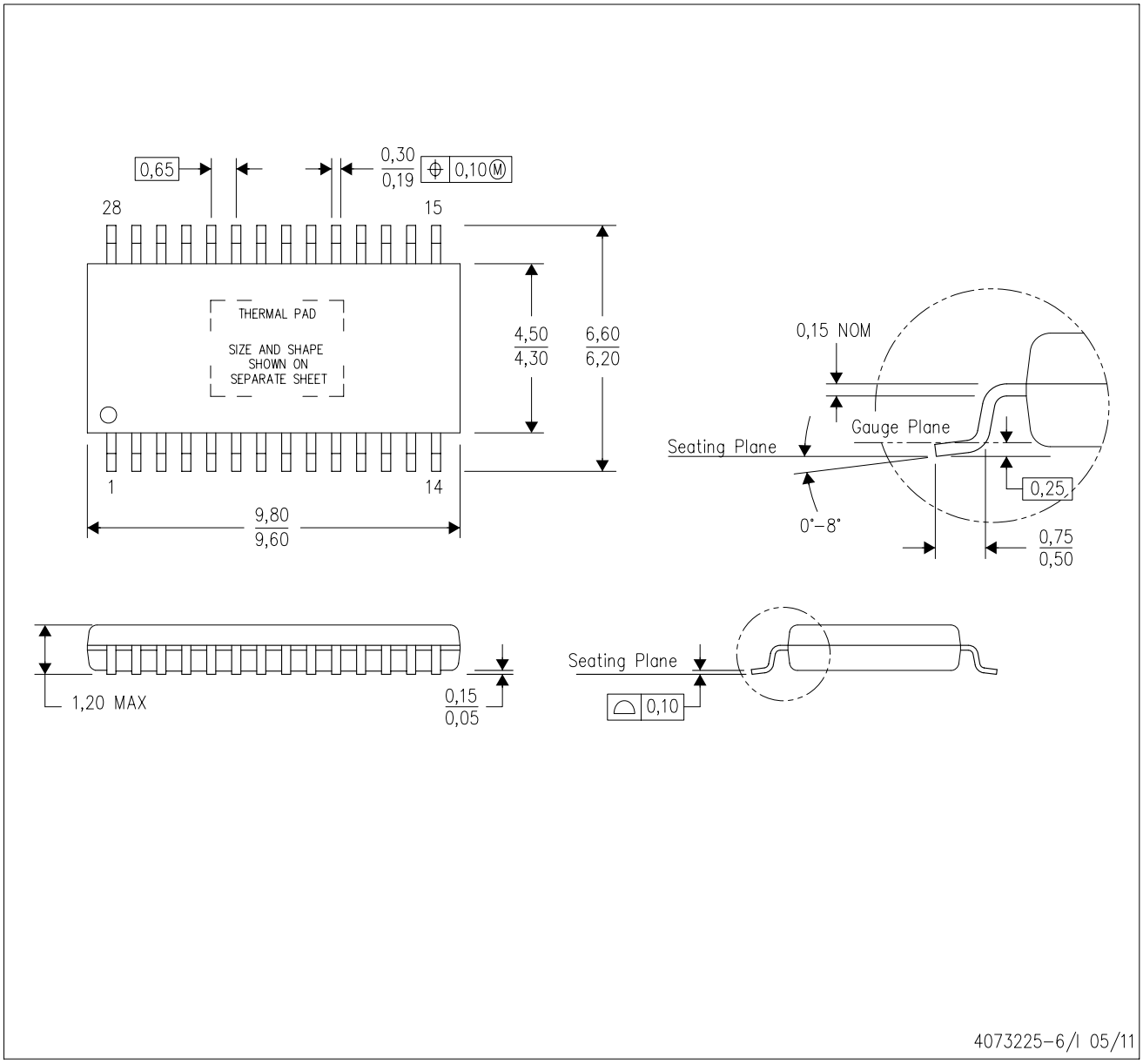
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

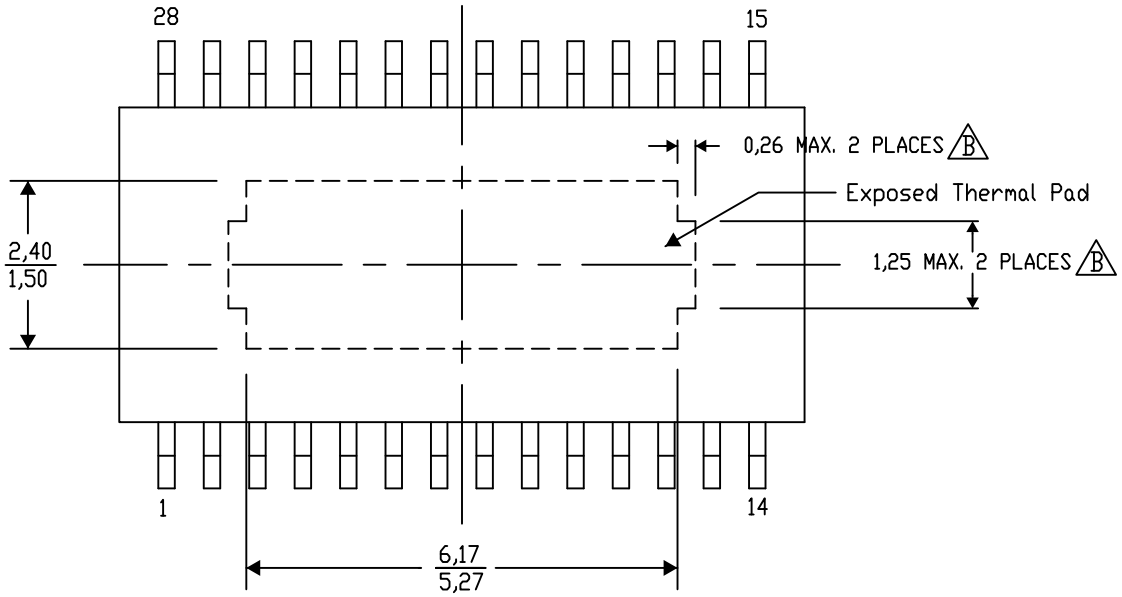
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

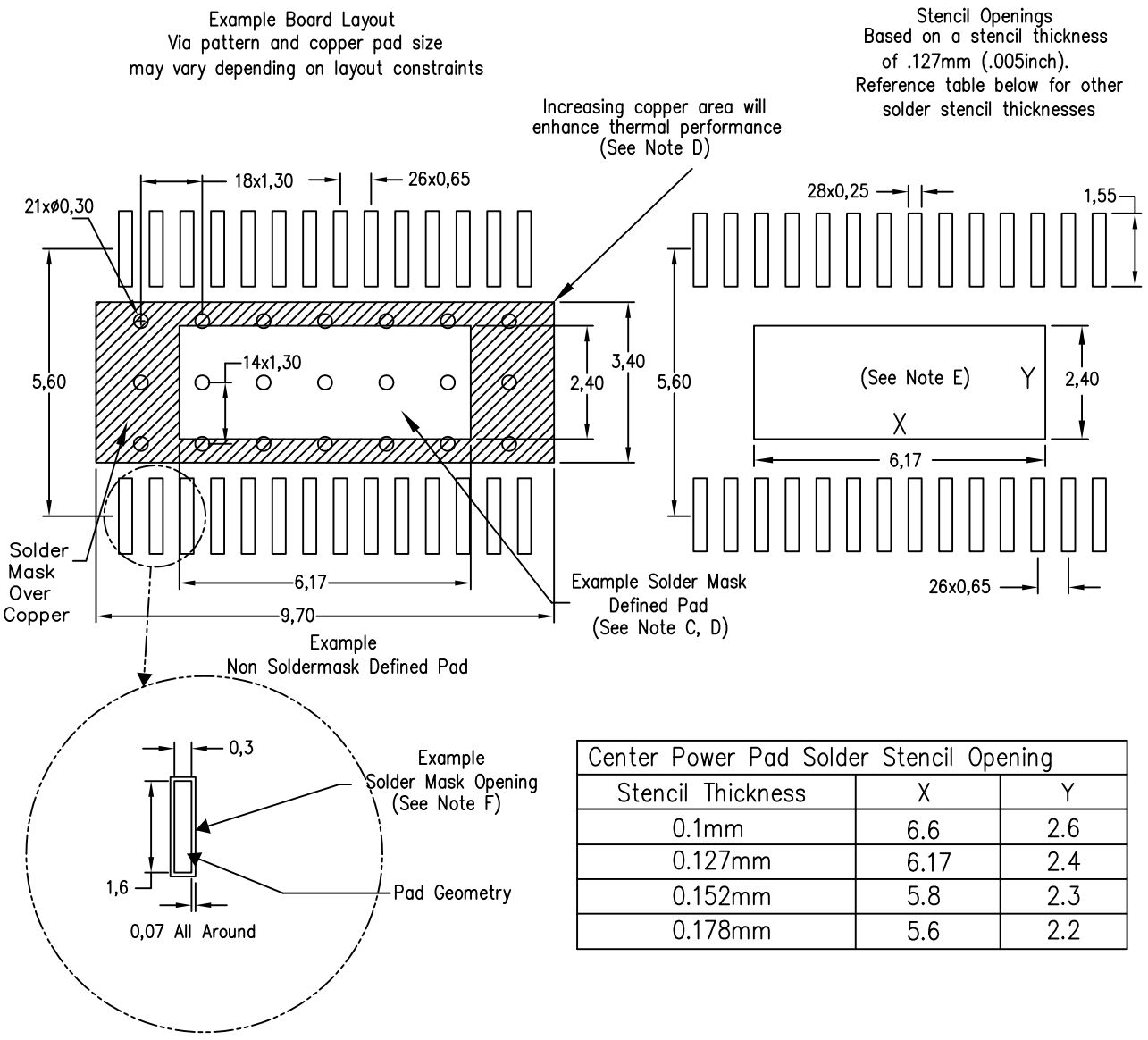
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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