SN65LVDS4 1.8V 高速差分线路接收器

1 特性

- 旨在实现高信号传输速率：
  - 500Mbps 接收器

(1) 线路的信号传输速率是指每秒钟的电压转换次数，单位为 bps（每秒比特数）

- 由 1.8V 或 2.5V 内核电源供电
- 采用 1.5mm × 2mm UQFN 封装
- 总线引脚静电放电 (ESD) 保护等级超过 2kV (HBM)
- 低电压差分信令，可向一个 100Ω 负载提供 350V 的典型输出电压
- 传播延迟时间
  - 典型值为 2.1ns（接收器）
- 250MHz 频率下的功耗
  - 典型值为 40mW
- 需要从外部提供故障安全保护
- 差分输入电压阈值 < 50mV
- 可基于外部 VDD 引脚提供输出电压逻辑电平（3.3V LVTTL、2.5V LVCMOS 和 1.8V LVCMOS），无需外部电平转换

2 应用

- 时钟分配
- 无线基站
- 网络路由器

3 说明

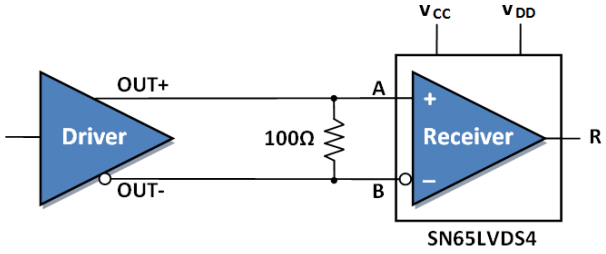
SN65LVDS4 是一款单通道、低电压差分线路接收器，采用小型 UQFN 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN65LVDS4	UQFN (10)	1.50mm x 2.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 3
6.1 Absolute Maximum Ratings 3
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Receiver Electrical Characteristics: V_{CC} = 2.5 V 5
6.6 Receiver Electrical Characteristics: V_{CC} = 1.8 V 5
6.7 Receiver Switching Characteristics: V_{CC} = 2.5 V 6
6.8 Receiver Switching Characteristics: V_{CC} = 1.8 V 6
6.9 Typical Characteristics 7
7 **Parameter Measurement Information** 10
8 **Detailed Description** 12
8.1 Overview 12
8.2 Functional Block Diagram 12
8.3 Feature Description 12
8.4 Device Functional Modes 13
9 **Application and Implementation** 14
9.1 Application Information 14
9.2 Typical Application 15
10 **Power Supply Recommendations** 19
11 **Layout** 20
11.1 Layout Guidelines 20
11.2 Layout Example 23
12 器件和文档支持 24
12.1 社区资源 24
12.2 商标 24
12.3 静电放电警告 24
12.4 Glossary 24
13 机械、封装和可订购信息 24

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

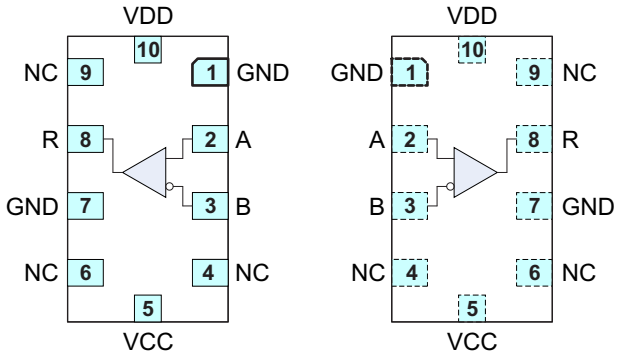
Changes from Original (July 2011) to Revision A **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

Copyright © 2011–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

RSE Package
10-Pin UQFN



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	2	I	LVDS input, positive
B	3	I	LVDS input, negative
GND	1, 7	–	Ground
NC	4, 6, 9	–	No connect
R	8	O	1.8/2.5 LVCMOS/3.3 LVTTL output
VCC	5	–	Core supply voltage
VDD	10	–	Output drive voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC} (2)		–0.5	4	V
Receiver output voltage logic level and driver input voltage logic level supply, V_{DD}		–0.5	4	V
Input voltage range, V_I	(A or B)	–0.5	V_{CC} + 0.3	V
Output voltage, V_O	(R)	–0.5	V_{DD} + 0.3	V
Differential input voltage magnitude, $\|V_{ID}\|$			1	V
Receiver output current, I_O		–12	12	mA
Continuous total power dissipation, P_D		See *Thermal Information*		
Storage temperature (non operating)		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Copyright © 2011–2015, Texas Instruments Incorporated

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins	2000	V
		Bus pins (A, B, Y, Z)	2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC1.8}$	Core supply voltage	1.62	1.8	1.98	V
$V_{CC2.5}$	Core supply voltage	2.25	2.5	2.75	V
$V_{DD1.8}$	Output drive voltage	1.62	1.8	1.98	V
$V_{DD2.5}$	Output drive voltage	2.25	2.5	2.75	V
$V_{DD3.3}$	Output drive voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
$\|V_{ID}\|$	Magnitude of differential input voltage	0.15		0.6	V
f_{op}	Operating frequency range	10		250	MHz
$\|VIN_{MAX}\|$	Input voltage (any combination of input or common-mode voltage) See [1]*Maximum Input Voltage, $V_{IN(max)}$*.	0		V_{CC}	V

(1) Any combination of input or common-mode voltage should not be below 0 V or above V_{CC}.

6.4 Thermal Information

THERMAL METRIC[1]		SN65LVDS4 RSE (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2011–2015, Texas Instruments Incorporated

6.5 Receiver Electrical Characteristics: V_{CC} = 2.5 V

over recommended operating conditions, V_{CC} = 2.5 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 17, $V_{CC1.8}$, $V_{CC2.5}$			50	mV
$V_{ITH–}$	Negative-going differential input voltage threshold	See Figure 17, $V_{CC1.8}$, $V_{CC2.5}$	–50			mV
V_{OH}	High-level output voltage	V_{DD} = 3.3 V, I_{OH} = –8 mA	V_{DD} – 0.25			V
		V_{DD} = 2.5 V, I_{OH} = –6 mA	V_{DD} – 0.25			
		V_{DD} = 1.8 V, I_{OH} = –4 mA	V_{DD} – 0.25			
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V, I_{OL} = 8 mA			0.25	V
		V_{DD} = 2.5 V, I_{OL} = 6 mA			0.25	
		V_{DD} = 1.8 V, I_{OL} = 4 mA			0.25	
P_{static}	Static power	No load, steady state, V_{DD} = 3.3 V, V_{ID}+		22	28	mW
		No load, steady state, V_{DD} = 2.5 V, V_{ID}+		20	25	
C_I	Input capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF
C_O	Output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.
(2) All typical values are at 25°C .

6.6 Receiver Electrical Characteristics: V_{CC} = 1.8 V

over recommended operating conditions, V_{CC} = 1.8 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 17, $V_{CC1.8}$, $V_{CC2.5}$			50	mV
$V_{ITH–}$	Negative-going differential input voltage threshold	See Figure 17, $V_{CC1.8}$, $V_{CC2.5}$	–50			mV
V_{OH}	High-level output voltage	V_{DD} = 3.3 V, I_{OH} = –8 mA	V_{DD} – 0.25			V
		V_{DD} = 2.5 V, I_{OH} = –6 mA	V_{DD} – 0.25			
		V_{DD} = 1.8 V, I_{OH} = –4 mA	V_{DD} – 0.25			
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V, I_{OL} = 8 mA			0.25	V
		V_{DD} = 2.5 V, I_{OL} = 6 mA			0.25	
		V_{DD} = 1.8 V, I_{OL} = 4 mA			0.25	
P_{static}	Static power	No load, steady state, V_{DD} = 3.3 V, V_{ID}+		18	21	mW
		No load, steady state, V_{DD} = 2.5 V, V_{ID}+		16	19	
		No load, steady state, V_{DD} = 1.8 V, V_{ID}+		13	16	
C_I	Input capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF
C_O	Output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		4		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.
(2) All typical values are at 25°C .

Copyright © 2011–2015, Texas Instruments Incorporated

6.7 Receiver Switching Characteristics: V_{CC} = 2.5 V

over recommended operating conditions, V_{CC} = 2.5 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 19			2.5	3.3	ns
t_{PHL}	Propagation delay time, high-to-low-level output				2.5	3.3	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)(2)					240	ps
t_r	Output signal rise time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
t_f	Output signal fall time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
t_{jit}	Residual jitter added	Carrier frequency = 122.8 MHz, input signal amplitude = 500 mVpp sine wave, integration bandwidth for rms jitter = 20 khz-20 MHz, VDD = 2.5 V			370		fs

(1) All typical values are at 25°C.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

6.8 Receiver Switching Characteristics: V_{CC} = 1.8 V

over recommended operating conditions, V_{CC} = 1.8 V, V_{ID} = 150 mV–600 mV, V_{CM} = V_{ID}/2 to V_{CC} – V_{ID}/2 V, 10 pF load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 19			3.2	3.8	ns
t_{PHL}	Propagation delay time, high-to-low-level output				3.2	3.8	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)(2)					240	ps
t_r	Output signal rise time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
			V_{DD} = 1.8 V			750	
t_f	Output signal fall time		V_{DD} = 3.3 V			550	ps
			V_{DD} = 2.5 V			600	
			V_{DD} = 1.8 V			750	
t_{jit}	Residual jitter added	Carrier frequency = 122.8 MHz, input signal amplitude = 500 mVpp sine wave, integration bandwidth for rms jitter = 20 khz-20 MHz, VDD = 1.8 V			370		fs

(1) All typical values are at 25°C.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

Copyright © 2011–2015, Texas Instruments Incorporated

6.9 Typical Characteristics

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

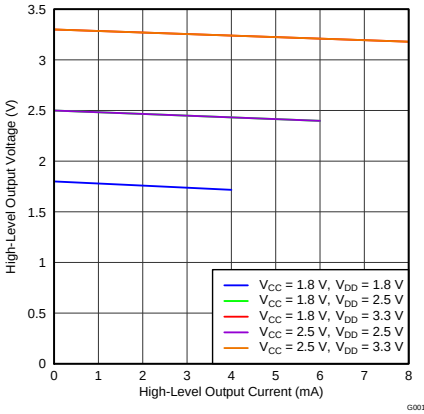


Figure 1. High-Level Output Voltage vs. High-Level Output Current

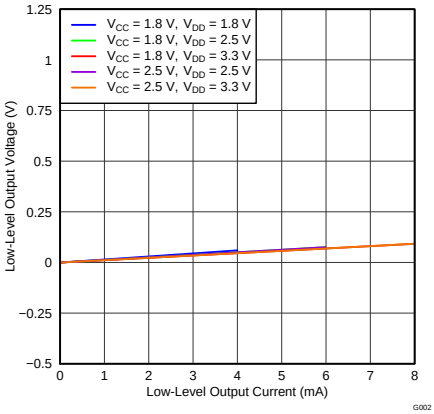


Figure 2. Low-Level Output Voltage vs. Low-Level Output Current

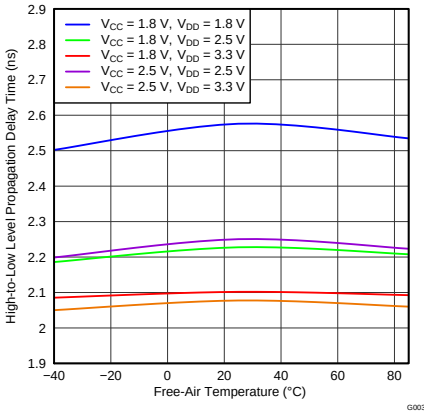


Figure 3. High- to Low-Level Propagation Delay Time vs. Free-Air Temperature

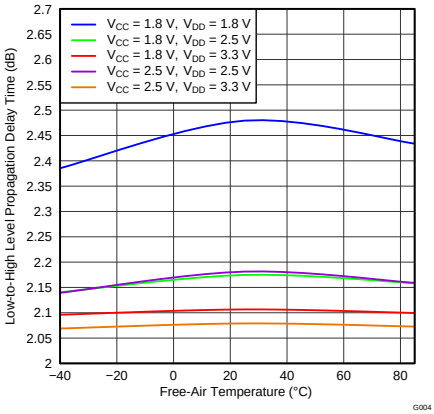


Figure 4. Low- to High-Level Propagation Delay Time vs. Free-Air Temperature

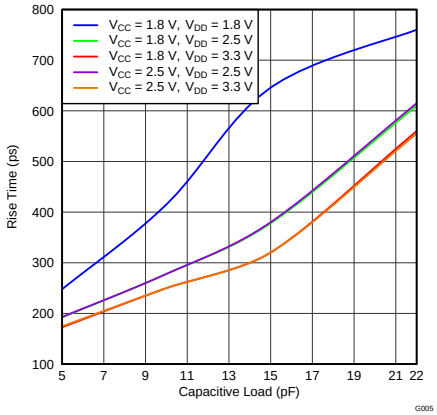


Figure 5. Rise Time vs. Capacitive Load

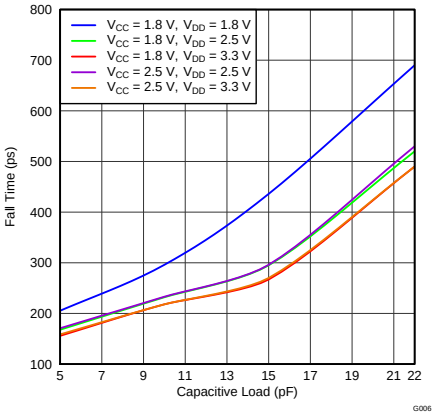


Figure 6. Fall Time vs. Capacitive Load

Copyright © 2011–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

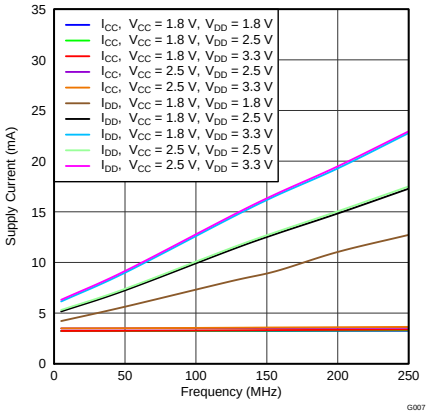


Figure 7. Supply Current vs. Frequency

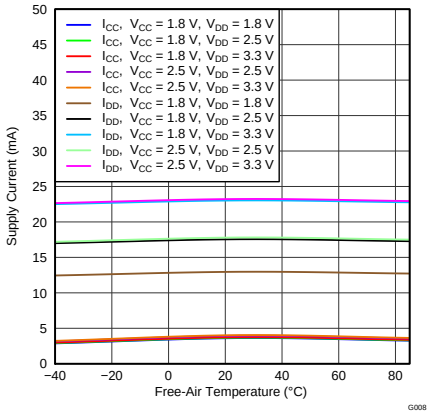


Figure 8. Supply Current vs. Temperature

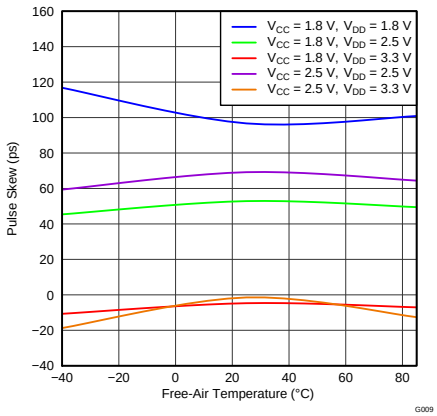


Figure 9. Pulse Skew vs. Temperature

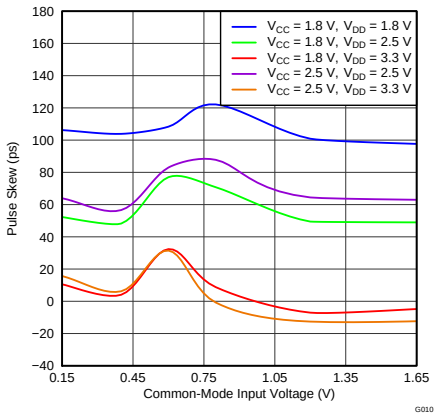


Figure 10. Pulse Skew vs. Common-Mode Voltage

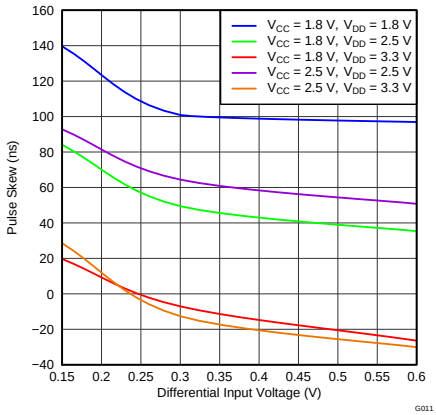


Figure 11. Pulse Skew vs. Differential Input Voltage

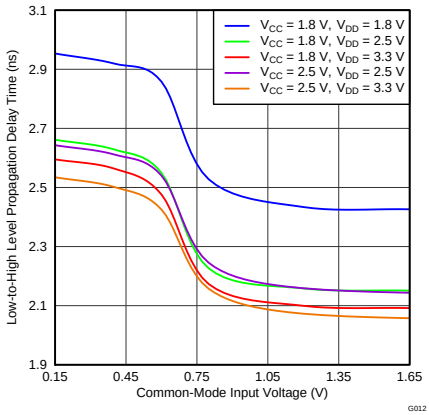


Figure 12. Propagation Delay, Low-to-High vs. Common-Mode Voltage

Copyright © 2011–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

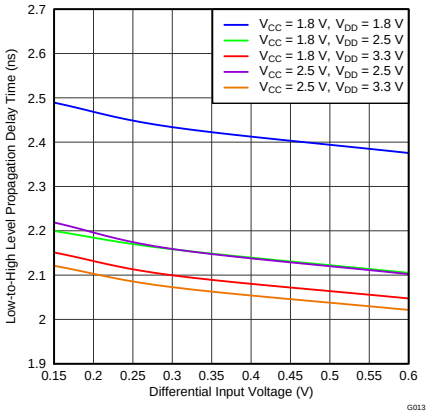


Figure 13. Propagation Delay, Low-to-High vs. Differential Input Voltage

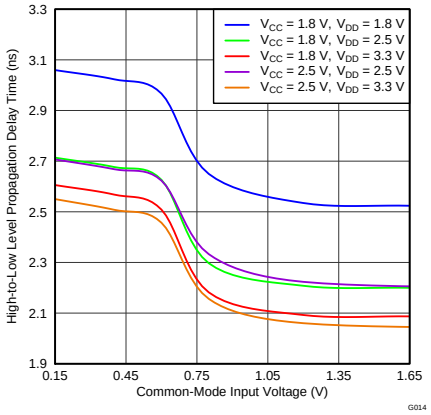


Figure 14. Propagation Delay, High-to-Low vs. Common-Mode Voltage

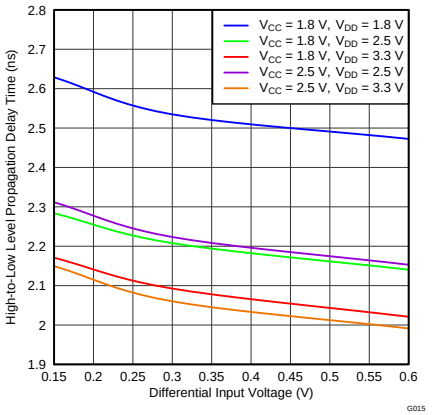


Figure 15. Propagation Delay, High-to-Low vs. Differential Input Voltage

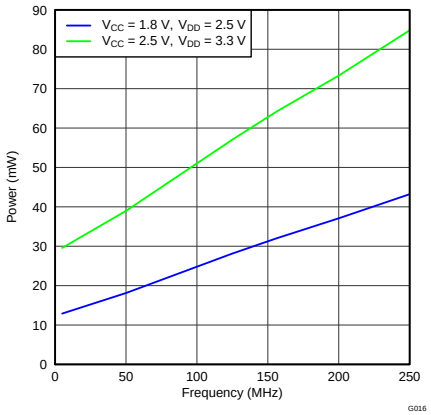


Figure 16. Power vs. Frequency

Copyright © 2011–2015, Texas Instruments Incorporated

7 Parameter Measurement Information

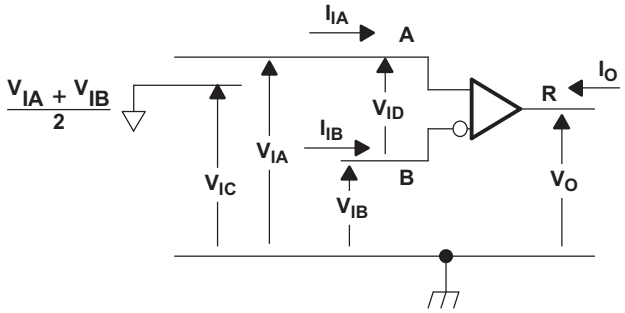
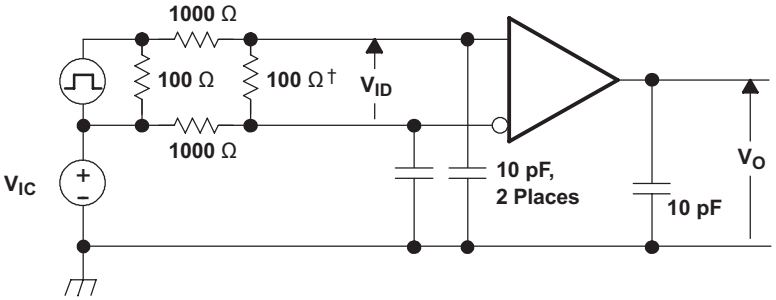
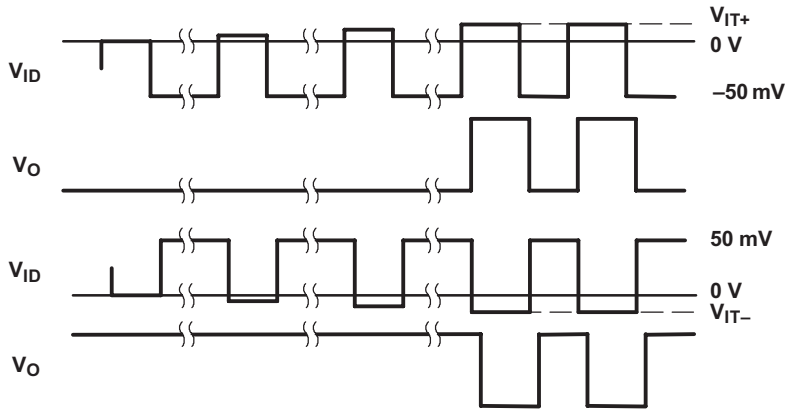


Figure 17. Receiver Voltage and Current Definitions



† Remove for testing LVDT device.
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.



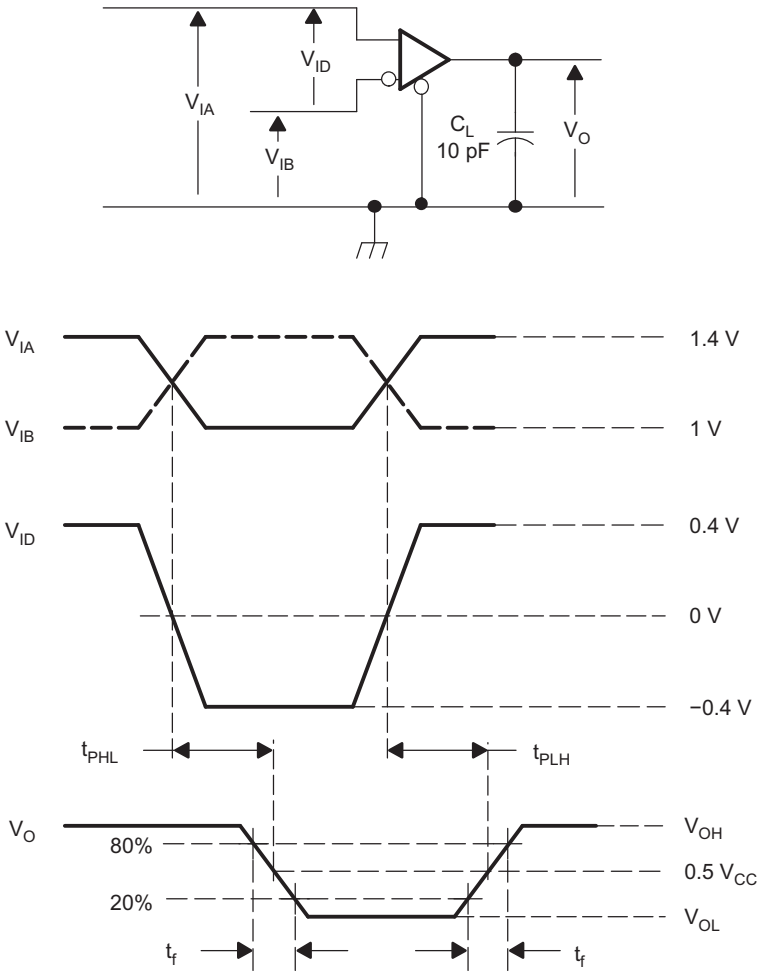
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

S0481-01

Figure 18. V_{IT+} and V_{IT-} Input Voltage Threshold Test Circuit and Definitions

Copyright © 2011–2015, Texas Instruments Incorporated

Parameter Measurement Information (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 19. Receiver Timing Test Circuit and Waveforms

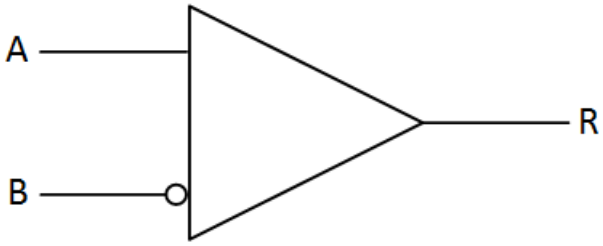
Copyright © 2011–2015, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN65LVDS4 device is a single-channel LVDS line receiver. It operates from two power supplies, VCC which is the core power supply and VDD which is the output drive power supply. The input signal to the SN65LVDS4 is a differential LVDS signal. The output of the device can be 3.3V LVTTL, 2.5V LVCMOS or 1.8V LVCMOS. This LVDS receiver requires ±50 mV of input signal to determine the correct state of the received signal. The SN65LVDS4 can be used in a point-to-point system or in a multidrop system.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Failsafe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that the output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, TI recommends to have an external failsafe solution as shown in Figure 20. In the external failsafe solution, the A side is pulled to V_{CC} via a weak pullup resistor and the B side is pulled down via a weak pulldown resistor. This creates a voltage offset and prevents the receiver from switching based on noise.

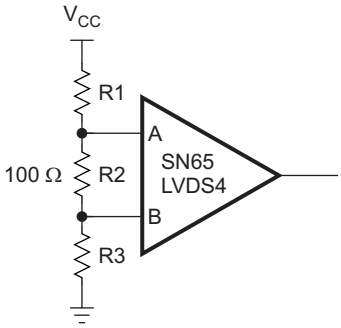


Figure 20. Open-Circuit Failsafe of the LVDS Receiver

8.3.1.1 R1 and R3 Calculation With VCC = 1.8 V

- Assume that an external failsafe bias of 25 mV is desired
- Bias current in this case is = 25 mV/100 Ω = 250 µA
- Next, determine the total resistance from VCC to ground = 1.8 V/250 µA = 7.2 kΩ
- Keeping the common mode bias of 1.25 V to the receiver, the value of R3 = 1.25 V/250 µA = 5 kΩ
- Thus, R1 = 2.2 kΩ

Copyright © 2011–2015, Texas Instruments Incorporated

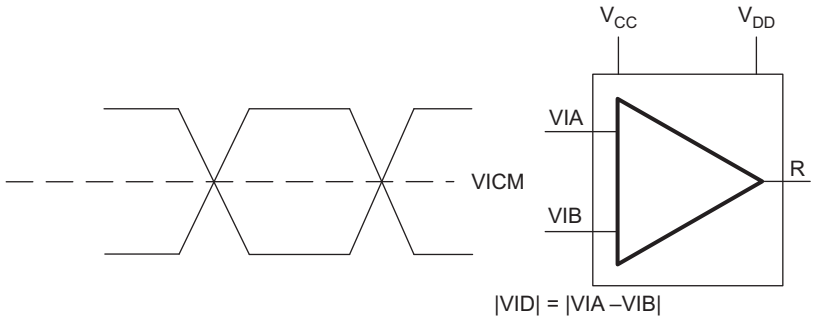
Feature Description (continued)

8.3.1.2 R1 and R3 Calculation With VCC = 2.5 V

- Assume that an external failsafe bias of 25 mV is desired
- Bias current in this case is = 25 mV/100 Ω = 250 µA
- Next, determine the total resistance from VCC to ground = 2.5 V/250 µA = 10 kΩ
- Keeping the common mode bias of 1.25 V to the receiver, the value of R3 = 1.25 V/250 µA = 5 kΩ
- Thus, R1 = 5 kΩ

8.4 Device Functional Modes

8.4.1 Maximum Input Voltage, $V_{IN(max)}$



$V_{CC2.5}$ (Note: Worst-Case VCC = 2.5 – 10% = 2.25 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.25	1.2	50	1.225
1.2	1.25	50	1.225
2.2	**2.25**	50	2.225
2.25	2.2	50	2.225
0.05	0	50	0.025
0	0.05	50	0.025

$V_{CC2.5}$ (Note: Worst-Case VCC = 2.5 – 10% = 2.25 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.5	0.9	600	1.2
0.9	1.5	600	1.2
1.65	**2.25**	600	1.95
2.25	1.65	600	1.95
0.6	0	600	0.3
0	0.6	600	0.3

$V_{CC1.8}$ (Note: Worst-Case VCC = 1.8 – 10% =1.62 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.25	1.2	50	1.225
1.2	1.25	50	1.225
1.57	**1.62**	50	1.595
1.62	1.57	50	1.595
0.05	0	50	0.025
0	0.05	50	0.025

$V_{CC1.8}$ (Note: Worst-Case VCC = 1.8 – 10% =1.62 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.5	0.9	600	1.2
0.9	1.5	600	1.2
1.02	**1.62**	600	1.32
1.62	1.02	600	1.32
0.6	0	600	0.3
0	0.6	600	0.3

Figure 21. Maximum Input Voltage Combination Allowed

Table 1. Function Table

INPUTS	OUTPUT(1)
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 50$ mV	H
$V_{ID} \leq –50$ mV	L

(1) H = high level, L = low level, ? = indeterminate

Copyright © 2011–2015, Texas Instruments Incorporated

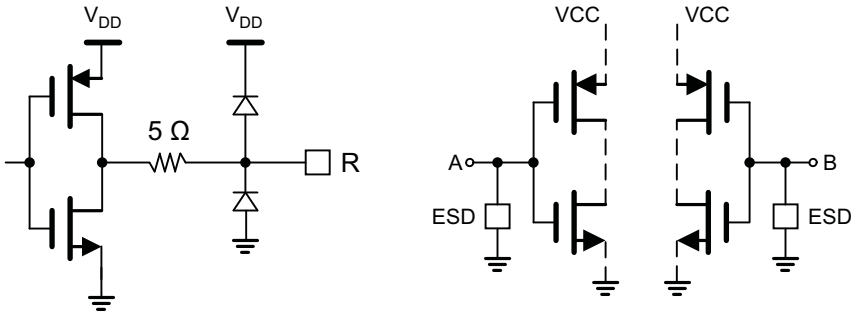


Figure 22. Receiver Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65LVDS4 device is a single-channel LVDS line receiver. This device is generally useful for building blocks for high-speed, point-to-point, data transmission where ground differences are less than 1 V. LVDS drivers and receivers provide high-speed signaling rates that are often implemented with ECL class devices without the ECL power and dual-supply requirements.

Copyright © 2011–2015, Texas Instruments Incorporated

9.2 Typical Application

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 23.

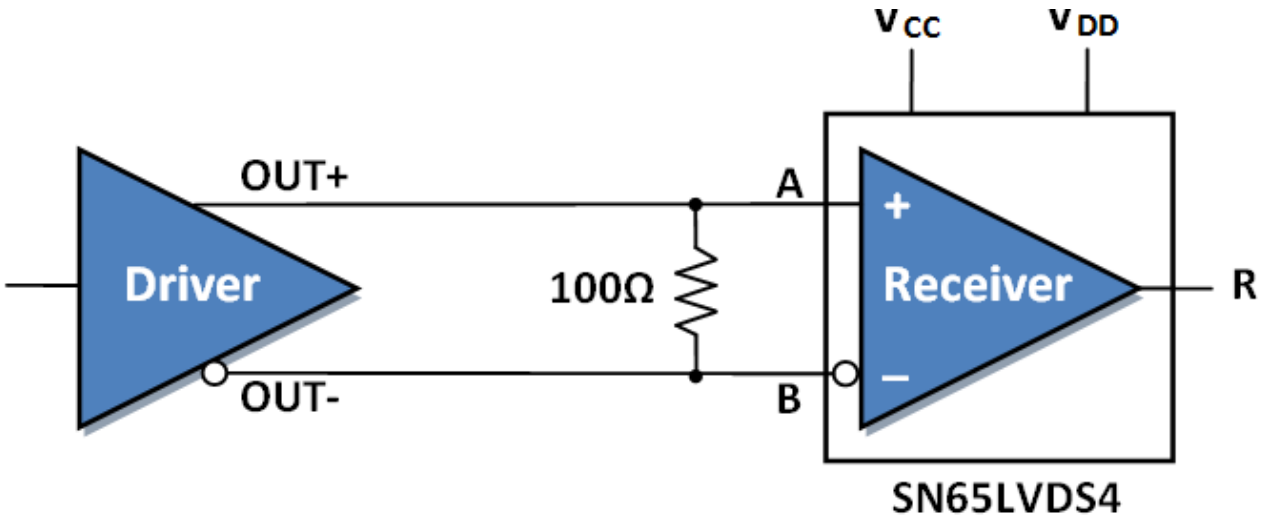


Figure 23. Point-to-point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 23 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

Copyright © 2011–2015, Texas Instruments Incorporated

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 500 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	1.8 to 2.5 V
Receiver Output Drive Voltage (VDDR)	0 to 3.6 V
Receiver Input Voltage	0 to 24 V
Receiver Signaling Rate	DC to 500 Mbps
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Receiver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very-low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one should resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson(1), equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.



Figure 24. Recommended LVDS Receiver Capacitor Layout

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

Copyright © 2011–2015, Texas Instruments Incorporated

9.2.2.2 Receiver Input Voltage

A standard-compliant LVDS driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 340 mV. This 340 mV is the absolute value of the differential swing (V_{OD} = $|V^+ – V^–|$). The peak-to-peak differential voltage is twice this value, or 680 mV.

9.2.2.3 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω).

9.2.2.4 PCB Transmission Lines

As per SNLA187, Figure 25 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 25 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

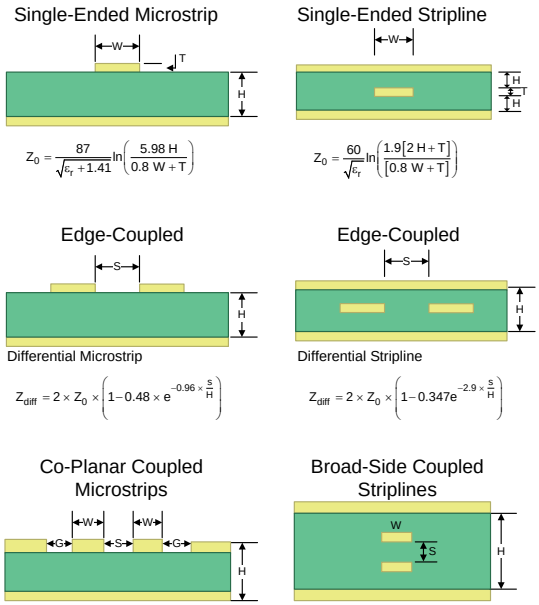


Figure 25. Controlled-Impedance Transmission Lines

Copyright © 2011–2015, Texas Instruments Incorporated

9.2.2.5 Termination Resistor

An LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 and 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line.

9.2.3 Application Curves

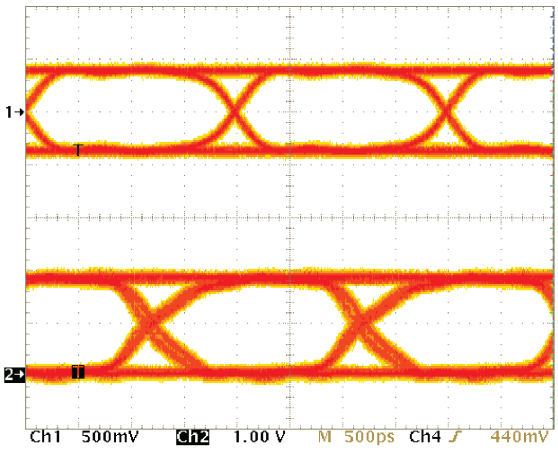


Figure 26. SN65LVDS4 Operating at 500 Mbps

Copyright © 2011–2015, Texas Instruments Incorporated

10 Power Supply Recommendations

There are two power supplies in SN65LVDS4, VCC which is the core power supply and VDD which is the output drive power supply. For proper device operation it is recommended that VCC should be powered up first and then VDD or VCC applied at the same time as VDD (VCC and VDD tied together). It is also recommended that VCC should be equal to or less than VDD as shown in Table 3.

Table 3. Power Supply Acceptable Combinations

VCC (V)	VDD (V)	Recommended
1.8	1.8	yes
1.8	2.5	yes
1.8	3.3	yes
2.5	1.8	no
2.5	2.5	yes
2.5	3.3	yes

Copyright © 2011–2015, Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 27.

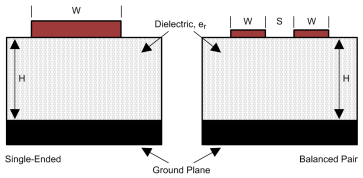


Figure 27. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1(1), 2(2), and 3(3) provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

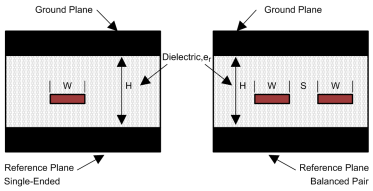


Figure 28. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 29.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Copyright © 2011–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

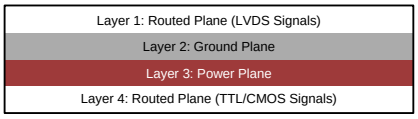


Figure 29. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 30.

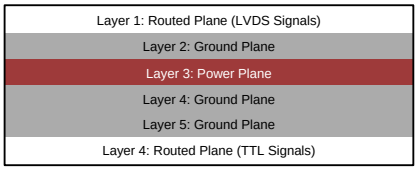


Figure 30. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

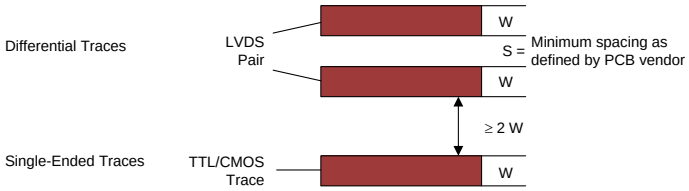


Figure 31. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

Copyright © 2011–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

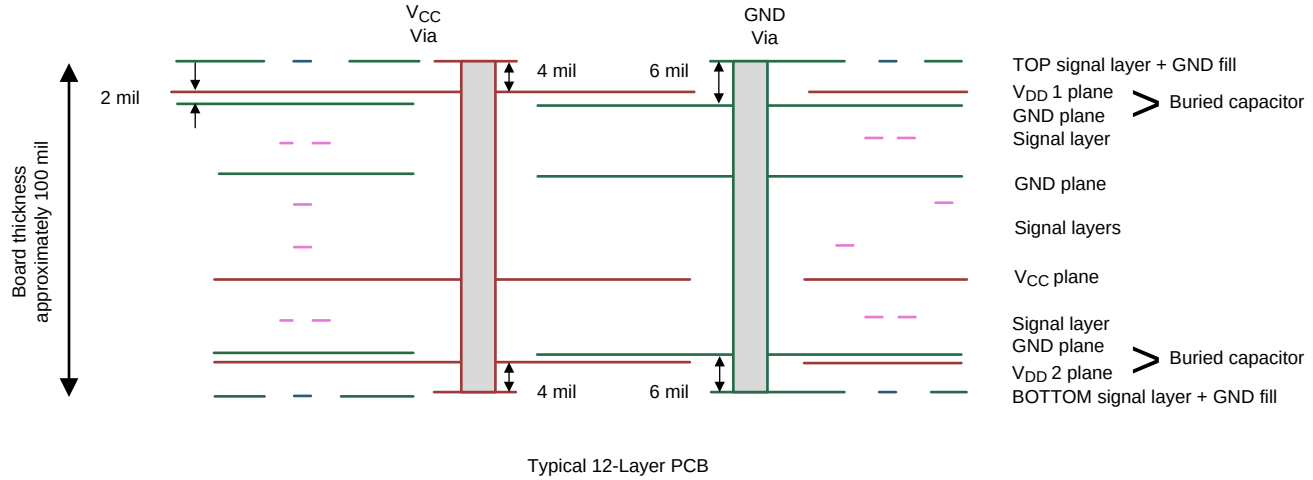


Figure 32. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 33(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 5-1 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 25) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in Figure 33(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

Copyright © 2011–2015, Texas Instruments Incorporated

Layout Guidelines (continued)



Figure 33. Typical Decoupling Capacitor Layouts

11.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 34.

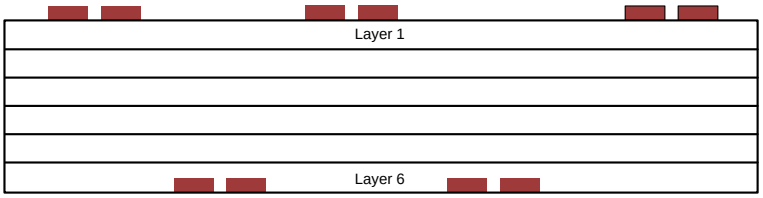


Figure 34. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 35. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

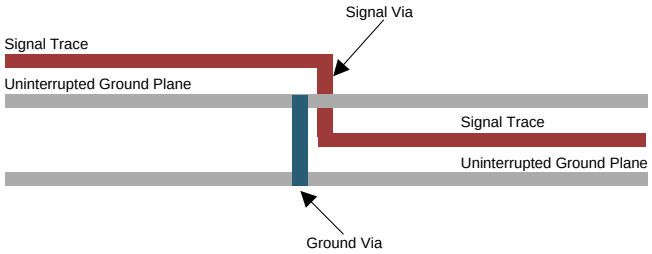


Figure 35. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

版权 © 2011–2015, Texas Instruments Incorporated

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

E2E is a trademark of Texas Instruments.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

版权 © 2011–2015, Texas Instruments Incorporated

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122
Copyright © 2016, 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS4RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	QXB	Samples
SN65LVDS4RSET	ACTIVE	UQFN	RSE	10	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	QXB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

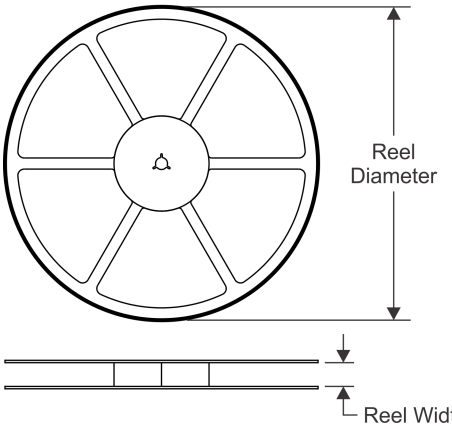
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

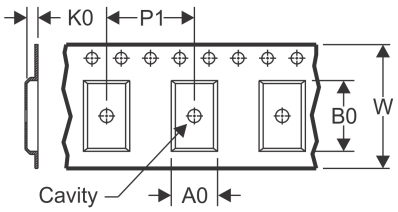
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

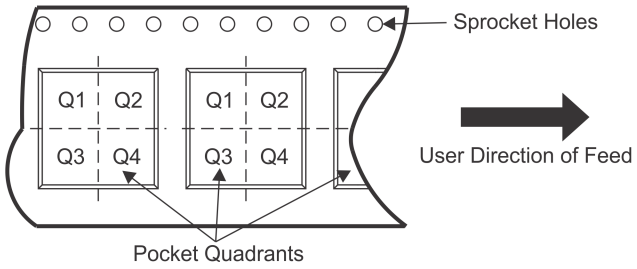


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

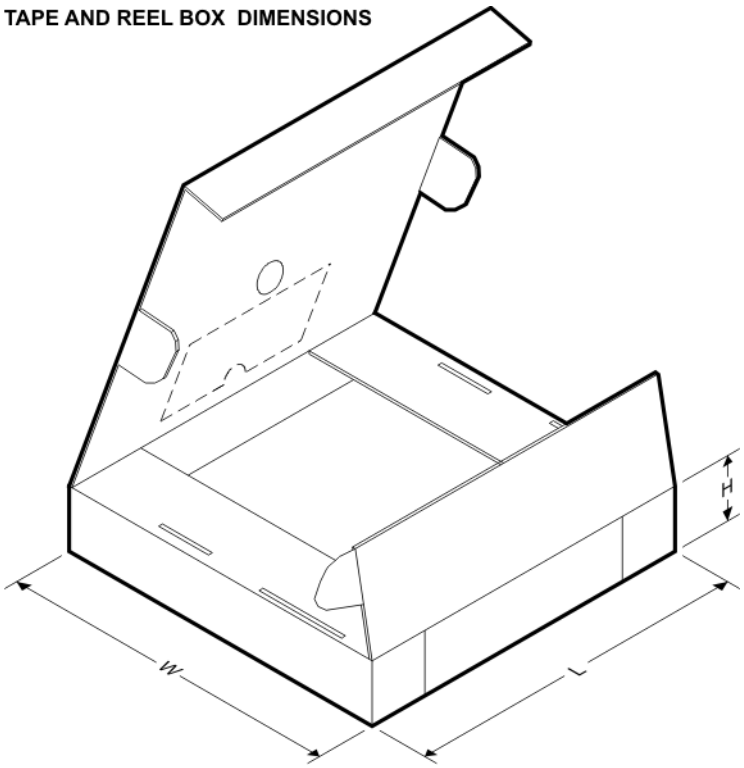
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS4RSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
SN65LVDS4RSET	UQFN	RSE	10	250	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

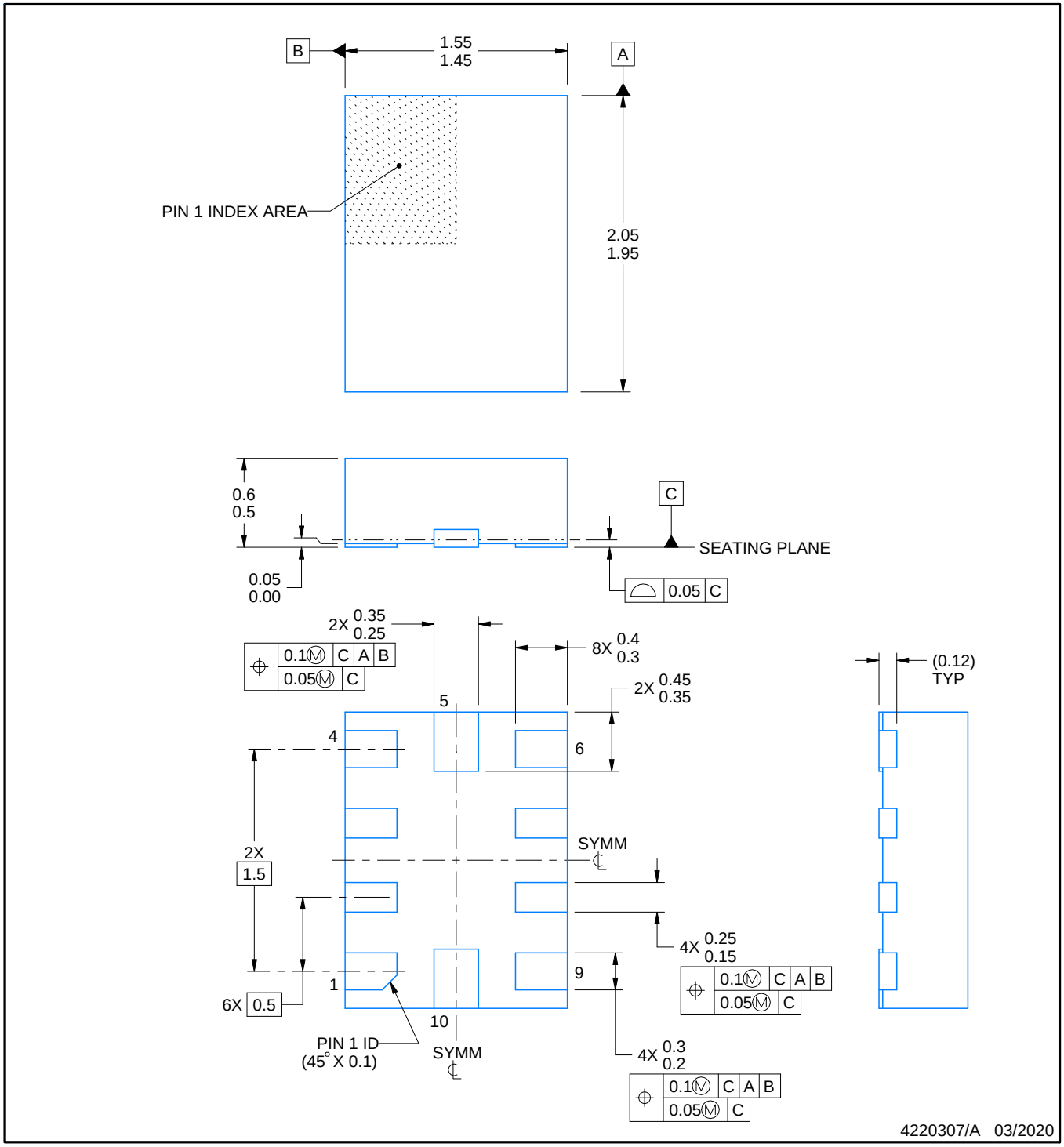
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS4RSER	UQFN	RSE	10	3000	202.0	201.0	28.0
SN65LVDS4RSET	UQFN	RSE	10	250	202.0	201.0	28.0

RSE0010A

PACKAGE OUTLINE

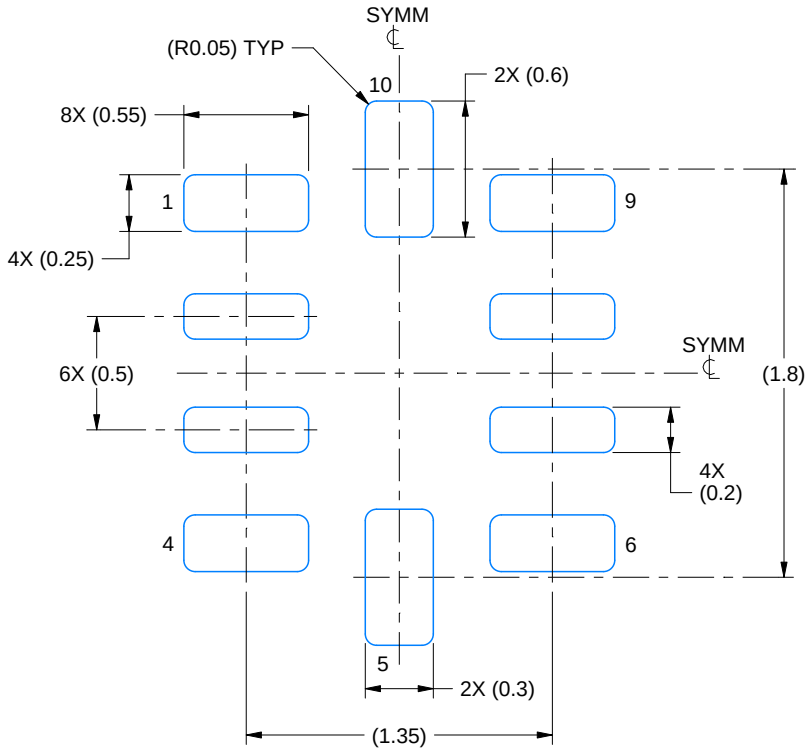
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

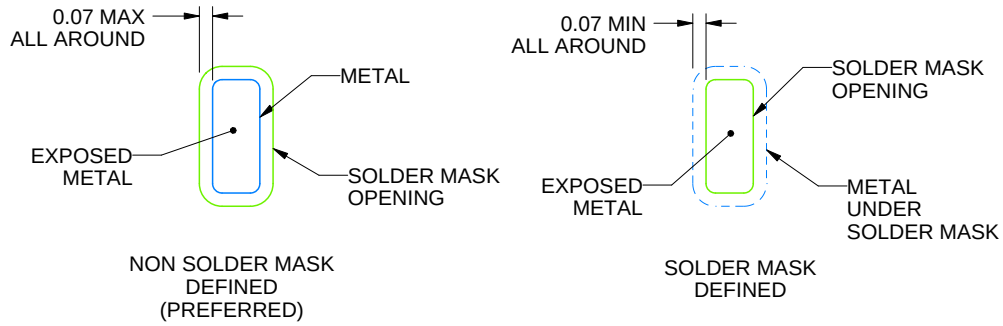


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

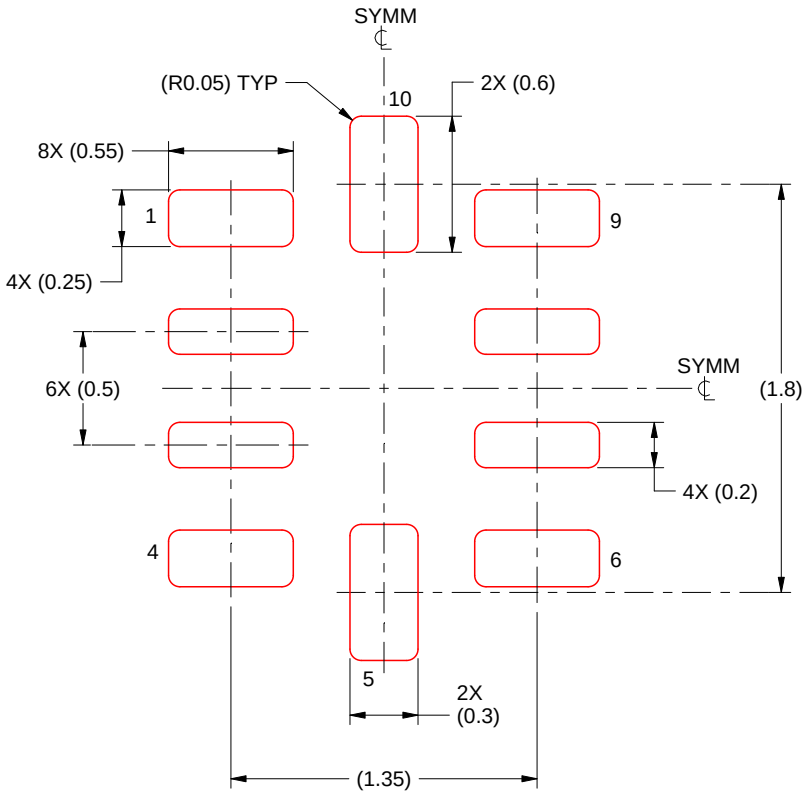


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司