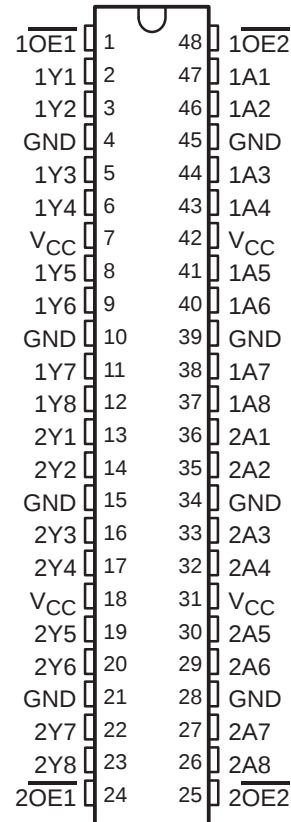


SN54ABT16541, SN74ABT16541A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS118C – FEBRUARY 1991 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54ABT16541 . . . WD PACKAGE
SN74ABT16541A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The SN54ABT16541 and SN74ABT16541A are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($\overline{1OE1}$ and $\overline{1OE2}$ or $\overline{2OE1}$ and $\overline{2OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16541 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16541A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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**TEXAS
INSTRUMENTS**

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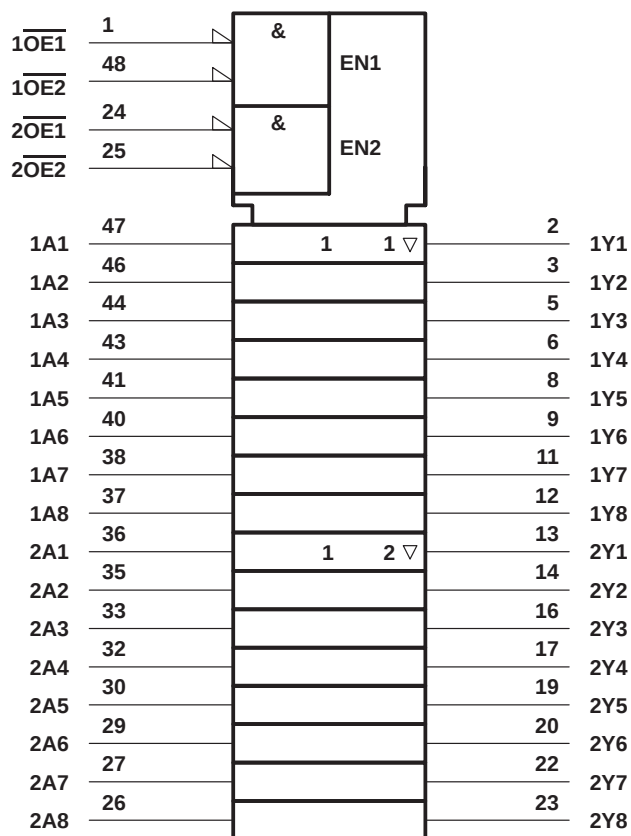
SN54ABT16541, SN74ABT16541A

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

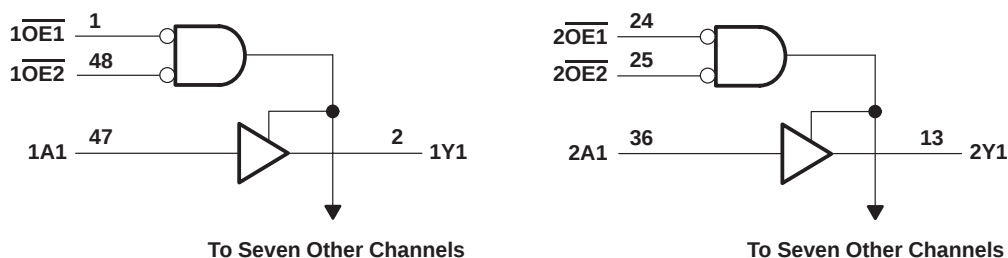
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT16541		SN74ABT16541A		UNIT	
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2		–1.2		V	
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5		V	
		V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3			
		V _{CC} = 4.5 V		I _{OH} = –24 mA		2		2				
				I _{OH} = –32 mA		2*				2		
V _{OL}		V _{CC} = 4.5 V		I _{OL} = 48 mA		0.55			0.55		V	
				I _{OL} = 64 mA		0.55*			0.55			
V _{hys}				100							mV	
I _I		V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA	
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		10			50		10		μA	
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.5 V		–10			–50		–10		μA	
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA	
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA	
I _{O‡}		V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA	
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		3		2		3		mA
				Outputs low		34		32		34		
				Outputs disabled		3		2		3		
ΔI _{CC} §	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		Outputs enabled		1		1.5		1		mA
				Outputs disabled		0.05		0.05		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5		1.5		1.5				
C _i		V _I = 2.5 V or 0.5 V		3.5							pF	
C _O		V _O = 2.5 V or 0.5 V		3.5							pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

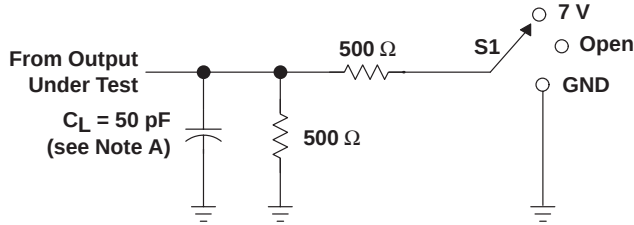
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

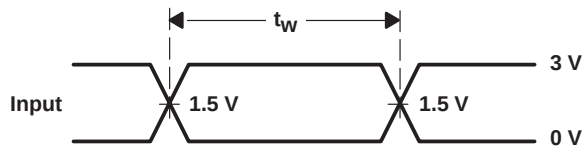
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT16541		SN74ABT16541A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1	2.1	3	1	3.5	1	3.4	ns
t _{PHL}			1	2.5	3.6	1	4.3	1	4.2	
t _{PZH}	$\overline{\text{OE}}$	Y	1.3	3.2	4.3	1.3	5.3	1.3	5.2	ns
t _{PZL}			1.6	3.8	4.7	1.6	6.2	1.6	6	
t _{PHZ}	$\overline{\text{OE}}$	Y	1.3	4.1	4.8	1.3	5.4	1.3	5.4	ns
t _{PLZ}			1	3.3	4	1	4.3	1	4.3	

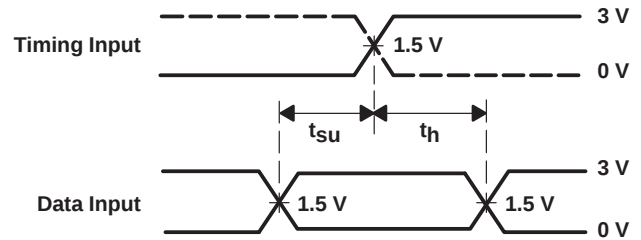
PARAMETER MEASUREMENT INFORMATION



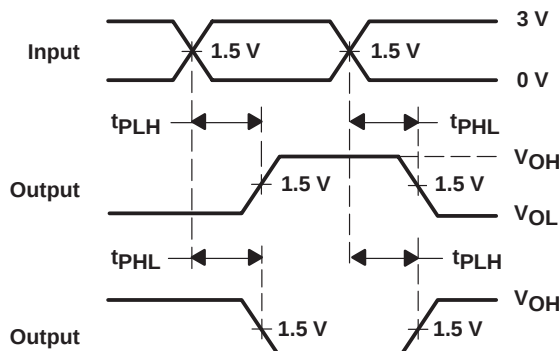
LOAD CIRCUIT



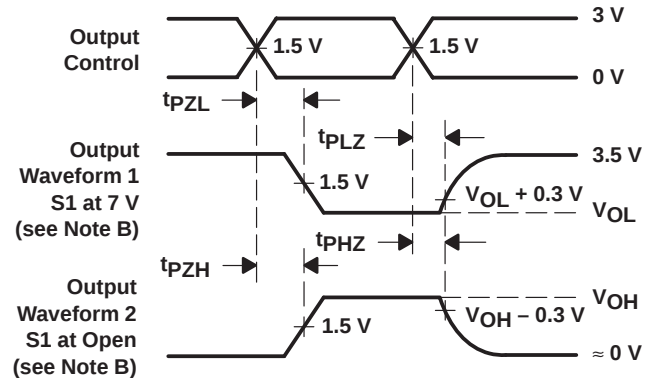
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT16541ADGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16541A	Samples
SN74ABT16541ADL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16541A	Samples
SN74ABT16541ADLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16541A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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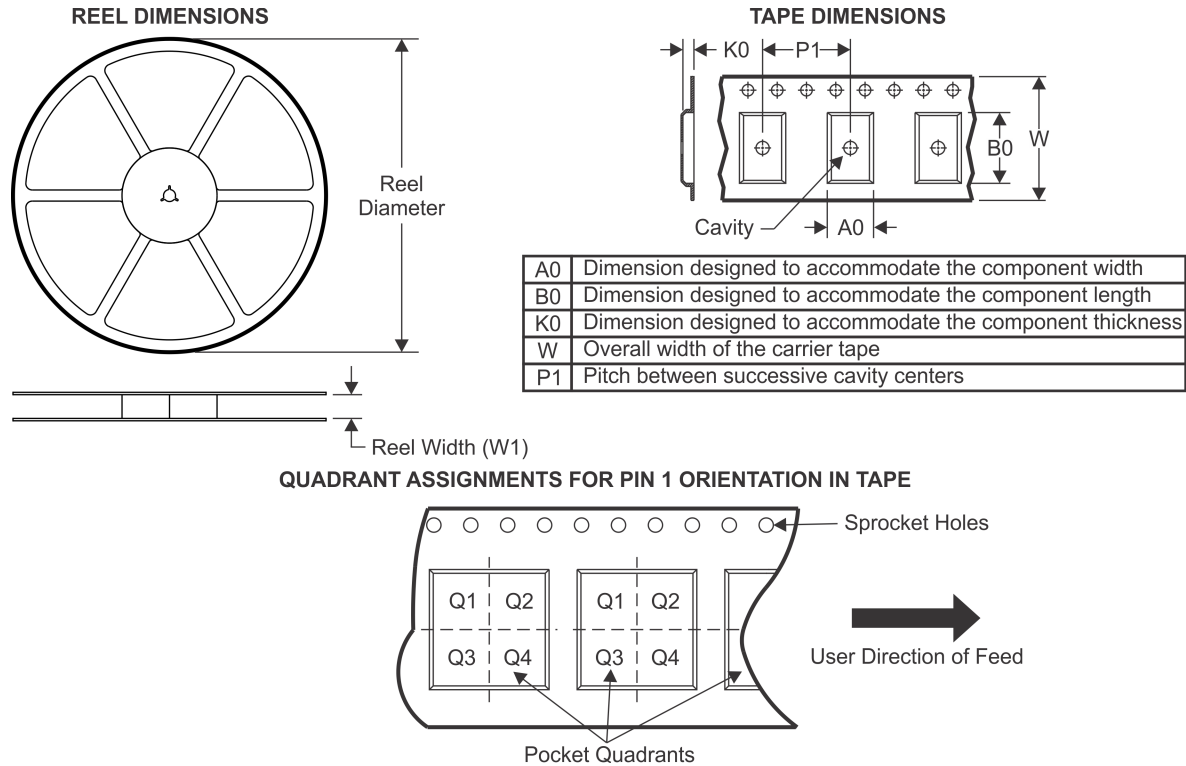
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PACKAGE OPTION ADDENDUM

10-Dec-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

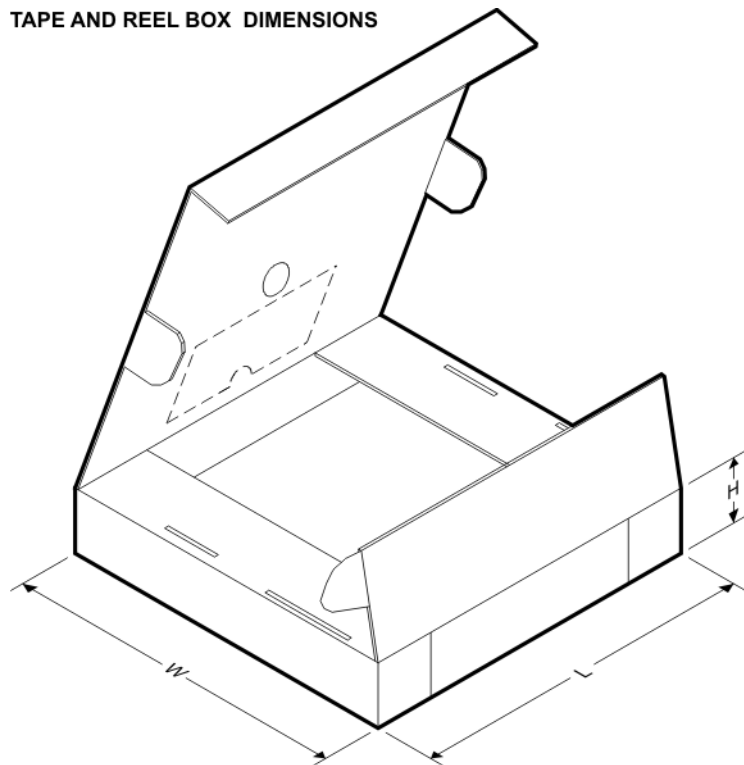
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16541ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT16541ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

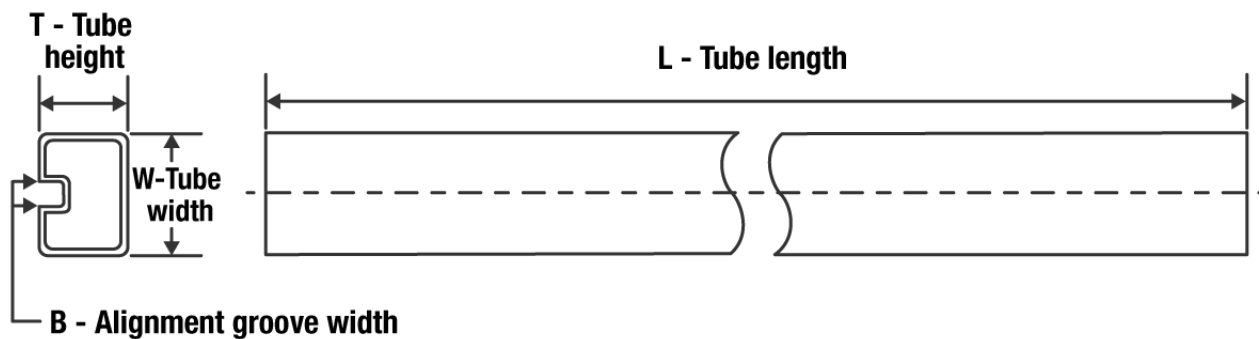
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16541ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16541ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

TUBE



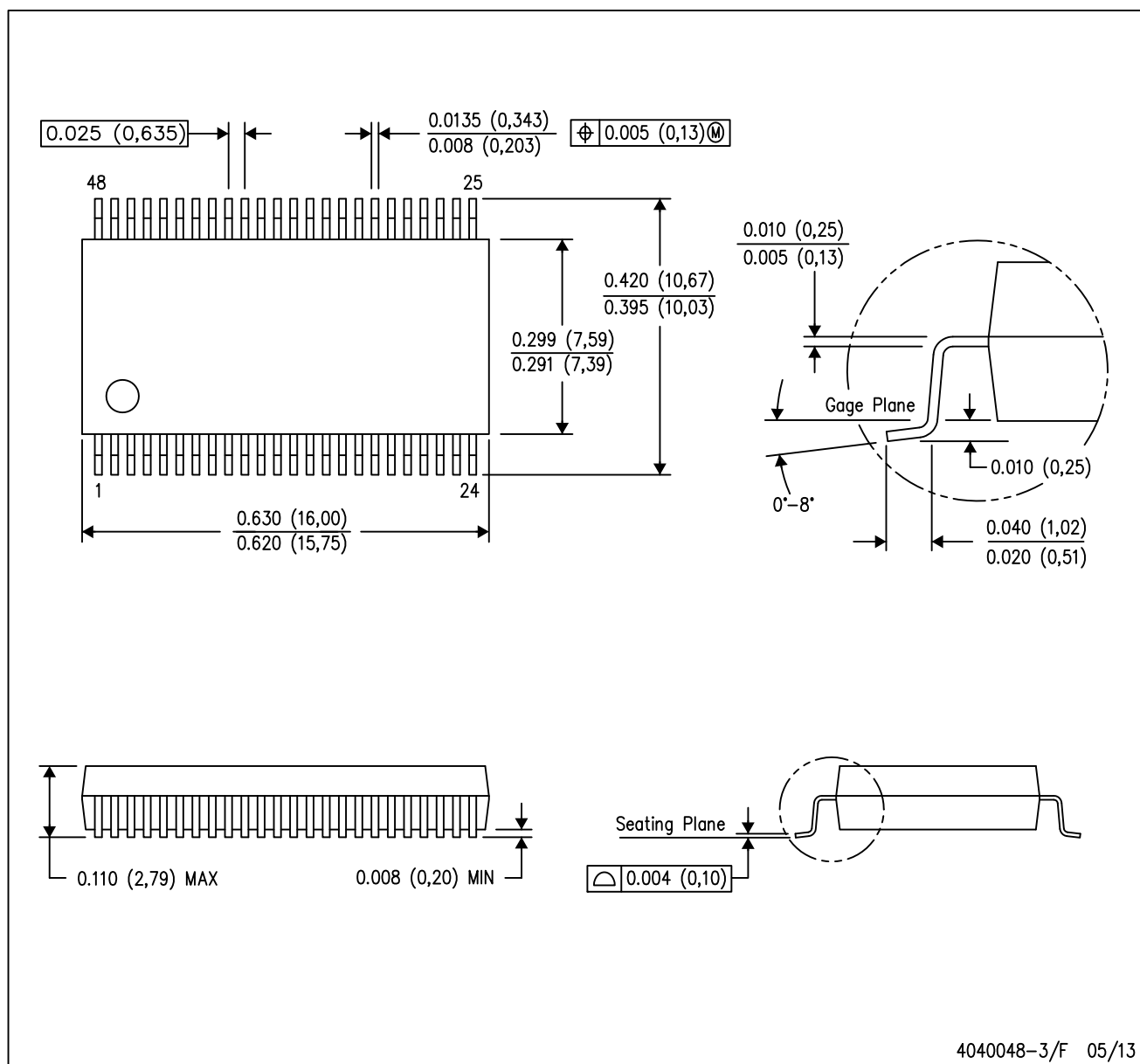
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16541ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87

MECHANICAL DATA

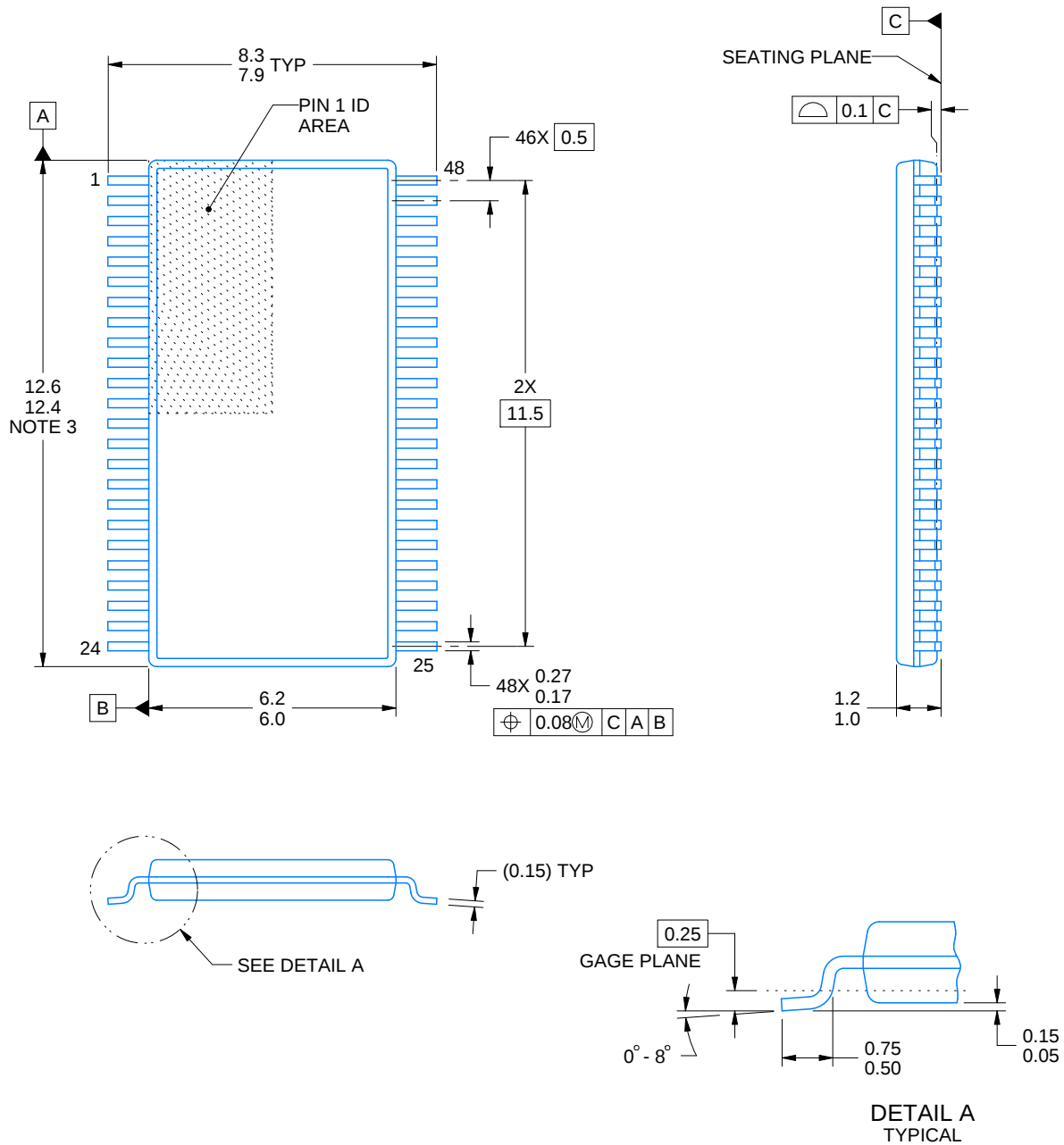
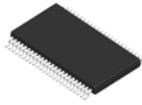
DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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4214859/B 11/2020

NOTES:

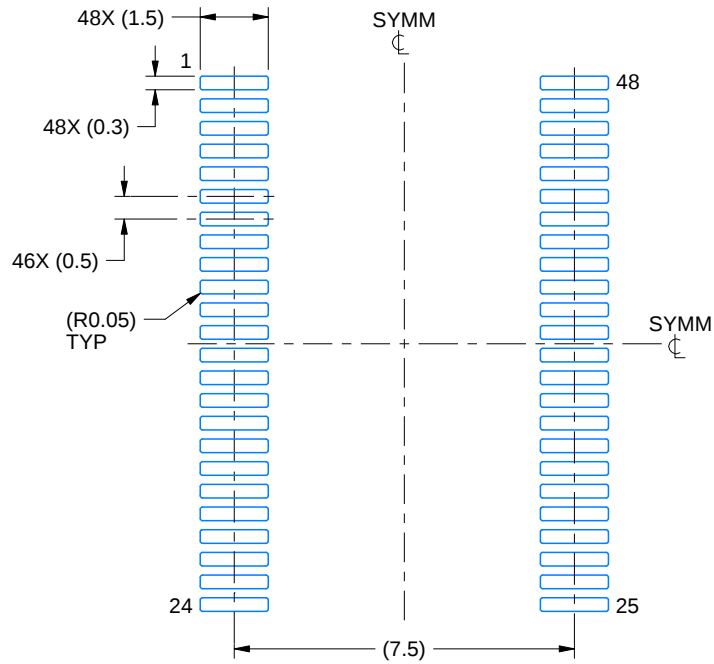
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

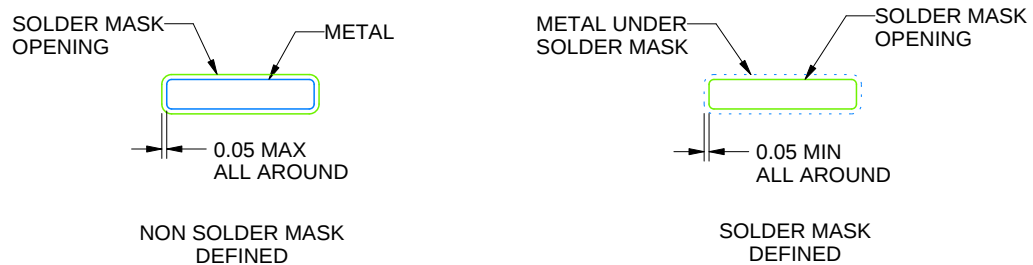
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

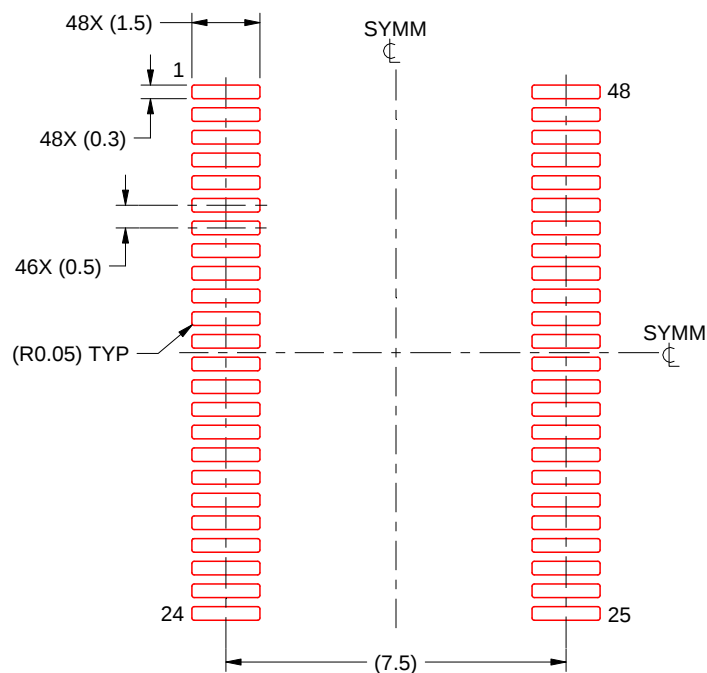
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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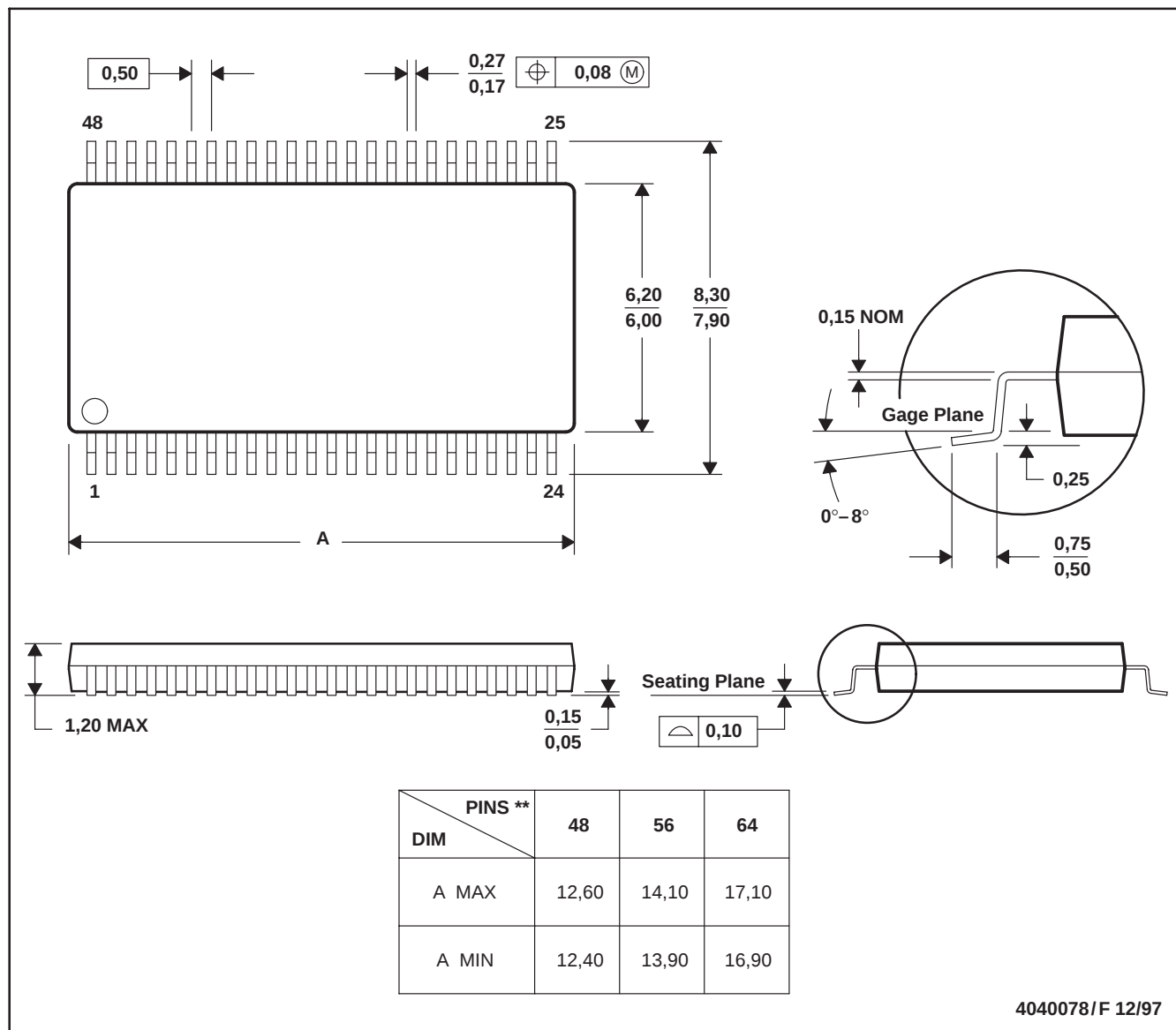
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
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