- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**

- **Typical V$_{OLP}$ (Output Ground Bounce) < 1 V at V$_{CC}$ = 5 V, T$_A$ = 25°C**

- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs**

SN54ABT2241 . . . J PACKAGE
SN74ABT2241 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

1OE	1	20	V$_{CC}$
1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN54ABT2241 . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4, 1A1, 1OE, V$_{CC}$, 2OE (pins 3, 2, 1, 20, 19)

1A2	4	18	1Y1
2Y3	5	17	2A4
1A3	6	16	1Y2
2Y2	7	15	2A3
1A4	8	14	1Y3

Bottom pins: 2Y1, GND, 2A1, 1Y4, 2A2 (pins 9, 10, 11, 12, 13)
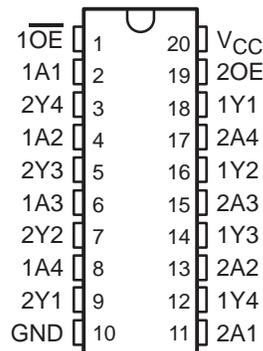
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT2240, SN74ABT2240A and 'ABT2244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.
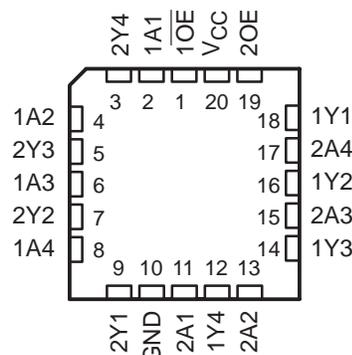
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V$_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT2241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2241 is characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS

SN54ABT2241, SN74ABT2241
OCTAL BUFFERS AND LINE/MOS DRIVERS
WITH 3-STATE OUTPUTS

SCBS233B – JANUARY 1991 – REVISED JANUARY 1997
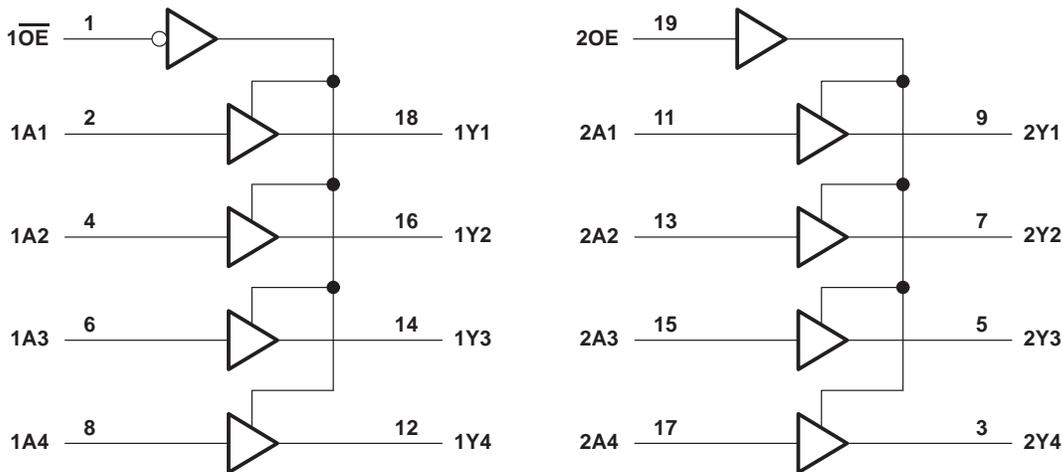
FUNCTION TABLES

INPUTS		OUTPUT
1$\overline{\text{OE}}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol[†]
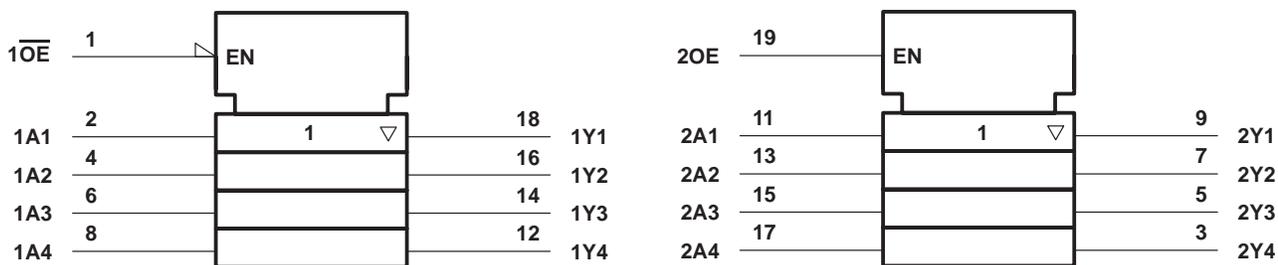
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

schematic of Y outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O .... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 115°C/W
                                                                     DW package .... 97°C/W
                                                                     N package .... 67°C/W
                                                                     PW package .... 128°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
         2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT2241, SN74ABT2241
OCTAL BUFFERS AND LINE/MOS DRIVERS
WITH 3-STATE OUTPUTS
SCBS233B – JANUARY 1991 – REVISED JANUARY 1997

recommended operating conditions (see Note 3)

			SN54ABT2241 MIN	SN54ABT2241 MAX	SN74ABT2241 MIN	SN74ABT2241 MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3:   Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER	TEST CONDITIONS		$T_A = 25°C$ MIN	TYP†	MAX	SN54ABT2241 MIN	MAX	SN74ABT2241 MIN	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
	V_{CC} = 4.5 V	I_{OH} = −24 mA	2			2				
		I_{OH} = −32 mA	2*					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	V
V_{hys}				100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50		50		50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50		−50		−50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high	1		250		250		250	µA
		Outputs low	24		30		30		30	mA
		Outputs disabled	0.5		250		250		250	µA
ΔI_{CC}§	Data inputs: V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			0.05		0.05		0.05	
	Control inputs: V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i	C_i	V_I = 2.5 V or 0.5 V		3						pF
C_o	C_o	V_O = 2.5 V or 0.5 V		8.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2241		SN74ABT2241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3	4.3	1	4.8	1	4.7	ns
t_{PHL}			1	4.3	5.3	1	5.7	1	5.6	
t_{PZH}	OE or $\overline{OE}$	Y	1.1	3.5	4.8	1.1	6.1	1.1	5.8	ns
t_{PZL}			2.1	6.2	7.6	2.1	8.6	2.1	8.4	
t_{PHZ}	OE or $\overline{OE}$	Y	1.7	4.2	5.6	1.7	6.7	1.7	6.6	ns
t_{PLZ}			1.7	3.9	5.8	1.7	6.9	1.7	6.4	

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

5

PARAMETER MEASUREMENT INFORMATION
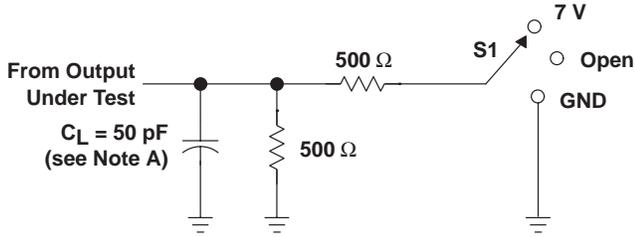
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
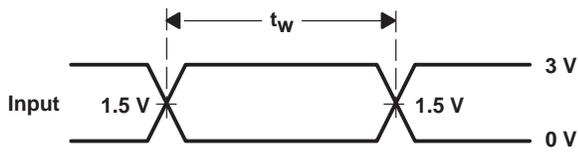
VOLTAGE WAVEFORMS
PULSE DURATION
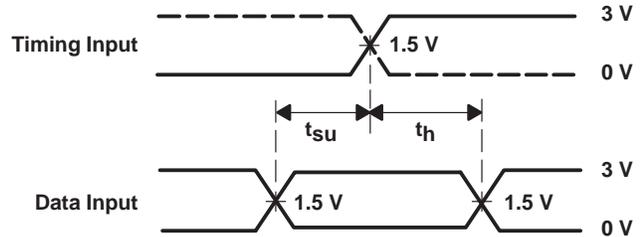
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
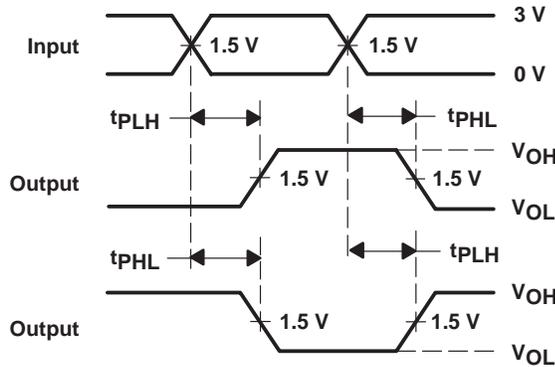
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
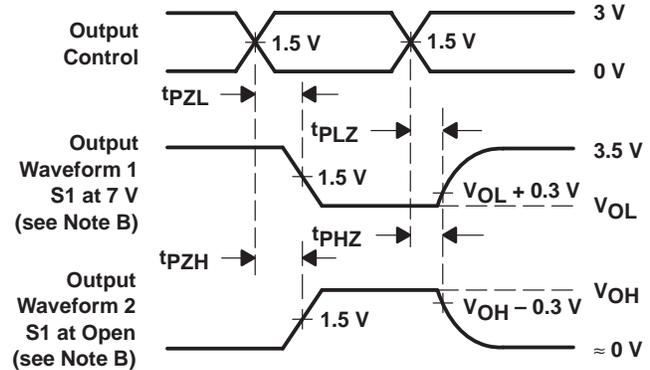
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
          Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
      D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT2241DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA241	Samples
SN74ABT2241DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2241	Samples
SN74ABT2241DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2241	Samples
SN74ABT2241PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA241	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
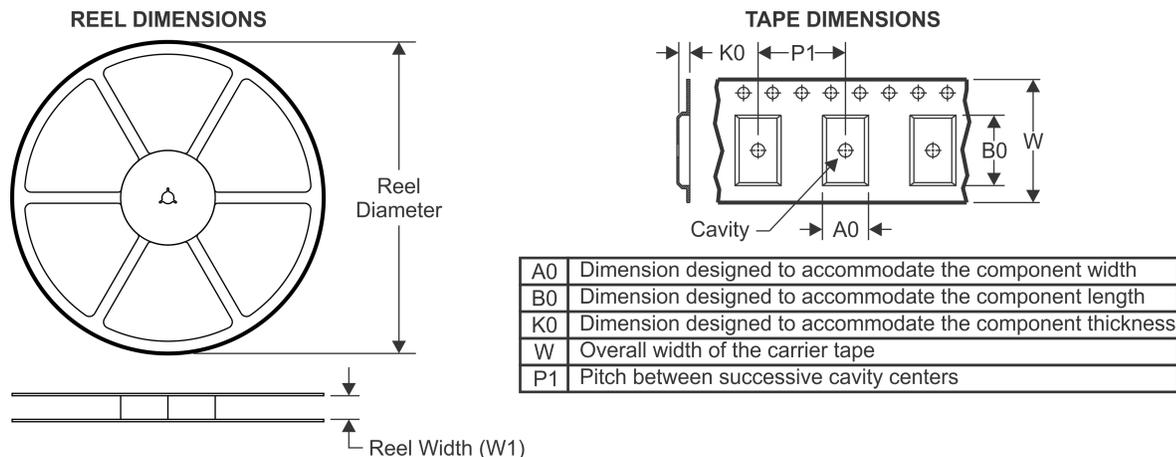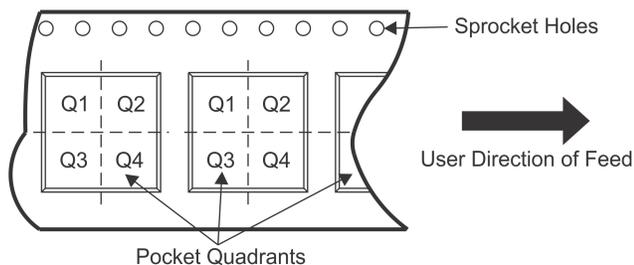
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2241DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT2241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT2241PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
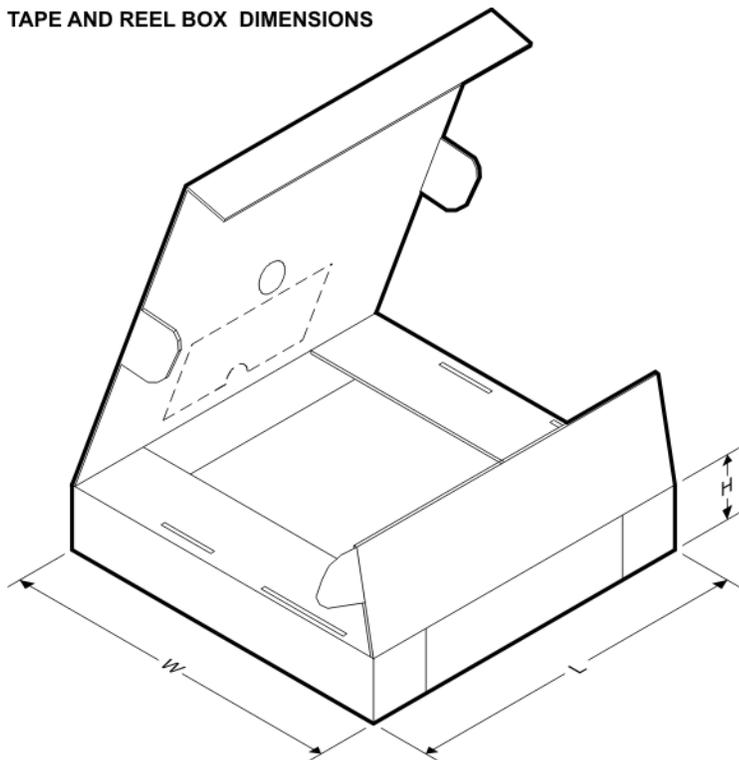
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2241DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74ABT2241DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT2241PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

PACKAGE MATERIALS INFORMATION

TUBE
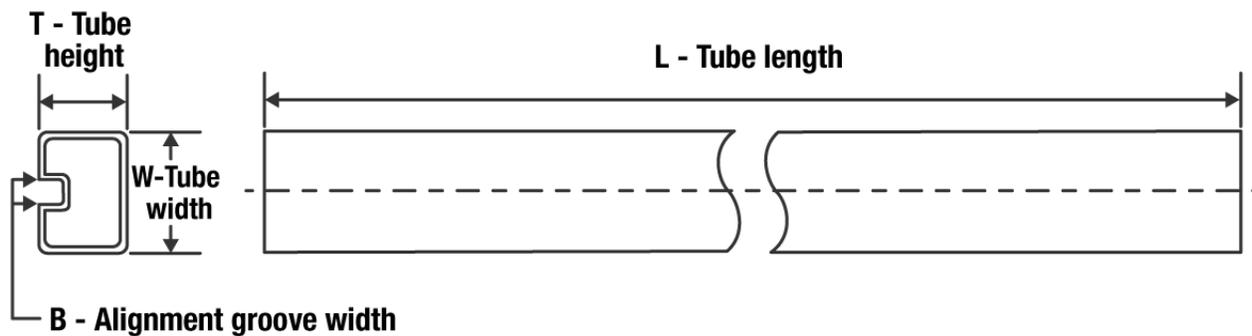
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT2241DW	DW	SOIC	20	25	507	12.83	5080	6.6

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

6.6
6.4
NOTE 3

2X

5.85

10

11

B

4.5
4.3
NOTE 4

20X 0.30
0.19

⊕ 0.1 Ⓜ C A B

C

SEATING PLANE

0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0° -8°

0.75
0.50

DETAIL A
TYPICAL
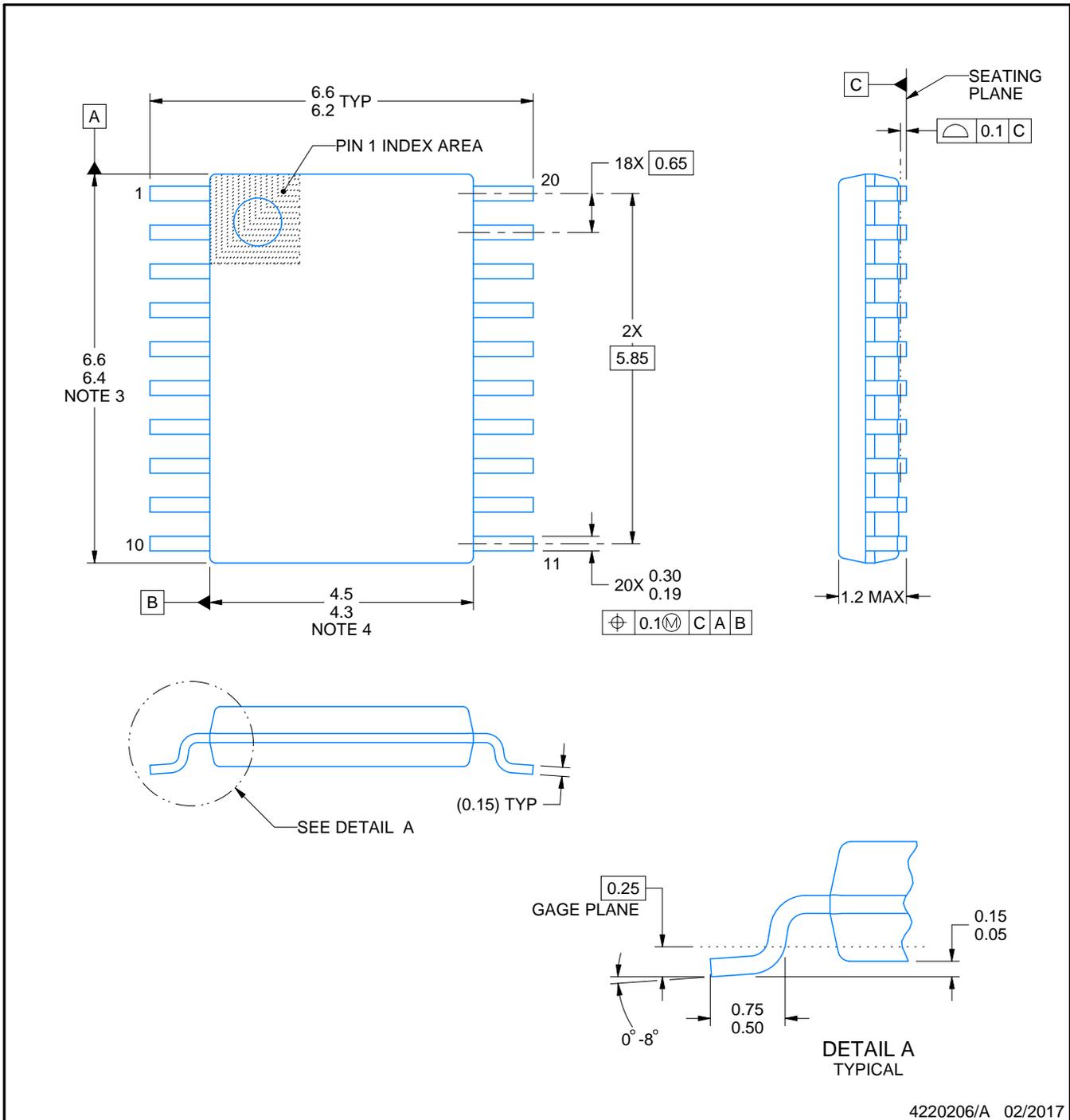
4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
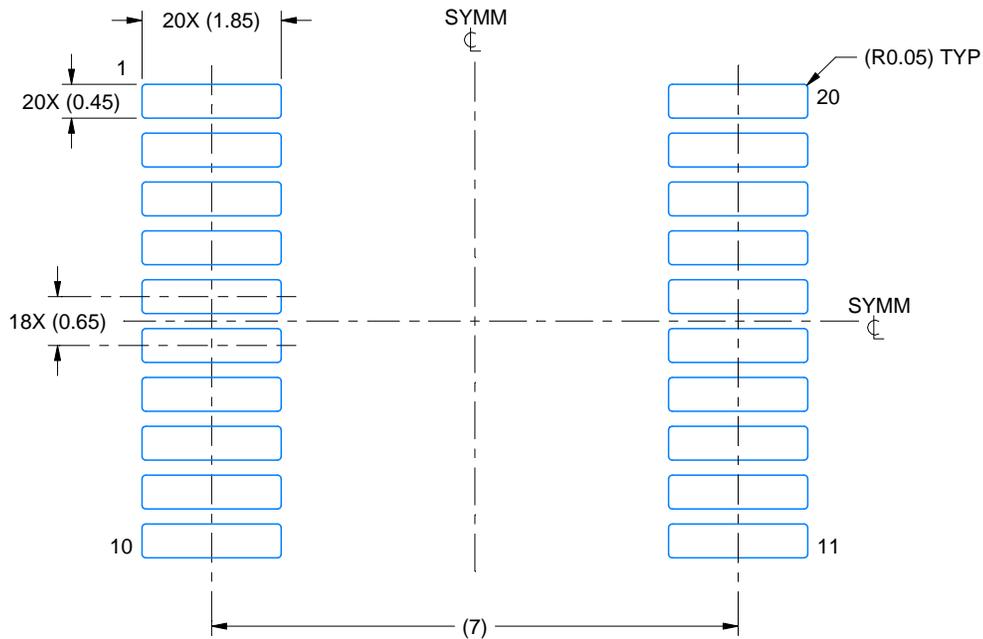2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS
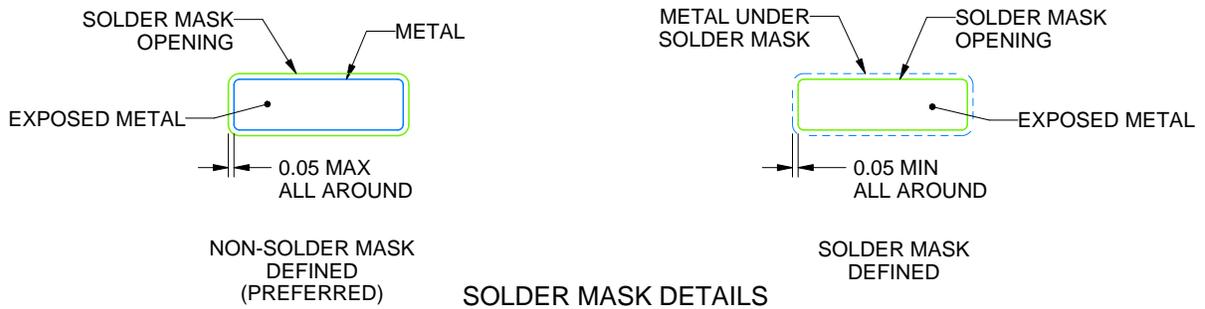
SOLDER MASK
DEFINED

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

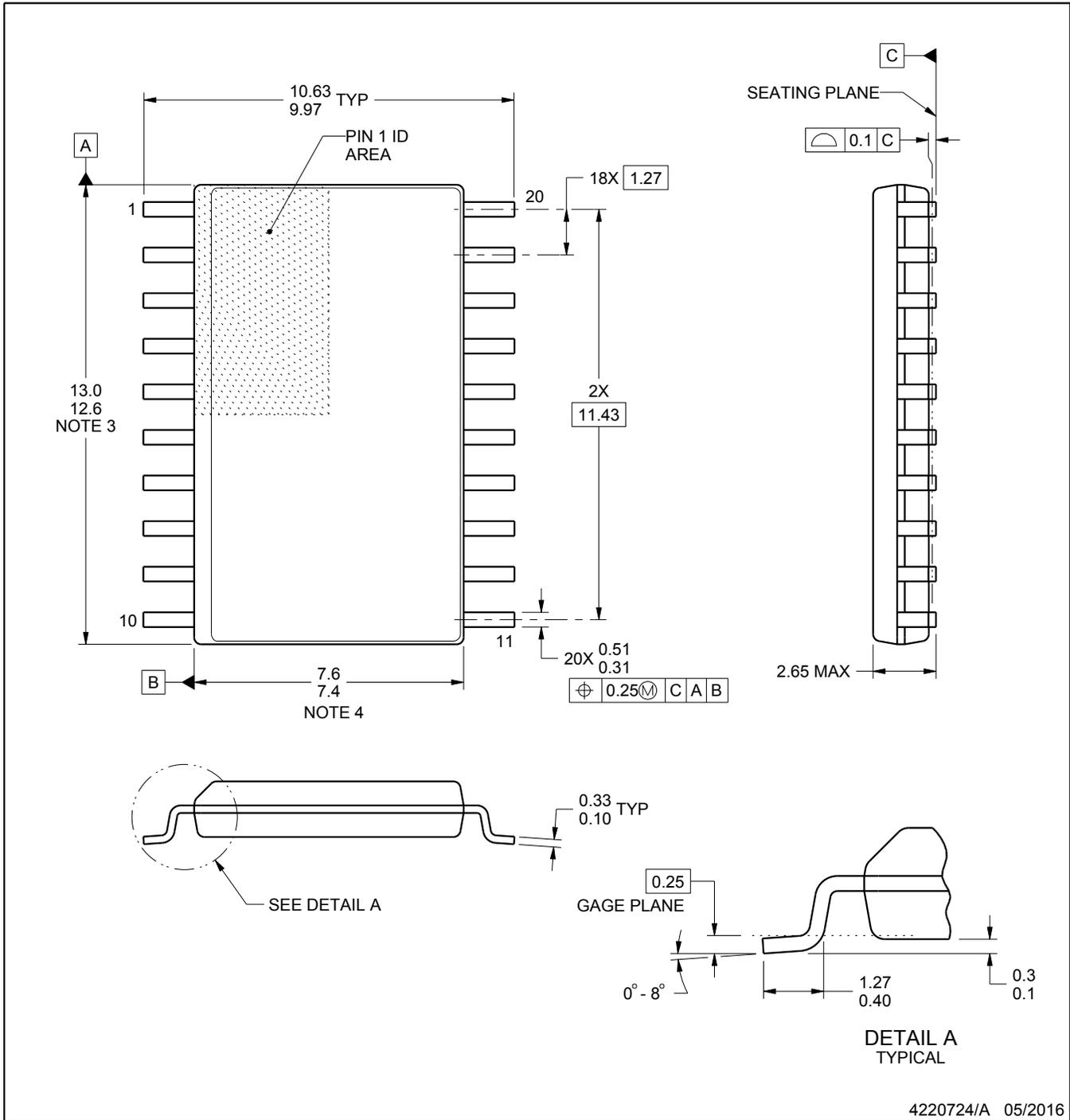PW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284-5/G   08/15
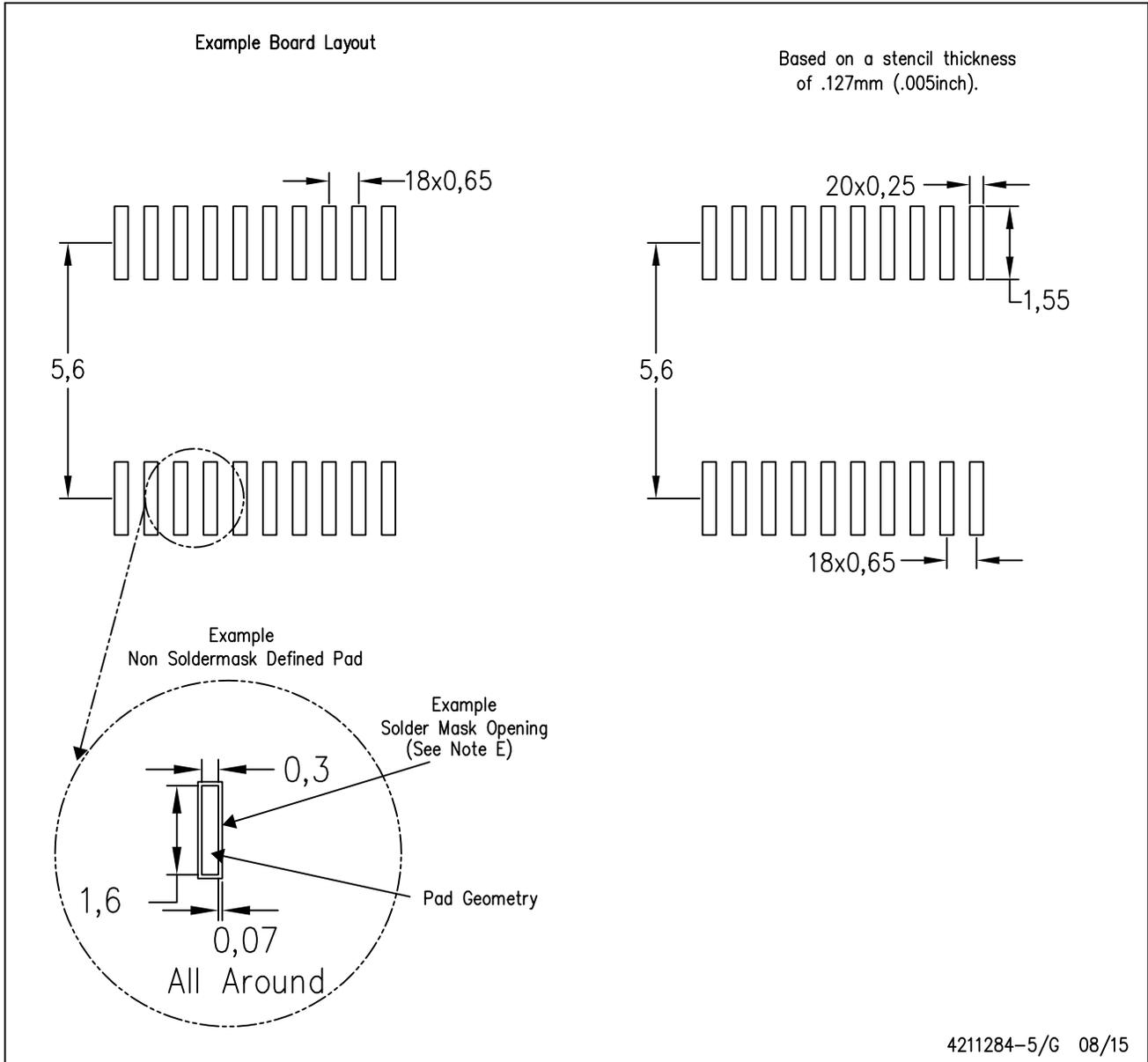
NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC-7351 is recommended for alternate design.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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8.2 TYP
7.4

A

PIN 1 INDEX AREA

1

18X 0.65

20

7.5
6.9
NOTE 3

2X
5.85

10

11

B

5.6
5.0
NOTE 4

20X 0.38
0.22

⊕ 0.1 Ⓜ C A B

C

◠ 0.1 C

SEATING
PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0° -8°

0.95
0.55

2 MAX

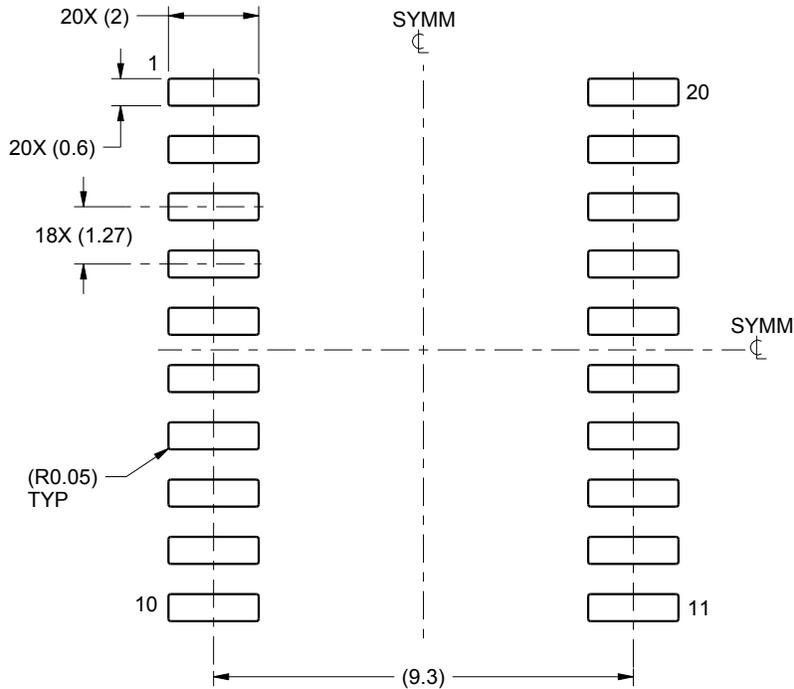0.05 MIN

DETAIL A
TYPICAL
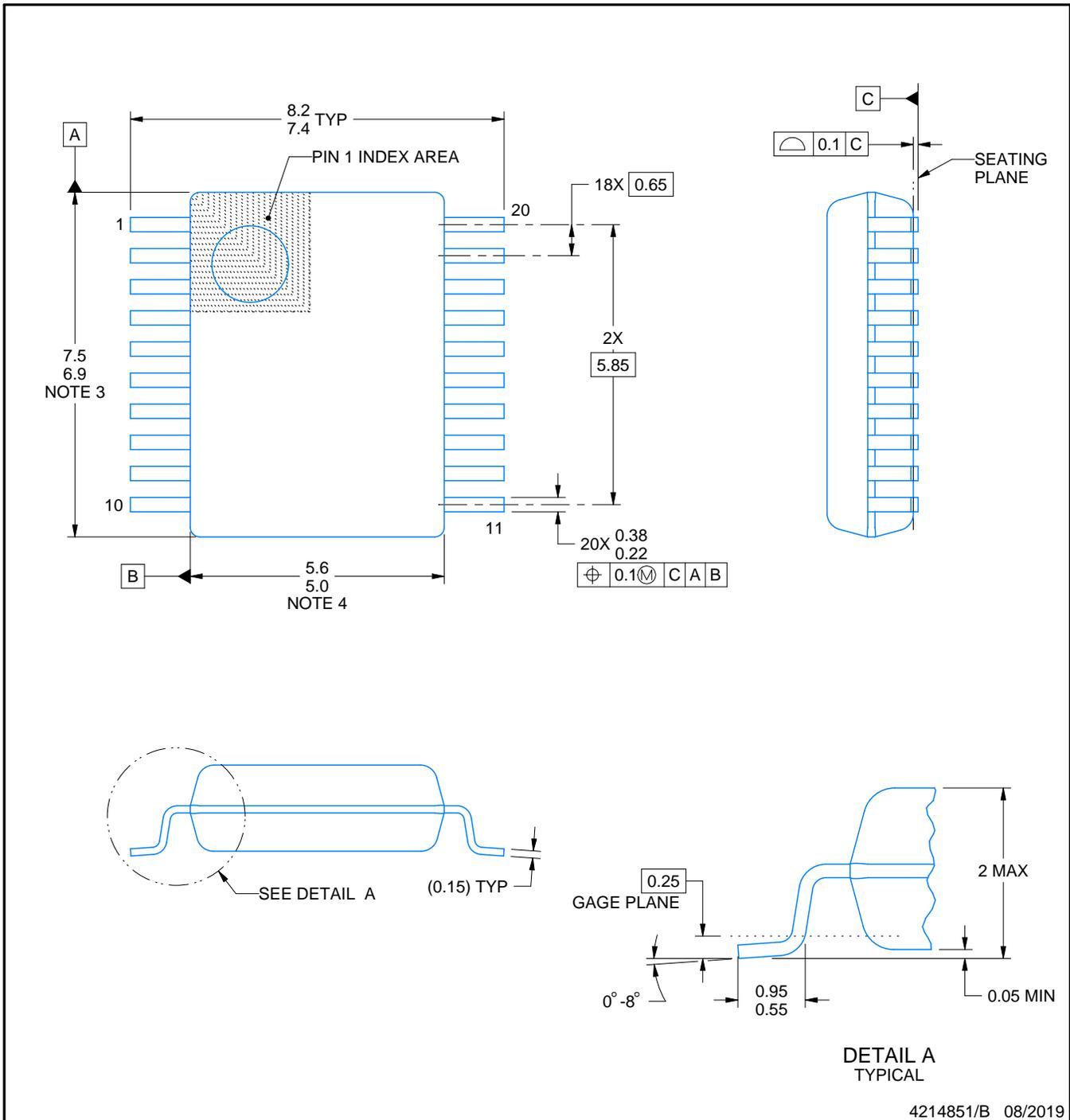
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
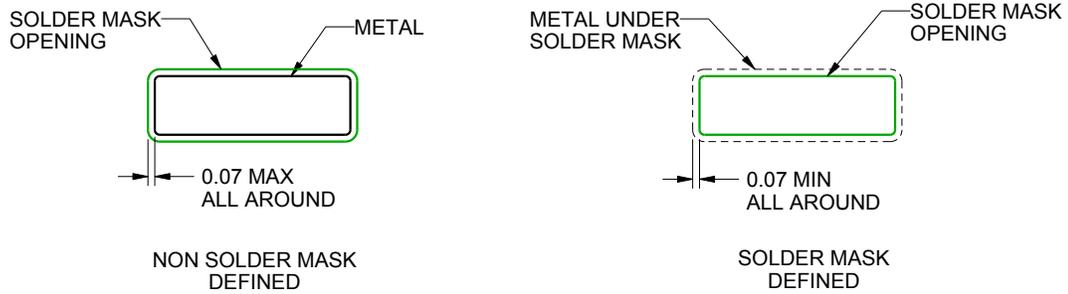5. Reference JEDEC registration MO-150.

DB0020A

20X (1.85)

1

20X (0.45)

20

(R0.05) TYP

SYMM

18X (0.65)

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

20X (1.85)

20X (0.45)

18X (0.65)

(R0.05) TYP

SYMM

SYMM

(7)

1

10

11

20

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

10.63 / 9.97 TYP

PIN 1 ID AREA

A

1

13.0 / 12.6 NOTE 3

10

B

7.6 / 7.4 NOTE 4

20

18X 1.27

2X 11.43

11

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

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7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)
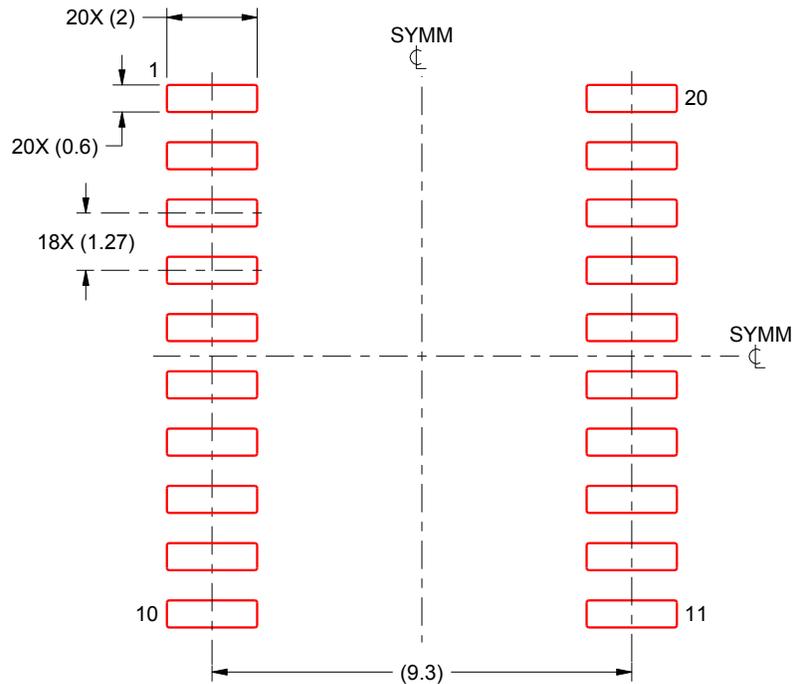
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

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