- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 8.5 ns at 5 V**
- **3-State Outputs Drive Bus Lines Directly**

description/ordering information

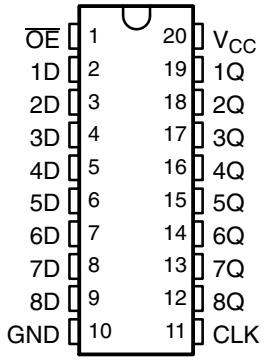
These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ′AC574 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

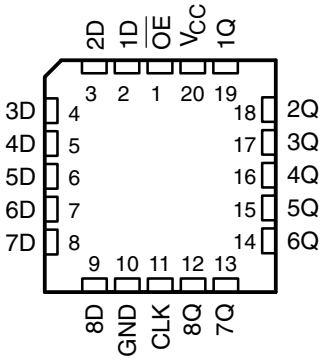
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC574 . . . J OR W PACKAGE
SN74AC574 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AC574 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AC574N	SN74AC574N
	SOIC – DW	Tube	SN74AC574DW	AC574
		Tape and reel	SN74AC574DWR	
	SOP – NS	Tape and reel	SN74AC574NSR	AC574
	SSOP – DB	Tape and reel	SN74AC574DBR	AC574
	TSSOP – PW	Tube	SN74AC574PW	AC574
		Tape and reel	SN74AC574PWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54AC574J	SNJ54AC574J
	CFP – W	Tube	SNJ54AC574W	SNJ54AC574W
	LCCC – FK	Tube	SNJ54AC574FK	SNJ54AC574FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

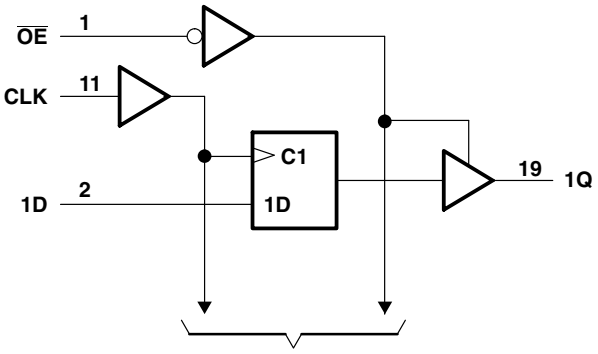
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AC574		SN74AC574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		–12		–12	mA
		V_{CC} = 4.5 V		–24		–24	
		V_{CC} = 5.5 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AC574		SN74AC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –12 mA	3 V	2.56			2.4		2.46		
	I_{OH} = –24 mA	4.5 V	3.94			3.7		3.76		
		5.5 V	4.94			4.7		4.76		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5		±2.5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AC574		SN74AC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		75		55		60	MHz
t_w	Pulse duration, CLK high or low	6		7.5		7		ns
t_{su}	Setup time, data before CLK↑	2.5		6.5		3		ns
t_h	Hold time, data after CLK↑	1.5		2.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AC574		SN74AC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		95		85		85	MHz
t_w	Pulse duration, CLK high or low	4		5		5		ns
t_{su}	Setup time, data before CLK↑	1.5		3.5		2		ns
t_h	Hold time, data after CLK↑	1.5		2.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC574		SN74AC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75	112		55		60		MHz
t_{PLH}	CLK	Q	3.5	8.5	13.5	1	16.5	3.5	15	ns
t_{PHL}			3.5	7.5	12	1	15	3.5	13.5	
t_{PZH}	$\overline{OE}$	Q	2.5	7	11	1	13	2.5	12	ns
t_{PZL}			3	6.5	10.5	1	12.5	3	11.5	
t_{PHZ}	$\overline{OE}$	Q	3.5	7.5	12	1	14	2.5	13	ns
t_{PLZ}			2	5.5	9	1	10.5	1.5	10	

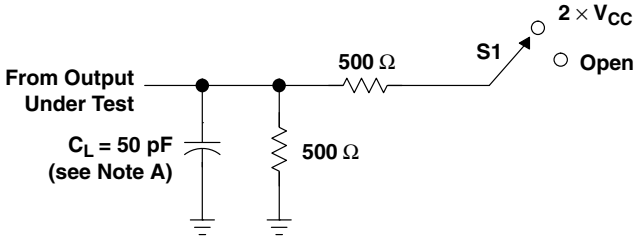
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC574		SN74AC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			95	153		85		85		MHz
t_{PLH}	CLK	Q	2	6	9.5	1.5	11.5	2	11	ns
t_{PHL}			2	5.5	8.5	1.5	10.5	2	9.5	
t_{PZH}	$\overline{OE}$	Q	2	5	8.5	1.5	9.5	2	9	ns
t_{PZL}			2	5	8	1.5	9.5	1.5	9	
t_{PHZ}	$\overline{OE}$	Q	2	6	9.5	1.5	11.5	1.5	10.5	ns
t_{PLZ}			1	4.5	7.5	1.5	9	1	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

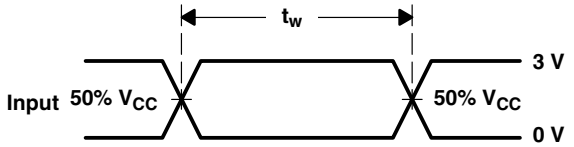
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION

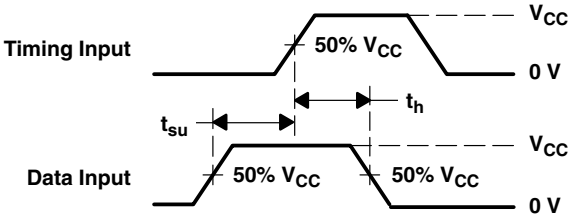


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

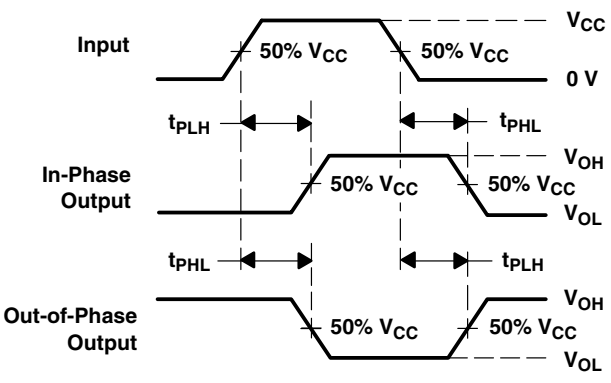
LOAD CIRCUIT



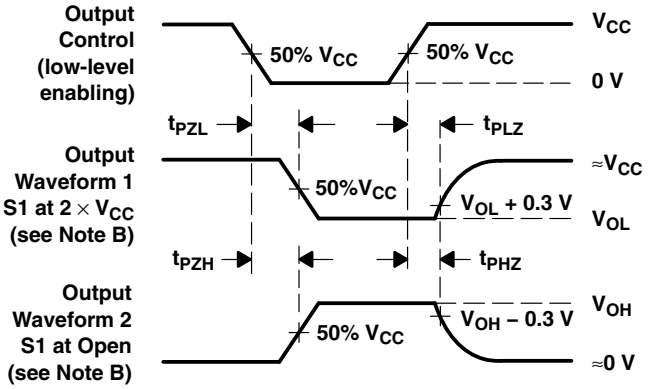
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9677301Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301Q2A SNJ54AC 574FK	Samples
5962-9677301QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J	Samples
5962-9677301QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W	Samples
SN74AC574DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	Samples
SN74AC574DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	Samples
SN74AC574DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	Samples
SN74AC574N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC574N	Samples
SN74AC574PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	Samples
SN74AC574PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	Samples
SN74AC574PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	Samples
SNJ54AC574FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301Q2A SNJ54AC 574FK	Samples
SNJ54AC574J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J	Samples
SNJ54AC574W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AC574, SN74AC574 :

- Catalog : SN74AC574
- Military : SN54AC574

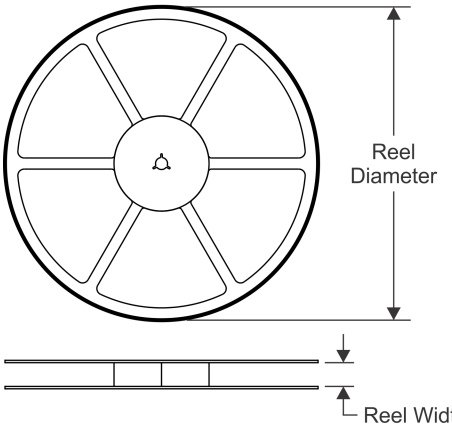
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

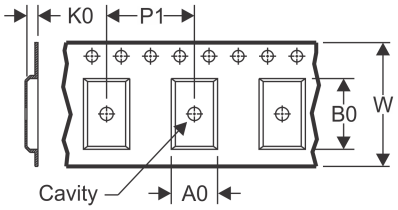
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

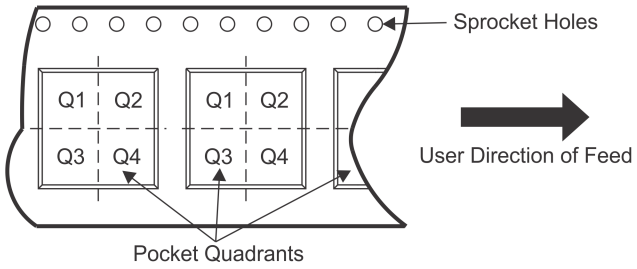


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

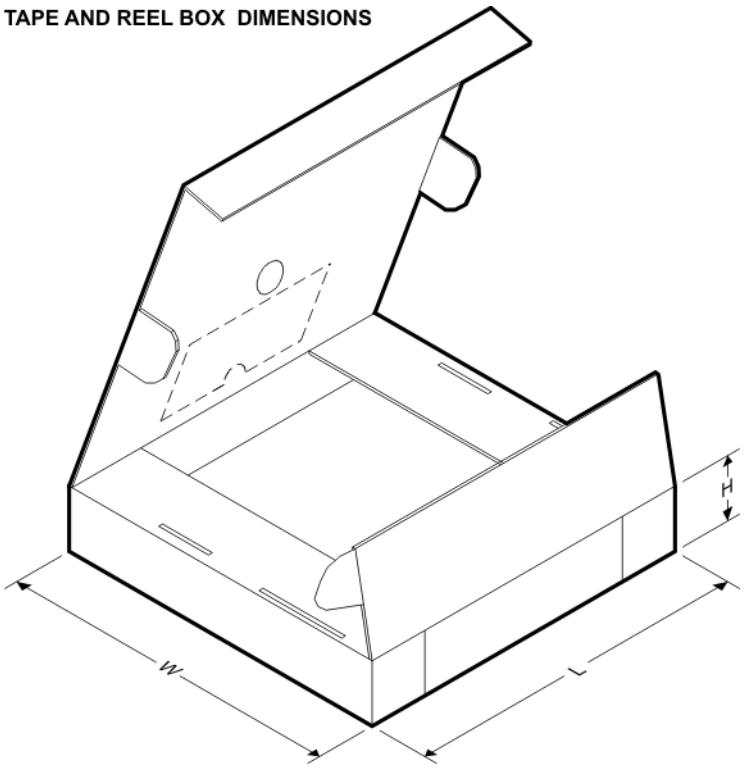
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

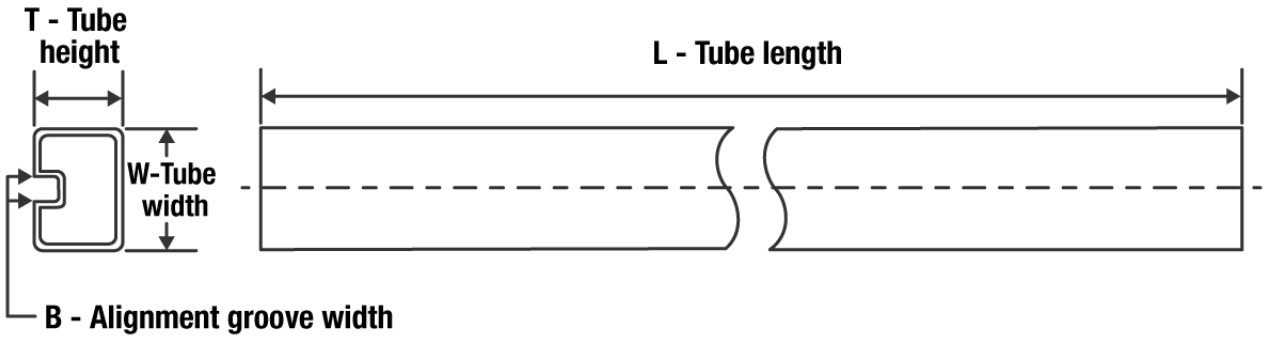
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC574DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74AC574DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC574PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

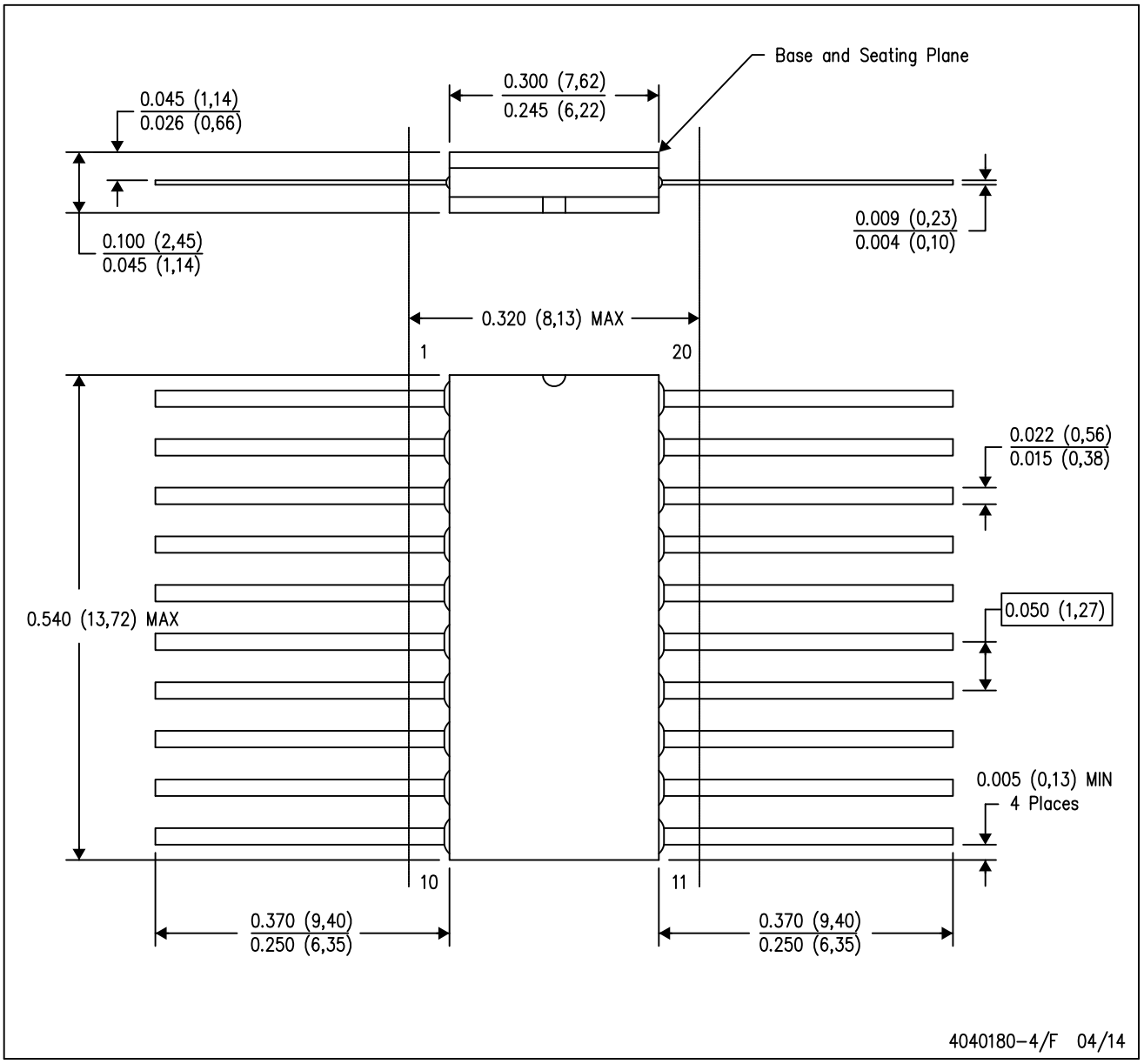
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9677301Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AC574DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AC574N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AC574PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54AC574FK	FK	LCCC	20	1	506.98	12.06	2030	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



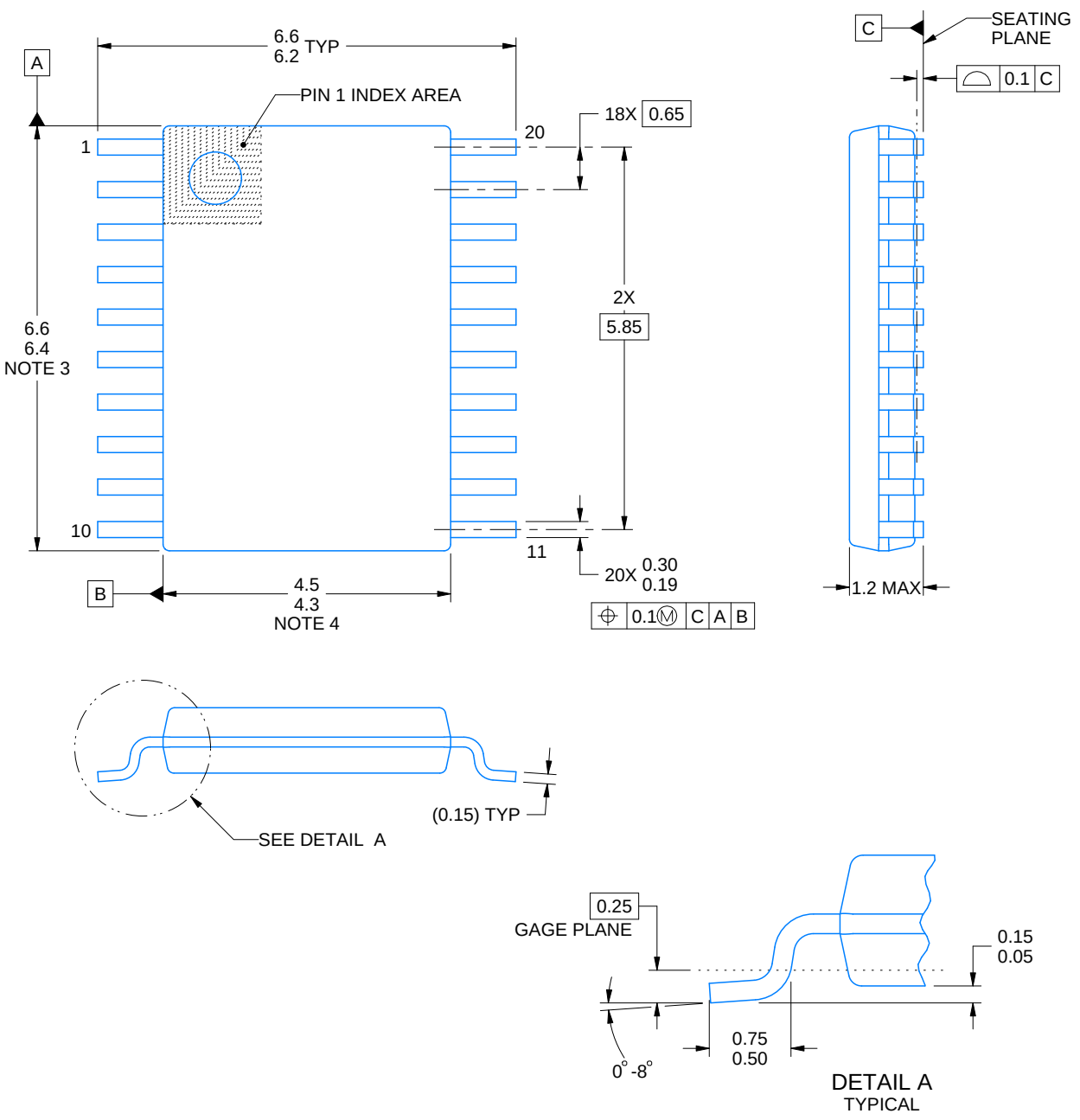
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

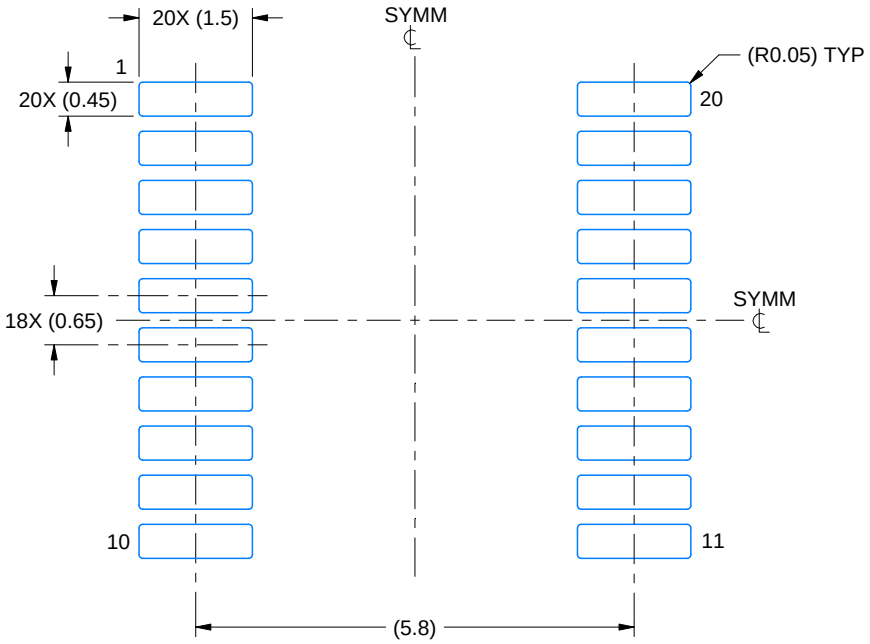
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

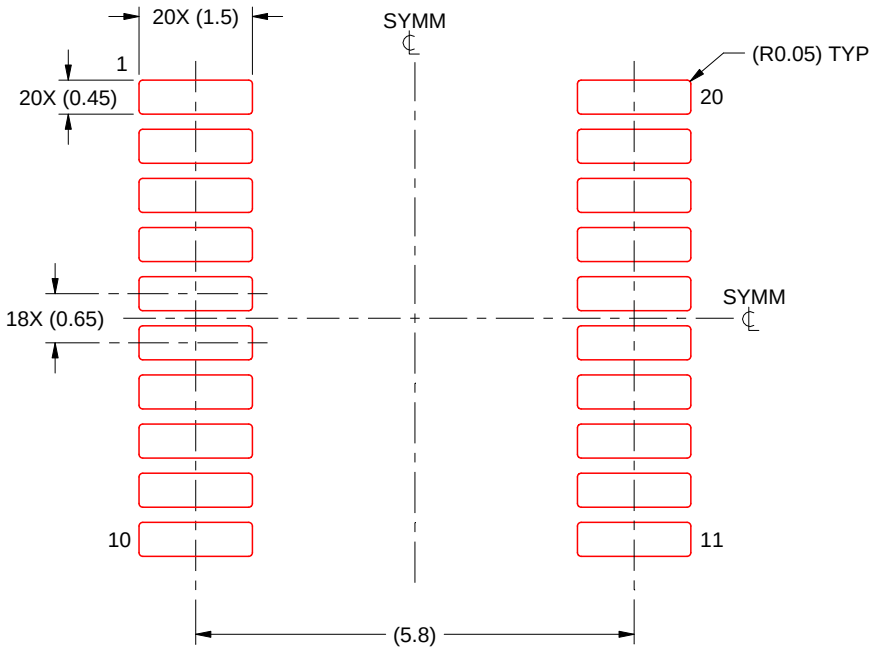


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



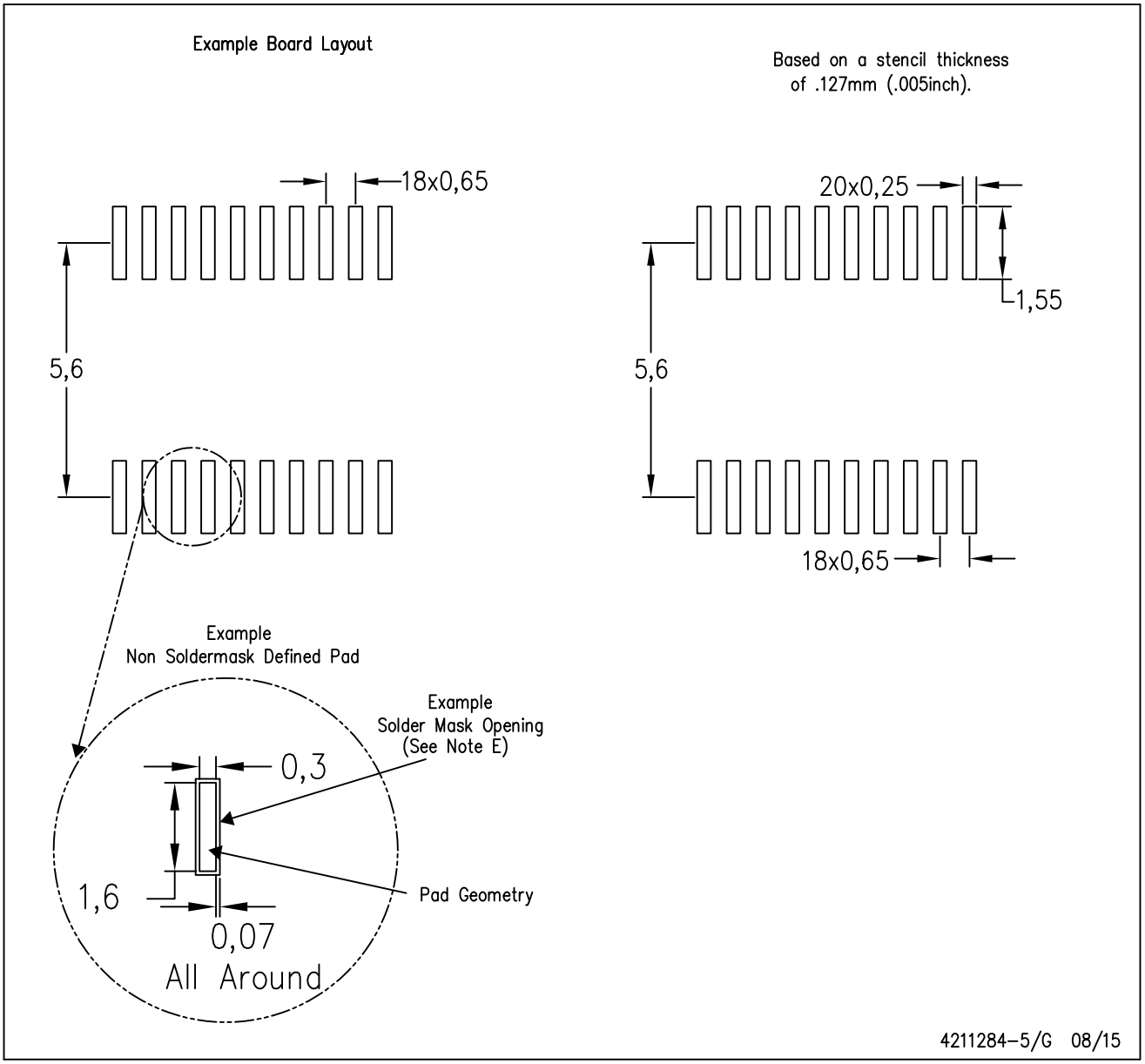
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

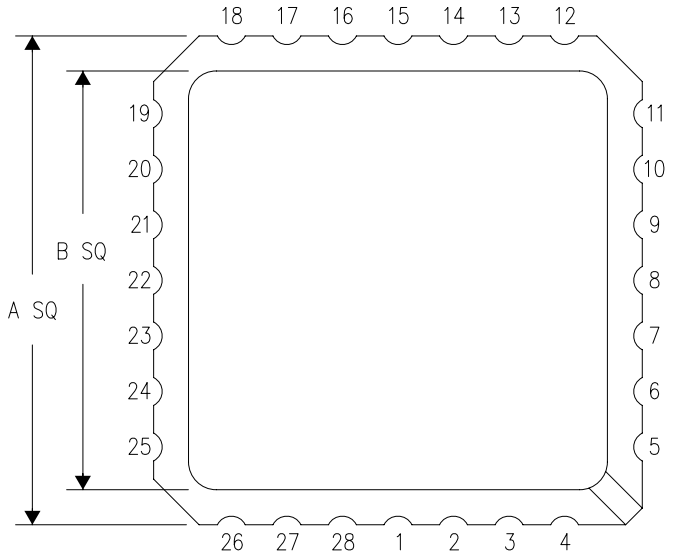
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



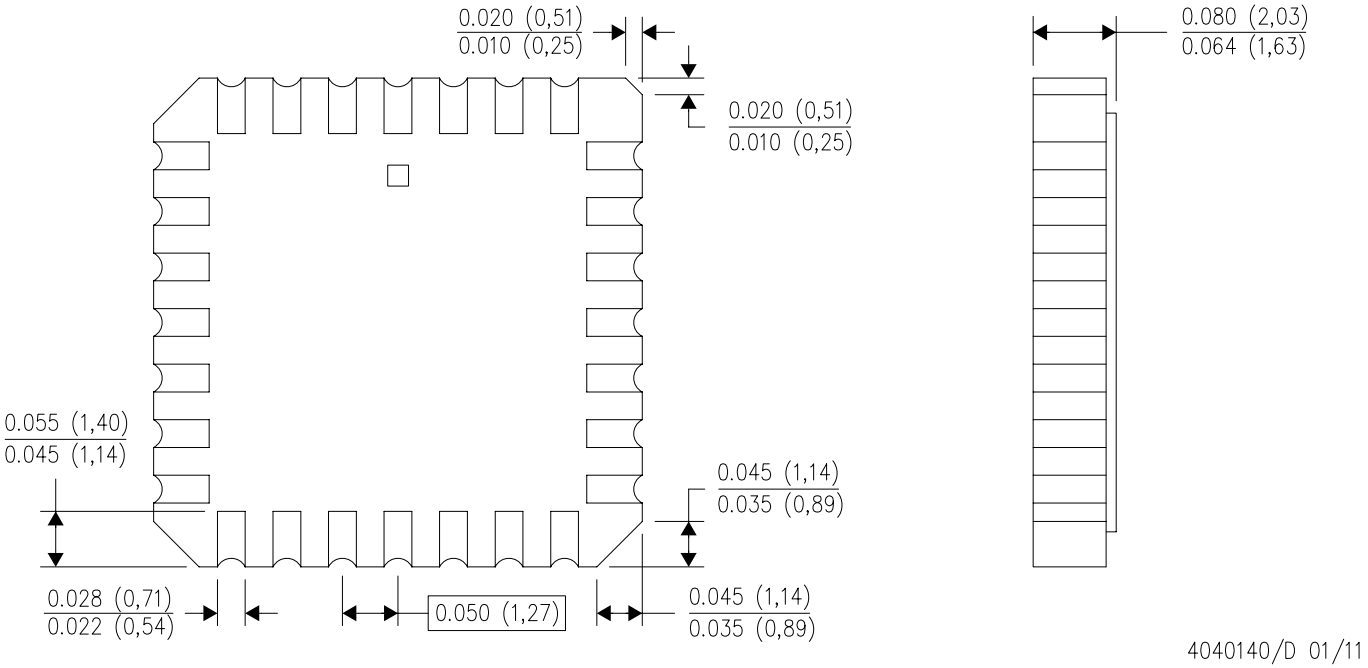
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

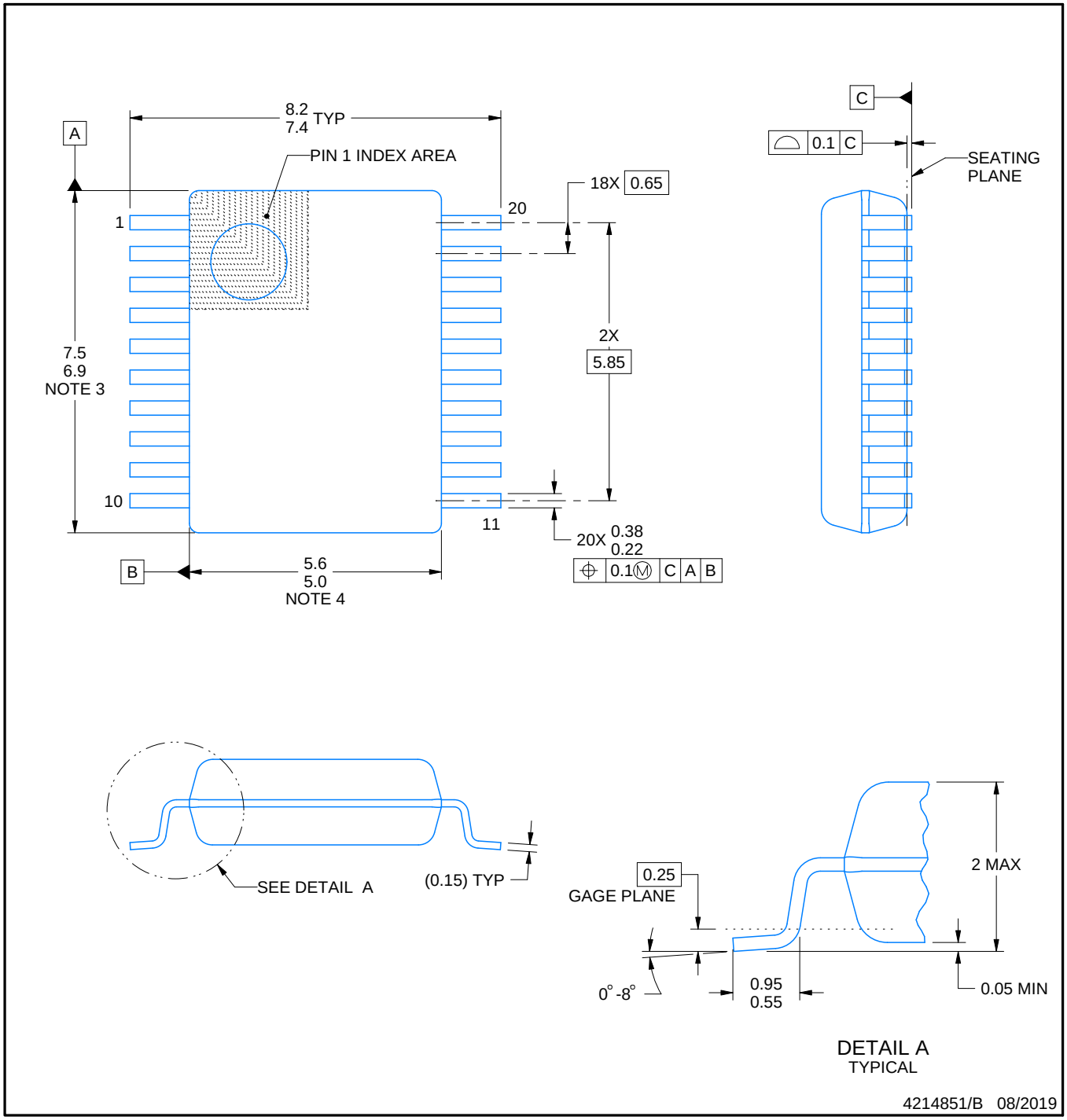
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

PACKAGE OUTLINE

DB0020A

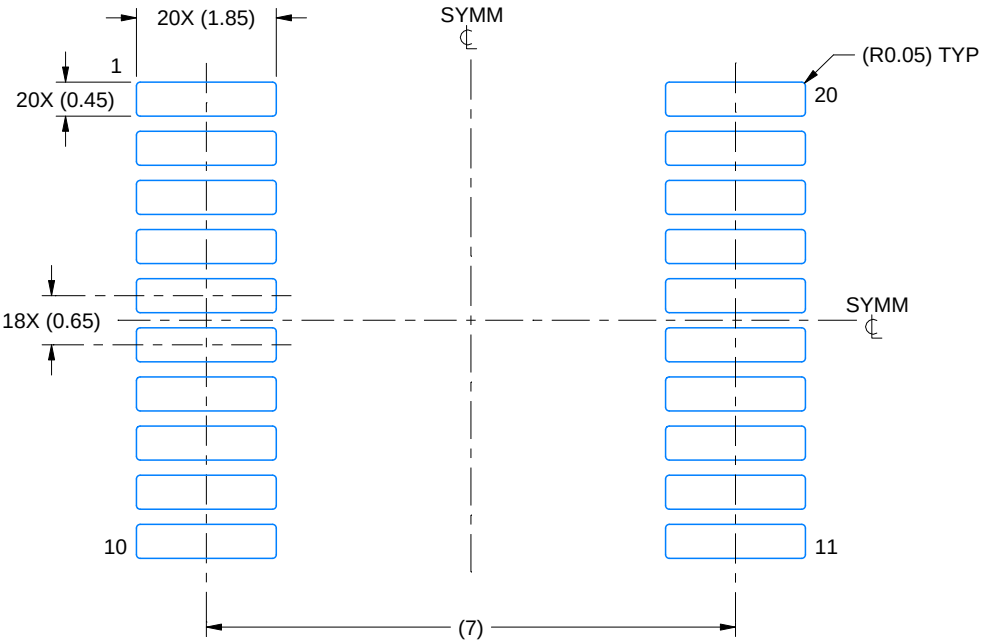
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

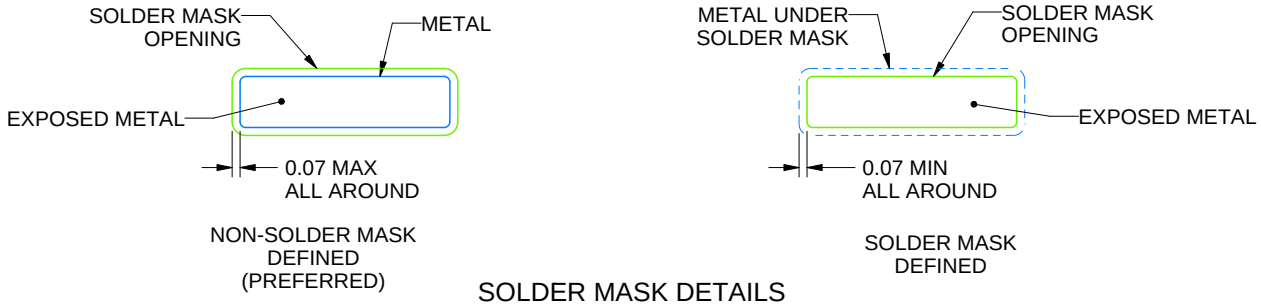


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

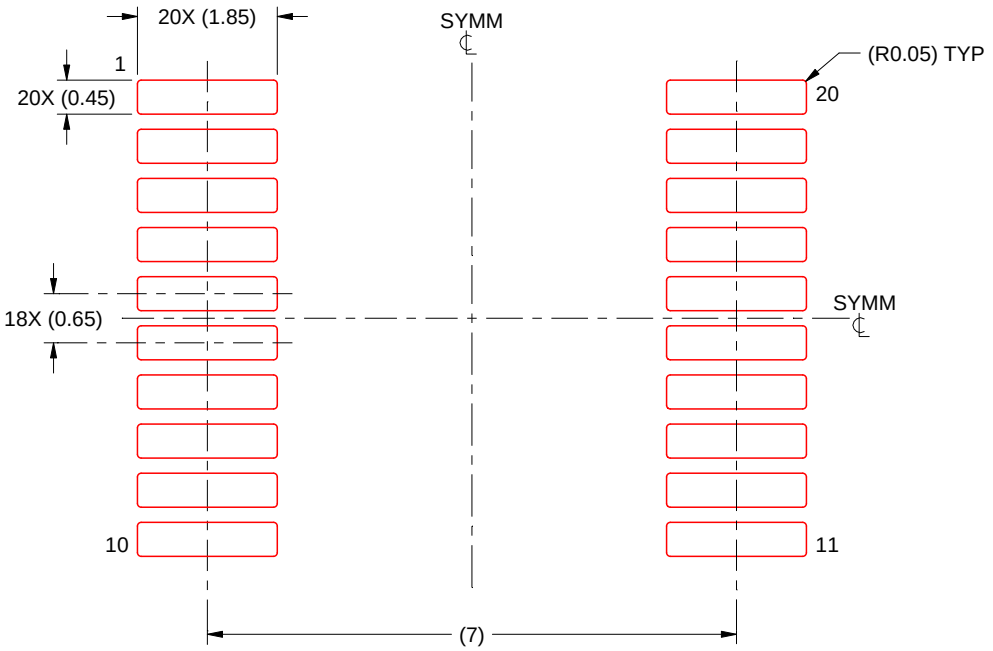
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

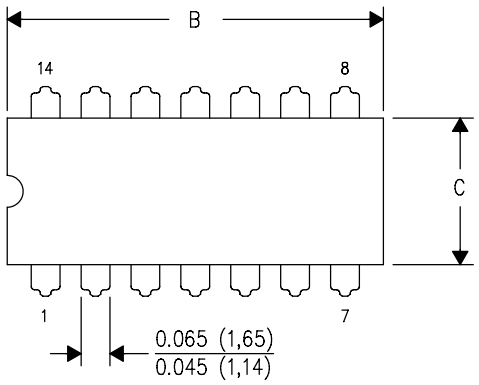
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

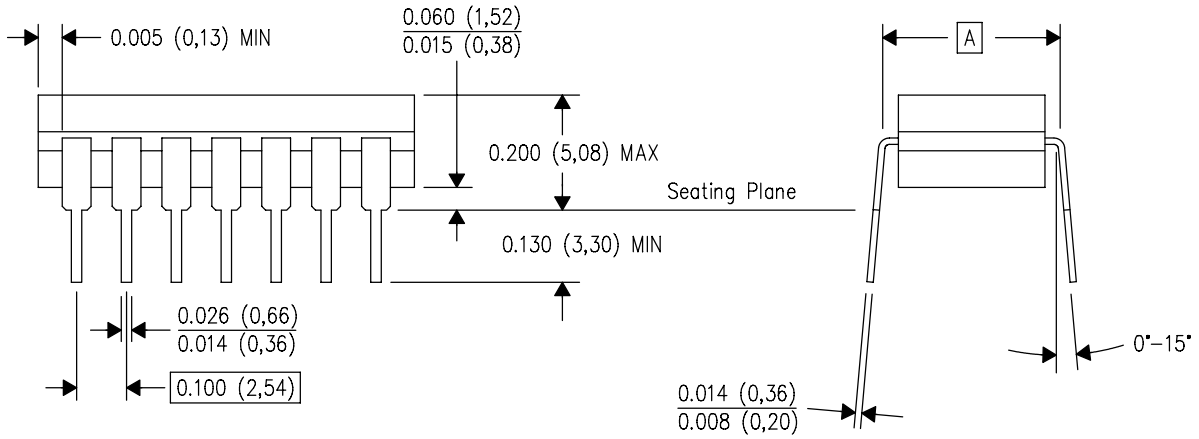
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



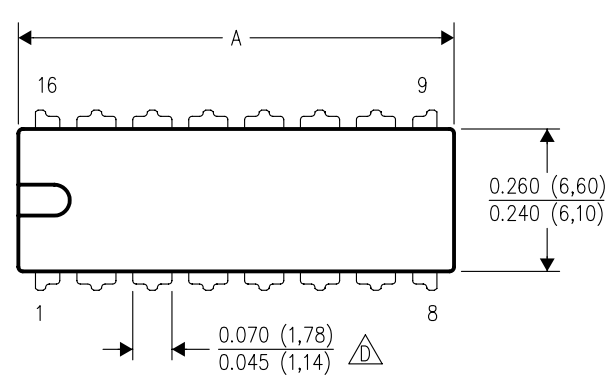
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

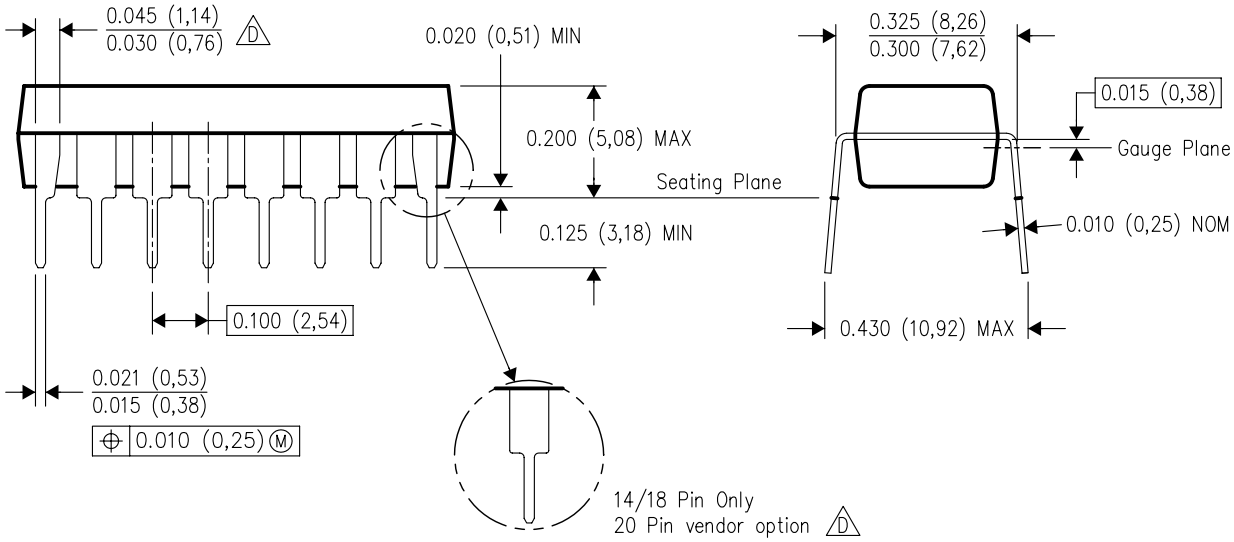
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

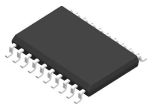


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

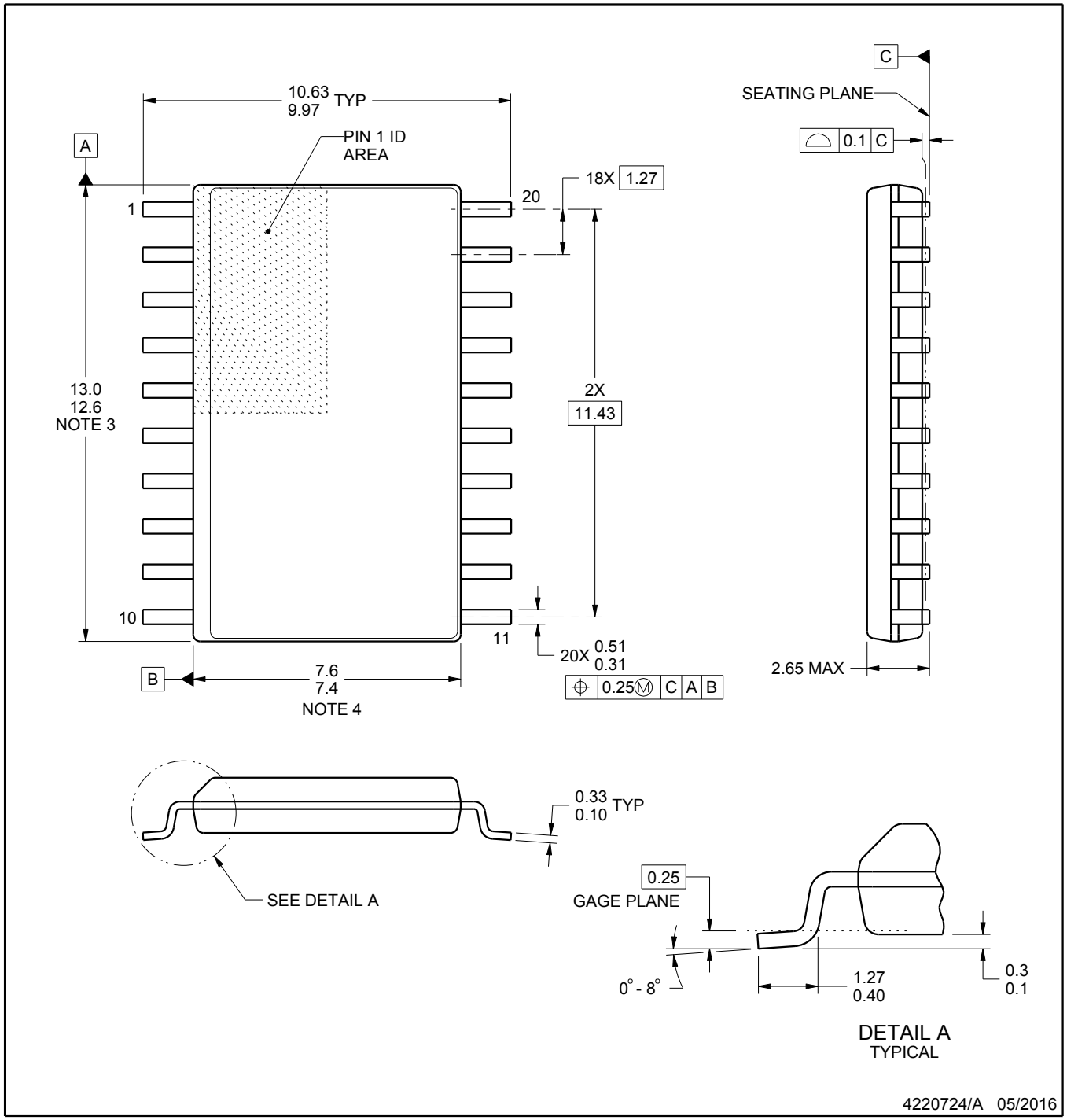


PACKAGE OUTLINE

DW0020A

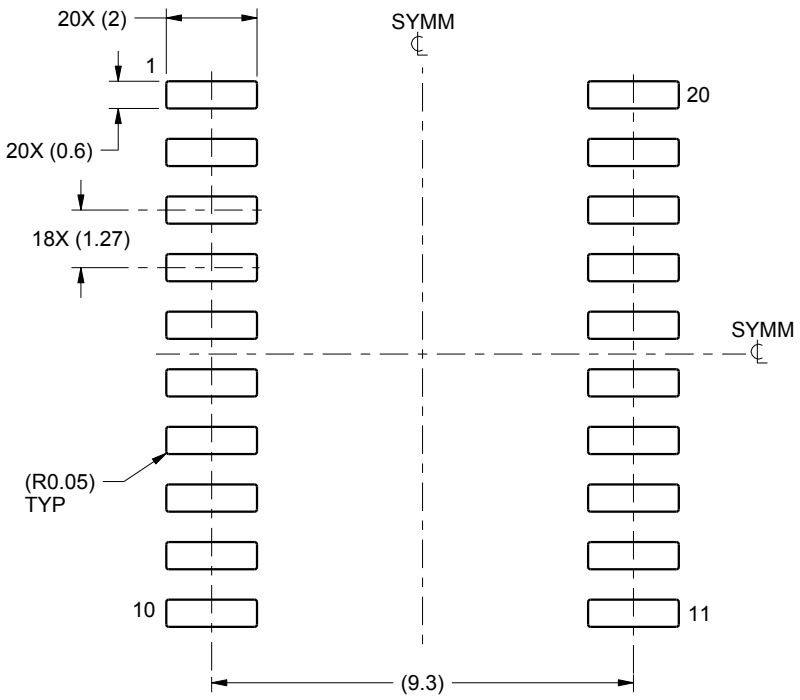
SOIC - 2.65 mm max height

SOIC

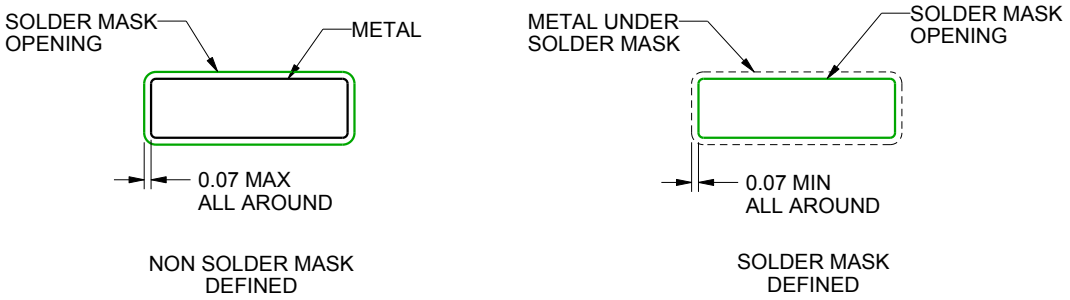


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

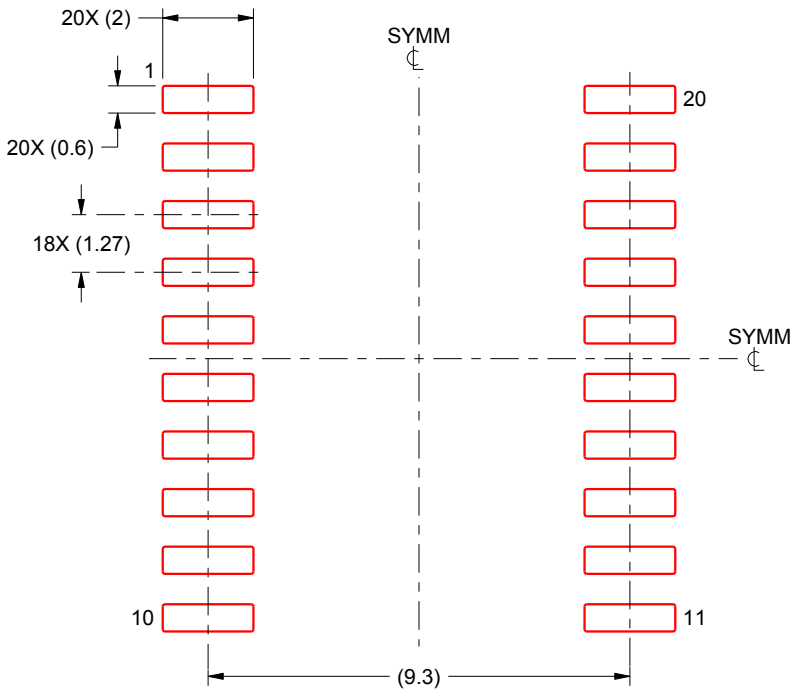


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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