

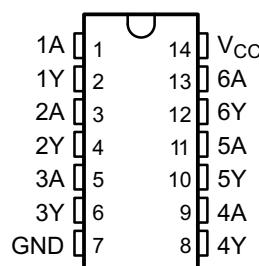
## HEX INVERTERS

Check for Samples: [SN74AHC04](#), [SN54AHC04](#)

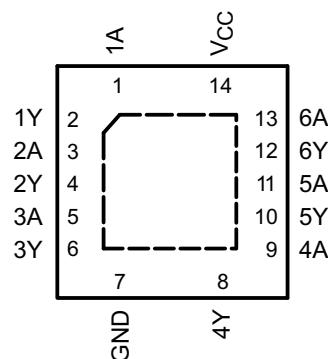
### FEATURES

- Operating Range 2-V to 5.5-V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

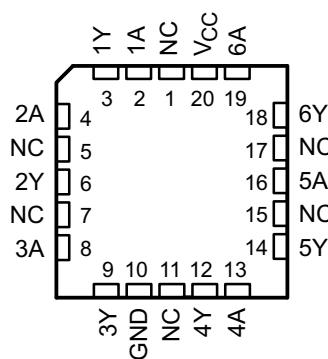
SN54AHC04 . . . JORWP PACKAGE  
SN74AHC04 . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74AHC04 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHC04 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

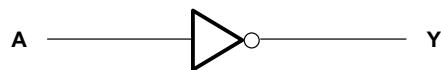
### DESCRIPTION

The 'AHC04 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ .

### FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	L
L	H

### LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, $V_{CC}$	–0.5 to 7	V
Input voltage range, $V_I$ <sup>(2)</sup>	–0.5 to 7	V
Output voltage range, $V_O$ <sup>(2)</sup>	–0.5 to $V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_O > V_{CC}$ )	–20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20	mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25	mA
Continuous current through $V_{CC}$ or GND	±50	mA
Package thermal impedance, $\theta_{JA}$	D package <sup>(3)</sup>	86
	DB package <sup>(3)</sup>	96
	DGV package <sup>(3)</sup>	127
	N package <sup>(3)</sup>	80
	NS package <sup>(3)</sup>	76
	PW package <sup>(3)</sup>	113
	RGY package <sup>(4)</sup>	47
Storage temperature range, $T_{stg}$	–65 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5

RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		SN54AHC04		SN74AHC04		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5	1.5	V
		$V_{CC} = 3$ V	2.1	2.1	2.1	
		$V_{CC} = 5.5$ V	3.85	3.85	3.85	
$V_{IL}$	Low-level Input voltage	$V_{CC} = 2$ V	0.5	0.5	0.5	V
		$V_{CC} = 3$ V	0.9	0.9	0.9	
		$V_{CC} = 5.5$ V	1.65	1.65	1.65	
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	–50	–50	mA
		$V_{CC} = 3.3$ V ± 0.3 V	–4	–4	–4	
		$V_{CC} = 5$ V ± 0.5 V	–8	–8	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	50	50	mA
		$V_{CC} = 3.3$ V ± 0.3 V	4	4	4	
		$V_{CC} = 5$ V ± 0.5 V	8	8	8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	100	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	20	20	
$T_A$	Operating free-air temperature	–55	125	–40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C	T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT	
				SN54AHC04		SN74AHC04		Recommended			
				MIN	TYP	MAX	MIN	MAX	MIN		
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		1.9	1.9	V	
		3 V	2.9	3		2.9		2.9	2.9		
		4.5 V	4.4	4.5		4.4		4.4	4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48	2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8	3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V		0.1		0.1		0.1	0.1	V	
		3 V		0.1		0.1		0.1	0.1		
		4.5 V		0.1		0.1		0.1	0.1		
	I <sub>OH</sub> = 4 mA	3 V		0.36		0.5		0.44	0.5		
	I <sub>OH</sub> = 8 mA	4.5 V		0.36		0.5		0.44	0.5		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1 <sup>(1)</sup>		±1	±1	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20		20	20	µA	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10			10		pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C	T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT	
					SN54AHC04		SN74AHC04		SN74AHC04			
					TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5 <sup>(1)</sup>	8.9 <sup>(1)</sup>	1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	10.5	ns
				5 <sup>(1)</sup>	8.9 <sup>(1)</sup>	1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	10.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	7.5	11.4	1	13	1	13	1	13	ns
				7.5	11.4	1	13	1	13	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C	T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT	
					SN54AHC04		SN74AHC04		SN74AHC04			
					TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	3.8 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	ns
				3.8 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.3	7.5	1	8.5	1	8.5	1	8.5	ns
				5.3	7.5	1	8.5	1	8.5	1	8.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## NOISE CHARACTERISTICS

$V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER	SN74AHC04			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$	0.4			V
$V_{OL(V)}$	-0.4			V
$V_{OH(V)}$	4.8			V
$V_{IH(D)}$	3.5			V
$V_{IL(D)}$	1.5			V

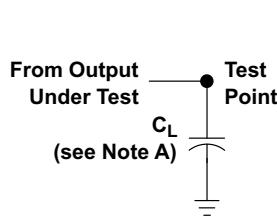
(1) Characteristics are for surface-mount packages only.

## OPERATING CHARACTERISTICS

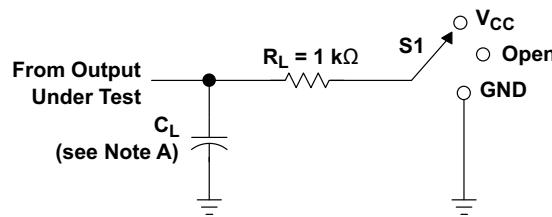
$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	No load, $f = 1 \text{ MHz}$	12	pF

## PARAMETER MEASUREMENT INFORMATION

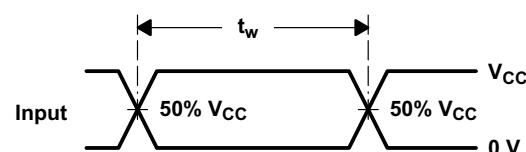


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

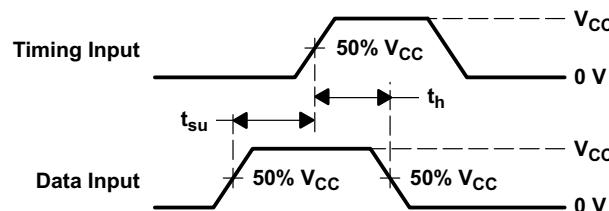


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

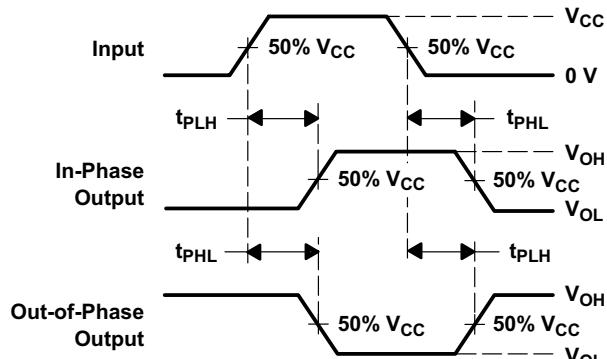
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



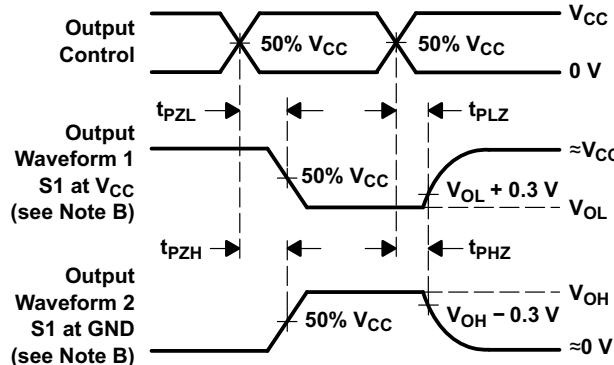
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## REVISION HISTORY

<b>Changes from Revision M (July 2003) to Revision N</b>	<b>Page</b>
• Changed document format from Quicksilver to DocZone. ....	<a href="#">1</a>
• Extended operating temperature range to 125°C ....	<a href="#">2</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680501Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680501Q2A SNJ54AHC04FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9680501QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680501QC A SNJ54AHC04J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9680501QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680501QD A SNJ54AHC04W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC04N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC04N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC04PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC04RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA04	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC04FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9680501Q2A SNJ54AHC 04FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC04J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680501QC A SNJ54AHC04J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC04W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680501QD A SNJ54AHC04W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC04, SN74AHC04 :**

- Catalog : [SN74AHC04](#)
- Automotive : [SN74AHC04-Q1](#), [SN74AHC04-Q1](#)
- Enhanced Product : [SN74AHC04-EP](#), [SN74AHC04-EP](#)
- Military : [SN54AHC04](#)

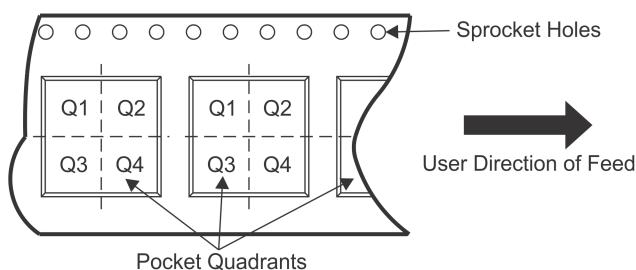
## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


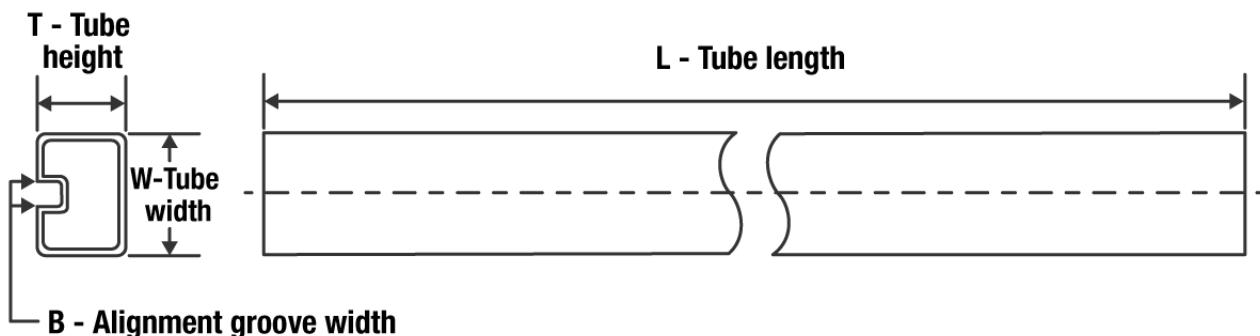
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC04DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC04DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC04NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC04RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC04DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74AHC04DGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74AHC04DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74AHC04NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74AHC04PWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74AHC04RGYR	VQFN	RGY	14	3000	853.0	449.0	35.0

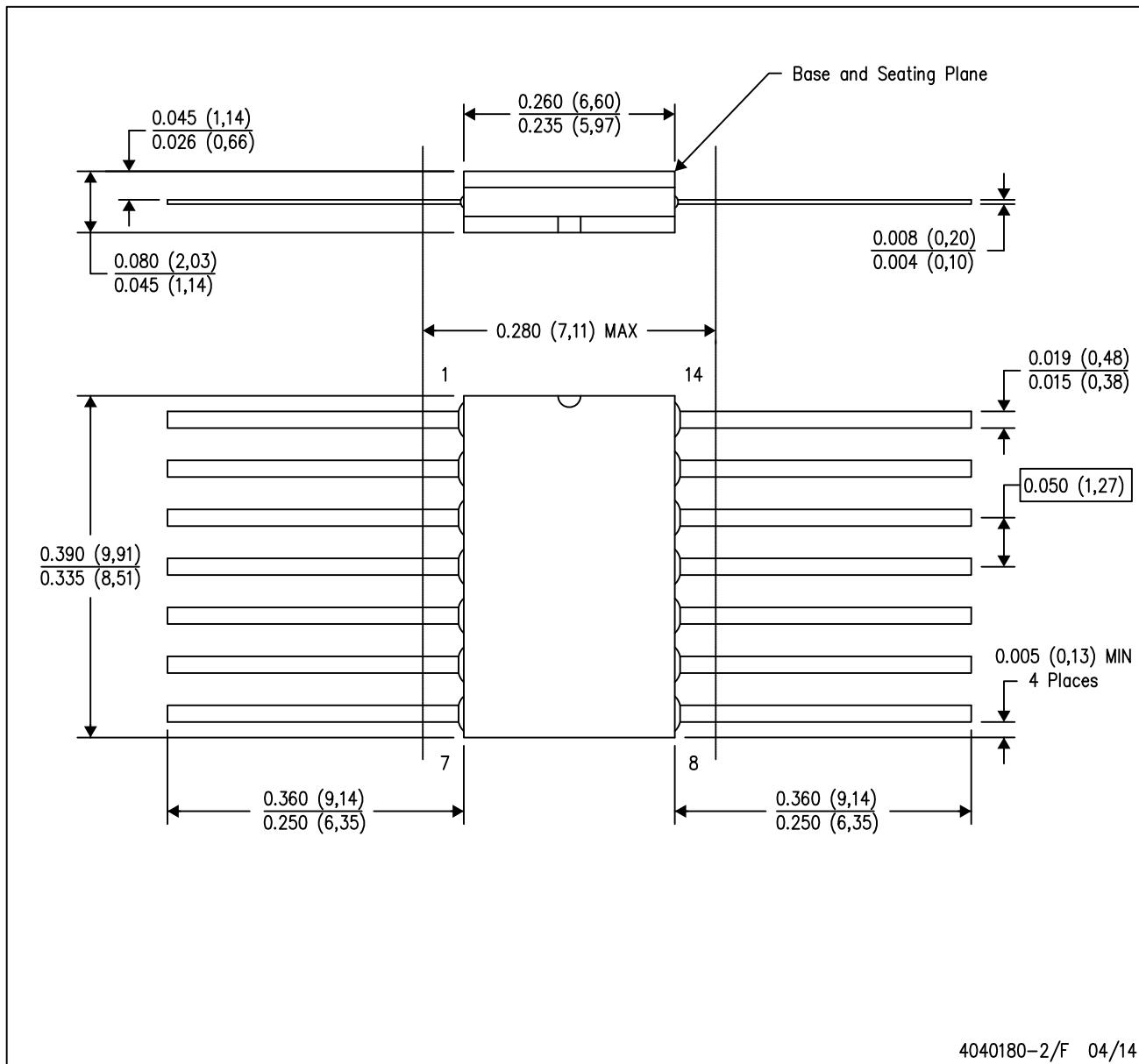
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9680501Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC04D	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC04DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC04DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC04PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54AHC04FK	FK	LCCC	20	1	506.98	12.06	2030	NA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

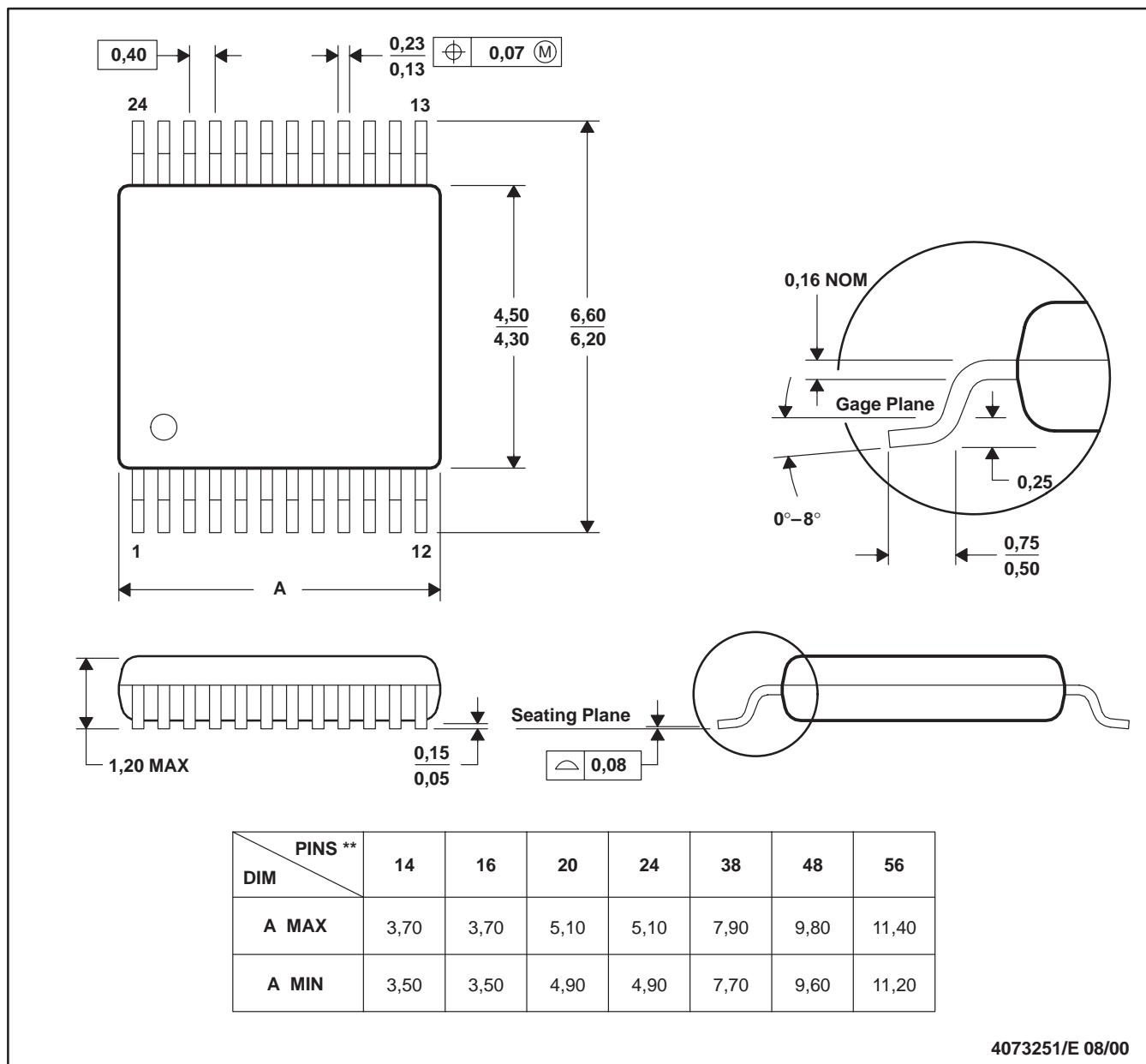
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

4040180-2/F 04/14

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



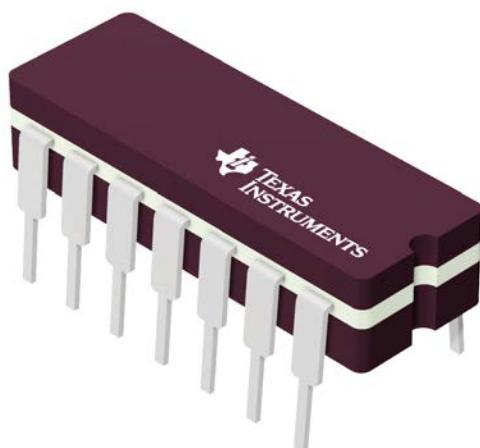
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

**J 14**

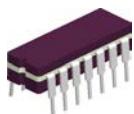
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

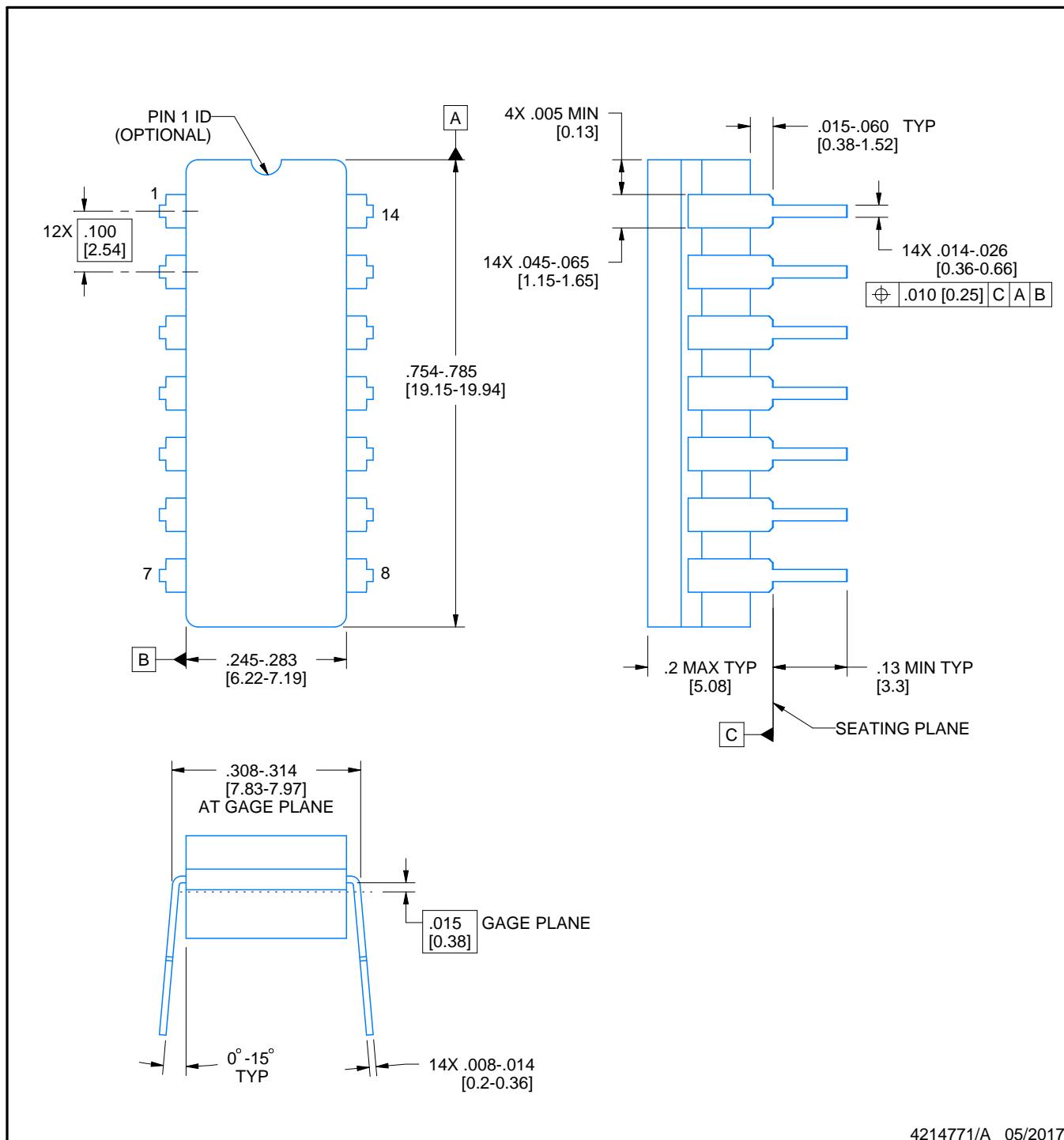


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

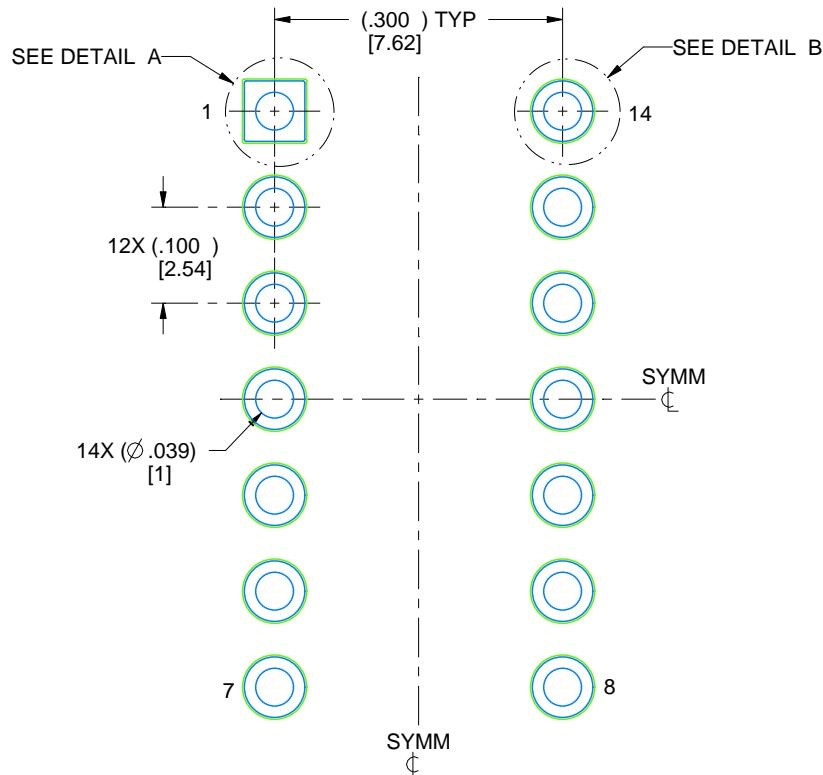
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

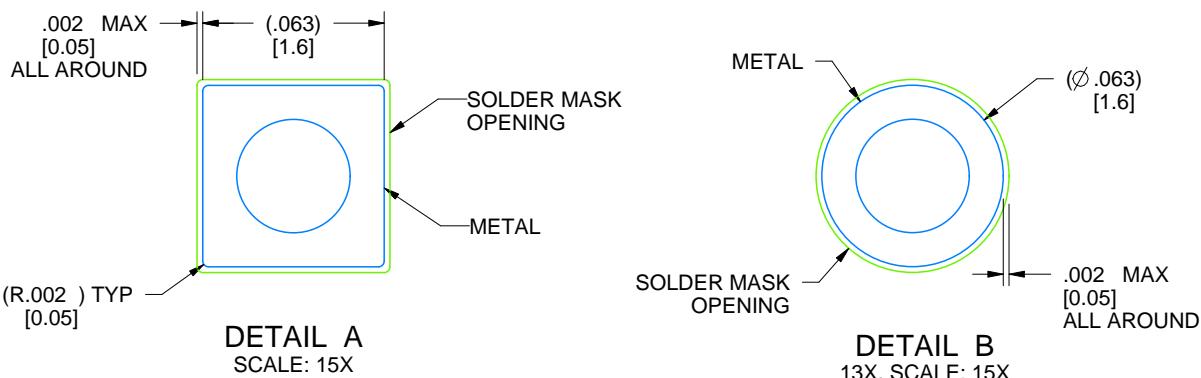
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



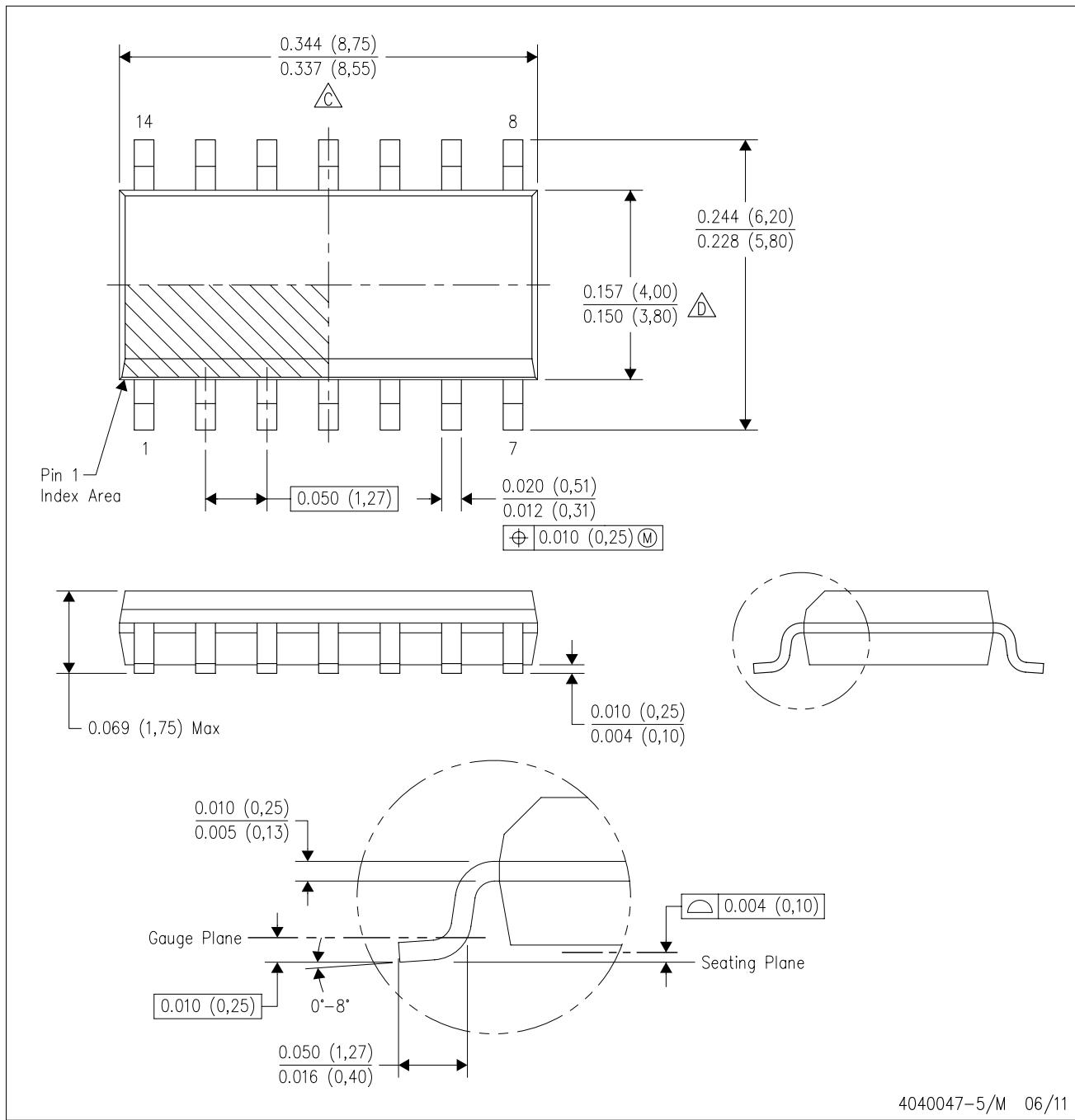
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

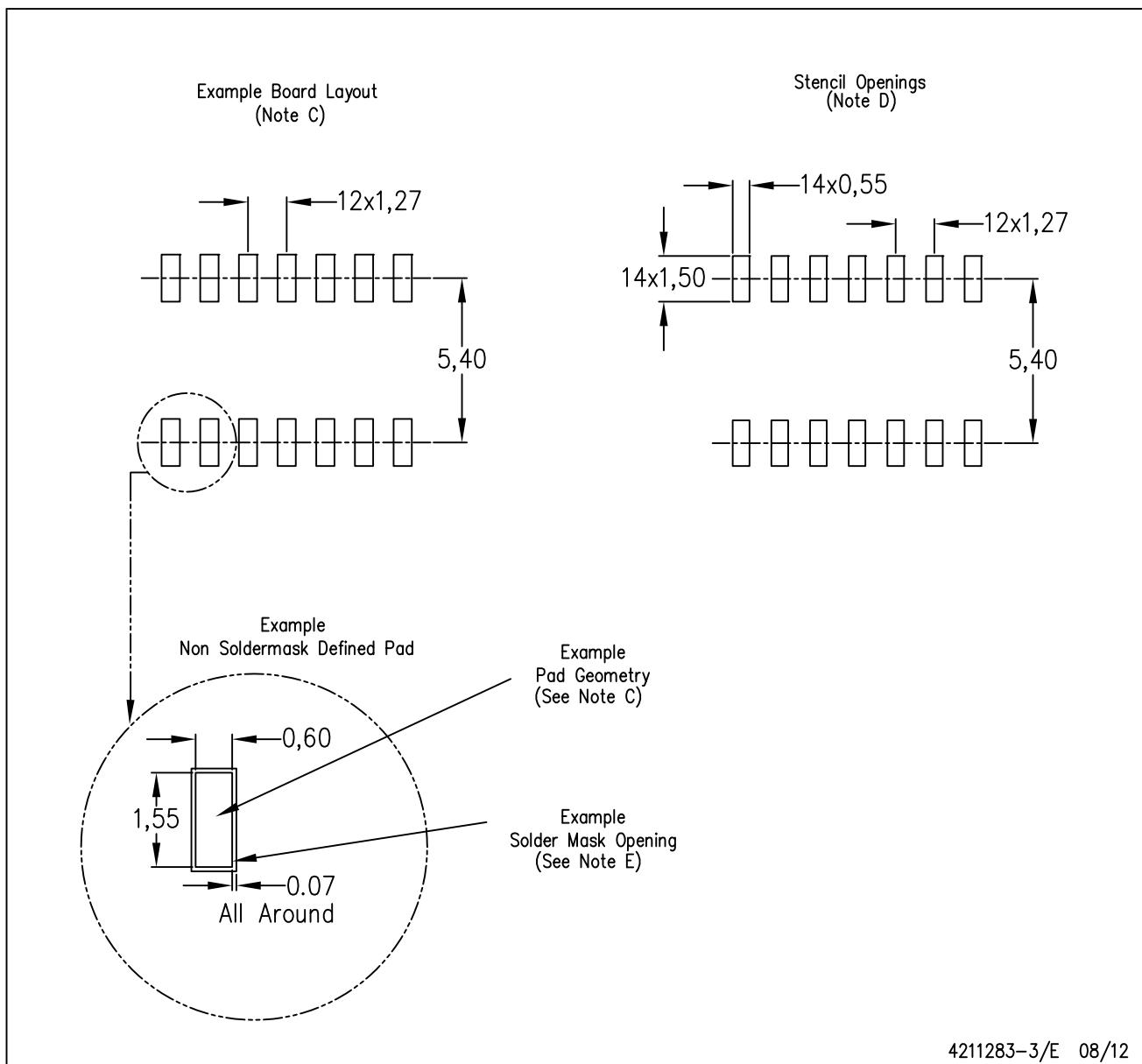
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



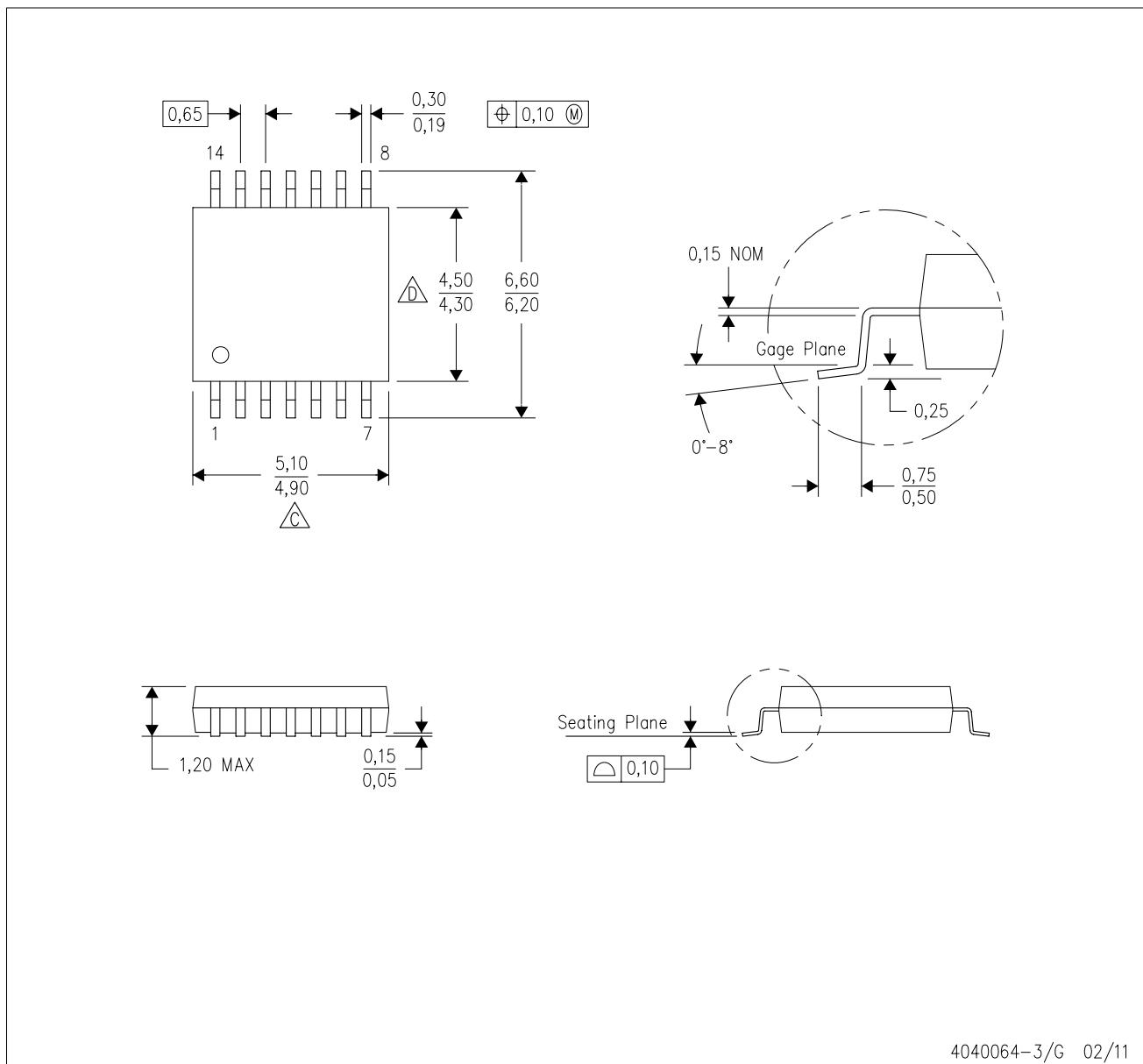
4211283-3/E 08/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

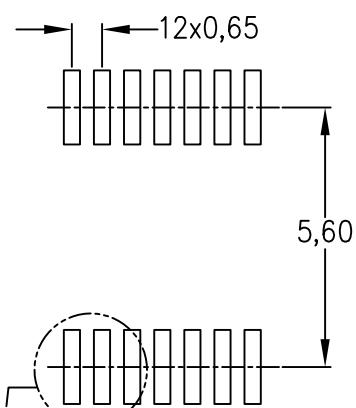
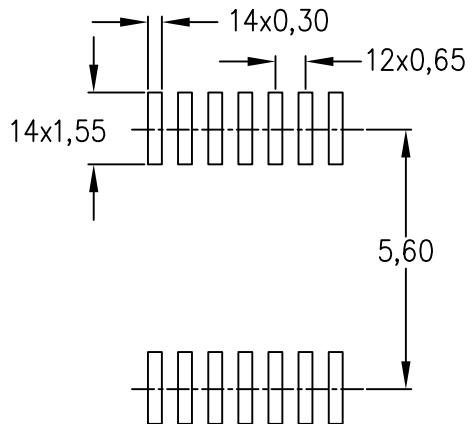
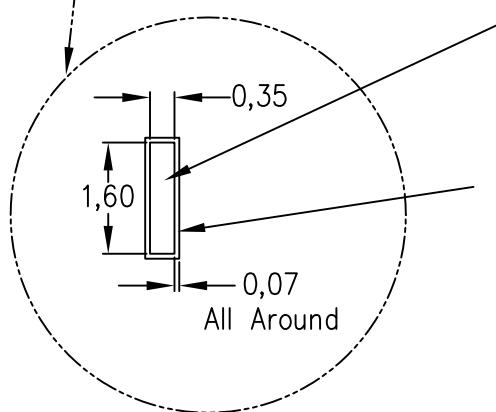
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211284-2/G 08/15

## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

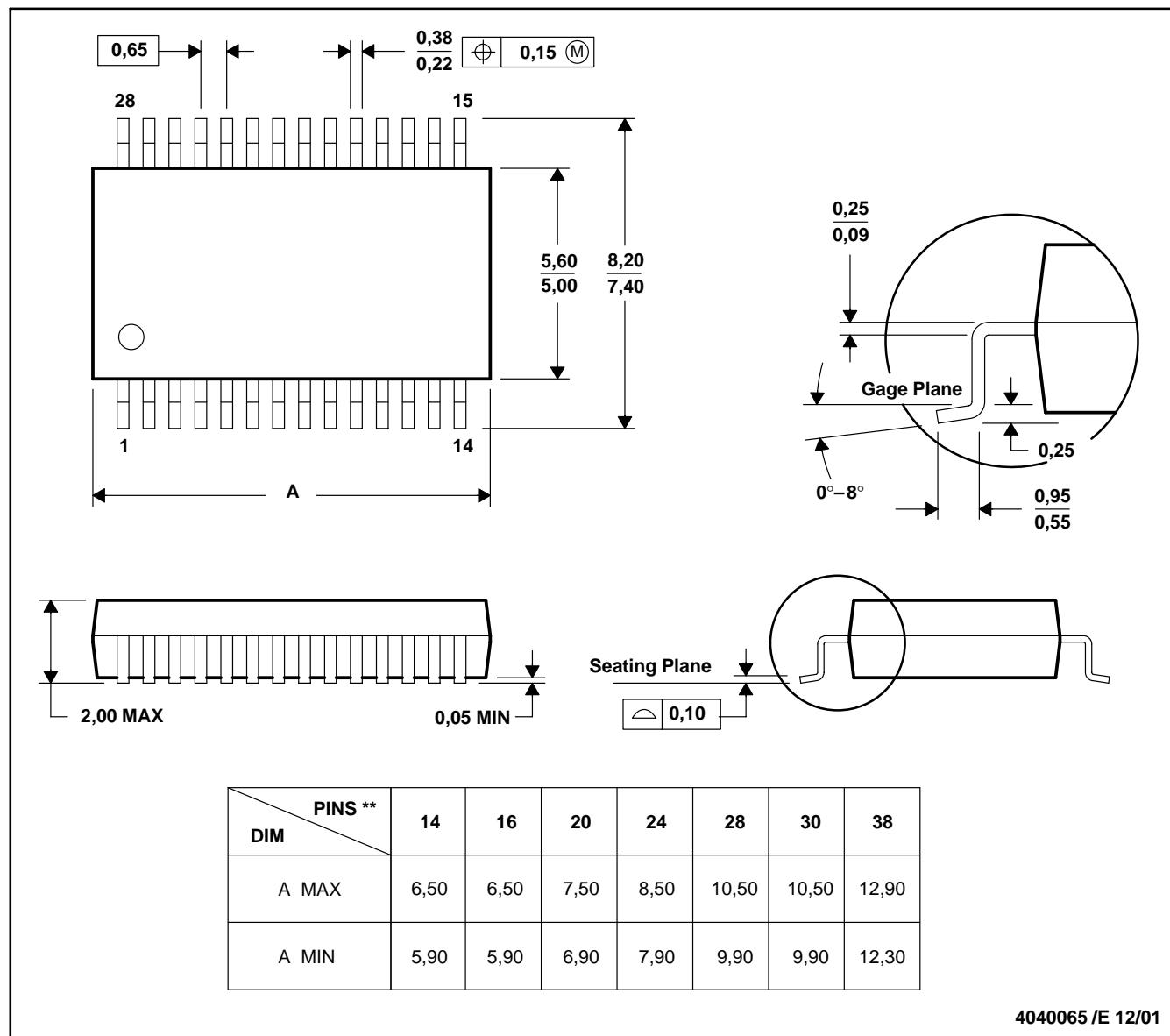
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

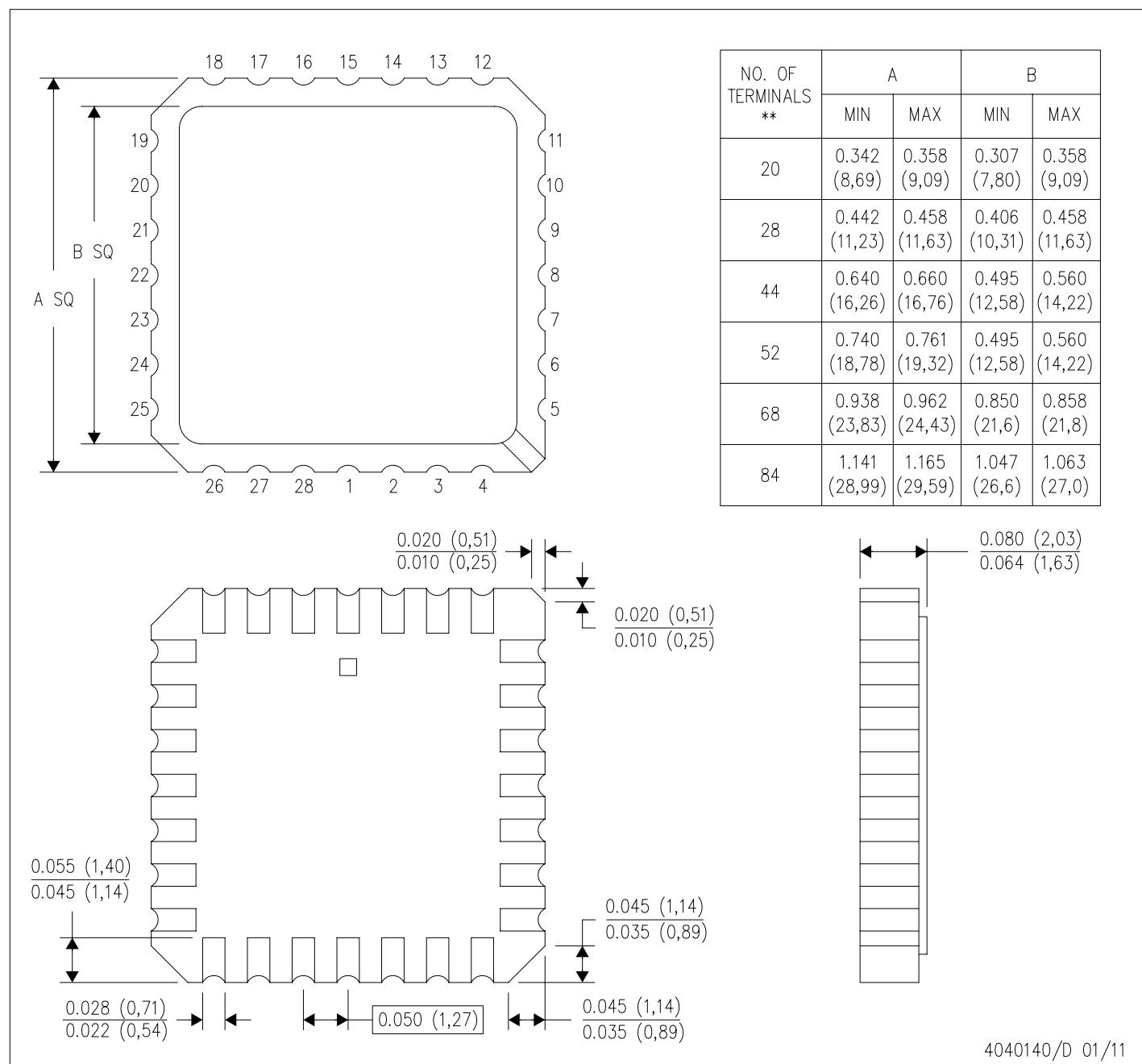


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

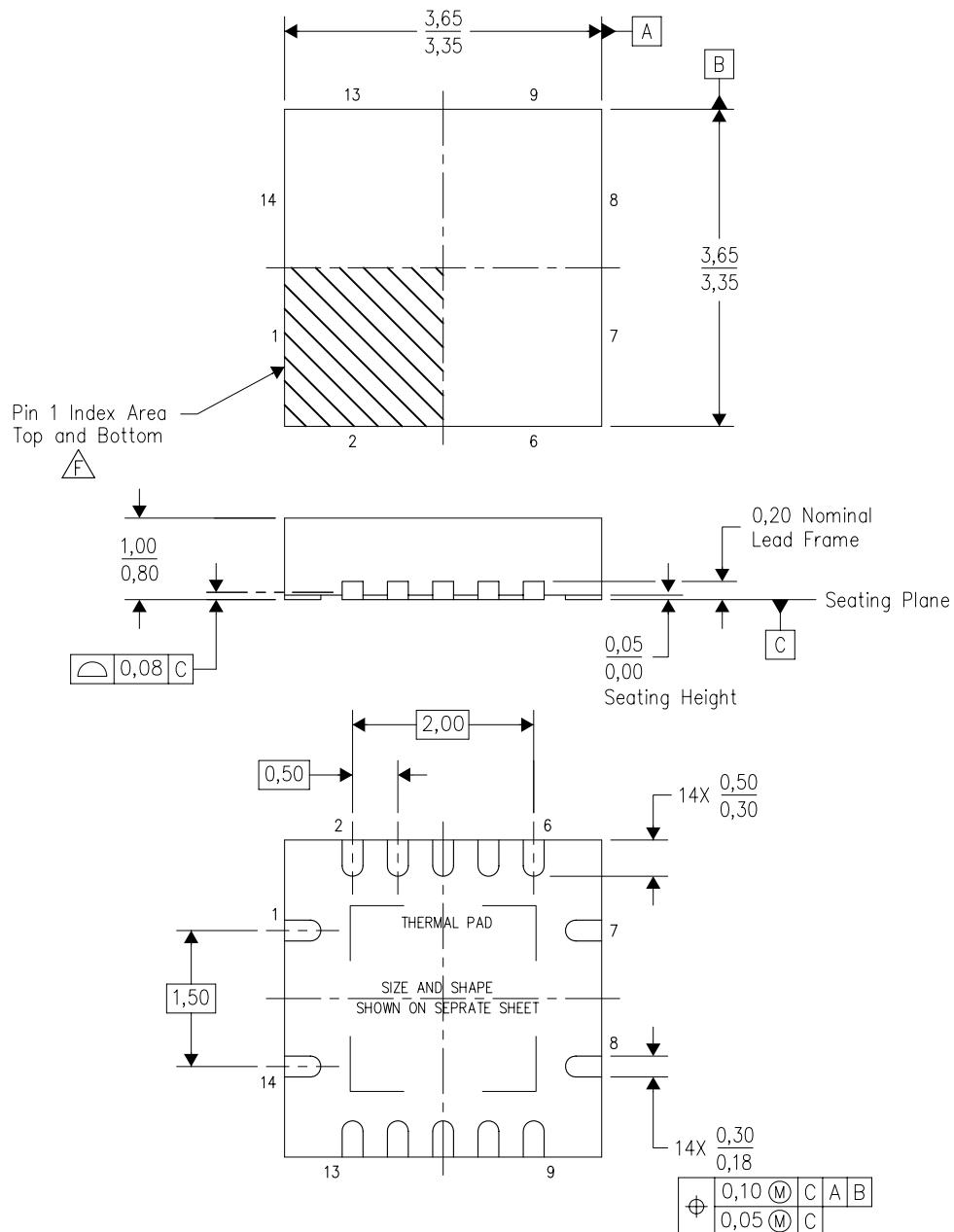
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## MECHANICAL DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-2/l 06/2011

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (S-PVQFN-N14)

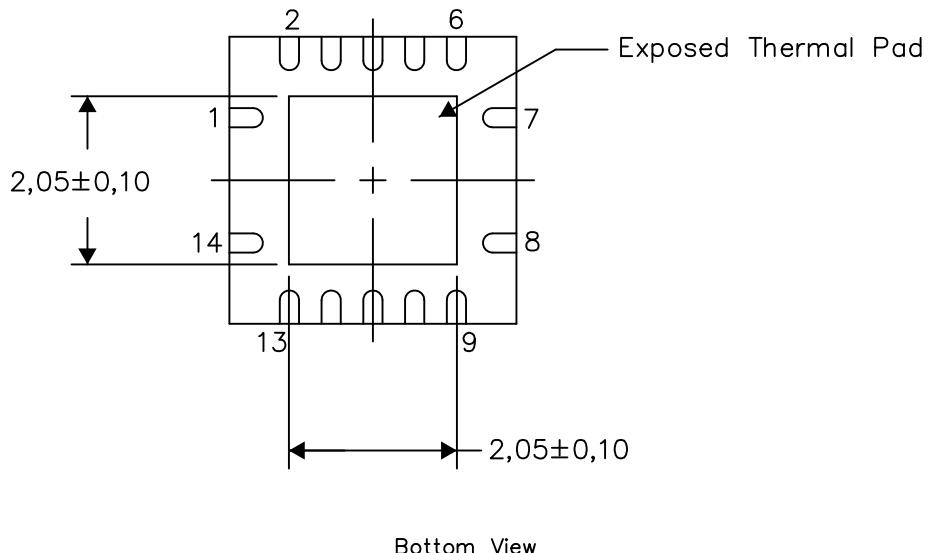
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

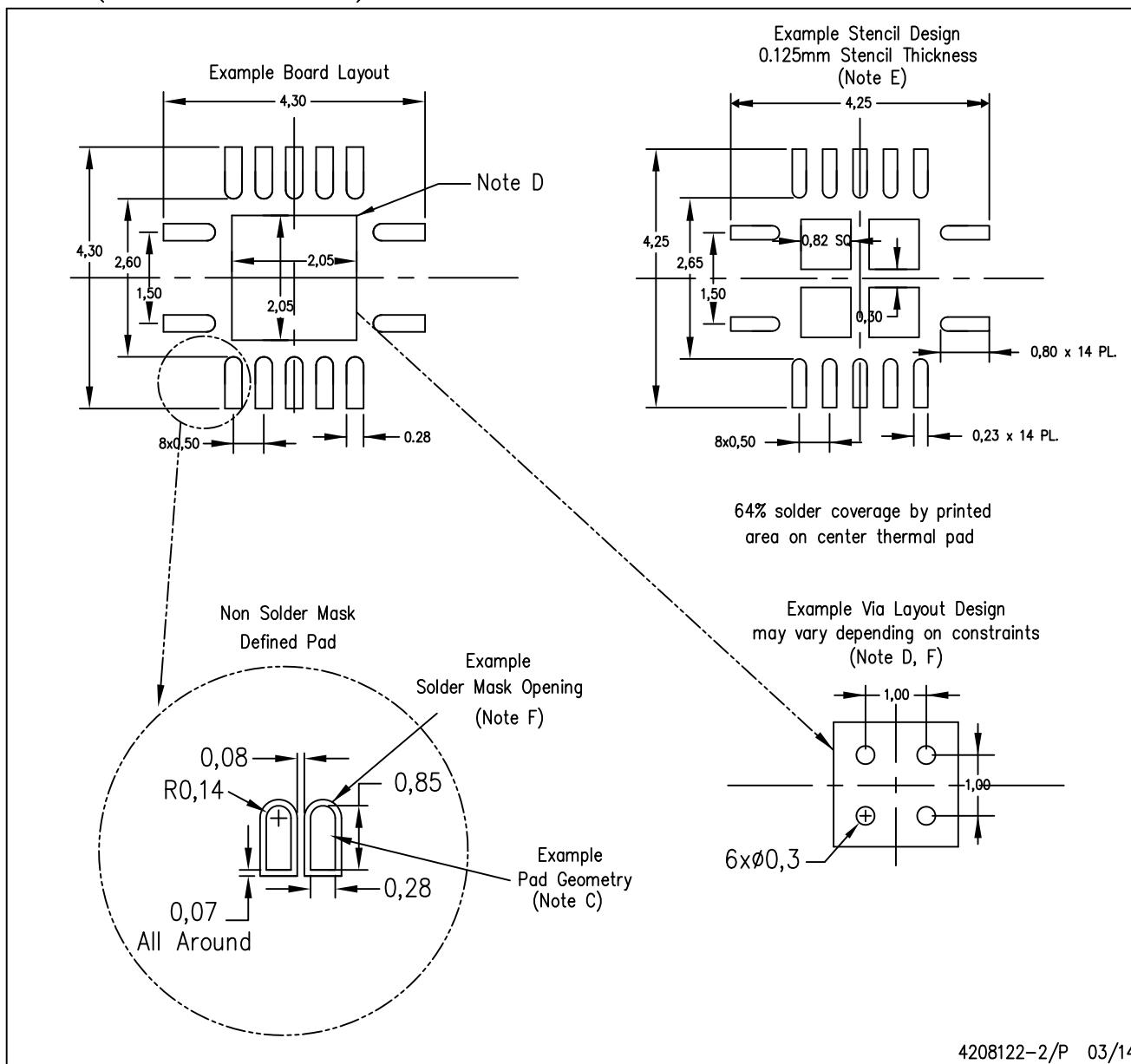
4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



**NOTES:**

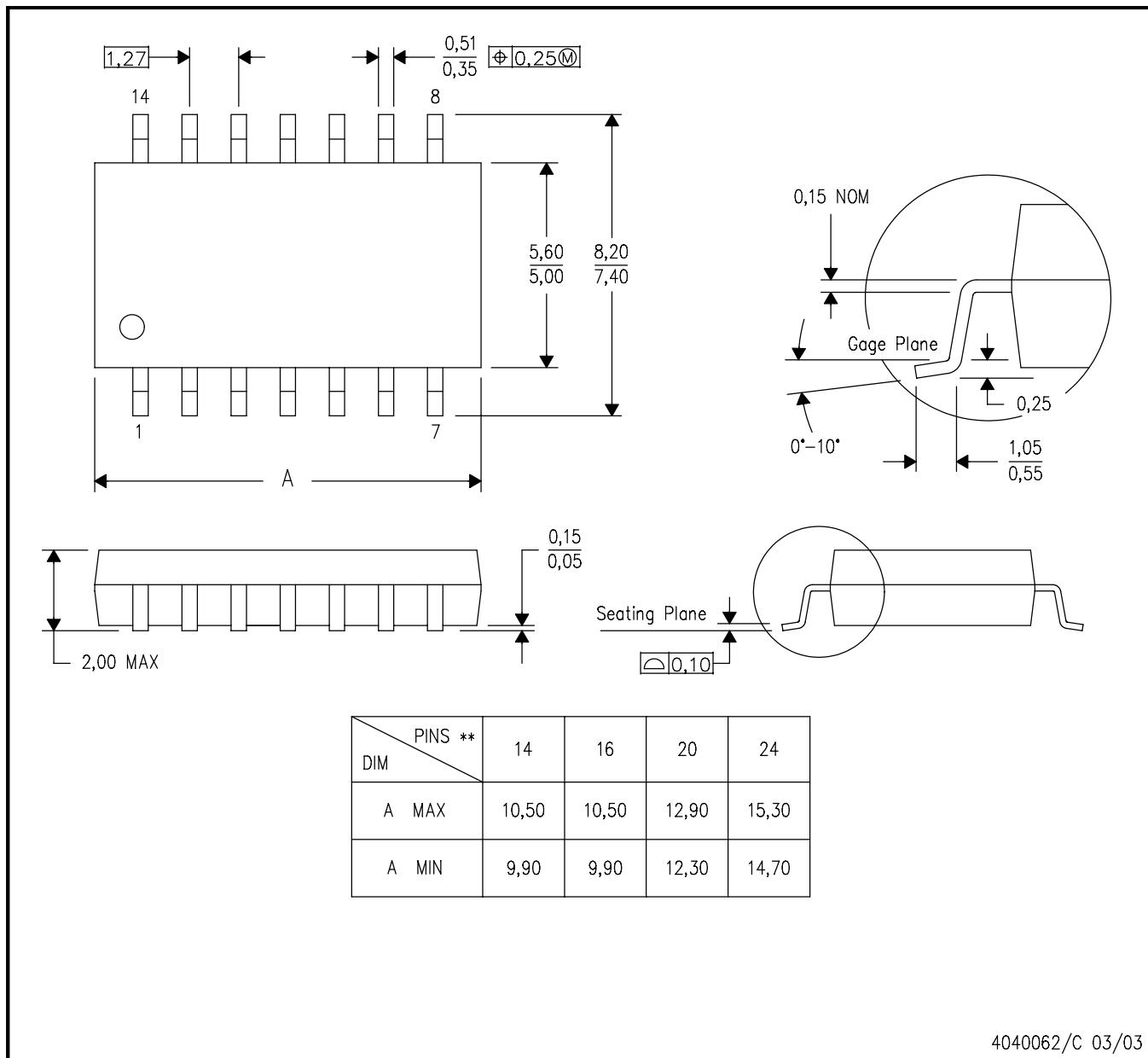
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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