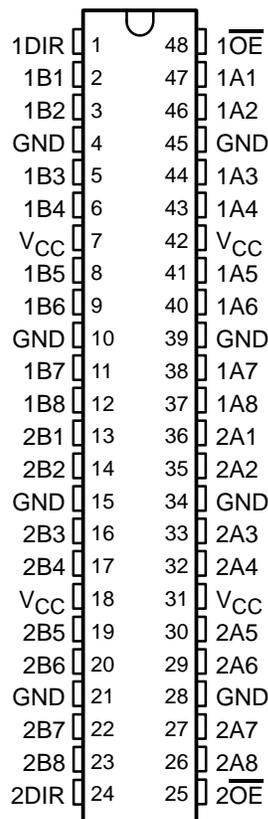


# SN54ALVTH162245, SN74ALVTH162245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES331A – APRIL 2000 – REVISED APRIL 2002

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **High Drive**
  - A Port =  $-12/12$  mA at 3.3-V  $V_{CC}$
  - B port =  $-32/64$  mA at 3.3-V  $V_{CC}$
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **A-Port Outputs Have Equivalent 30- $\Omega$  Series Resistors, So No External Resistors Are Required**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

SN54ALVTH162245 . . . WD PACKAGE  
SN74ALVTH162245 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ALVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 30- $\Omega$  series resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.



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 **TEXAS  
INSTRUMENTS**

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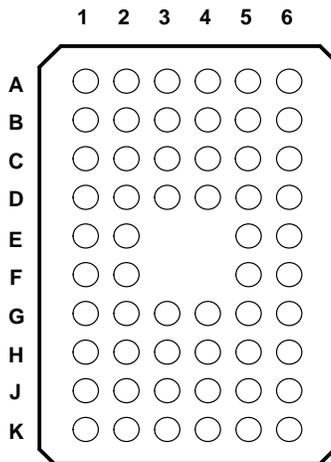
# SN54ALVTH162245, SN74ALVTH162245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## description (continued)

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### SN74ALVTH162245 . . . GQL PACKAGE (TOP VIEW)



### terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$\overline{1OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	$V_{CC}$	$V_{CC}$	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	$V_{CC}$	$V_{CC}$	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$\overline{2OE}$

NC – No internal connection

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tape and reel	SN74ALVTH162245LR	ALVTH162245
	TSSOP – DGG	Tape and reel	SN74ALVTH162245GR	ALVTH162245
	TVSOP – DGV	Tape and reel	SN74ALVTH162245VR	VT2245
	VFBGA – GQL	Tape and reel	SN74ALVTH162245QR	
–55°C to 125°C	CFP – WD	Tube	SNJ54ALVTH162245WD	SNJ54ALVTH162245WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

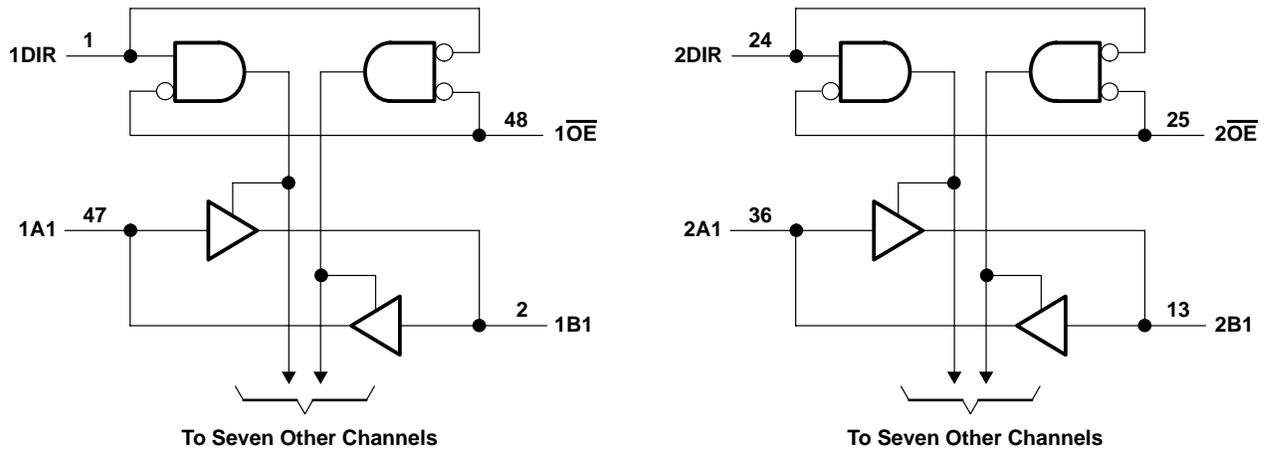
### FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

# SN54ALVTH162245, SN74ALVTH162245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output current in the low state, $I_{OL}$ : SN54ALVTH162245 .....	96 mA
SN74ALVTH162245 .....	128 mA
Output current in the high state, $I_{OH}$ : SN54ALVTH162245 .....	-48 mA
SN74ALVTH162245 .....	-64 mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	70°C/W
DGV package .....	58°C/W
DL package .....	63°C/W
GQL package .....	42°C/W
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN54ALVTH162245, SN74ALVTH162245**  
**2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (see Note 3)**

		SN54ALVTH162245			SN74ALVTH162245			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	2.3		2.7	2.3		2.7	V
$V_{IH}$	High-level input voltage	1.7			1.7			V
$V_{IL}$	Low-level input voltage			0.7			0.7	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current (A port)			-6			-8	mA
	High-level output current (B port)			-6			-8	
$I_{OL}$	Low-level output current (A port)			6			12	mA
	Low-level output current (B port)			6			8	
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$ (B port)			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**recommended operating conditions,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (see Note 3)**

		SN54ALVTH162245			SN74ALVTH162245			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	3		3.6	3		3.6	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current (A port)			-8			-12	mA
	High-level output current (B port)			-24			-32	
$I_{OL}$	Low-level output current (A port)			8			12	mA
	Low-level output current (B port)			24			32	
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$ (B port)			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54ALVTH162245, SN74ALVTH162245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALVTH162245		SN74ALVTH162245		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
$V_{IK}$	$V_{CC} = 2.3\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2	V	
$V_{OH}$	A port	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$	V	
		$V_{CC} = 2.3\text{ V}$	$I_{OH} = -6\text{ mA}$	1.7				
	B port	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$	$I_{OH} = -8\text{ mA}$			1.7		
			$V_{CC} = 2.3\text{ V}$	$I_{OH} = -6\text{ mA}$	1.7			
		$V_{CC} = 2.3\text{ V}$	$I_{OH} = -8\text{ mA}$			1.7		
			$I_{OH} = -8\text{ mA}$					1.7
$V_{OL}$	A port	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2	V	
		$V_{CC} = 2.3\text{ V}$	$I_{OL} = 6\text{ mA}$		0.4			
	$I_{OL} = 12\text{ mA}$					0.4		
	B port	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2
			$I_{OL} = 6\text{ mA}$		0.4			
		$V_{CC} = 2.3\text{ V}$	$I_{OL} = 8\text{ mA}$					0.4
			$I_{OL} = 18\text{ mA}$		0.5			
	$I_I$	Control inputs	$V_{CC} = 2.7\text{ V}$ , $V_I = \text{GND}$		$\pm 1$			$\pm 1$
$V_{CC} = 0\text{ or }2.7\text{ V}$ , $V_I = 5.5\text{ V}$				10		10		
A or B ports		$V_{CC} = 2.7\text{ V}$	$V_I = 5.5\text{ V}$		20		20	
			$V_I = V_{CC}$		1		1	
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$	$V_I = 0$				$\pm 100$		
		$V_O = 0$				$\pm 100$		
$I_{BHL}^\ddagger$	$V_{CC} = 2.3\text{ V}$ , $V_I = 0.7\text{ V}$		115		115	$\mu\text{A}$		
$I_{BHH}^\S$	$V_{CC} = 2.3\text{ V}$ , $V_I = 1.7\text{ V}$		-10		-10	$\mu\text{A}$		
$I_{BHLO}^\P$	$V_{CC} = 2.7\text{ V}$ , $V_I = 0\text{ to }V_{CC}$		300		300	$\mu\text{A}$		
$I_{BHHO}^\#$	$V_{CC} = 2.7\text{ V}$ , $V_I = 0\text{ to }V_{CC}$		-300		-300	$\mu\text{A}$		
$I_{EX}^\parallel$	$V_{CC} = 2.3\text{ V}$ , $V_O = 5.5\text{ V}$		125		125	$\mu\text{A}$		
$I_{OZ}(\text{PU/PD})^*$	$V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V to }V_{CC}$ , $V_I = \text{GND or }V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$	$\mu\text{A}$		
$I_{CC}$	$V_{CC} = 2.7\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high	0.04	0.1	0.04	0.1	mA	
		Outputs low	2.3	4.5	2.3	4.5		
		Outputs disabled	0.04	0.1	0.04	0.1		
$C_i$	$V_{CC} = 2.5\text{ V}$ , $V_I = 2.5\text{ V or }0$		3.5		3.5	pF		
$C_{io}$	$V_{CC} = 2.5\text{ V}$ , $V_O = 2.5\text{ V or }0$		8		8	pF		

† All typical values are at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

\* High-impedance state during power up or power down

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electrical characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH162245		SN74ALVTH162245		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 3 V, I <sub>I</sub> = -18 mA		-1.2		-1.2		V
V <sub>OH</sub>	A port	V <sub>CC</sub> = 3 V to 3.6 V, I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V
		V <sub>CC</sub> = 3 V		2				
			I <sub>OH</sub> = -8 mA					
			I <sub>OH</sub> = -12 mA		2			
B port		V <sub>CC</sub> = 3 V to 3.6 V, I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V
		V <sub>CC</sub> = 3 V		2				
			I <sub>OH</sub> = -24 mA					
			I <sub>OH</sub> = -32 mA		2			
V <sub>OL</sub>	A port	V <sub>CC</sub> = 3 V to 3.6 V, I <sub>OL</sub> = 100 μA		0.2		0.2		V
		V <sub>CC</sub> = 3 V		?				
				I <sub>OL</sub> = 8 mA				
	B port	V <sub>CC</sub> = 3 V to 3.6 V, I <sub>OL</sub> = 100 μA		0.2		0.2		
		V <sub>CC</sub> = 3 V		0.5				
				I <sub>OL</sub> = 24 mA				
				I <sub>OL</sub> = 32 mA		0.5		
				I <sub>OL</sub> = 48 mA		0.55		
		I <sub>OL</sub> = 64 mA		0.55				
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1		±1		μA
		V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V		10		10		
	A or B ports	V <sub>CC</sub> = 3.6 V		20		20		
		V <sub>I</sub> = 5.5 V		1		1		
		V <sub>I</sub> = V <sub>CC</sub>		-5		-5		
		V <sub>I</sub> = 0						
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V				±100		μA	
I <sub>BHL</sub> ‡	V <sub>CC</sub> = 3 V, V <sub>I</sub> = 0.8 V		75		75		μA	
I <sub>BHH</sub> §	V <sub>CC</sub> = 3 V, V <sub>I</sub> = 2 V		-75		-75		μA	
I <sub>BHLO</sub> ¶	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 to V <sub>CC</sub>		500		500		μA	
I <sub>BHHO</sub> #	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 to V <sub>CC</sub>		-500		-500		μA	
I <sub>EX</sub>	V <sub>CC</sub> = 3 V, V <sub>O</sub> = 5.5 V		125		125		μA	
I <sub>OZ</sub> (PU/PD)*	V <sub>CC</sub> ≤ 1.2 V, V <sub>O</sub> = 0.5 V to V <sub>CC</sub> , V <sub>I</sub> = GND or V <sub>CC</sub> , OE = don't care		±100		±100		μA	
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs high		0.07 0.1		mA	
			Outputs low		3.2 5			
			Outputs disabled		0.07 0.1			
ΔI <sub>CC</sub> □	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.2		0.2		mA	
C <sub>i</sub>	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 3.3 V or 0		3.5		3.5		pF	
C <sub>io</sub>	V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = 3.3 V or 0		8		8		pF	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

¶ An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

# An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

|| Current into an output in the high state when V<sub>O</sub> > V<sub>CC</sub>

\* High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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# SN54ALVTH162245, SN74ALVTH162245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 30$  pF,  $V_{CC} = 2.5$  V  $\pm$  0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH162245		SN74ALVTH162245		UNIT
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	0.3	3.6	0.3	3.6	ns
t <sub>PHL</sub>			0.5	3.5	0.5	3.5	
t <sub>PLH</sub>	B	A	1.1	4.3	1.1	4.3	ns
t <sub>PHL</sub>			1.1	3.8	1.1	3.8	
t <sub>PZH</sub>	$\overline{OE}$	A	2	5.6	2	5.6	ns
t <sub>PZL</sub>			1.8	4.4	1.8	4.4	
t <sub>PZH</sub>	$\overline{OE}$	B	1.5	5.1	1.5	5.1	ns
t <sub>PZL</sub>			1.5	4.1	1.5	4.1	
t <sub>PHZ</sub>	$\overline{OE}$	A	1.9	4.9	1.9	4.9	ns
t <sub>PLZ</sub>			1.5	4.3	1.5	4.3	
t <sub>PHZ</sub>	$\overline{OE}$	B	1.9	4.8	1.9	4.8	ns
t <sub>PLZ</sub>			1.5	4.1	1.5	4.1	

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF,  $V_{CC} = 3.3$  V  $\pm$  0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH162245		SN74ALVTH162245		UNIT
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	0.5	3.1	0.5	3.1	ns
t <sub>PHL</sub>			0.5	3	0.5	3	
t <sub>PLH</sub>	B	A	1	3.7	1	3.7	ns
t <sub>PHL</sub>			1	3.4	1	3.4	
t <sub>PZH</sub>	$\overline{OE}$	A	1.4	4.7	1.4	4.7	ns
t <sub>PZL</sub>			1.4	3.9	1.4	3.9	
t <sub>PZH</sub>	OE	B	1	3.8	1	3.8	ns
t <sub>PZL</sub>			0.7	3.4	0.7	3.4	
t <sub>PHZ</sub>	$\overline{OE}$	A	2.4	5	2.4	5	ns
t <sub>PLZ</sub>			2.6	4.9	2.6	4.9	
t <sub>PHZ</sub>	$\overline{OE}$	B	2.4	4.7	2.4	4.7	ns
t <sub>PLZ</sub>			2.3	4.8	2.3	4.8	

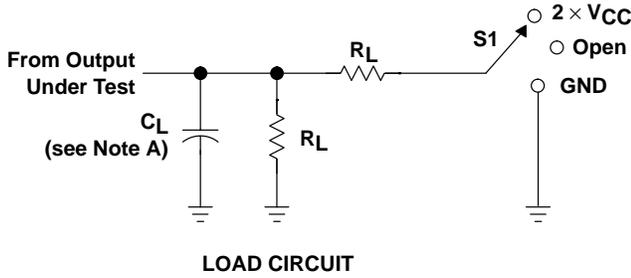
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



**SN54ALVTH162245, SN74ALVTH162245**  
**2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

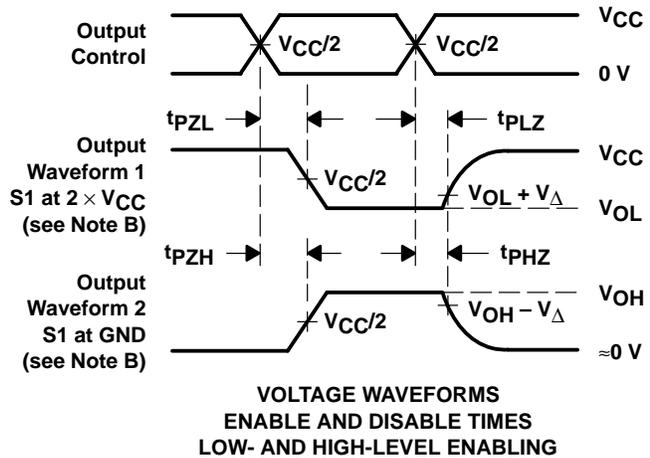
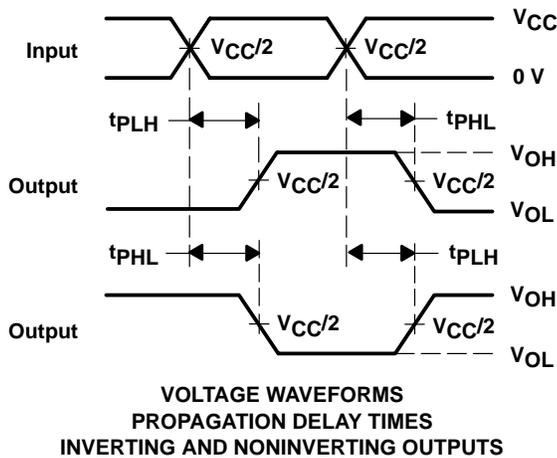
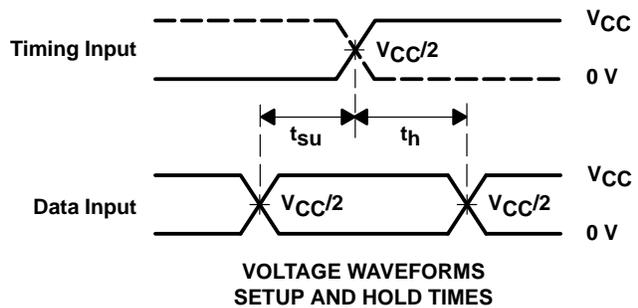
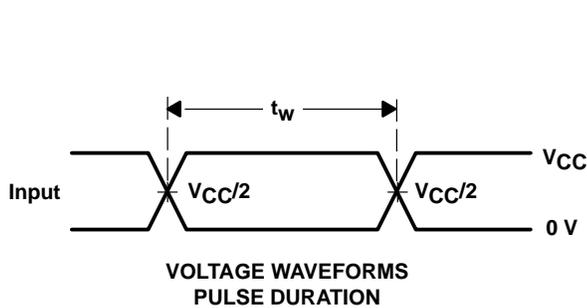
SCES331A – APRIL 2000 – REVISED APRIL 2002

**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>CC</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2 ns, t<sub>f</sub> ≤ 2 ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVTH162245LRG4	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH162245	<a href="#">Samples</a>
SN74ALVTH162245DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH162245	<a href="#">Samples</a>
SN74ALVTH162245GR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH162245	<a href="#">Samples</a>
SN74ALVTH162245LR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH162245	<a href="#">Samples</a>
SN74ALVTH162245VR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VT2245	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

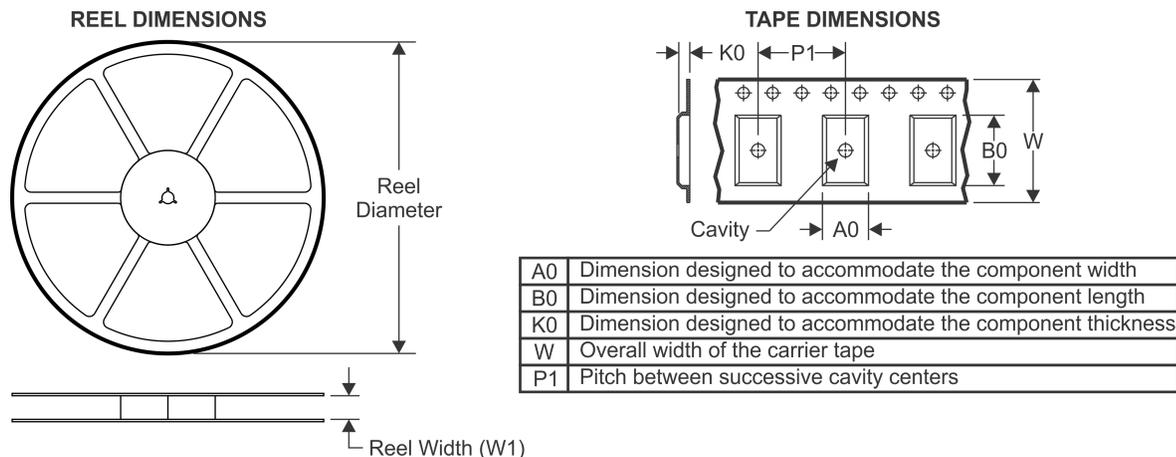
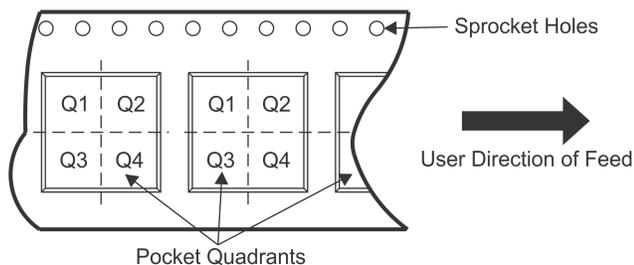
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

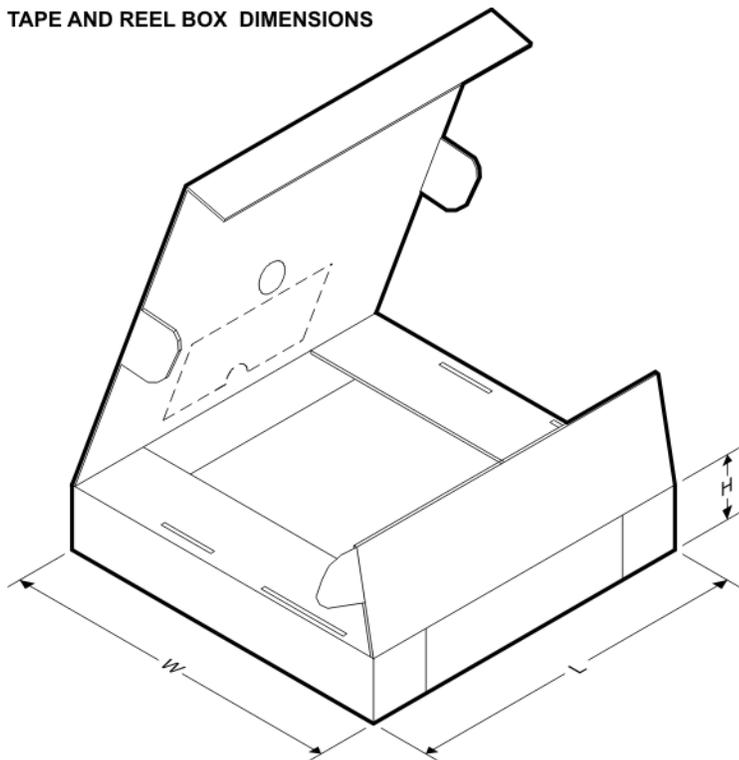
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


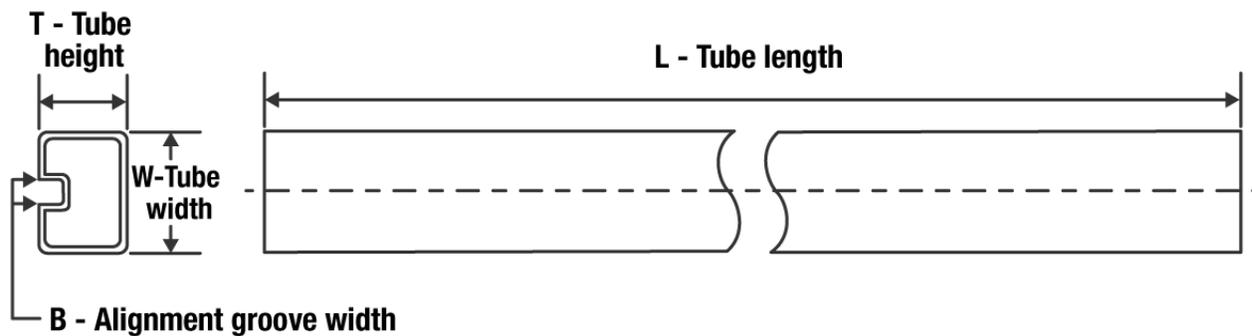
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVTH162245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVTH162245LR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVTH162245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVTH162245GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVTH162245LR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74ALVTH162245VR	TVSOP	DGV	48	2000	853.0	449.0	35.0

**TUBE**


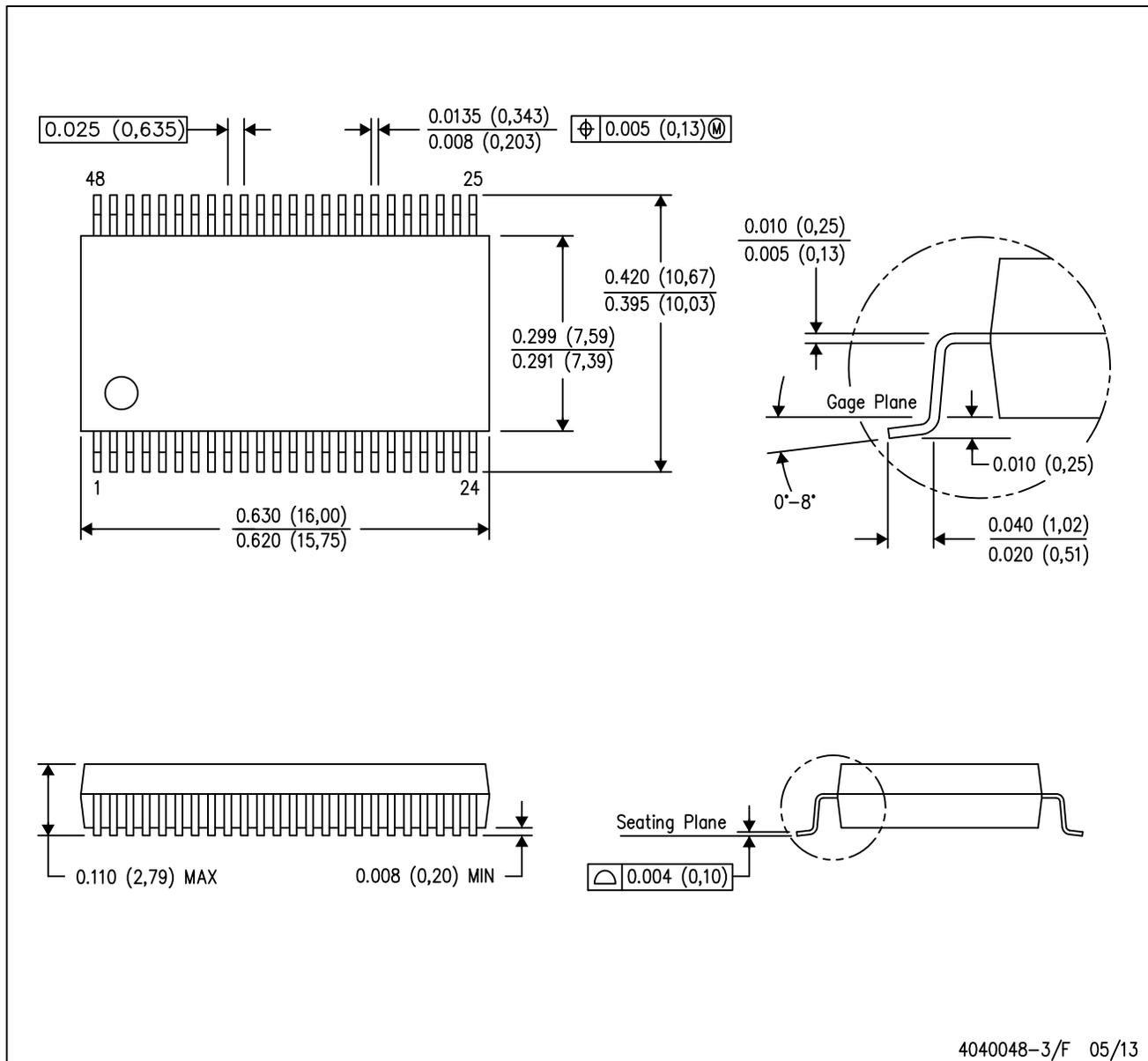
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALVTH162245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



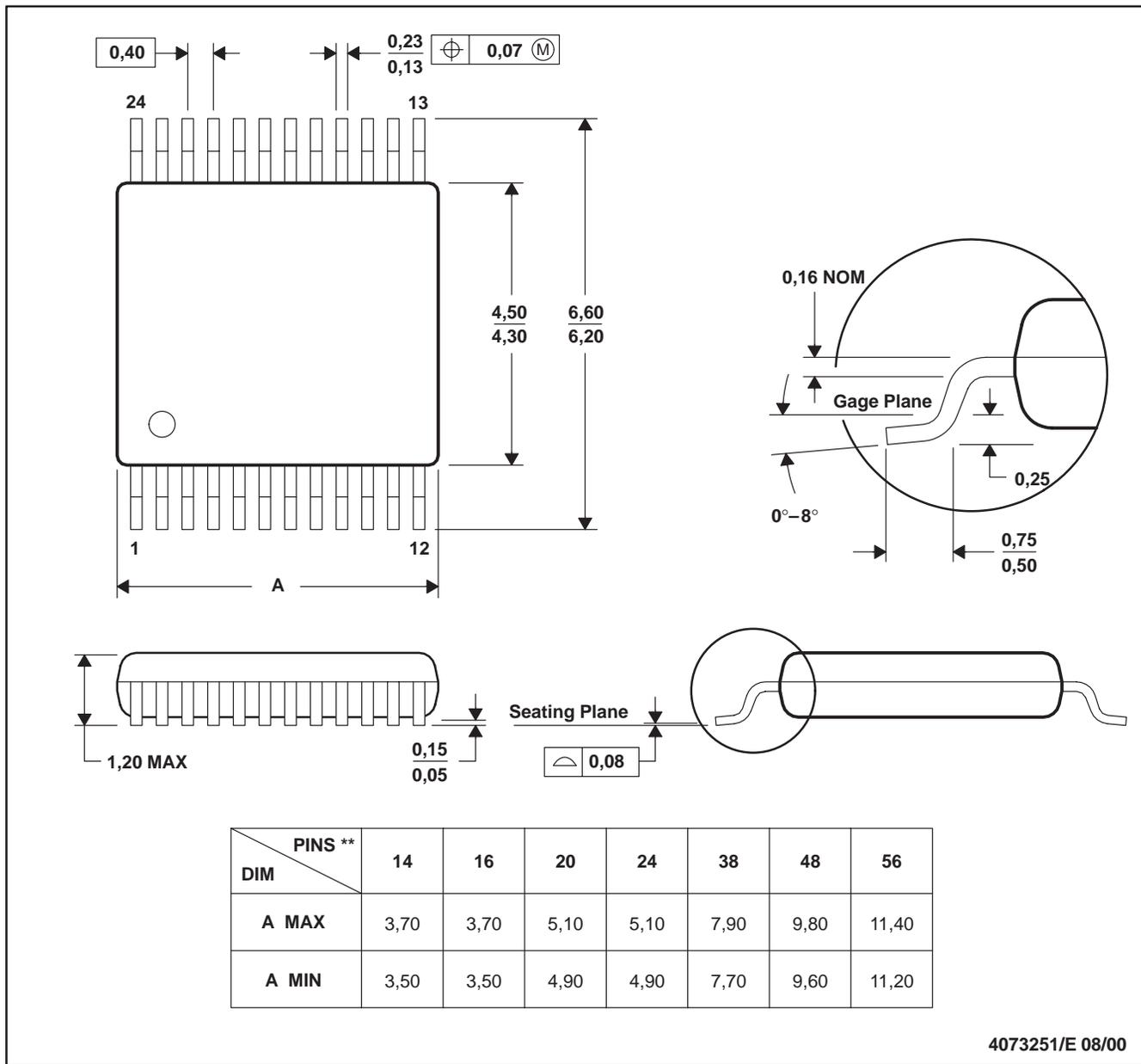
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

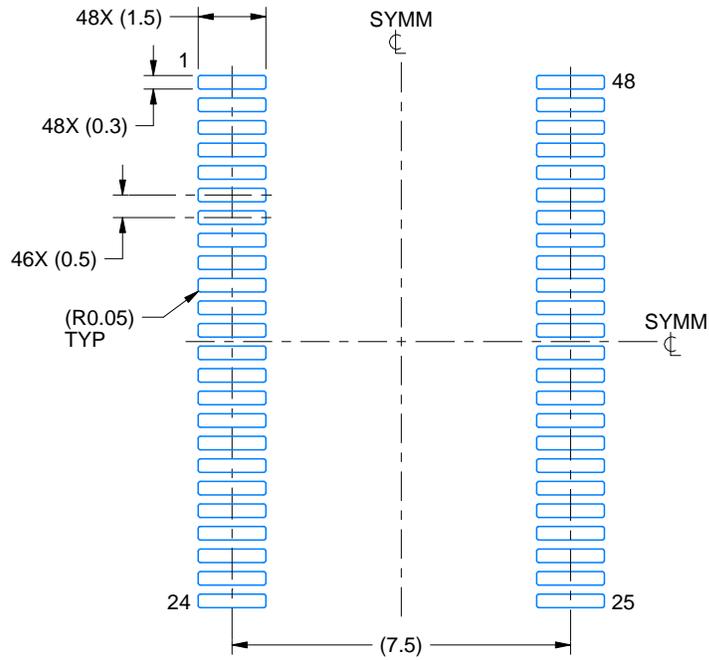


# EXAMPLE BOARD LAYOUT

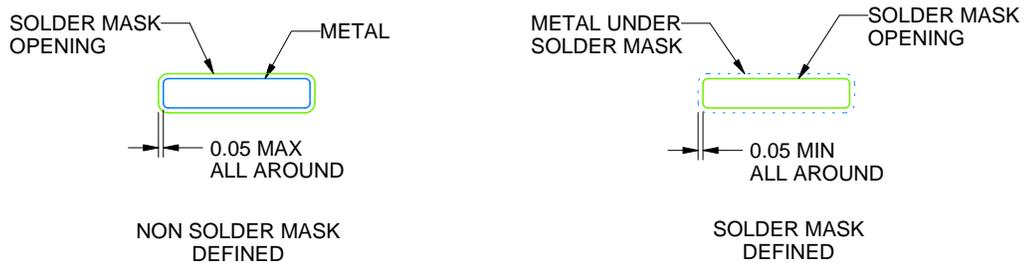
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

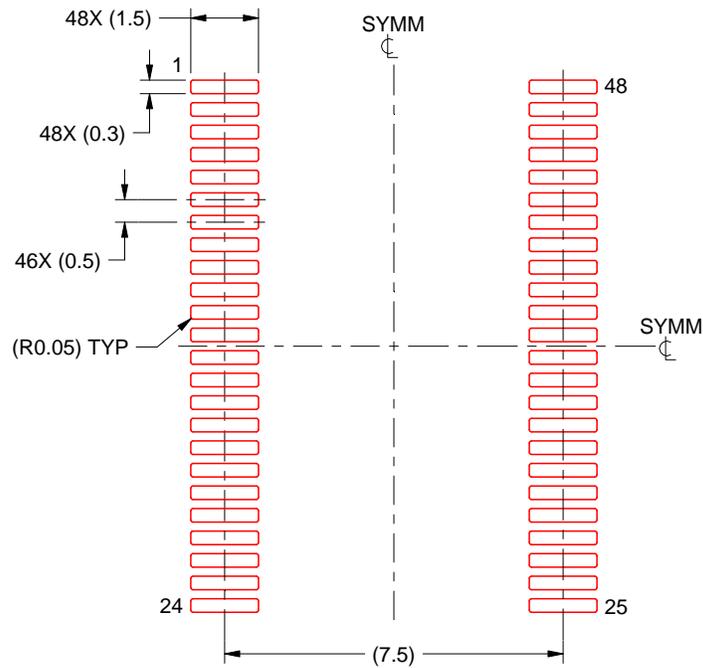
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

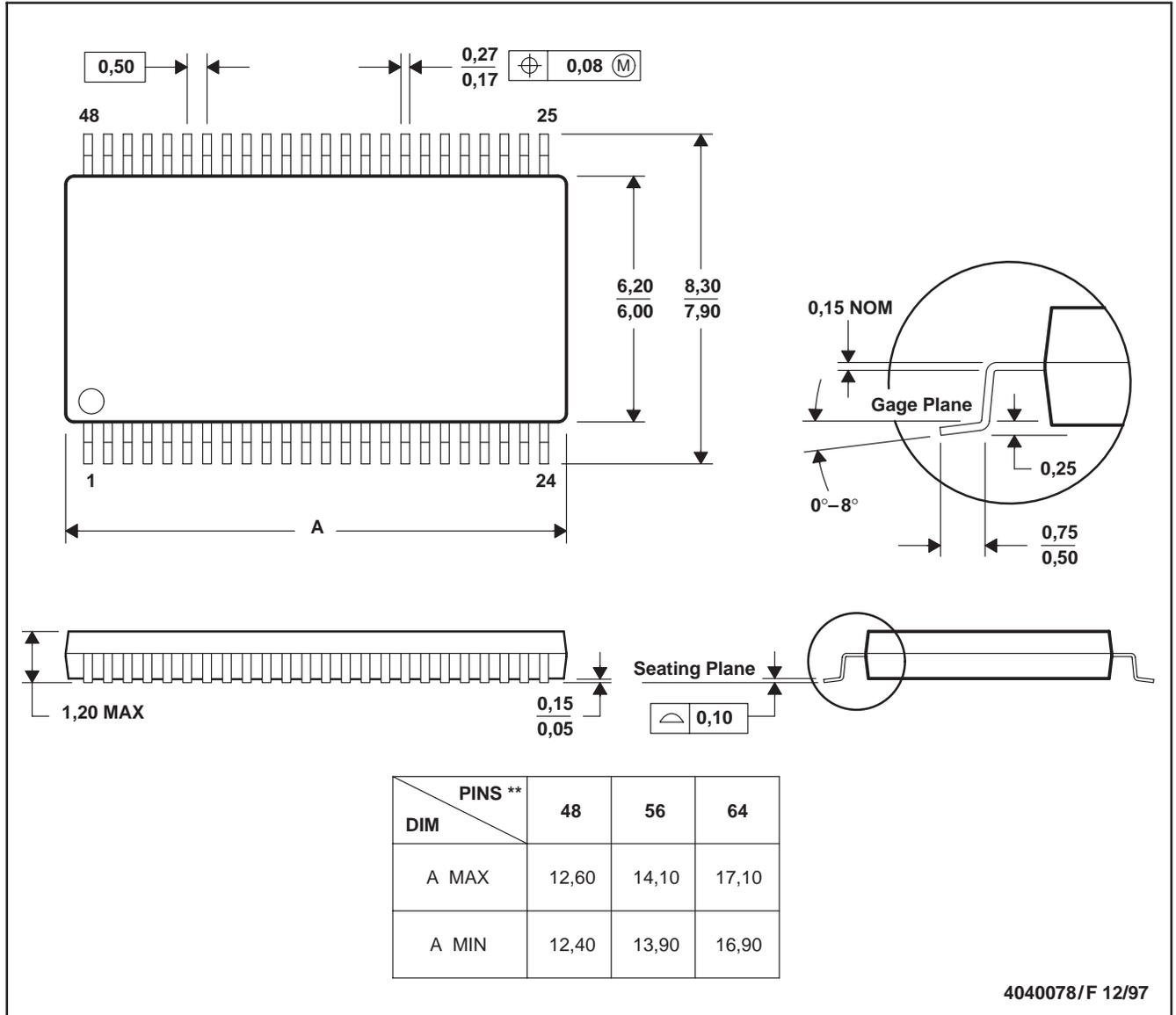
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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