SN74CB3Q3257 4 位 2 选 1 FET 多路复用器/多路信号分离器 2.5V/3.3V 低电压高带宽总线开关

1 特性

- 高带宽数据路径（高达 500 MHz）
- 可耐受 5V 电压和支持器件上电或断电的 I/O 端口
- 在运行范围内具有平缓的低通态电阻 (r_{on}) 特性（r_{on} 典型值 = 4 Ω）
- 数据 I/O 端口上的轨到轨切换
  - 3.3V V_{CC} 时的 0 至 5V 切换
  - 2.5V V_{CC} 时的 0 至 3.3V 切换
- 支持近零传播延迟的双向数据流
- 低输入和输出电容可最大限度地减小负载和信号失真（$C_{io(OFF)}$ 典型值 = 3.5 pF）
- 快速开关频率（$f_{\overline{OE}}$ 最大值 = 20 MHz）
- 数据与控制输入提供下冲钳位二极管
- 低功耗（I_{CC} 典型值 = 0.7 mA）
- 2.3V 至 3.6V 的 V_{CC} 工作电压范围
- 数据 I/O 支持 0 至 5 V 信号传输级 (0.8V，1.2V，1.5V，1.8V，2.5V，3.3V，5V)
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- I_{off} 支持局部关断模式运行
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)
- 支持数字和模拟 应用：USB 接口、微分信号接口，总线隔离、低失真信号门控 (1)

(1) 有关 CB3Q 系列器件性能特点的更多信息，请参考 TI 应用报告 *CBT-C、CB3T 和 CB3Q 信号开关系列*，SCDA008。

2 应用

- IP 电话：有线和无线
- 光学模块
- 光纤网络：光纤和 EPON 视频
- 专用交换机 (PBX)
- WiMAX 和无线基础设施设备

3 说明

SN74CB3Q3257 器件是一款高带宽 FET 总线开关，此开关利用一个电荷泵来提升通道晶体管的栅极电压，从而提供一个平缓的低通态电阻 (r_{on})。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74CB3Q3257DGV	TVSOP (16)	3.60mm × 4.40mm
SN74CB3Q3257DBQ	SSOP (16)	4.90mm × 3.90mm
SN74CB3Q3257PW	TSSOP (16)	5.00mm × 4.40mm
SN74CB3Q3257RGY	VQFN (16)	4.00mm × 3.50mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

逻辑图（正逻辑）

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

Changes from Revision C (April 2017) to Revision D — **Page**

- Changed the pinout images appearance ... 3
- Added *Thermal Information* table values ... 5

Changes from Revision B (June 2015) to Revision C — **Page**

- Added MAX values for T_A = –40°C to 105°C to the *Electrical Characteristics* table ... 5
- Added MAX values for T_A = –40°C to 105°C to the *Switching Characteristics, V_{CC} = 2.5 V* table. ... 6
- Added separate *Switching Characteristics, V_{CC} = 3.3 V* for V_{CC} = 3.3 V ± 0.3 V. Added TYP values and MAX values for T_A = –40°C to 105°C ... 6

Changes from Revision A (November 2003) to Revision B — **Page**

- 删除了*订购信息* 表。 ... 1
- 添加了*器件信息* 表、*引脚配置和功能* 部分、*ESD 额定值* 表、*特性 说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分和*机械、封装和可订购信息*部分 ... 1

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5 Pin Configuration and Functions

D, DB, DGV, DBQ, or PW Package
16-Pin SOIC, SSOP TVSOP, or TSSOP
Top View

RGY Package
16-Pin VQFN
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
S	1	I	Select Pin
1B1	2	I/O	Channel 1 I/O 1
1B2	3	I/O	Channel 1 I/O 2
1A	4	I/O	Channel 1 common
2B1	5	I/O	Channel 2 I/O 1
2B2	6	I/O	Channel 2 I/O 2
2A	7	I/O	Channel 2 common
GND	8	—	Ground
3A	9	I/O	Channel 3 common
3B2	10	I/O	Channel 3 I/O 2
3B1	11	I/O	Channel 3 I/O 1
4A	12	I/O	Channel 4 common
4B2	13	I/O	Channel 4 I/O 2
4B1	14	I/O	Channel 4 I/O 1
$\overline{OE}$	15	I	Output Enable (Active Low)
V_{CC}	16	—	Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage[2][3]		–0.5	7	V
$V_{I/O}$	Switch I/O voltage[2][3][4]		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
I_{IO}	ON-state switch current			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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6.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3257				UNIT
		DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.3	126.0	112.7	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.4	51.3	47.5	61.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8	57.8	57.8	25.9	
ψ_{JT}	Junction-to-top characterization parameter	18.3	5.9	6.0	2.3	
ψ_{JB}	Junction-to-board characterization parameter	56.4	57.3	57.3	26.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	11.4	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to 105°C. Typical values stated are over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V, I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ}[3]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF V_{IN} = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0				1	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND			0.7	1.5	mA
ΔI_{CC}[4]	Control inputs	V_{CC} = 3.6 V, One input at 3 V, Other inputs at V_{CC} or GND				30	µA
I_{CCD}[5]	Per control input	V_{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle			0.3	0.35	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or 0			5.5	7	pF
	B port	V_{CC} = 3.3 V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or 0			3.5	5	pF
$C_{io(ON)}$	A port	V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or 0			10.5	13	pF
	B port				10.5	13	
r_{on}[6]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0, I_O = 30 mA		4	8	Ω
			V_I = 1.7 V, I_O = –15 mA		4	9	
		V_{CC} = 3 V	V_I = 0, I_O = 30 mA		4	6	
			V_I = 2.4 V, I_O = –15 mA		4	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data terminals.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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6.6 Switching Characteristics, V_{CC} = 2.5 V

Typical values stated are over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V			UNIT
			MIN	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B		10	10	MHz
t_{pd} (2)	A or B	B or A		0.12	0.21	ns
$t_{pd(s)}$	S	A	1.5	6.5	7.5	ns
t_{en}	S	B	1.5	6.5	7.5	ns
	$\overline{OE}$	A or B	1.5	6.5	7.5	
t_{dis}	S	B	1	6	7	ns
	$\overline{OE}$	A or B	1	6	7	

(1) Maximum switching frequency for control inputs ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Switching Characteristics, V_{CC} = 3.3 V

Typical values stated are over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V				UNIT
			MIN	TYP (1)	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (2)	$\overline{OE}$ or S	A or B			20	20	MHz
t_{pd} (3)	A or B	B or A			0.2	0.32	ns
$t_{pd(s)}$	S	A	1.5	4.1	5.5	6.5	ns
t_{en}	S	B	1.5	4.6	5.5	6.5	ns
	$\overline{OE}$	A or B	1.5	4.7	5.5	6.5	
t_{dis}	S	B	1	3.3	6	7	ns
	$\overline{OE}$	A or B	1	3.1	6	7	

(1) TYP taken from average in 105°C
(2) Maximum switching frequency for control inputs ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).
(3) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.8 Typical Characteristics

Figure 1. Typical r_{on} vs V_I

Figure 2. Typical I_{CC} vs $\overline{OE}$ or S Switching Frequency

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7 Parameter Measurement Information

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CB3Q3257 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3257 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3257 device is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

(1) EN is the internal enable signal applied to the switch.

Figure 4. Simplified Schematic, Each FET Switch (SW)

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8.2 Functional Block Diagram

8.3 Feature Description

The SN74CB3Q3257 device has a high-bandwidth data path (up to 500 MHz) and has 5-V tolerant I/Os with the device powered up or powered down. It also has low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 4 Ω Typical).

This device also has rail-to-rail switching on data I/O ports for 0- to 5-V switching with 3.3-V $V_{CC}$and 0- to 3.3-V switching with 2.5-V V_{CC}as well as bidirectional data flow with near-zero propagation delay and low input/output capacitance that minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5 pF Typical).

The SN74CB3Q3257 also provides a fast switching frequency ($f_{\overline{OE}}$ = 20 MHz Max) with data and control inputs that provide undershoot clamp diodes as well as low power consumption (I_{CC} = 0.6 mA Typical).

The V_{CC} operating range is from 2.3 V to 3.6 V and the data I/Os support 0- to 5-V signal levels of (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V).

The control inputs can be driven by TTL or 5-V / 3.3-V CMOS outputs as well as I_{off} Supports Partial-Power-Down Mode Operation.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CB3Q3257.

Table 1. Function Table

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CB3Q3257 can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus being multiplexed between two devices. the $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

9.2 Typical Application

Figure 5. Typical Application of the SN74CB3Q3257

9.2.1 Design Requirements

1. Recommended Input Conditions:
   – For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   – Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6 V at any valid V_{CC}.
2. Recommended Output Conditions:
   – Load currents should not exceed ±128 mA per channel.
3. Frequency Selection Criterion:
   – Maximum frequency tested is 500 MHz.
   – Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

9.2.2 Detailed Design Procedure

The 0.1-µF capacitor should be place as close as possible to the device.

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Typical Application (continued)

9.2.3 Application Curve

Figure 6. Propagation Delay (t_{pd}) Simulation Result at V_{CC} = 2.5 V.

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Absolute Maximum Ratings* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 7 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

Figure 7. Trace Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《CMOS 输入缓慢变化或悬空的影响》*，SCBA004
- *选择合适的德州仪器 (TI) 信号开关*，SZZA030

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

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12.5 静电放电警告

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12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CB3Q3257DBQRE4	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	Samples
74CB3Q3257RGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	Samples
SN74CB3Q3257DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	Samples
SN74CB3Q3257DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	Samples
SN74CB3Q3257PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	Samples
SN74CB3Q3257PWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	Samples
SN74CB3Q3257PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	Samples
SN74CB3Q3257PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU257	Samples
SN74CB3Q3257PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257	Samples
SN74CB3Q3257RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3Q3257PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74CB3Q3257PWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74CB3Q3257PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

PW0016A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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