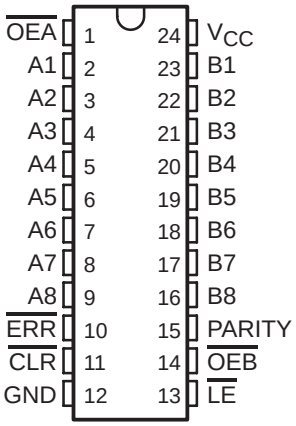
- **BiCMOS Process With TTL Inputs and Outputs**
- **State-of-the-Art BiCMOS Design Significantly Reduces Standby Current**
- **Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Functionally Equivalent to AMD Am29854**
- **High-Speed Bus Transceiver With Parity Generator/Checker**
- **Parity-Error Flag With Open-Collector Output**
- **Latch for Storage of the Parity-Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT29854 is an 8-bit to 9-bit parity transceiver designed for asynchronous communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the parity-error ($\overline{ERR}$) output will indicate whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$, $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector parity-error ($\overline{ERR}$) flag. $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{LE}$) and clear ($\overline{CLR}$) control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition which gives the designer more system diagnostic capability. The SN74BCT29854 provides inverting logic.

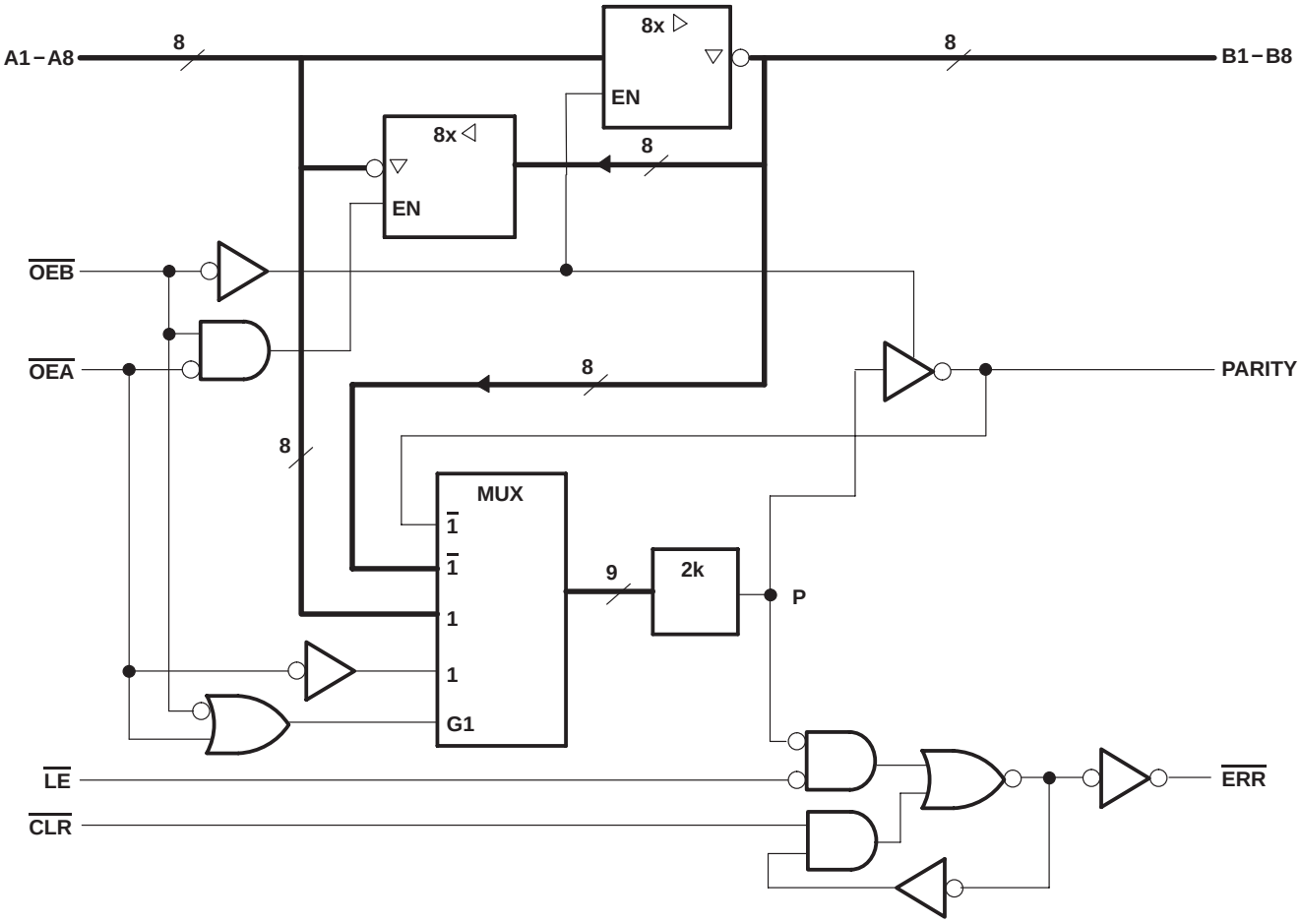
The SN74BCT29854 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai ∑ of H's	Bi† ∑ of L's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ data to B bus and generate parity
H	L	X	L	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N−1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of low-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output, when enabled, shows noninverted parity of the A bus.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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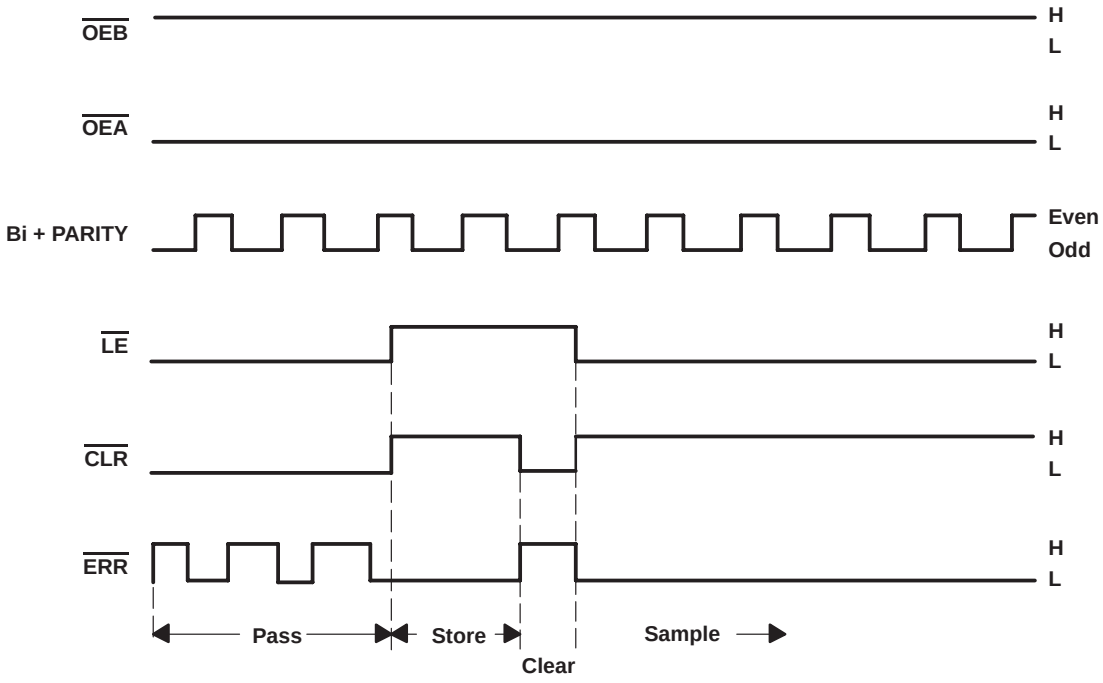
error-flag waveforms



ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
L	L	L H	X	L H	Pass
L	H	L X H	X L H	L L H	Sample
H	L	X	X	H	Clear
H	H	X	L H	L H	Store

† $\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	$\overline{ERR}$			2.4	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4			V
			I_{OH} = −24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 2.4 V			20	µA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}‡	Data	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Control					−0.75	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−75		−250	mA
I_{CCL}		V_{CC} = 5.5 V,	Outputs open		55	80	mA
I_{CCZ}		V_{CC} = 5.5 V,	Outputs open		30	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters include off-state output current for I/O ports only.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	$\overline{LE}$ low	10		ns
		$\overline{CLR}$ low	10		
t_{su}	Setup time before $\overline{LE}$↓	Bi and PARITY	18		ns
t_h	Hold time after $\overline{LE}$↓	Bi and PARITY	8		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1	5	7	1	8	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	12	15	2	17	ns
t_{PZL}			2	13	16	2	19	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	8	11	2	15	ns
t_{PLZ}			2	10	14	2	17	
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	11	13	1.5	15	ns
t_{PHL}	$\overline{LE}$		1.5	5	7	1.5	9	
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	16	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	1.5	15	18	1.5	20	ns
t_{PHL}			1.5	10	13	1.5	15	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74BCT29854DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT29854	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

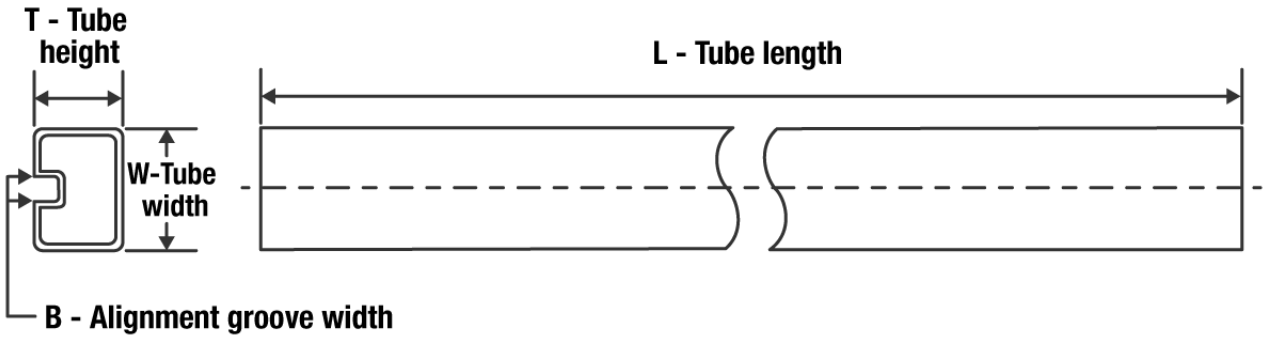
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

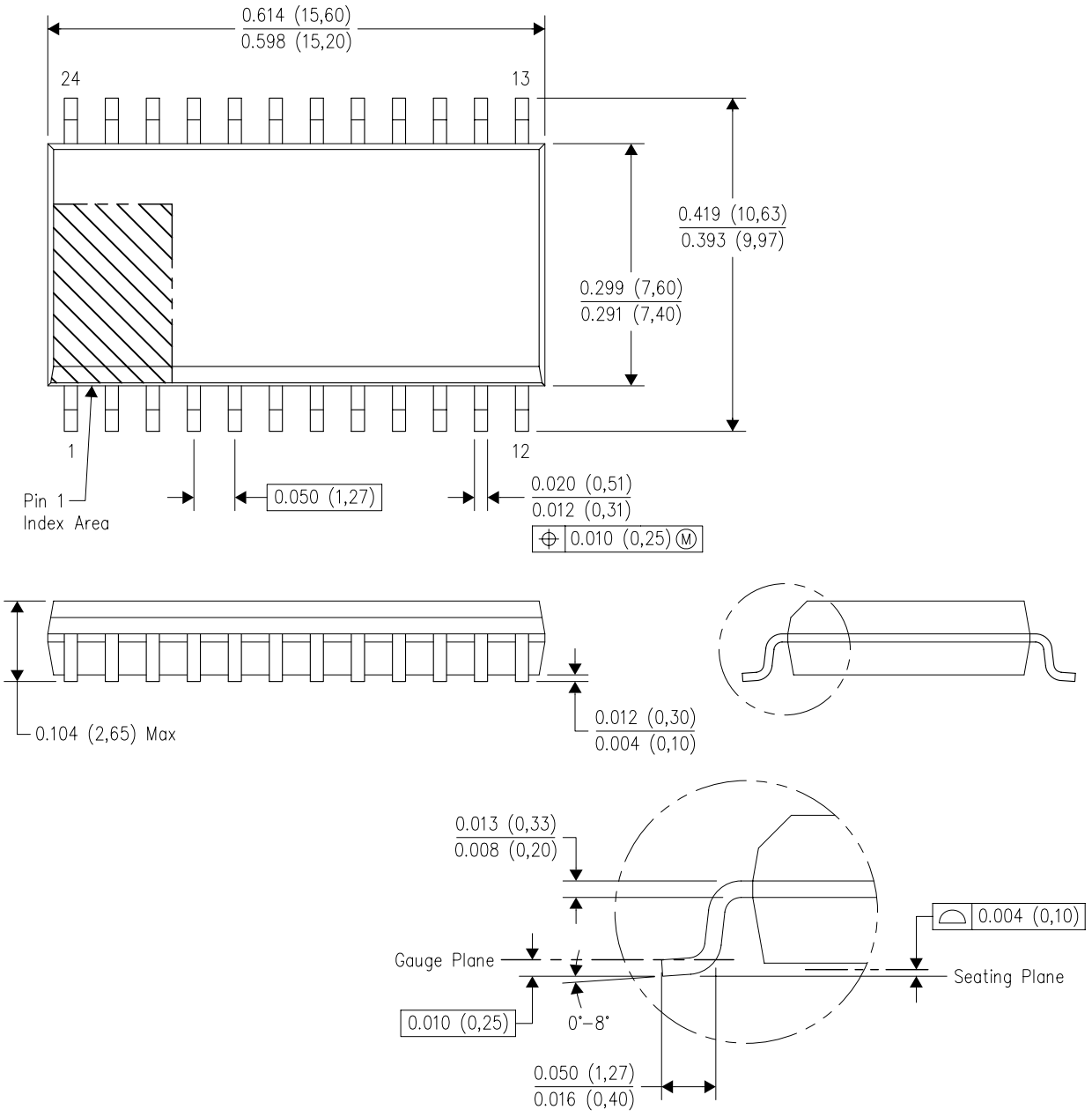
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74BCT29854DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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