

## FEATURES

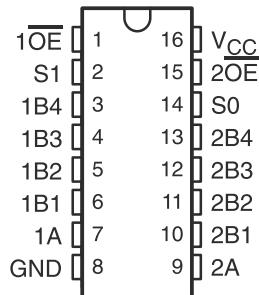
- SN74CBT3253C Functionally Identical to Industry-Standard '3253 Function
- Undershoot Protection for Off-Isolation on A and B Ports up to -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 5.5 \text{ pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3 \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports I<sup>2</sup>C Bus Expansion
- Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating

## DESCRIPTION/ORDERING INFORMATION

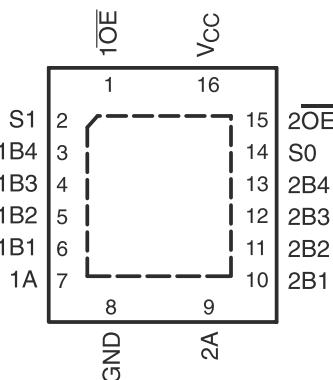
The SN74CBT3253C is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3253C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3253C is organized as two 1-of-4 multiplexer/demultiplexers with separate output-enable ( $\overline{OE}$ ,  $\overline{2OE}$ ) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When  $\overline{OE}$  is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

D, DB, DBQ, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

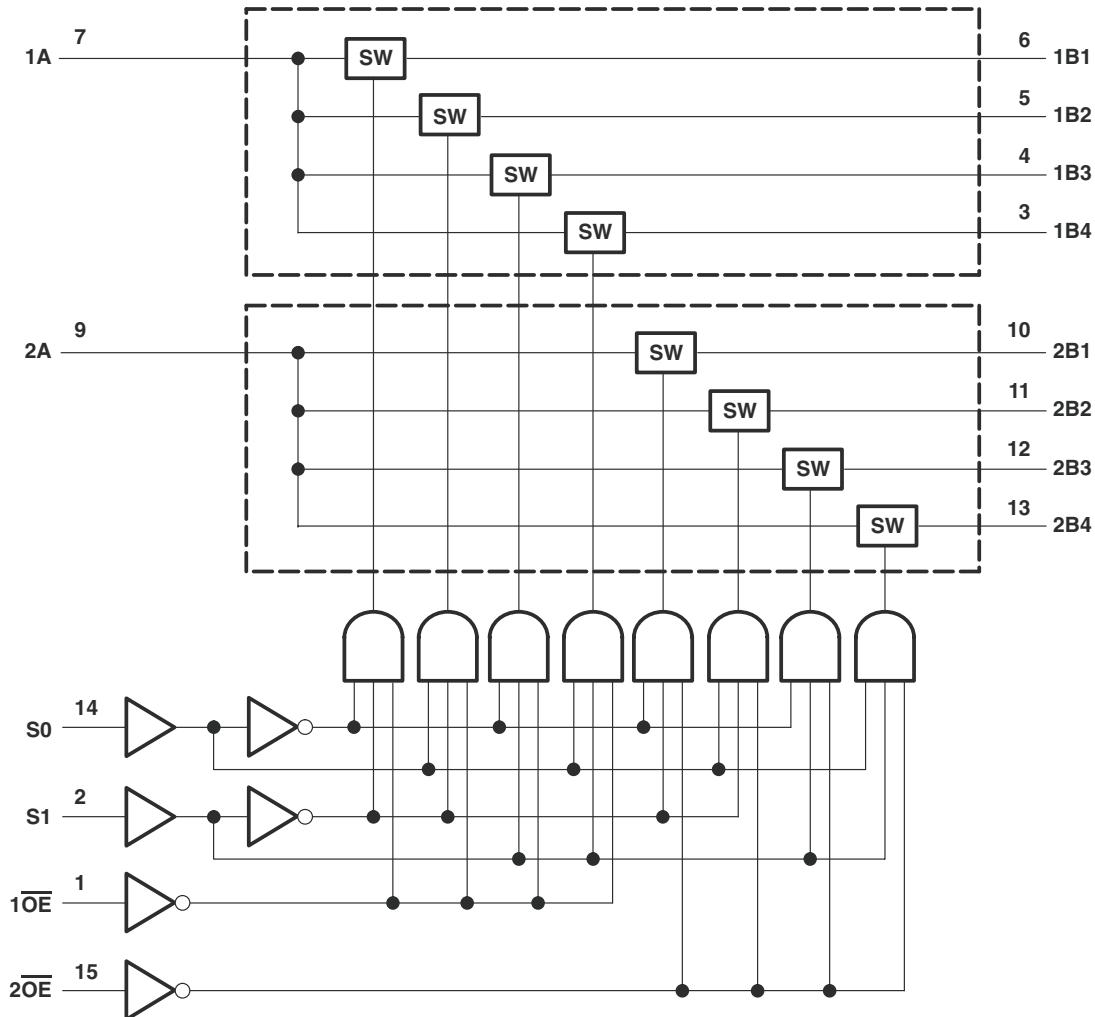
$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	QFN – RGY	Reel of 1000	SN74CBT3253CRGYR	CU253C
	SOIC – D	Tube of 40	SN74CBT3253CD	CBT3253C
		Reel of 2500	SN74CBT3253CDR	
	SSOP – DB	Tube of 80	SN74CBT3253CDB	CU253C
		Reel of 2000	SN74CBT3253CDBR	
	SSOP (QSOP) – DBQ	Reel of 2500	SN74CBT3253CDBQR	CU253C
	TSSOP – PW	Tube of 90	SN74CBT3253CPW	CU253C
		Reel of 2000	SN74CBT3253CPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

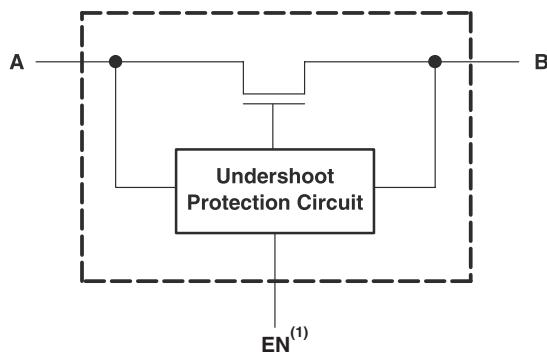
### FUNCTION TABLE (each multiplexer/demultiplexer)

INPUTS			INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	X	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	7	V
$I_{IK}$	Control input clamp current	$V_{IN} < 0$	-50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$	-50	mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		$\pm 128$	mA
	Continuous current through $V_{CC}$ or GND terminals		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance	D package <sup>(6)</sup>	73	°C/W
		DB package <sup>(6)</sup>	82	
		DBQ package <sup>(6)</sup>	90	
		PW package <sup>(6)</sup>	108	
		RGY package <sup>(7)</sup>	39	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.
- (7) The package thermal impedance is calculated in accordance with JESD 51-5.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2	5.5	V
$V_{IL}$	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics<sup>(1)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IK</sub>	Control inputs	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA					-1.8	V
V <sub>IKU</sub>	Data inputs	V <sub>CC</sub> = 5 V, 0 mA > I <sub>I</sub> ≥ -50 mA, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch OFF					-2	V
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub> or GND					±1	µA
I <sub>OZ</sub> <sup>(3)</sup>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, V <sub>IN</sub> = V <sub>CC</sub> or GND					±10	µA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0					10	µA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>I/O</sub> = 0, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch ON or OFF					3	µA
ΔI <sub>CC</sub> <sup>(4)</sup>	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					2.5	mA
C <sub>in</sub>	Control inputs	V <sub>IN</sub> = 3 V or 0					3.5	pF
C <sub>io(OFF)</sub>	A port	V <sub>I/O</sub> = 3 V or 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND					14	pF
	B port						5.5	
C <sub>io(ON)</sub>		V <sub>I/O</sub> = 3 V or 0, Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND					22	pF
r <sub>on</sub> <sup>(5)</sup>	V <sub>CC</sub> = 4 V, TYP at V <sub>CC</sub> = 4 V		V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA		8	12		Ω
	V <sub>CC</sub> = 4.5 V		V <sub>I</sub> = 0	I <sub>O</sub> = 64 mA	3	6		
				I <sub>O</sub> = 30 mA	3	6		
			V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA		5	10		

 (1) V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

 (2) All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

 (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

 (4) This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**Switching Characteristics**

 over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>(1)</sup>	A or B	B or A	0.24		0.15		ns
t <sub>pd(s)</sub>	S	A	5.9		1.5	5.4	ns
t <sub>en</sub>	S	B	6.2		1.5	5.8	ns
	OE	A or B	5.7		1.5	5.3	
t <sub>dis</sub>	S	B	6.2		1.5	5.8	ns
	OE	A or B	5.7		1.5	5.3	

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## Undershoot Characteristics

See [Figure 1](#) and [Figure 2](#)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OUTU}$	$V_{CC} = 5.5$ V, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

(1) All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

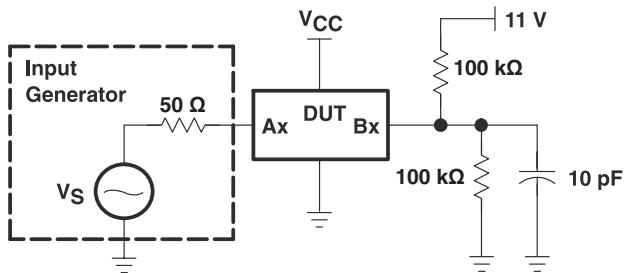


Figure 1. Device Test Setup

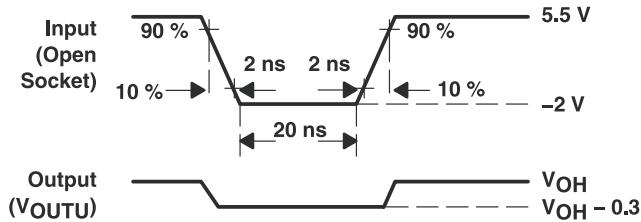
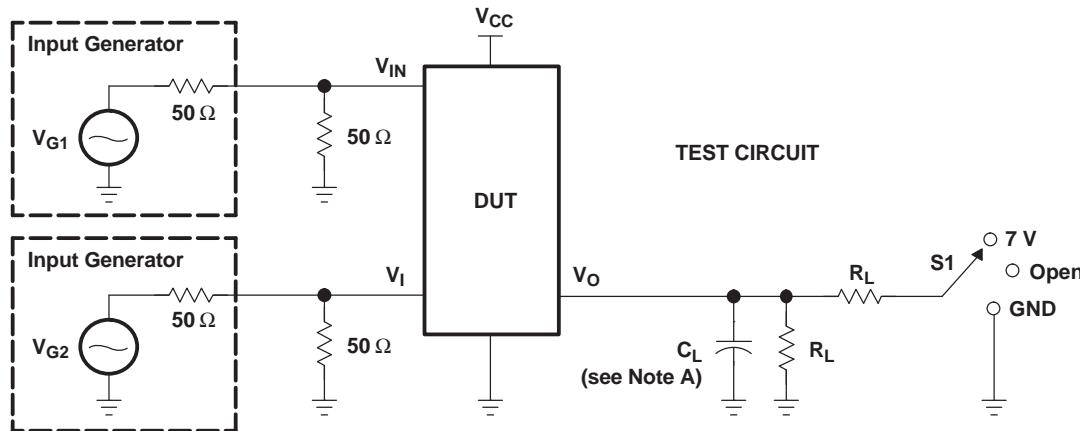
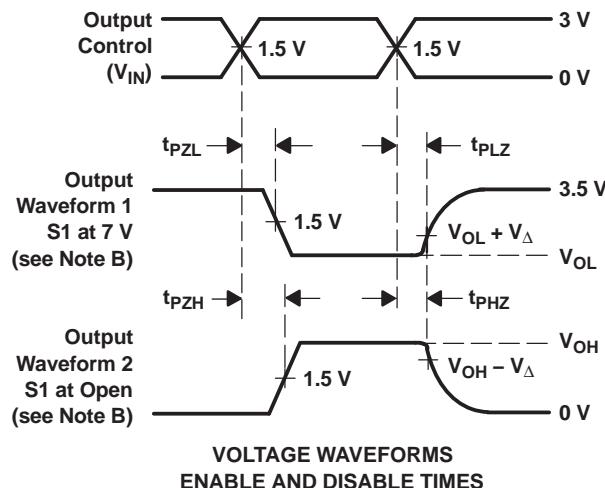
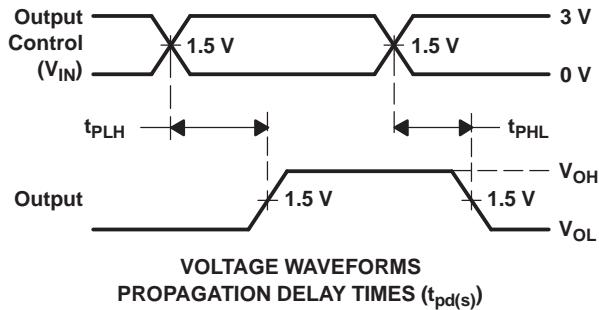


Figure 2. Transient Input Voltage ( $V_i$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION



TEST	$V_{CC}$	S1	$R_L$	$V_I$	$C_L$	$V_\Delta$
$t_{pd(s)}$	$5 \text{ V} \pm 0.5 \text{ V}$ $4 \text{ V}$	Open Open	$500 \Omega$ $500 \Omega$	$V_{CC}$ or GND $V_{CC}$ or GND	$50 \text{ pF}$ $50 \text{ pF}$	
$t_{PLZ}/t_{PZL}$	$5 \text{ V} \pm 0.5 \text{ V}$ $4 \text{ V}$	7 V 7 V	$500 \Omega$ $500 \Omega$	GND GND	$50 \text{ pF}$ $50 \text{ pF}$	$0.3 \text{ V}$ $0.3 \text{ V}$
$t_{PHZ}/t_{PZH}$	$5 \text{ V} \pm 0.5 \text{ V}$ $4 \text{ V}$	Open Open	$500 \Omega$ $500 \Omega$	$V_{CC}$ $V_{CC}$	$50 \text{ pF}$ $50 \text{ pF}$	$0.3 \text{ V}$ $0.3 \text{ V}$



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd(s)}$ . The  $t_{pd}$  propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3253CD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3253CRGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU253C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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## PACKAGE OPTION ADDENDUM

10-Dec-2020

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

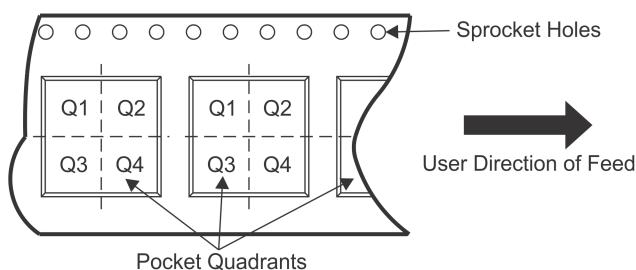
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

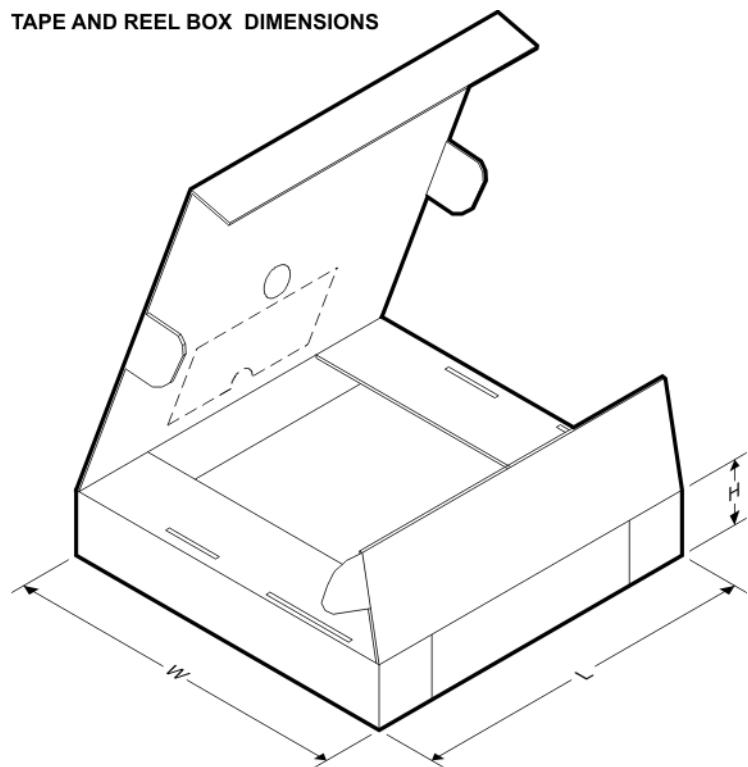
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


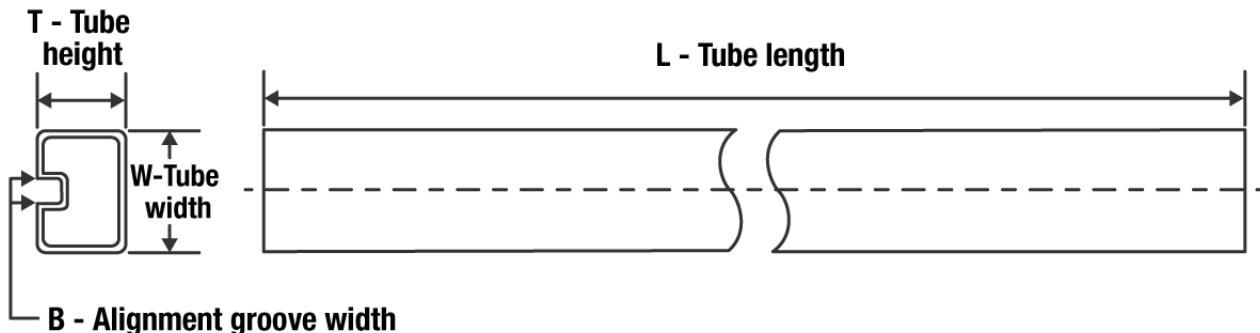
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3253CDBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3253CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74CBT3253CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBT3253CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3253CRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3253CDBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBT3253CDBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74CBT3253CDR	SOIC	D	16	2500	340.5	336.1	32.0
SN74CBT3253CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBT3253CRGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

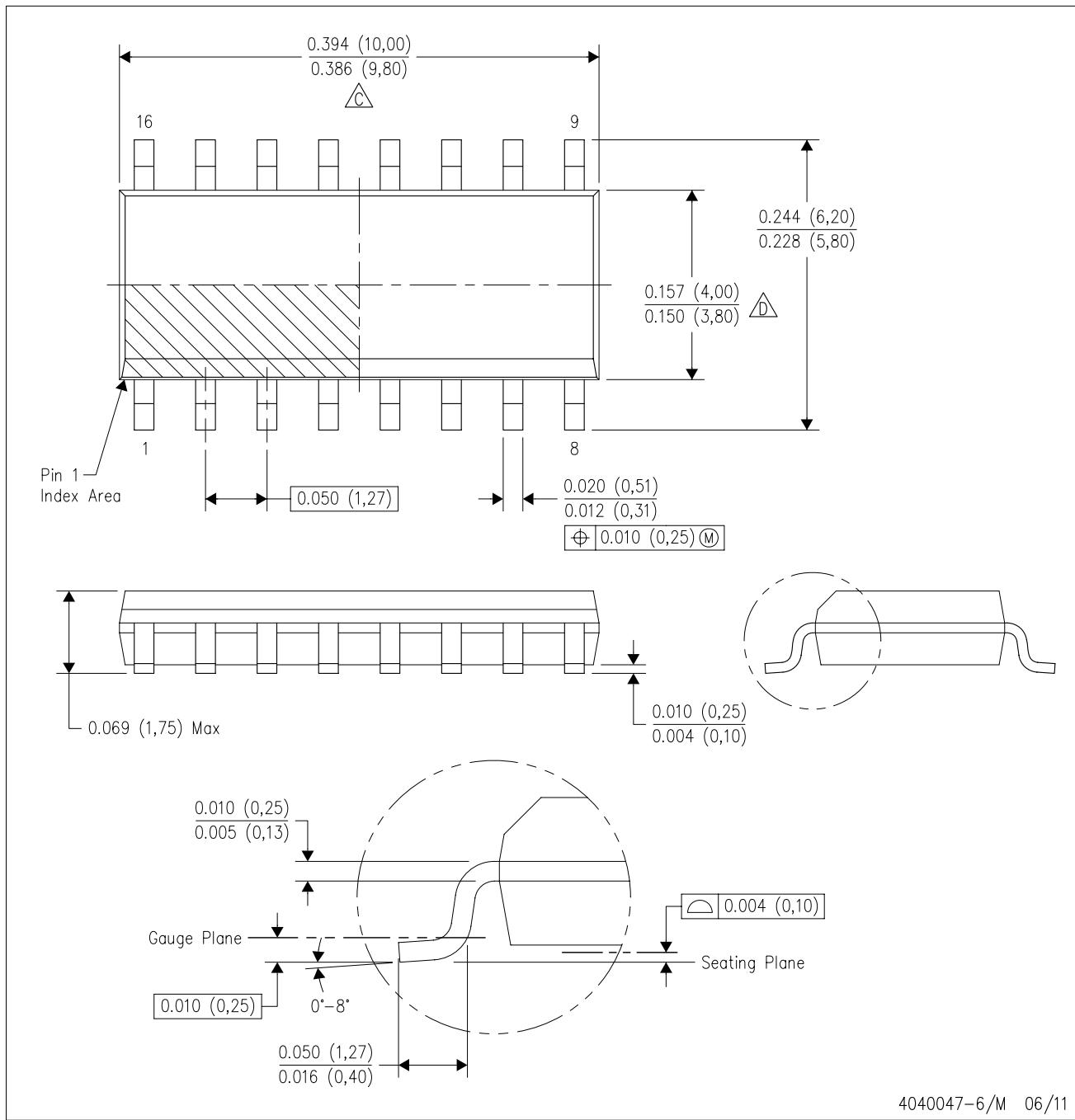
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3253CD	D	SOIC	16	40	507	8	3940	4.32
SN74CBT3253CPW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

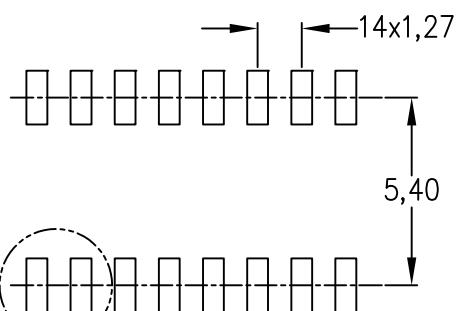
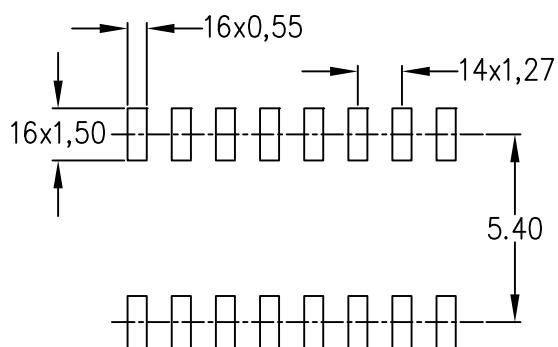
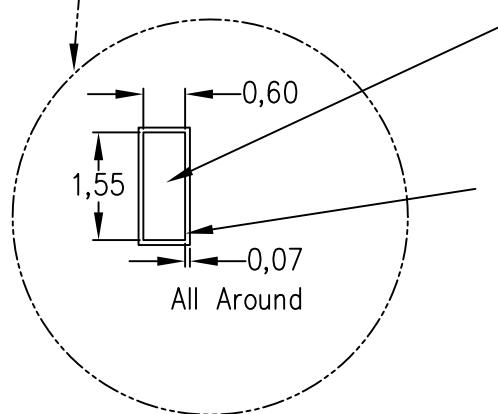
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

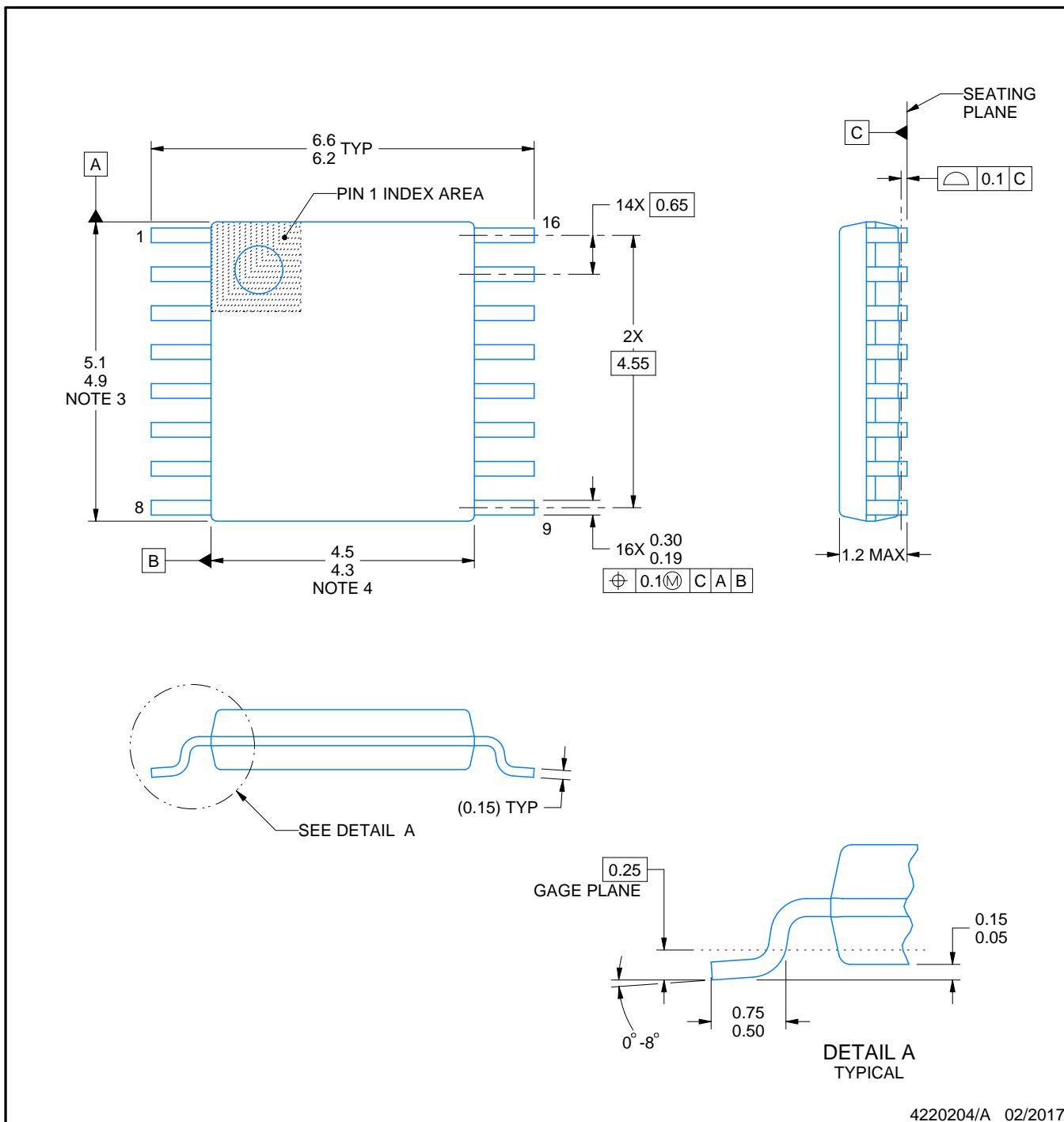
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

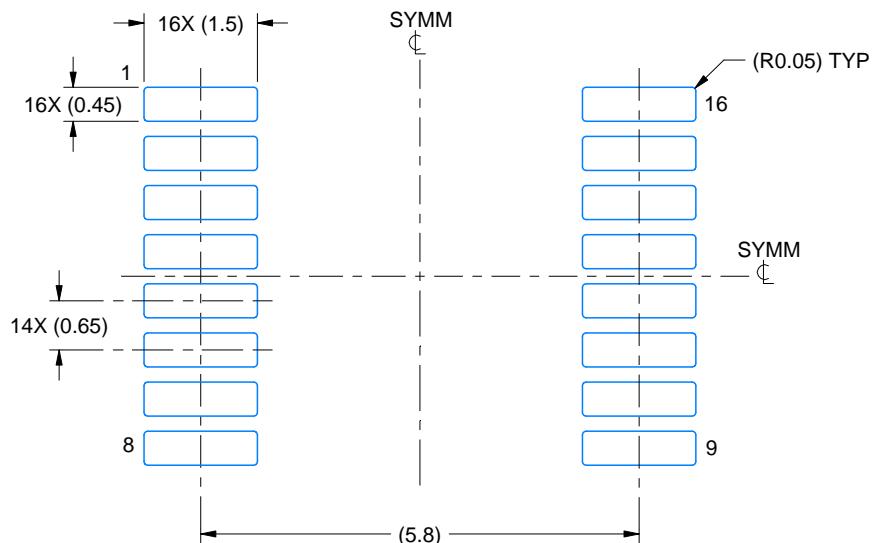
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

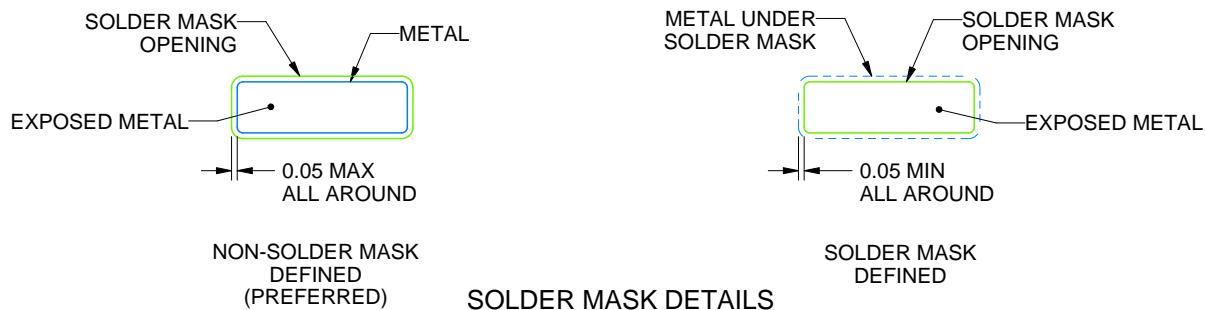
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

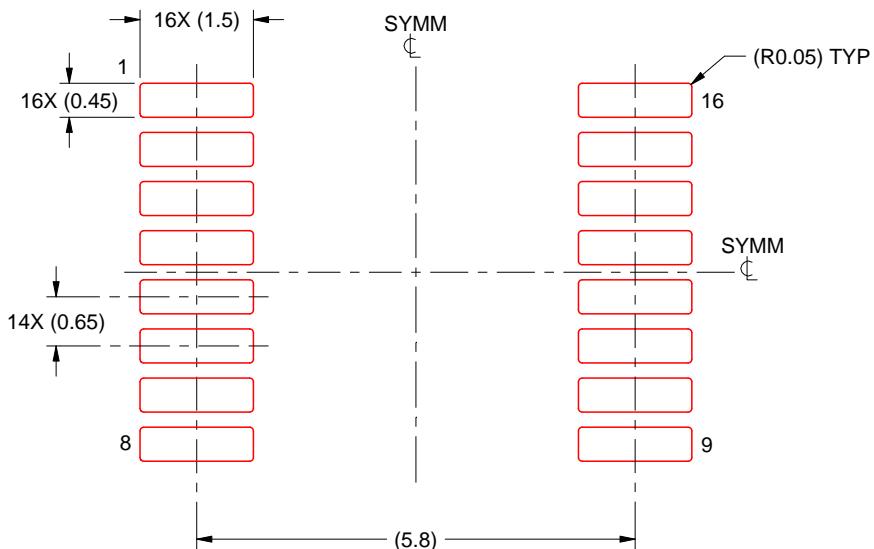
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

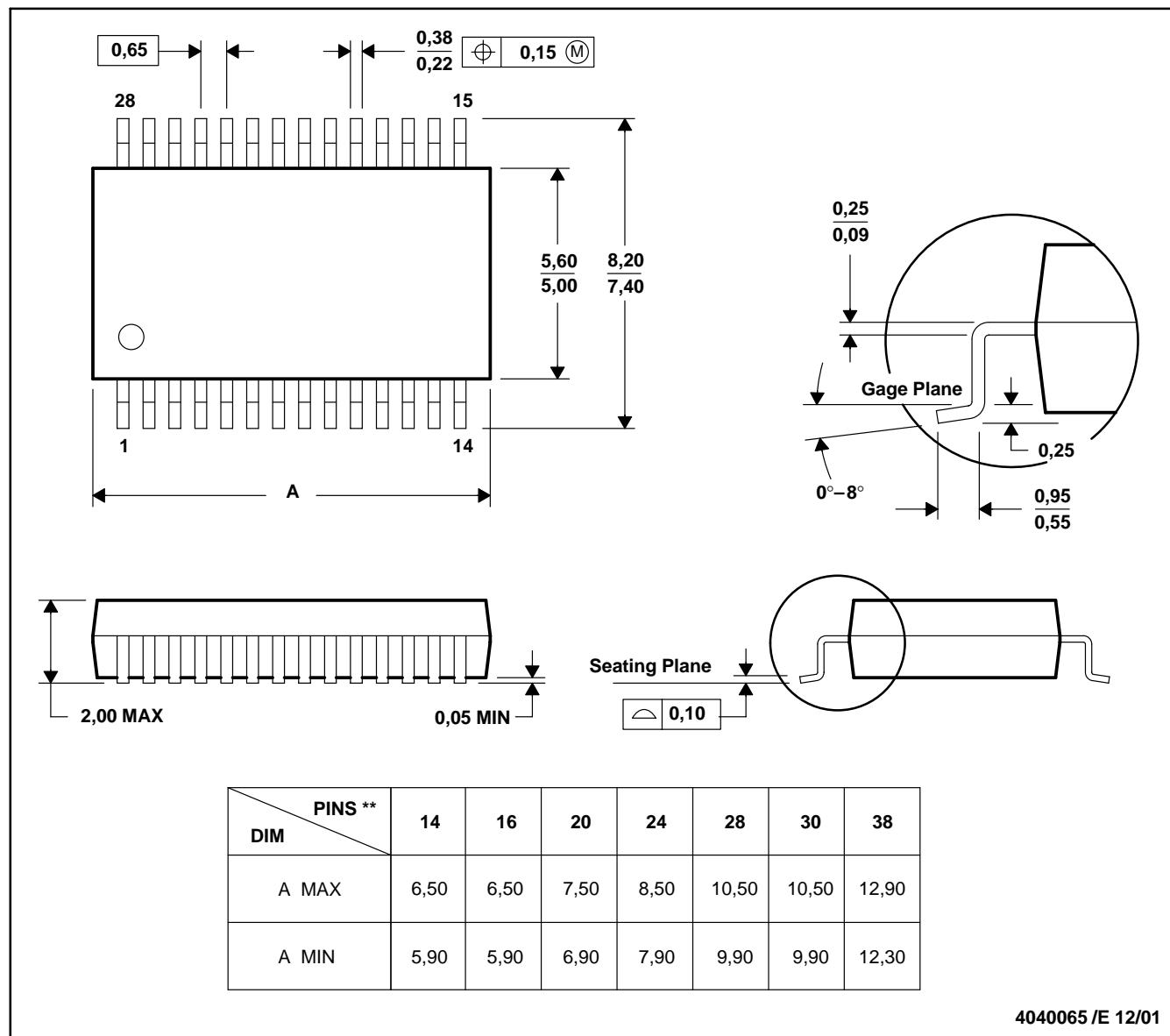
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

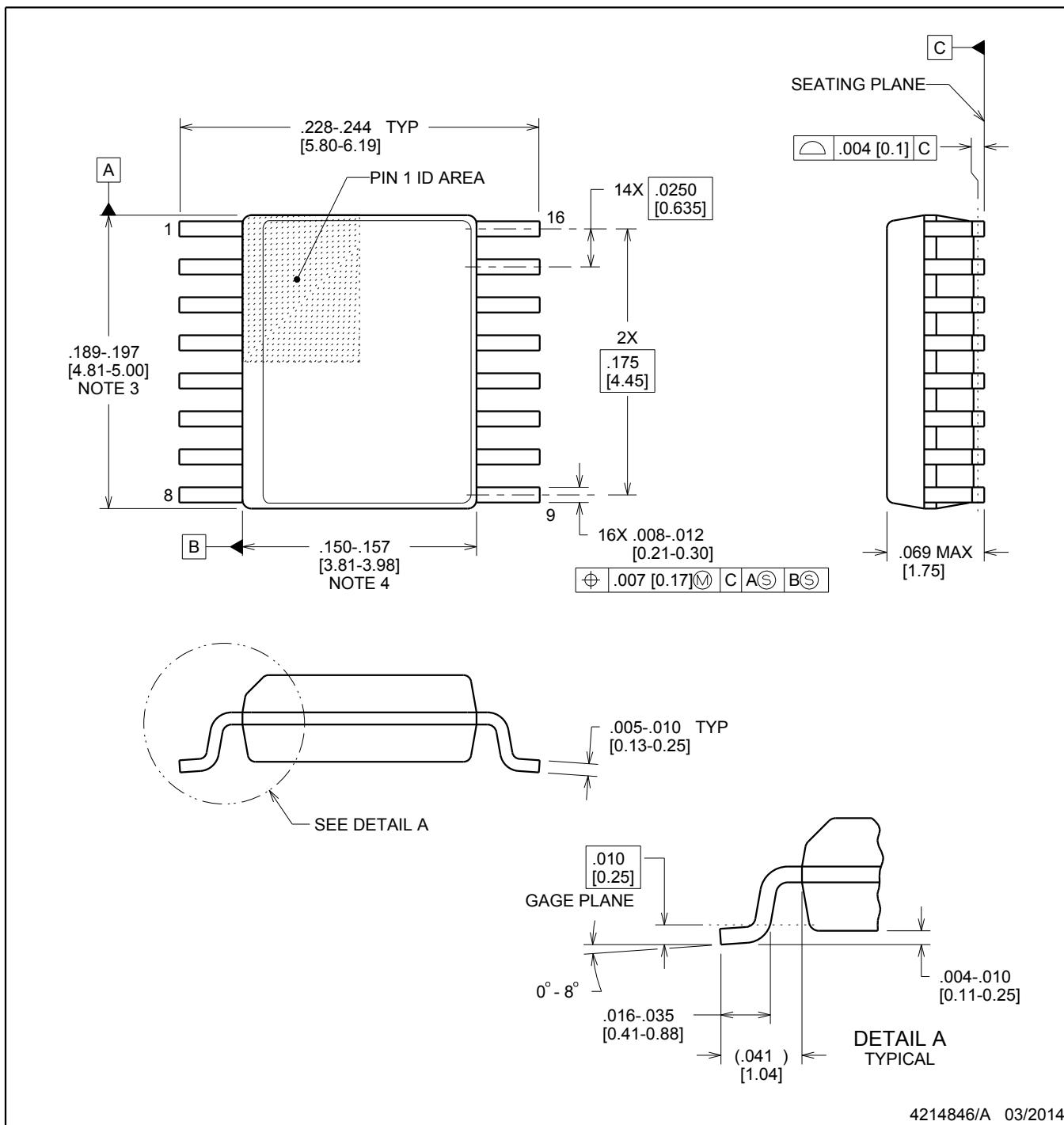


# PACKAGE OUTLINE

**DBQ0016A**

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

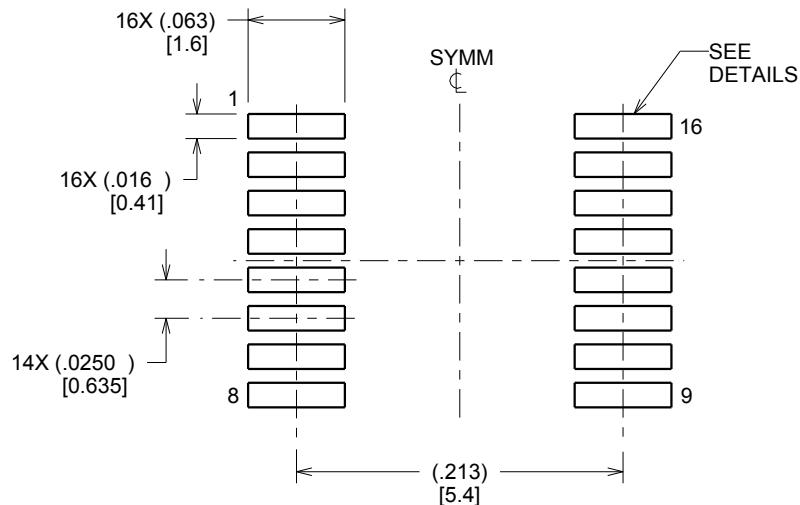
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

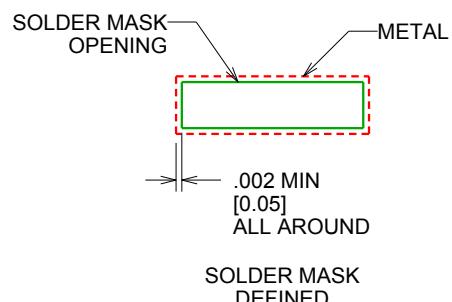
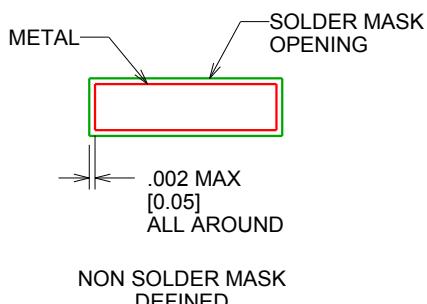
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

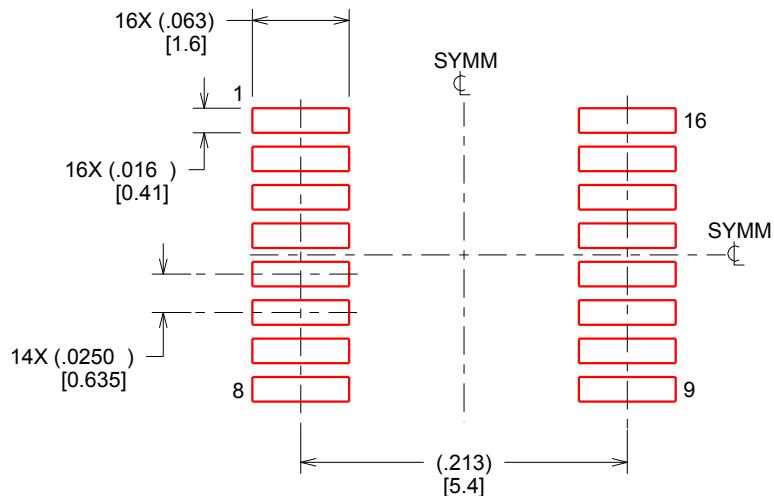
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

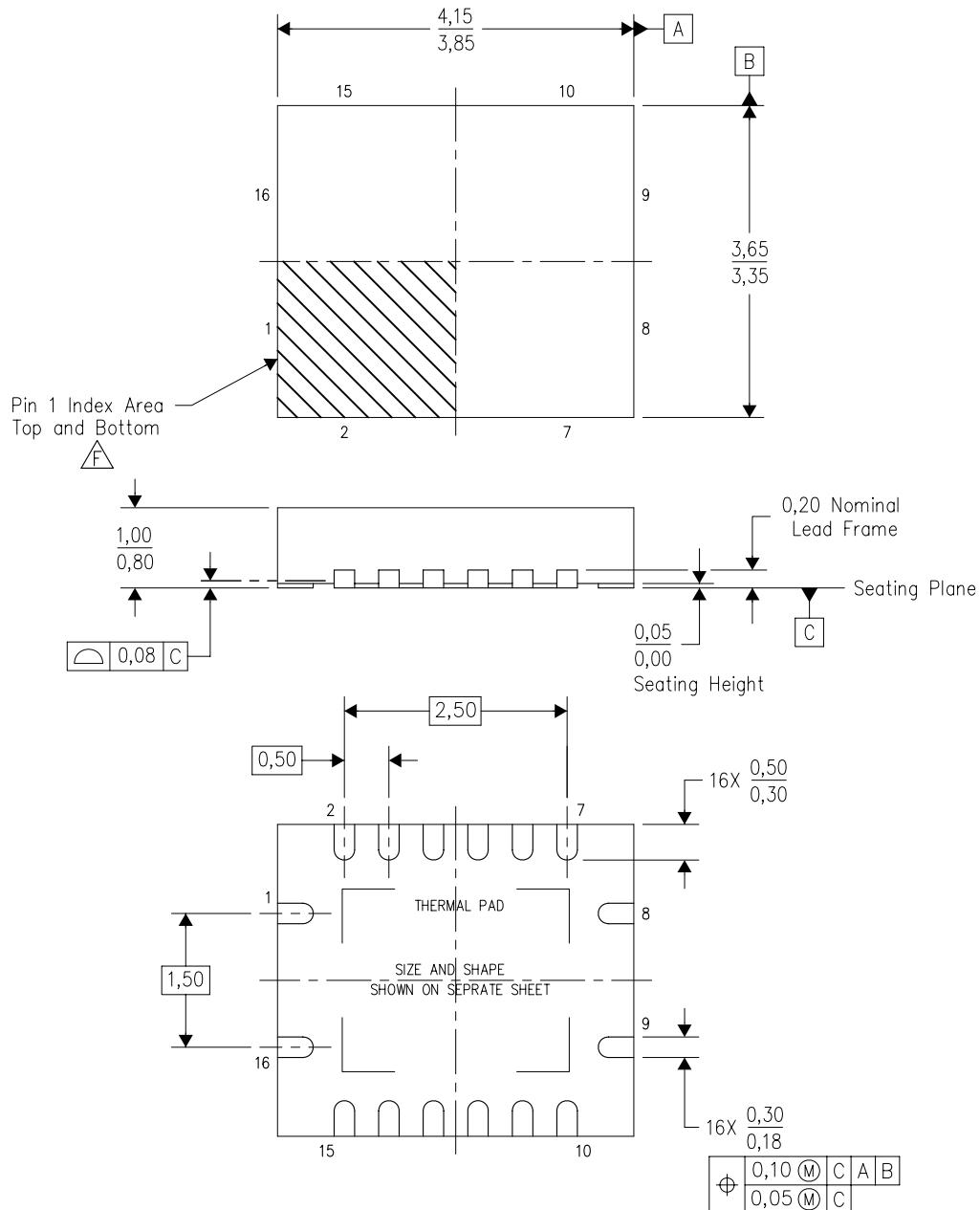
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



### Bottom View

4203539-3/l 06/2011

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

 F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.  
The Pin 1 identifiers are either a molded, marked, or metal feature.

- G. Package complies to JEDEC MO-241 variation BA.

## THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N16)

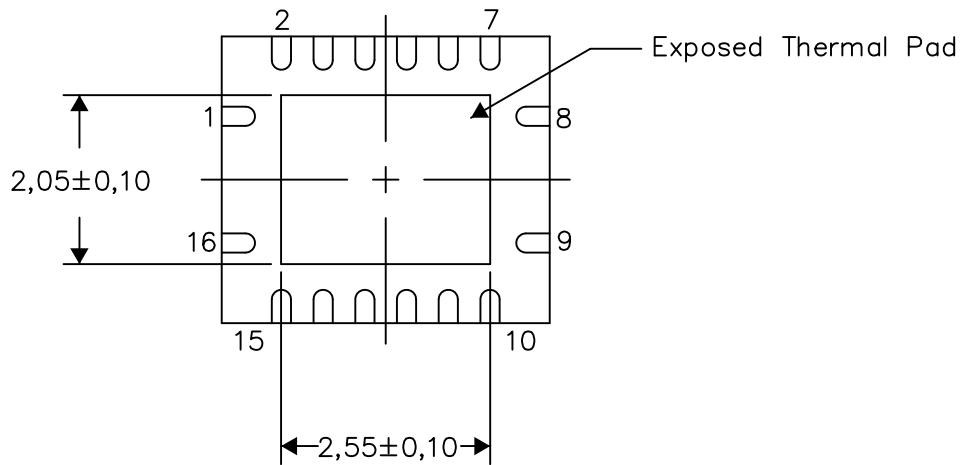
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

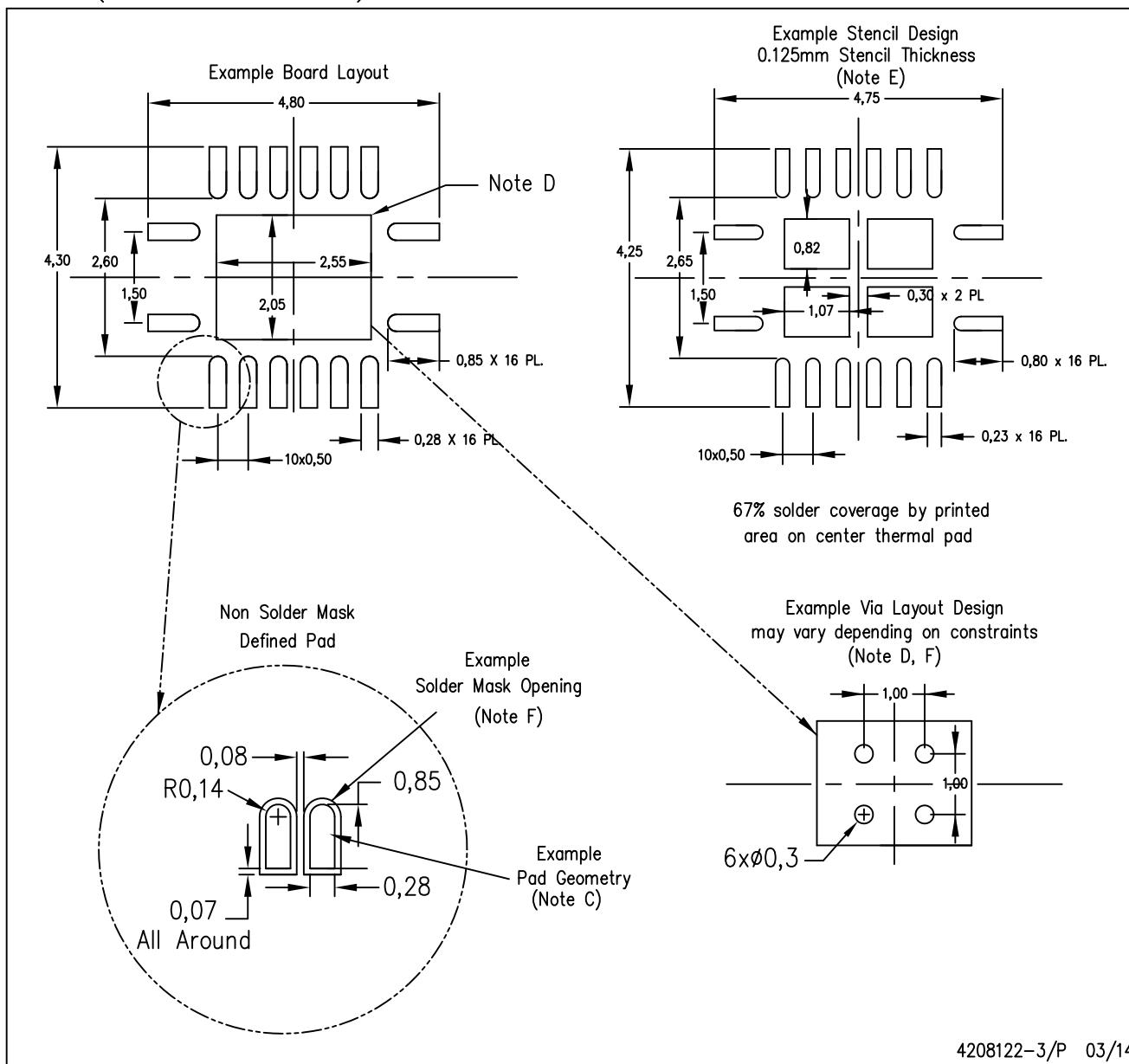
4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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