

# SDLS037 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SN54109, SN54LS109A,

SN74109, SN74LS109A

DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and tying J high. They also can perform as D-type flip-flops if J and K are tied together.

The SN54109 and SN54LS109A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74109 and SN74LS109A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}_0$

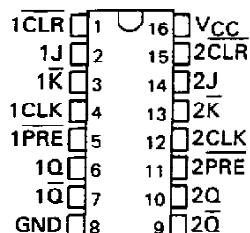
<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

SN54109, SN54LS109A . . . J OR W PACKAGE

SN74109 . . . N PACKAGE

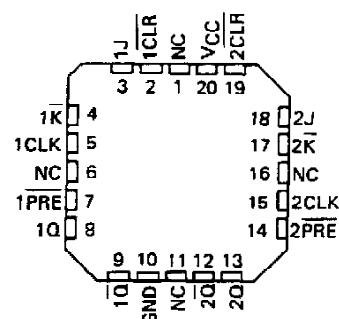
SN74LS109A . . . D OR N PACKAGE

(TOP VIEW)

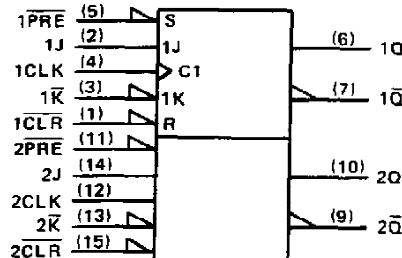


SN54LS109A . . . FK PACKAGE

(TOP VIEW)



## logic symbol<sup>‡</sup>

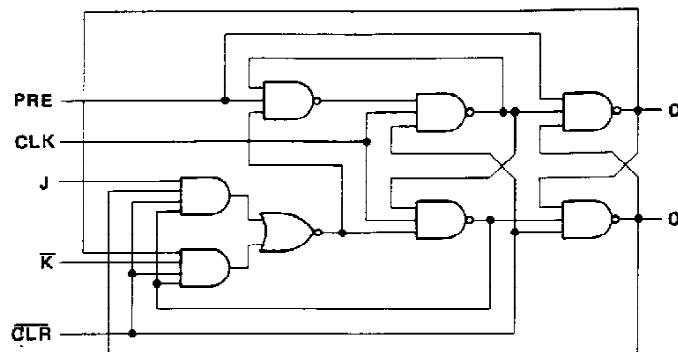


<sup>‡</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, N, and W packages.

**SN54109, SN74109**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

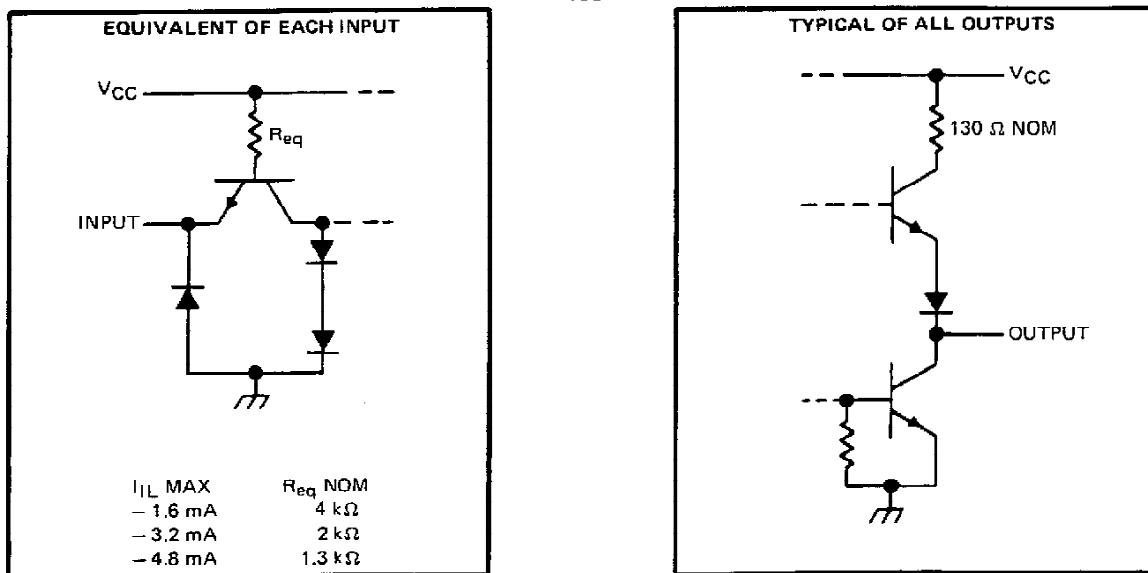
logic diagram (positive logic)

109



schematics of inputs and outputs

109

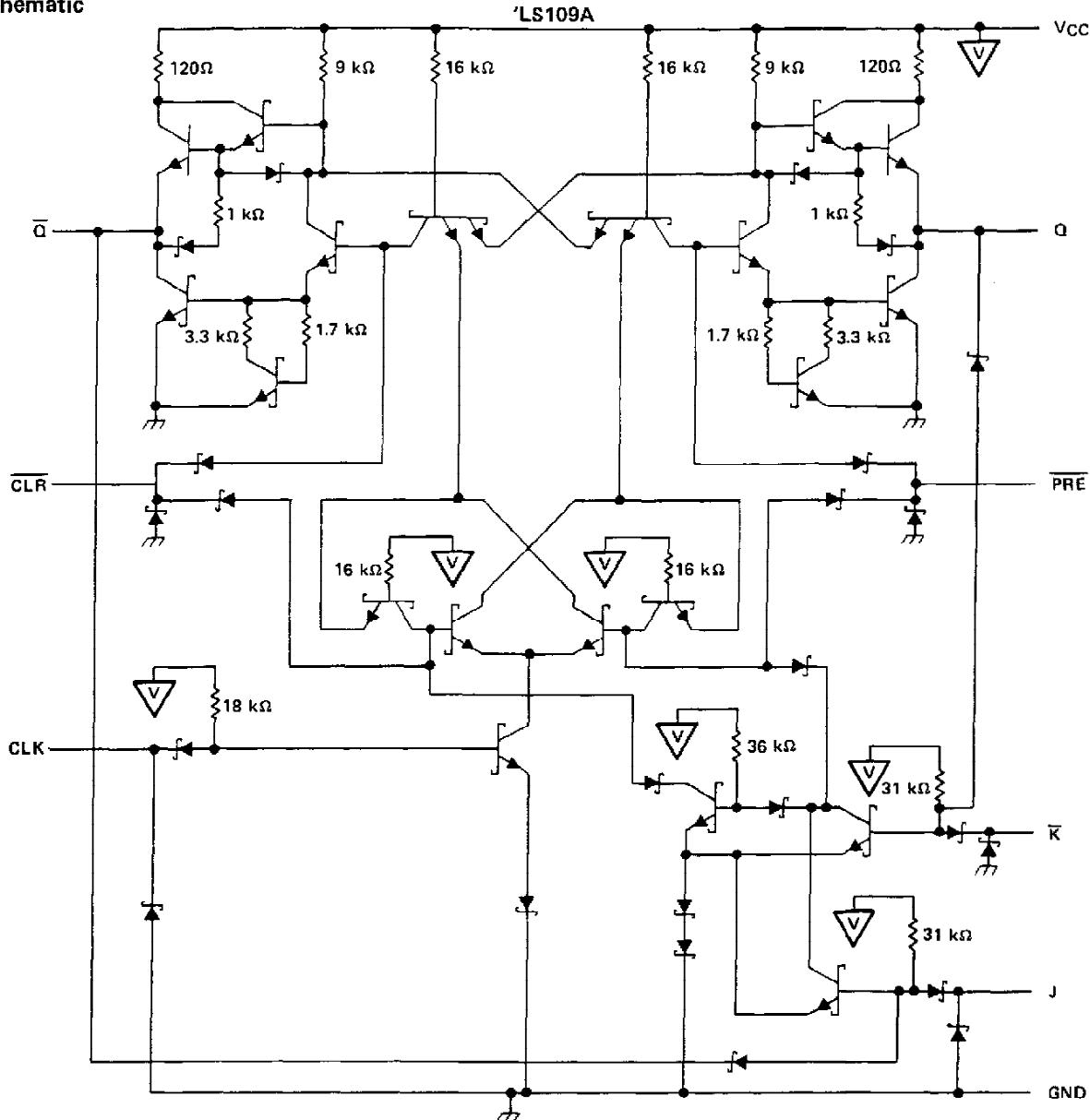


**TEXAS**  
**INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54109, SN54LS109A,  
SN74109, SN74LS109A  
DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . .	7 V
Input voltage: '109 . . . . .	5.5 V
'LS109A . . . . .	7 V
Operating free-air temperature range: SN54' . . . . .	-55°C to 125°C
SN74' . . . . .	0°C to 70°C
Storage temperature range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54109, SN74109**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

		SN54109			SN74109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-0.8			-0.8	mA
I <sub>OL</sub>	Low-level output current			16			16	mA
t <sub>w</sub>	Pulse duration	CLK high or low	20		20			ns
		PRE or CLR low	20		20			
t <sub>su</sub>	Input setup time before CLK↑		10		10			ns
t <sub>h</sub>	Input hold time-data after CLK↑		6		6			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54109			SN74109			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.8 mA	2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	J or K CLR PRE or CLK	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	40		40			μA
			160		160			
			80		80			
I <sub>IL</sub>	J or K CLR PRE CLK	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-1.6		-1.6			mA
			-4.8		-4.8			
			-3.2		-3.2			
			-3.2		-3.2			
I <sub>OS</sub> <sup>§</sup>	V <sub>CC</sub> = MAX	-30	-85	-30	-85			mA
I <sub>CC</sub> <sup>#</sup>	V <sub>CC</sub> = MAX, See Note 2		9	15		9	15	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time.

<sup>#</sup> Clear is tested with preset high and preset is tested with clear high.

<sup>#</sup> Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>				25	33		MHz
t <sub>PLH</sub>	PRE	Q		10	15		ns
t <sub>PHL</sub>		$\bar{Q}$		23	35		ns
t <sub>PLH</sub>	CLR	$\bar{Q}$	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF	10	15		ns
t <sub>PHL</sub>		Q		17	25		ns
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$		10	16		ns
t <sub>PHL</sub>				18	28		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**TEXAS**  
**INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS109A, SN74LS109A**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

			SN54LS109A			SN74LS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
I <sub>OH</sub>	High-level output current				-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current				4			8	mA
f <sub>clock</sub>	Clock frequency		0	25		0	25		MHz
t <sub>W</sub>	Pulse duration	CLK high	25			25			ns
		PRE or CLR low	25			25			
t <sub>su</sub>	Setup time before CLK t	High-level data	35			35			ns
		Low-level data	25			25			
t <sub>h</sub>	Hold time-data after CLK↑		5			5			ns
T <sub>A</sub>	Operating free-air temperature		-55	125	0	0	70		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>		SN54LS109A			SN74LS109A			UNIT
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA					-1.5		-1.6	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA		2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA			0.25	0.4	0.25	0.4		V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA					0.35	0.5		
I <sub>I</sub>	J, K or CLK CLR or PRE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1		0.1			mA
I <sub>II</sub>				0.2		0.2			
I <sub>IIH</sub>	J, R or CLK CLR or PRE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20		20			μA
I <sub>IIL</sub>				40		40			
I <sub>OS</sub> <sup>§</sup>	J, K or CLK CLR or PRE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4		-0.4			mA
				-0.8		-0.8			
I <sub>CC</sub> (Total)	V <sub>CC</sub> = MAX, See Note 4		-20	-100	-20	-100	-100		mA
I <sub>CC</sub> (Total)	V <sub>CC</sub> = MAX, See Note 2		4	8		4	8		mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively with the minimum and maximum limits reduced to one half of their stated values.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT
f <sub>max</sub>			R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF			25	33		MHz
t <sub>PLH</sub>	CLR, PRE or CLK	Q or $\bar{Q}$				13	25		ns
t <sub>PHL</sub>						25	40		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/30109BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BEA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/30109BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BEA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/30109BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BEA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS109AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS109AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ADRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ADRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS109ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS109ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS109A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS109AW	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS109AW	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS109A, SN74LS109A :**

- Catalog : [SN74LS109A](#)
- Military : [SN54LS109A](#)

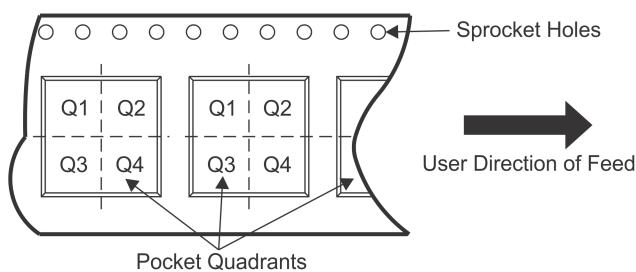
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

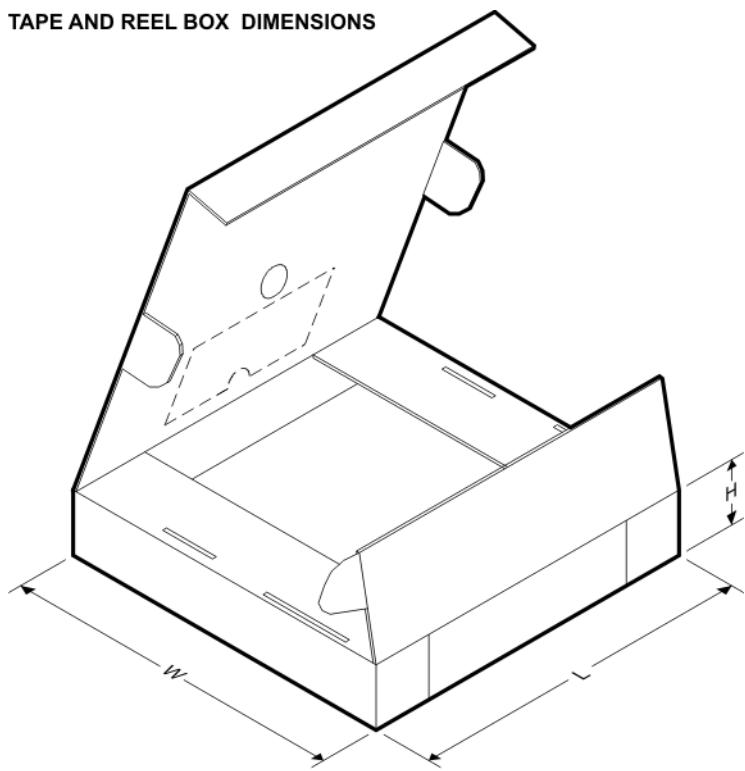
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


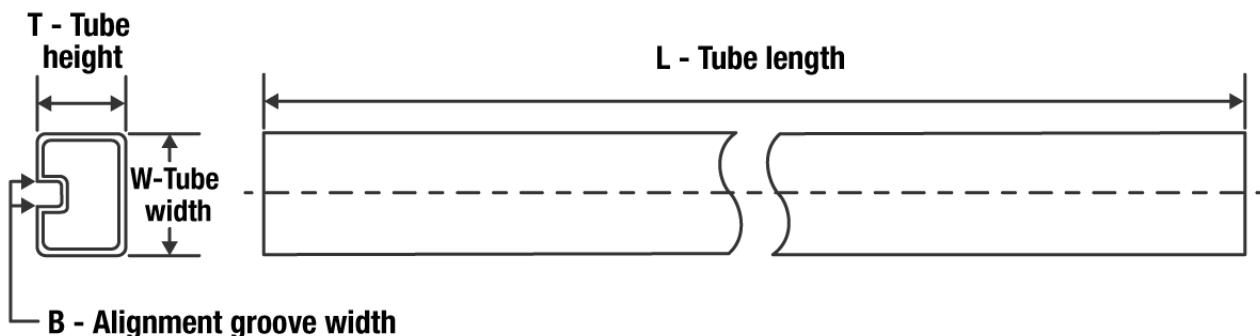
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS109ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS109ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS109ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS109ANSR	SO	NS	16	2000	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/30109BFA	W	CFP	16	1	506.98	26.16	6220	NA
M38510/30109BFA	W	CFP	16	1	506.98	26.16	6220	NA
SN74LS109AD	D	SOIC	16	40	507	8	3940	4.32
SN74LS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS109ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS109ANE4	N	PDIP	16	25	506	13.97	11230	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated