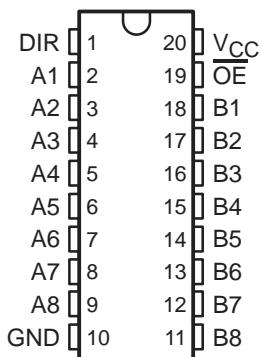
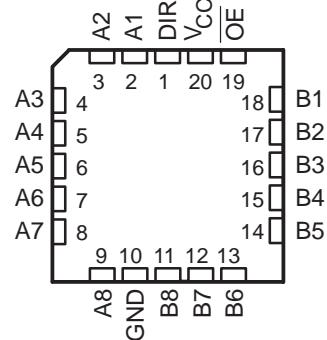


- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- True Logic

SN54HCT645 . . . J OR W PACKAGE  
SN74HCT645 . . . DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCT645 . . . FK PACKAGE  
(TOP VIEW)



### description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 20	SN74HCT645N	SN74HCT645N
	SOIC – DW	Tube of 25	SN74HCT645DW	HCT645
		Reel of 2000	SN74HCT645DWR	
	SOP – NS	Reel of 2000	SN74HCT645NSR	HCT645
	TSSOP – PW	Tube of 70	SN74HCT645PW	HT645
		Reel of 2000	SN74HCT645PWR	
		Reel of 250	SN74HCT645PWT	
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54HCT645J	SNJ54HCT645J
	CFP – W	Tube of 85	SNJ54HCT645W	SNJ54HCT645W
	LCCC – FK	Tube of 55	SNJ54HCT645FK	SNJ54HCT645FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

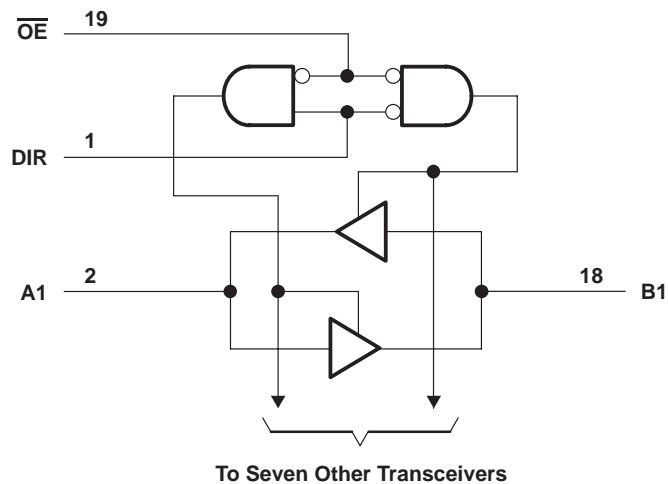
# SN54HCT645, SN74HCT645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS019D – MARCH 1984 – REVISED AUGUST 2003

## FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HCT645			SN74HCT645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		2	2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8	0.8		V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise/fall time			500	500			ns
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT645	SN74HCT645	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	4.4	4.499		4.4	4.4	V
			3.98	4.3		3.7	3.84	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	0.001	0.1		0.1	0.1	V
			0.17	0.26		0.4	0.33	
I <sub>I</sub>	DIR or $\overline{OE}$	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V	$\pm 0.1$	$\pm 100$	$\pm 1000$	$\pm 1000$	nA
I <sub>OZ</sub>	A or B	V <sub>O</sub> = V <sub>CC</sub> or 0	5.5 V	$\pm 0.01$	$\pm 0.5$	$\pm 10$	$\pm 5$	$\mu A$
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	5.5 V		8	160	80	$\mu A$
ΔI <sub>CC</sub> <sup>†</sup>		One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5 V	1.4	2.4	3	2.9	mA
C <sub>i</sub>	DIR or $\overline{OE}$		4.5 V to 5.5 V	3	10	10	10	pF

<sup>†</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT645	SN74HCT645	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	4.5 V	16	22		33	28	ns
			5.5 V	14	20		30	25	
t <sub>en</sub>	$\overline{OE}$	A or B	4.5 V	25	46		69	58	ns
			5.5 V	22	41		62	52	
t <sub>dis</sub>	$\overline{OE}$	A or B	4.5 V	26	40		60	50	ns
			5.5 V	23	36		54	45	
t <sub>t</sub>		A or B	4.5 V	9	12		18	15	ns
			5.5 V	8	11		16	14	

**SN54HCT645, SN74HCT645  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

SCLS019D - MARCH 1984 - REVISED AUGUST 2003

**switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT645	SN74HCT645	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	4.5 V	20	30	45	38		ns
			5.5 V	18	27	41	34		
t <sub>en</sub>	OE	A or B	4.5 V	36	59	89	74		ns
			5.5 V	30	53	80	67		
t <sub>t</sub>		A or B	4.5 V	17	42	63	53		ns
			5.5 V	14	38	57	48		

**operating characteristics, T<sub>A</sub> = 25°C**

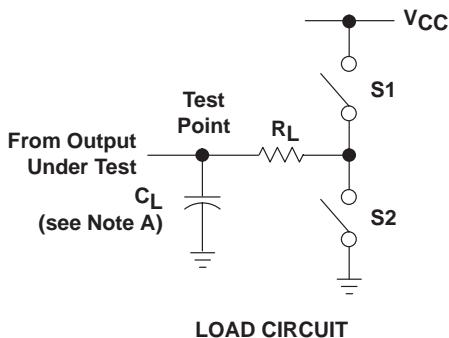
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per transceiver	No load	40	pF

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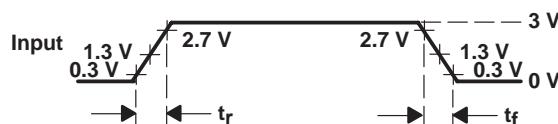


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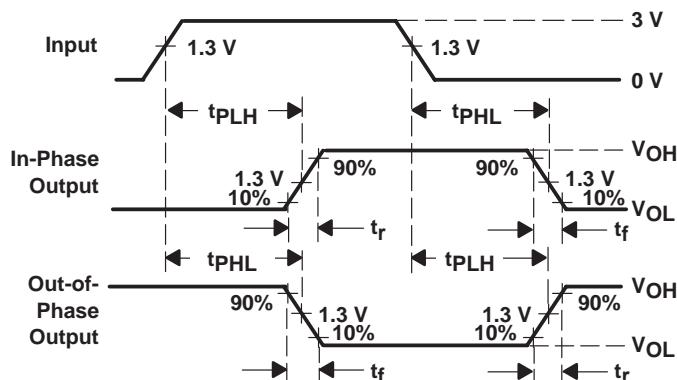
PARAMETER MEASUREMENT INFORMATION



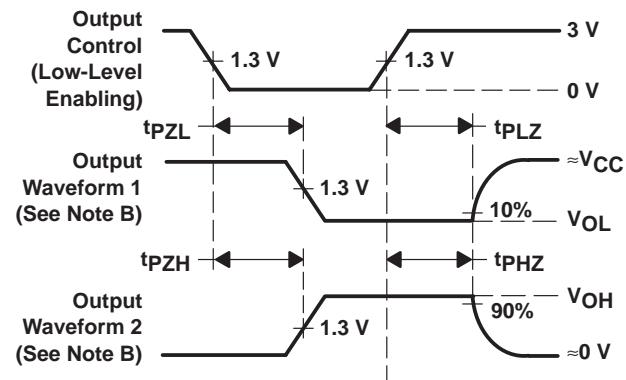
PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM  
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_r$  = 6 ns,  $t_f$  = 6 ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT645DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT645	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT645DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT645	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT645N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT645N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT645PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT645	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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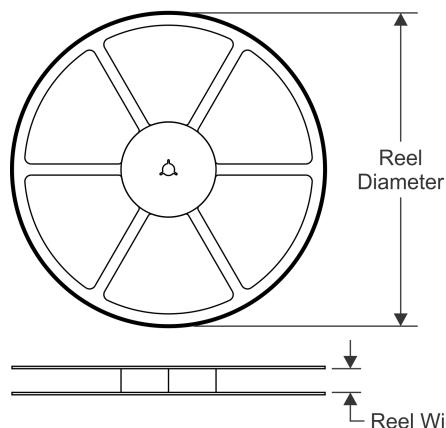
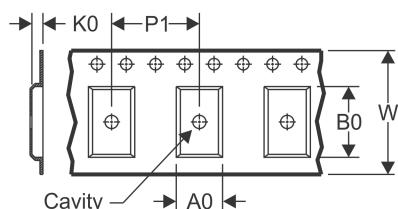
## PACKAGE OPTION ADDENDUM

10-Dec-2020

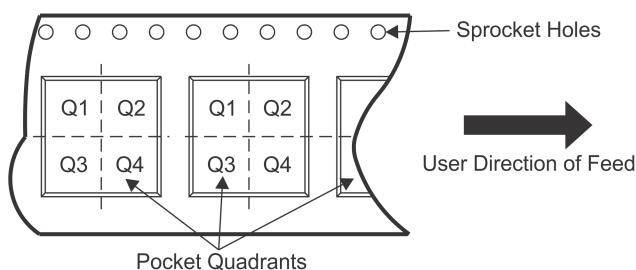
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


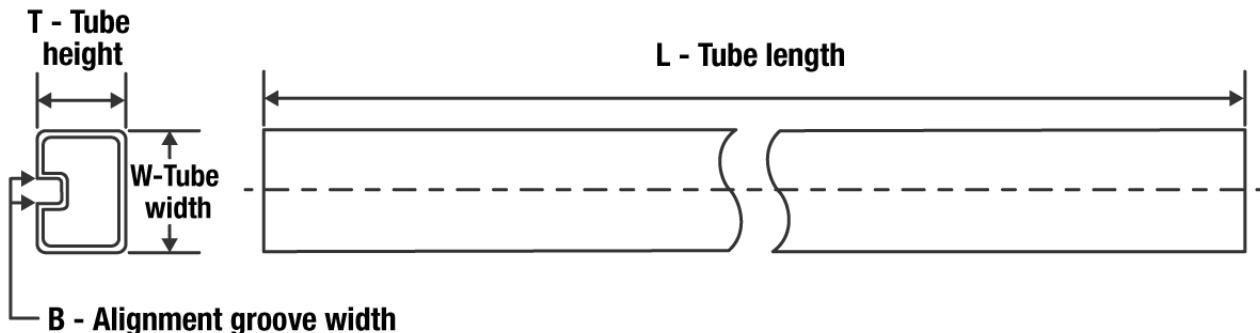
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT645DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT645DWR	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT645DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT645N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT645PW	PW	TSSOP	20	70	530	10.2	3600	3.5

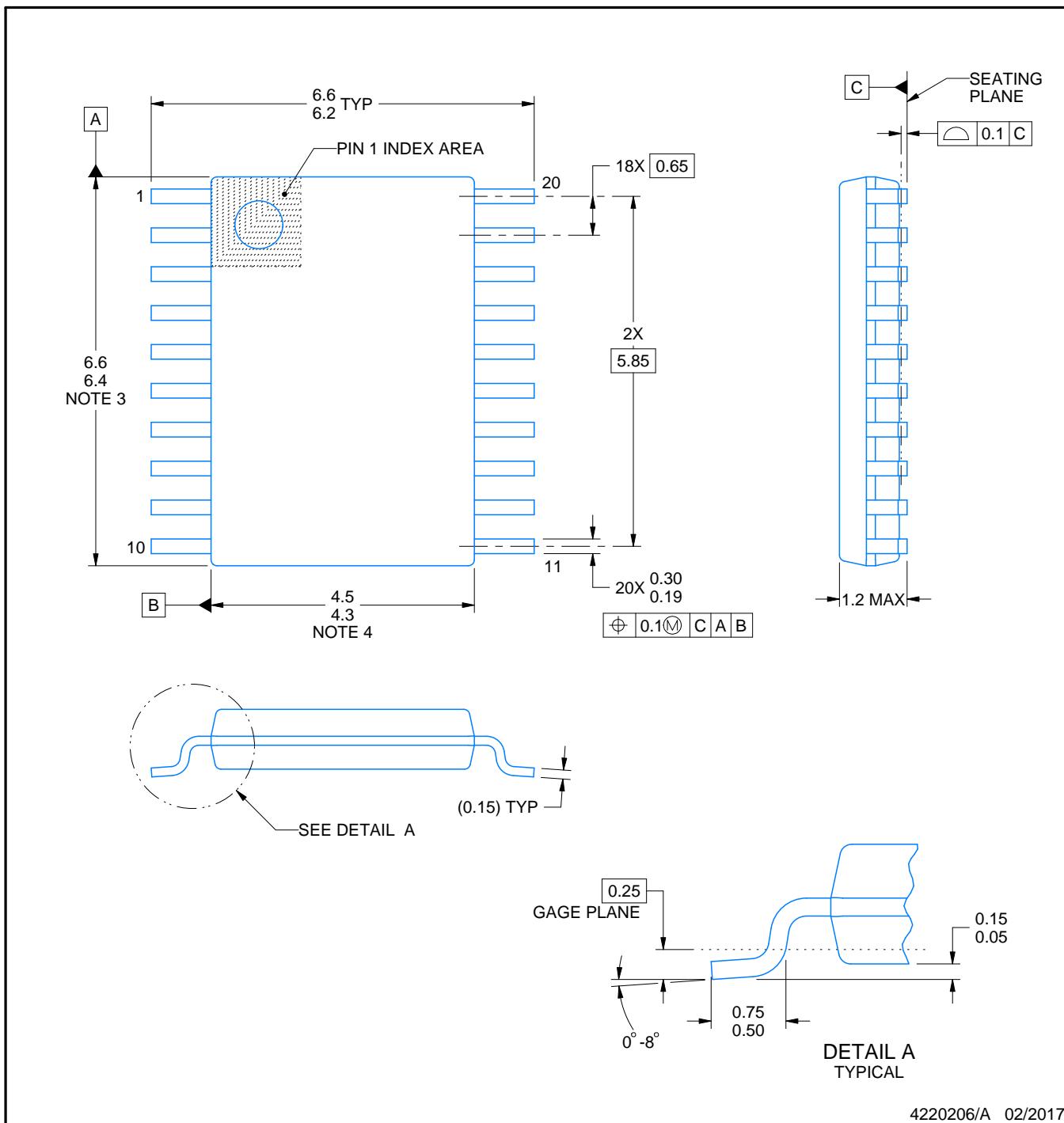
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

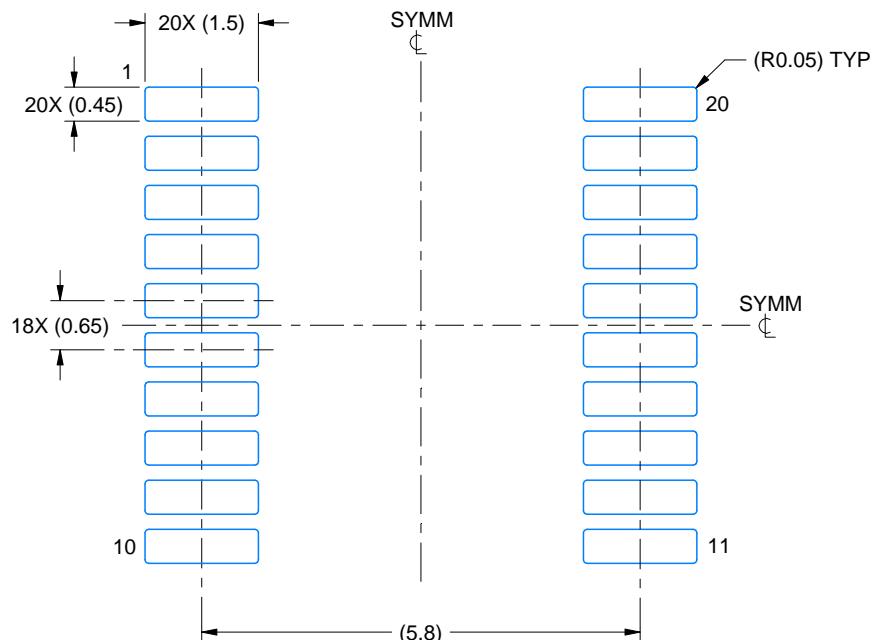
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

## EXAMPLE BOARD LAYOUT

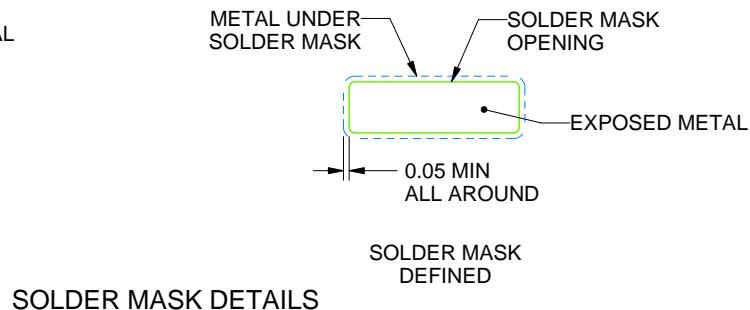
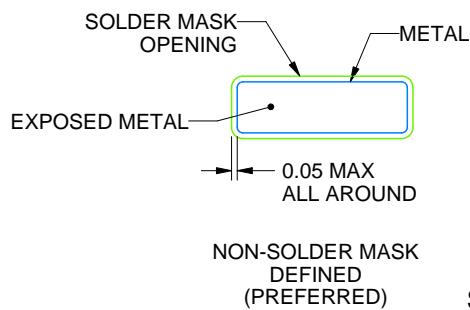
**PW0020A**

## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

#### NOTES: (continued)

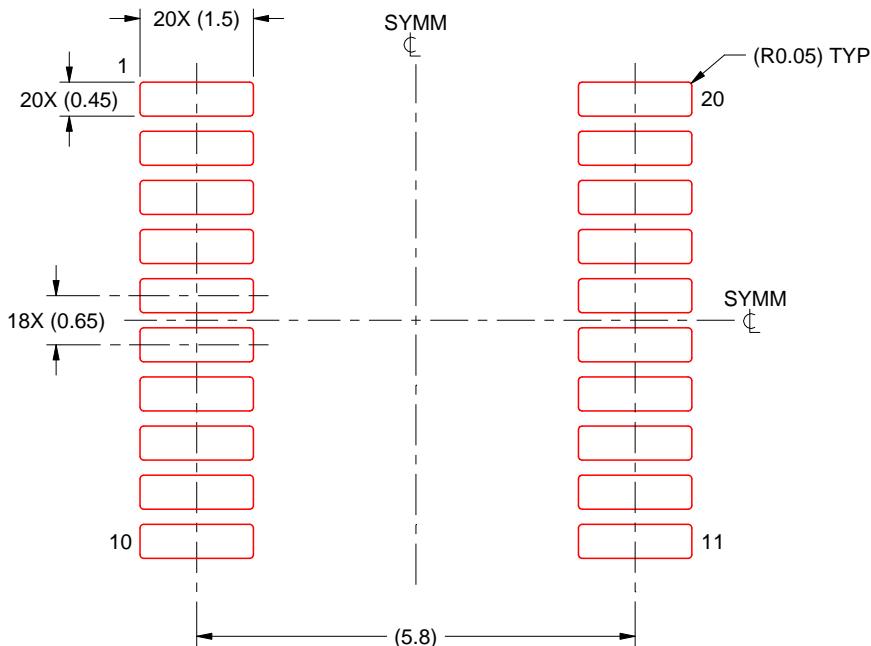
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

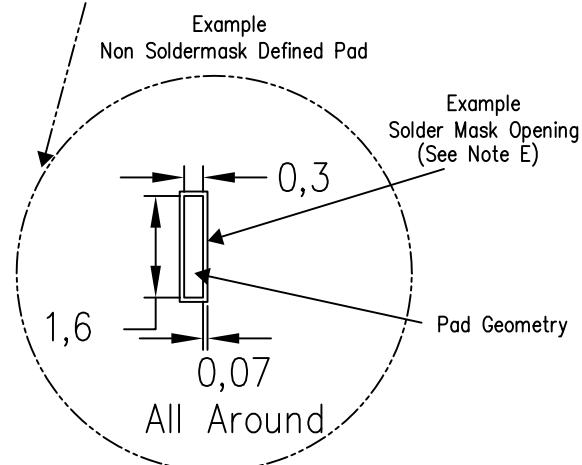
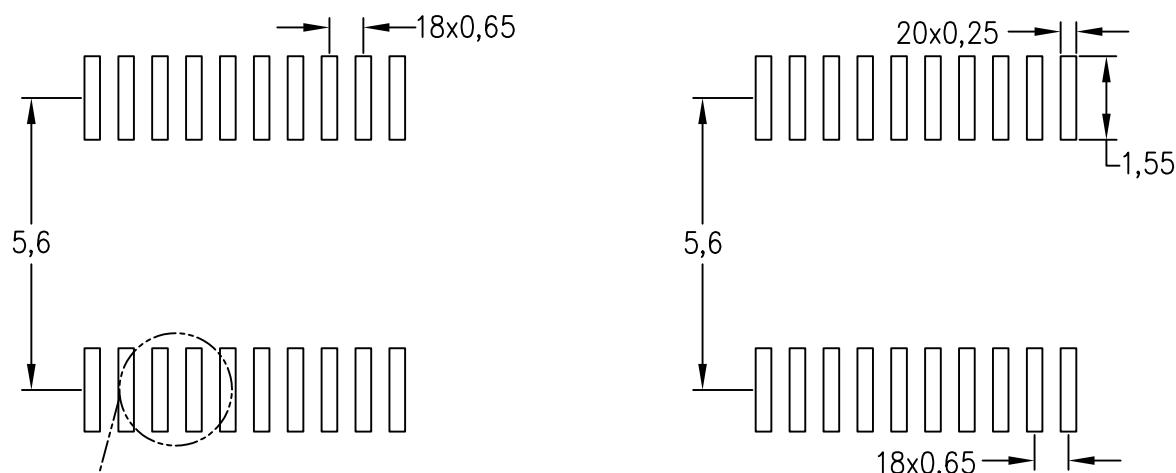
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).

4211284-5/G 08/15

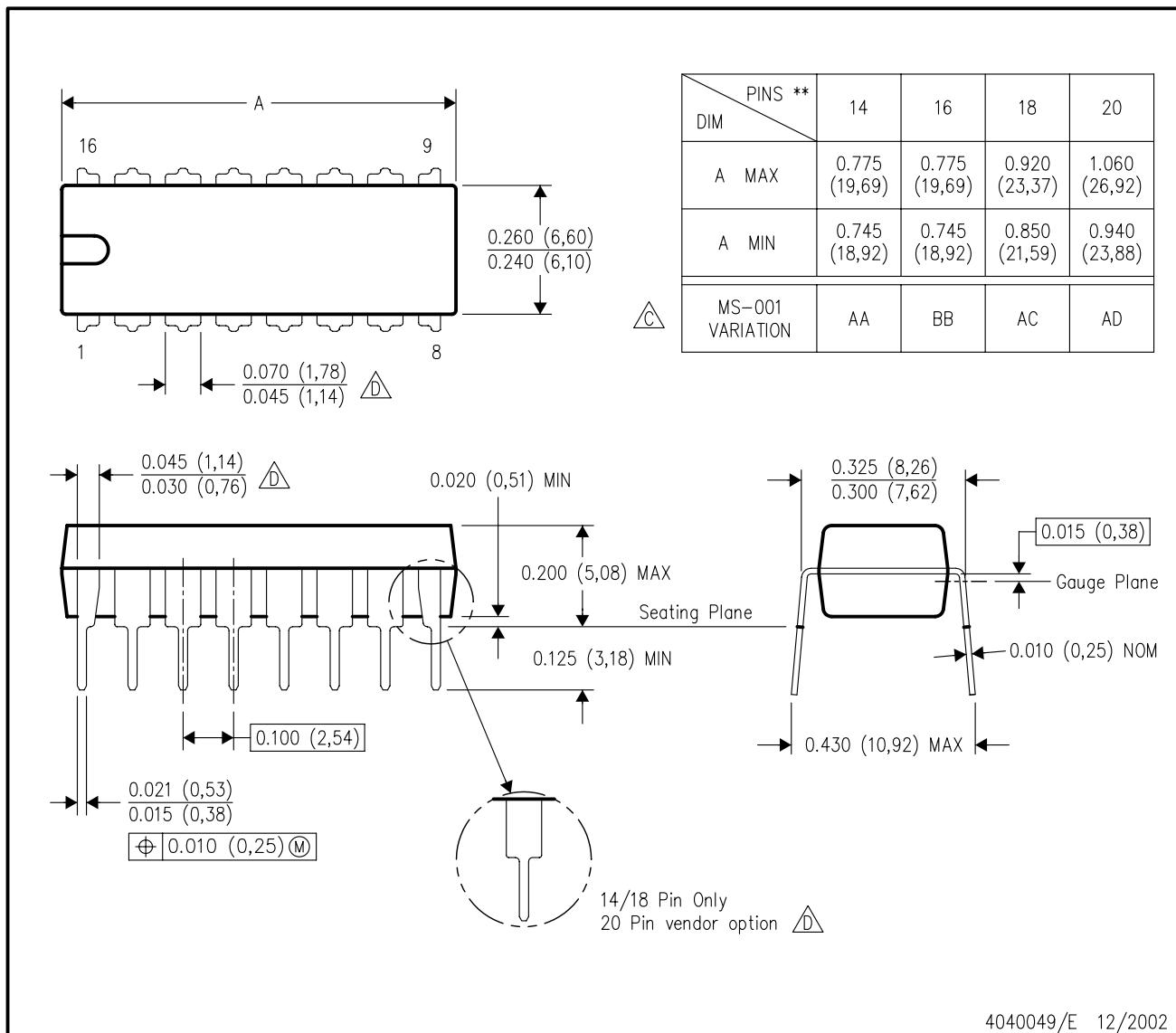
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

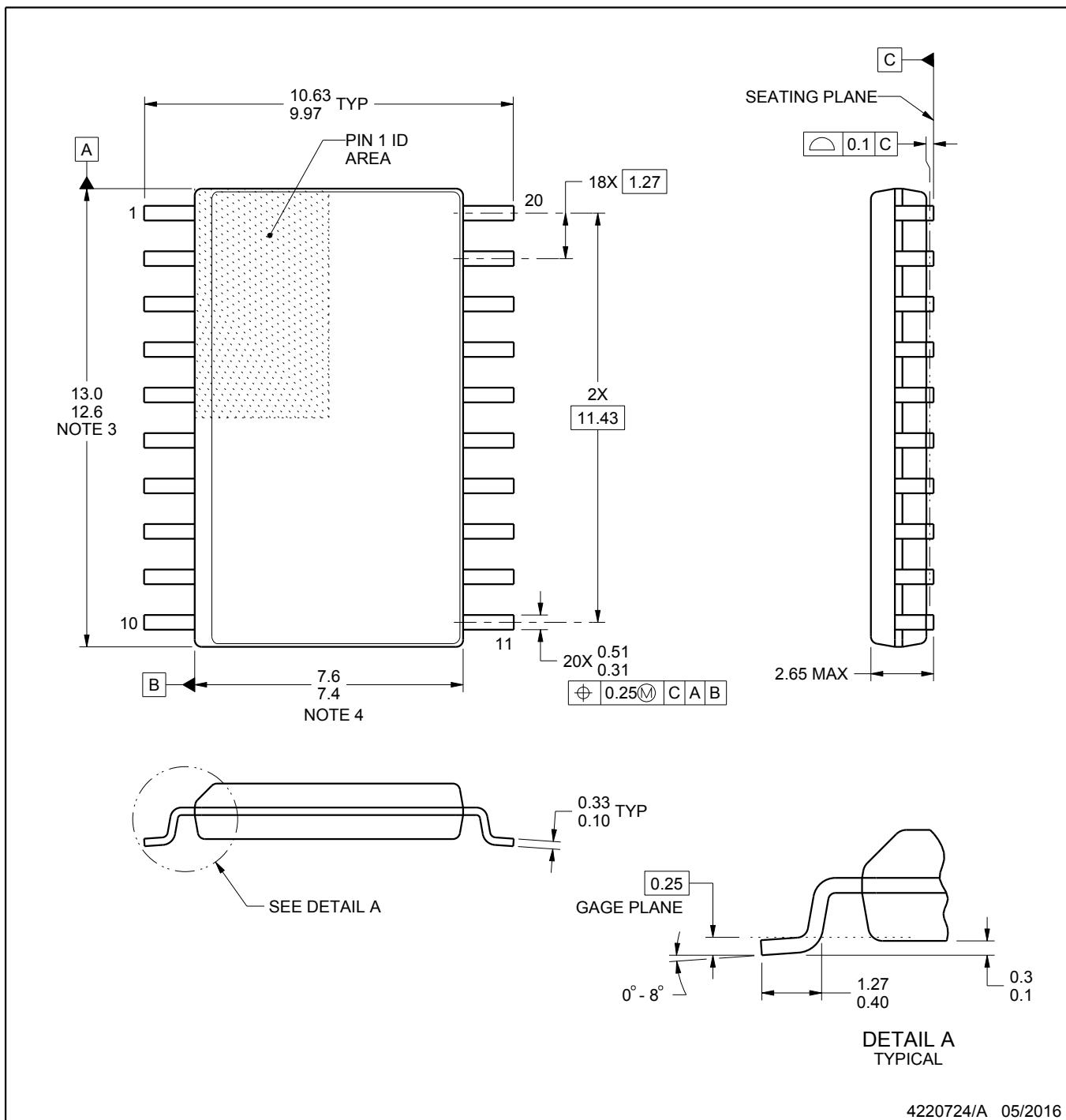
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



## NOTES:

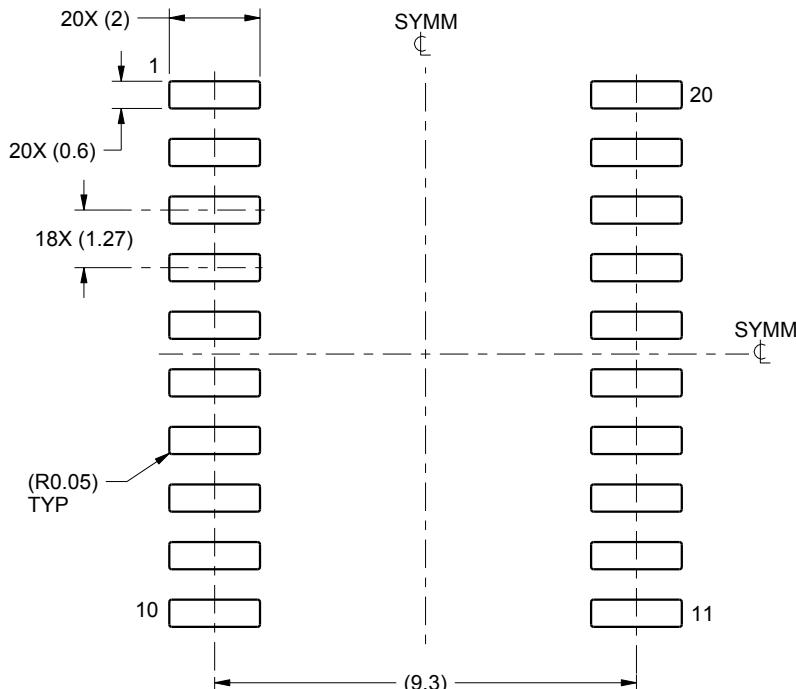
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

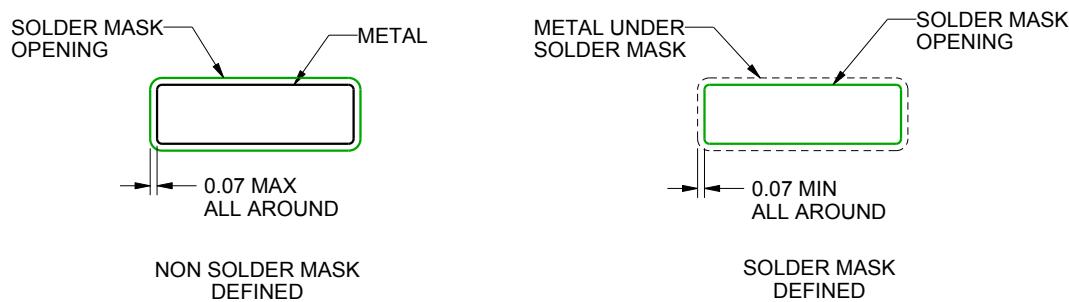
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

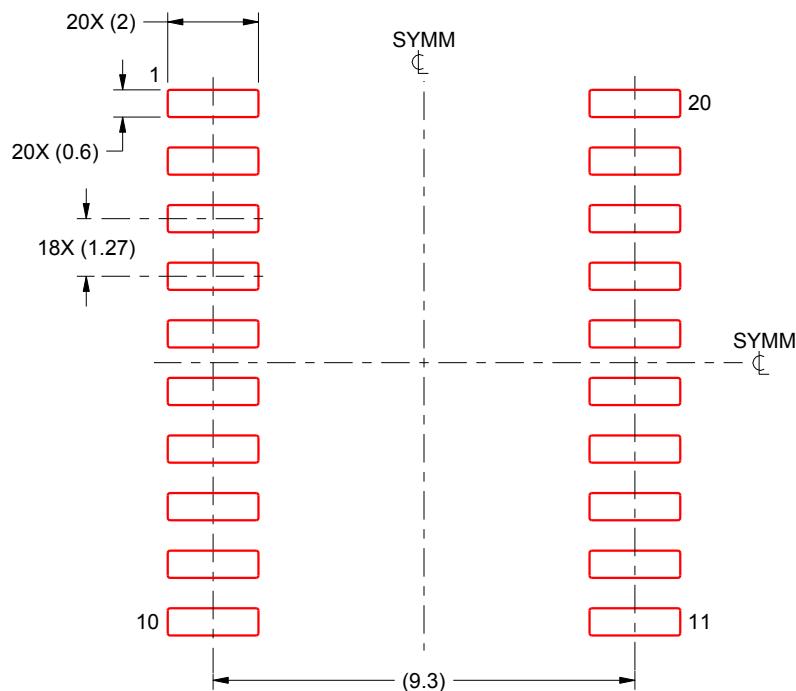
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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