SN74LV4052A Dual 4-Channel Analog Multiplexers and Demultiplexers

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Fast Switching
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22:
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Telecomunications
- Infotainment
- Signal Gating and Isolation
- Home Appliances
- Programmable Logic Circuits
- Modulation and Demodulation

3 Description

The SN74LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2-V to 5.5-V V_{CC} operation.

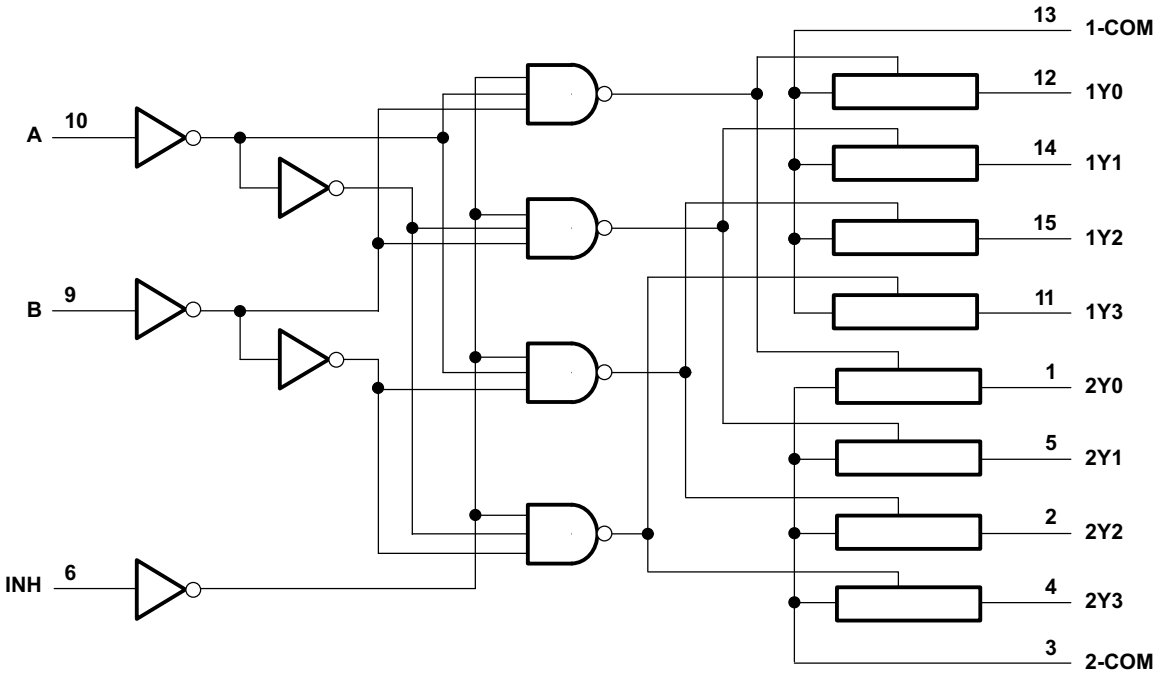
The SN74LV4052A device handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4052AD	SOIC (16)	9.90 mm × 3.91 mm
SN74LV4052ADB	SSOP (16)	6.20 mm × 5.30 mm
SN74LV4052ADGV	TVSOP (16)	3.60 mm × 4.40 mm
SN74LV4052ANS	SO (16)	10.30 mm × 5.30 mm
SN74LV4052AN	PDIP (16)	19.30 mm × 6.35 mm
SN74LV4052APW	TSSOP (16)	5.00 mm × 4.40 mm
SN74LV4052ARGY	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V ... 6
6.7 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V ... 6
6.8 Switching Characteristics: V_{CC} = 5 V ± 0.5 V ... 6
6.9 Switching Characteristics: Analog ... 7
6.10 Operating Characteristics ... 7
6.11 Typical Characteristics ... 7
7 Parameter Measurement Information ... 8
8 Detailed Description ... 12
8.1 Overview ... 12
8.2 Functional Block Diagram ... 12
8.3 Feature Description ... 12
8.4 Device Functional Modes ... 12
9 Application and Implementation ... 13
9.1 Application Information ... 13
9.2 Typical Application ... 13
10 Power Supply Recommendations ... 15
11 Layout ... 15
11.1 Layout Guidelines ... 15
11.2 Layout Example ... 15
12 Device and Documentation Support ... 16
12.1 Documentation Support ... 16
12.2 Receiving Notification of Documentation Updates 16
12.3 Community Resource ... 16
12.4 Trademarks ... 16
12.5 Electrostatic Discharge Caution ... 16
12.6 Glossary ... 16
13 Mechanical, Packaging, and Orderable Information ... 16

4 Revision History

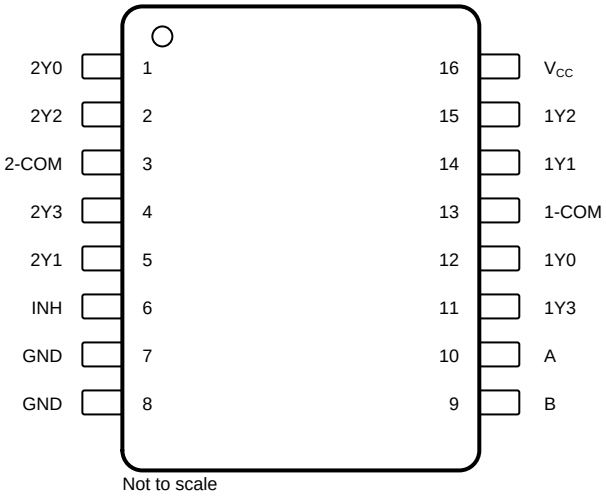
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2012) to Revision K	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet	1
• Deleted SN54LV4052A from data sheet	1
• Changed Package thermal impedance, $R_{\theta JA}$, values in the *Thermal Information* table From: 73 To: 90.9 (D), From: 82 To: 102.8 (DB), From: 120 To: 125.7 (DGV), From: 67 To: 54.8 (N), From: 64 To: 89.7 (NS), From: 108 To: 113.2 (PW), and From: 39 To: 48.9 (RGY)	5

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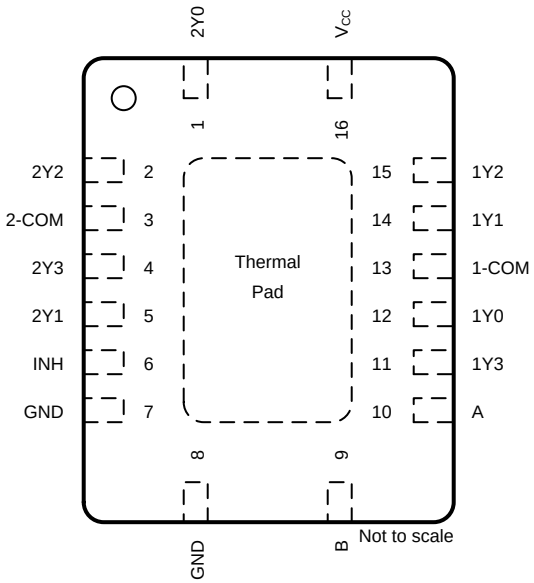
5 Pin Configuration and Functions

D, DB, DGV, N, NS, or PW Package
16-Pin SOIC, SSOP, TVSOP, SO, PDIP, or TSSOP
Top View



Not to scale

RGY Package
16-Pin VQFN With Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	2Y0	I/O	Port 2 channel 0
2	2Y2	I/O	Port 2 channel 2
3	2-COM	I/O	Port 2 common channel
4	2Y3	I/O	Port 2 channel 3
5	2Y1	I/O	Port 2 channel 1
6	INH	I	Inhibit input
7	GND	—	Device ground
8	GND	—	Device ground
9	B	I	Logic input selector B
10	A	I	Logic input selector A
11	1Y3	I/O	Port 1 channel 3
12	1Y0	I/O	Port 1 channel 0
13	1-COM	I/O	Port 1 common channel
14	1Y1	I/O	Port 1 channel 1
15	1Y2	I/O	Port 1 channel 2
16	V_{CC}	—	Device power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	7	V
Input voltage, V_I(2)		–0.5	7	V
Switch I/O voltage, V_{IO}(2)(3)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–20	mA
I/O diode current, I_{IOK}	V_{IO} < 0 and V_{IO} > V_{CC}		50	mA
Switch through current, I_T	V_{IO} = 0 to V_{CC}		±25	mA
Continuous current through V_{CC} or GND			±50	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Tested on D package

6.3 Recommended Operating Conditions

see(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2(2)	5.5	V
V_{IH}	High-level input voltage (control inputs)	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage (control inputs)	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
V_{IO}	Input or output voltage		0	V_{CC}	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. TI recommends that only digital signals be transmitted at these low supply voltages.

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6.4 Thermal Information

THERMAL METRIC[1]		SN74LV4052A							UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	102.8	125.7	54.8	89.7	113.2	48.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	53.3	50.9	42.1	48.1	48.2	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	53.4	57.5	34.8	50.1	58.3	25	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	16.5	5.6	26.9	16.7	6.3	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.8	52.9	57	34.7	49.8	57.8	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	11.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
r_{on}	On-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 2)	V_{CC} = 2.3 V	T_A = 25°C		43	180	Ω
				T_A = –40 to 85°C			225	
			V_{CC} = 3 V	T_A = 25°C		34	150	
				T_A = –40 to 85°C			190	
			V_{CC} = 4.5 V	T_A = 25°C		25	75	
				T_A = –40 to 85°C			100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	V_{CC} = 2.3 V	T_A = 25°C		133	500	Ω
				T_A = –40 to 85°C			600	
			V_{CC} = 3 V	T_A = 25°C		63	180	
				T_A = –40 to 85°C			225	
			V_{CC} = 4.5 V	T_A = 25°C		35	100	
				T_A = –40 to 85°C			125	
Δr_{on}	Difference in on-state resistance between switches	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	V_{CC} = 2.3 V	T_A = 25°C		1.5	30	Ω
				T_A = –40 to 85°C			40	
			V_{CC} = 3 V	T_A = 25°C		1.1	20	
				T_A = –40 to 85°C			30	
			V_{CC} = 4.5 V	T_A = 25°C		0.7	15	
				T_A = –40 to 85°C			20	
I_I	Control input current	V_I = 5.5 V or GND, and V_{CC} = 0 to 5.5 V		T_A = 25°C			±0.1	µA
				T_A = –40 to 85°C			±1	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH} , and V_{CC} = 5.5 V (see Figure 3)		T_A = 25°C			±0.1	µA
				T_A = –40 to 85°C			±1	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL}, and V_{CC} = 5.5 V (see Figure 4)		T_A = 25°C			±0.1	µA
				T_A = –40 to 85°C			±1	
I_{CC}	Supply current	V_I = V_{CC} or GND, V_{CC} = 5.5 V, and T_A = –40 to 85°C					20	µA
C_{IC}	Control input capacitance	f = 10 MHz, V_{CC} = 3.3 V, and T_A = 25°C				2.1		pF
C_{IS}	Common terminal capacitance	V_{CC} = 3.3 V and T_A = 25°C				13.1		pF
C_{OS}	Switch terminal capacitance	V_{CC} = 3.3 V and T_A = 25°C				5.6		pF
C_F	Feedthrough capacitance	V_{CC} = 3.3 V and T_A = 25°C				0.5		pF

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6.6 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range and V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		1.9	10	ns
					T_A = –40 to 85°C			16	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF (seeFigure 6)	T_A = 25°C		8	18	ns
					T_A = –40 to 85°C			23	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF (see Figure 6)	T_A = 25°C		8.3	18	ns
					T_A = –40 to 85°C			23	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		3.8	12	ns
					T_A = –40 to 85°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		9.4	28	ns
					T_A = –40 to 85°C			35	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		12.4	28	ns
					T_A = –40 to 85°C			35	

6.7 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range and V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		1.2	6	ns
					T_A = –40 to 85°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF (seeFigure 6)	T_A = 25°C		5.7	12	ns
					T_A = –40 to 85°C			15	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF (see Figure 6)	T_A = 25°C		6.6	12	ns
					T_A = –40 to 85°C			15	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		2.5	9	ns
					T_A = –40 to 85°C			12	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		6.7	20	ns
					T_A = –40 to 85°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		9.5	20	ns
					T_A = –40 to 85°C			25	

6.8 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range and V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF (see Figure 5)	T_A = 25°C		0.7	4	ns
					T_A = –40 to 85°C			7	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF (seeFigure 6)	T_A = 25°C		4	8	ns
					T_A = –40 to 85°C			10	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF (see Figure 6)	T_A = 25°C		5	8	ns
					T_A = –40 to 85°C			10	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 5)	T_A = 25°C		1.5	6	ns
					T_A = –40 to 85°C			8	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		4.7	14	ns
					T_A = –40 to 85°C			18	

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Switching Characteristics: V_{CC} = 5 V ± 0.5 V (continued)

over recommended operating free-air temperature range and V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 6)	T_A = 25°C		6.9	14	ns
					T_A = –40 to 85°C			18	

6.9 Switching Characteristics: Analog

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)(1)	V_{CC} = 2.3 V		30		MHz
				V_{CC} = 3 V		35		
				V_{CC} = 4.5 V		50		
Crosstalk (between any switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 8)(2)	V_{CC} = 2.3 V		–45		dB
				V_{CC} = 3 V		–45		
				V_{CC} = 4.5 V		–45		
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	V_{CC} = 2.3 V		20		mV
				V_{CC} = 3 V		35		
				V_{CC} = 4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 10)(2)	V_{CC} = 2.3 V		–45		dB
				V_{CC} = 3 V		–45		
				V_{CC} = 4.5 V		–45		
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 11)	V_I = 2 V_{p-p} and V_{CC} = 2.3 V		0.1%		
				V_I = 2.5 V_{p-p} and V_{CC} = 3 V		0.1%		
				V_I = 4 V_{p-p} and V_{CC} = 4.5 V		0.1%		

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase fin frequency until dB meter reads –3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF and f = 10 MHz	11.8	pF

6.11 Typical Characteristics

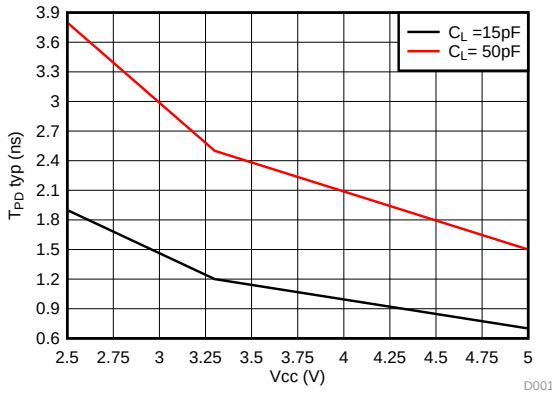


Figure 1. Typical Propagation Delay vs V_{cc}

7 Parameter Measurement Information

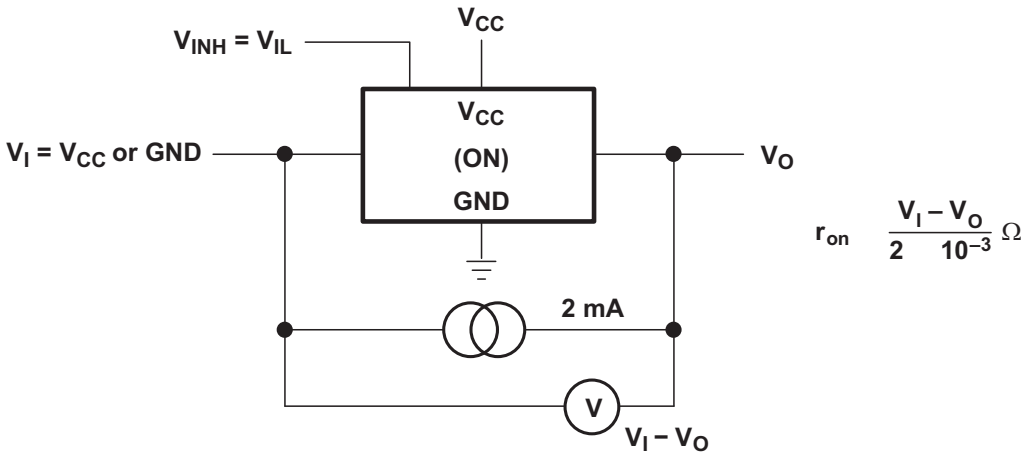
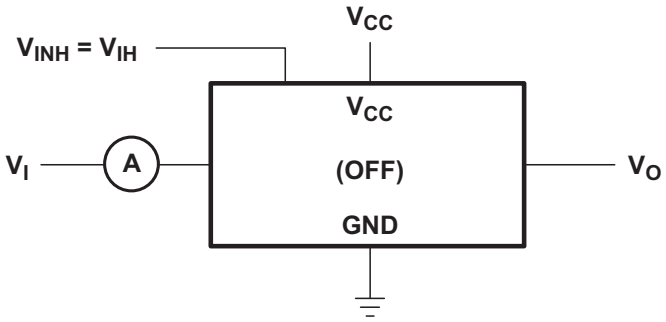
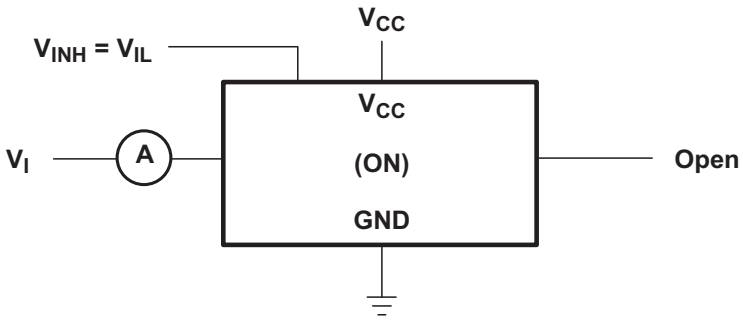


Figure 2. ON-State Resistance Test Circuit



Condition 1: V_I = 0, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = 0

Figure 3. OFF-State Switch Leakage-Current Test Circuit



$V_I = V_{CC}$ or GND

Figure 4. ON-State Switch Leakage-Current Test Circuit

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Parameter Measurement Information (continued)

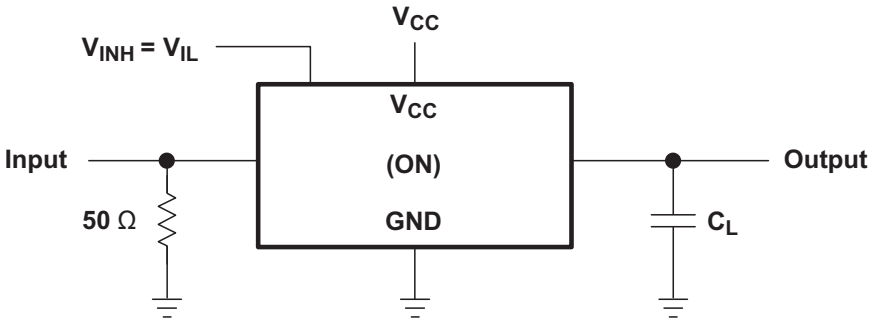
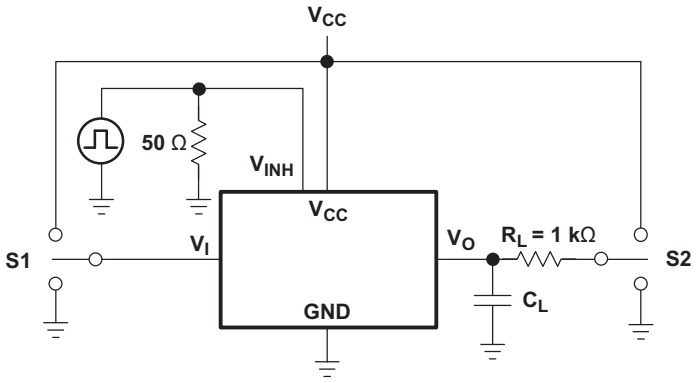
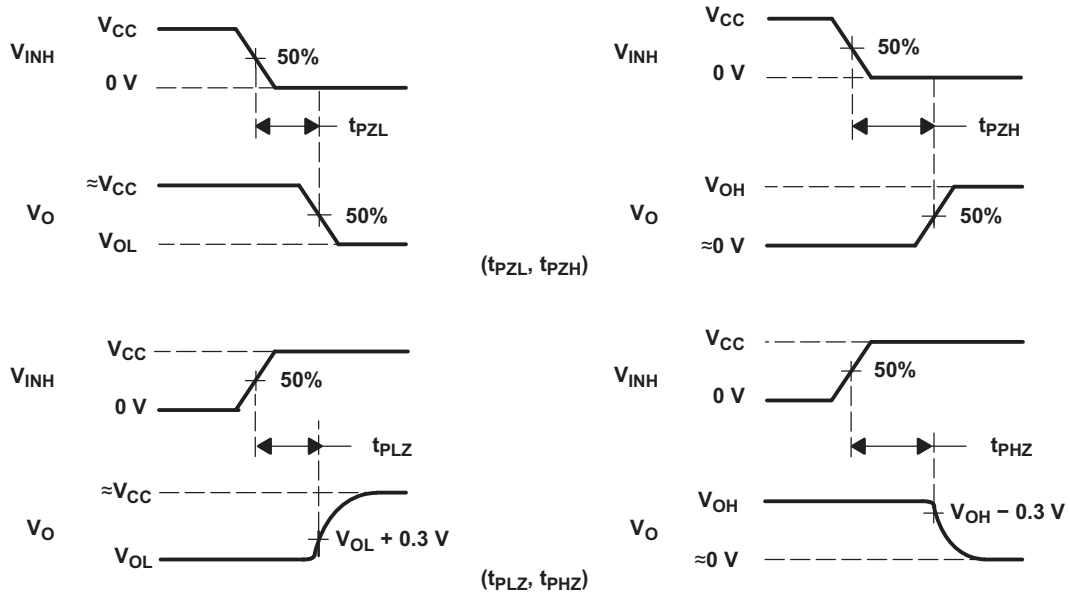


Figure 5. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	GND V_{CC}	V_{CC} GND

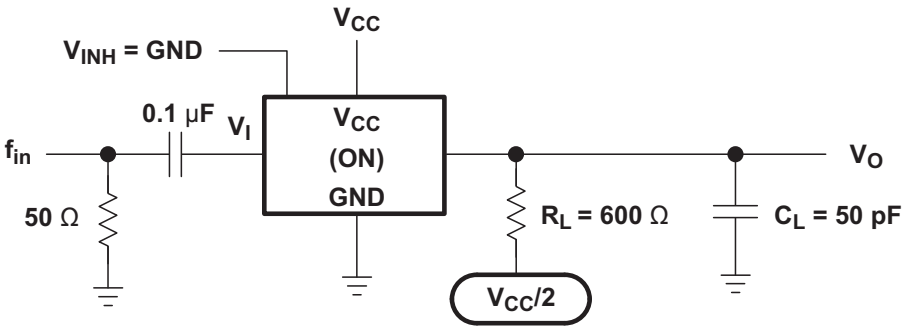
TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

Parameter Measurement Information (continued)



NOTE A: f_{in} is a sine wave.

Figure 7. Frequency Response (Switch ON)

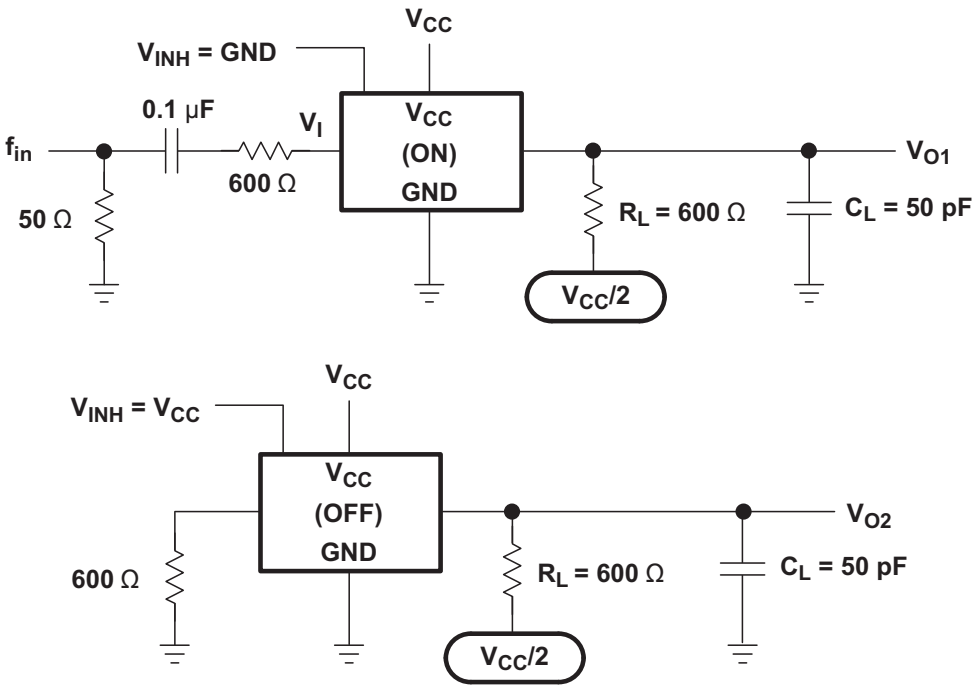


Figure 8. Crosstalk Between Any Two Switches

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Parameter Measurement Information (continued)

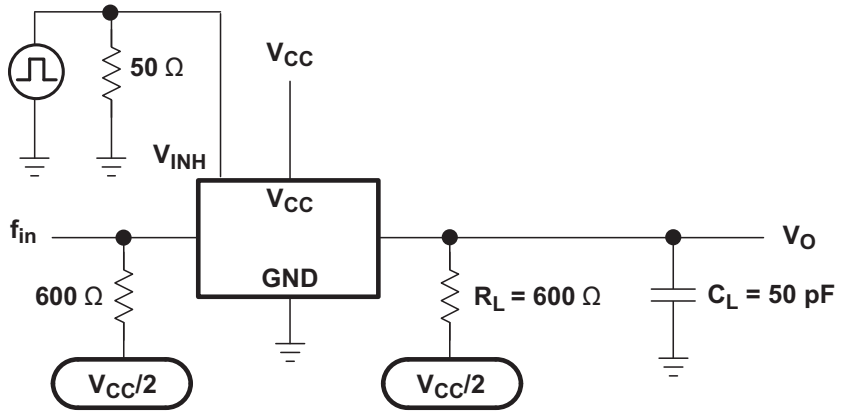


Figure 9. Crosstalk Between Control Input and Switch Output

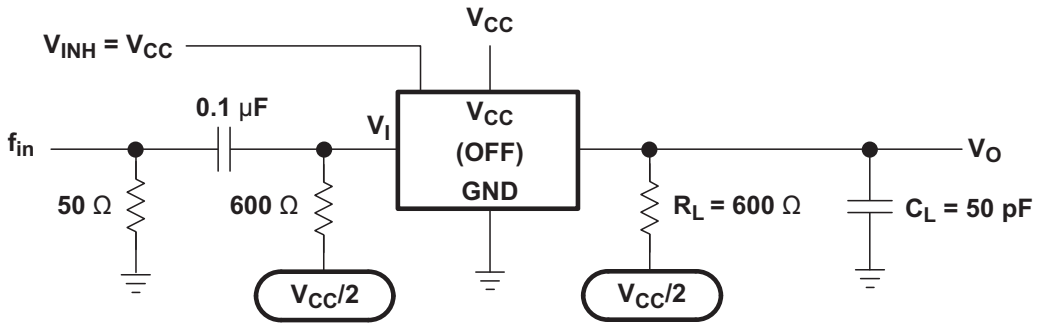


Figure 10. Feedthrough Attenuation (Switch OFF)

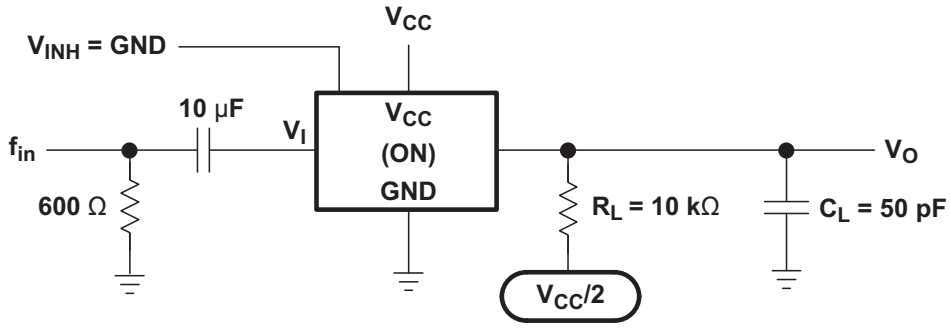


Figure 11. Sine-Wave Distortion

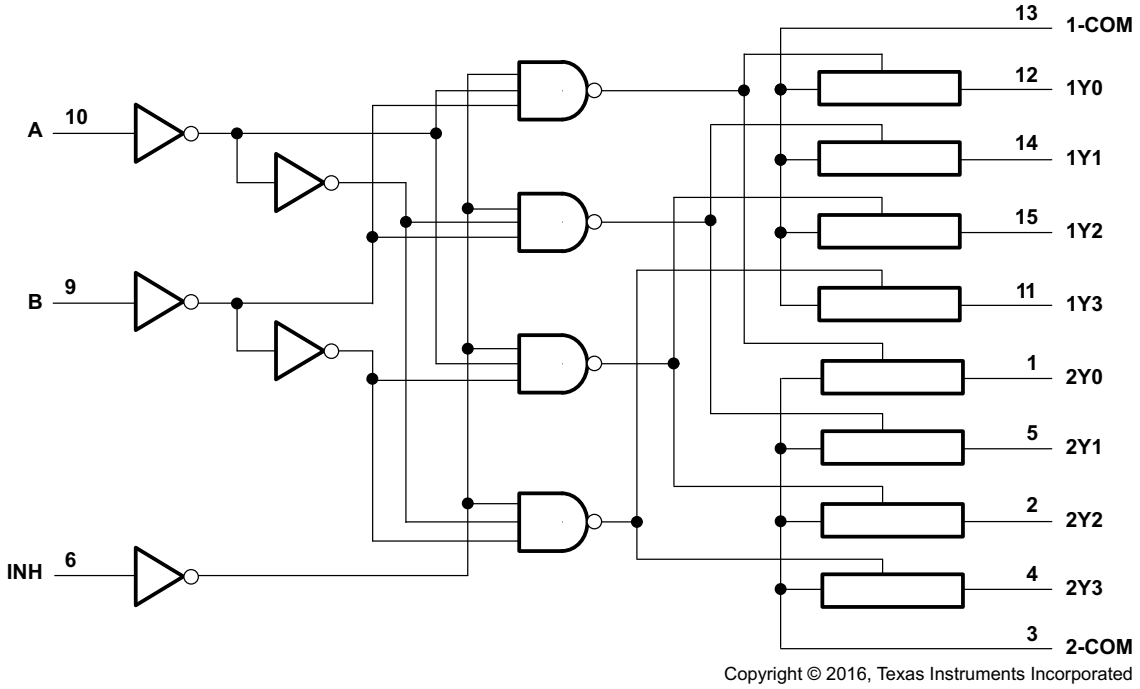
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8 Detailed Description

8.1 Overview

The SN74LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2-V to 5.5-V V_{CC} operation. It has low input current consumption at the digital input pins and low crosstalk between switches. The active low Inhibit (INH) tri-state all the channels when high and when low, depending on the A and B inputs, one of the four independent input/outputs (nY0 - nY3) connects to the COM channel. The SN74LV4052A is available in multiple package options including TSSOP (PW) and QFN (RGY).

8.2 Functional Block Diagram



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Figure 12. Logic Diagram (Positive Logic)

8.3 Feature Description

- The SN74LV4052A operates from 2-V to 5.5-V V_{CC} with extremely low input current consumption at the CMOS input pins of A, B and INH.
- The SN74LV4052A enables fast switching with low crosstalk between the switches. 5.5 V peak level bidirectional transmission allowed with the either analog or digital signals.

8.4 Device Functional Modes

Table 1 lists the functional modes of SN74LV4052A.

Table 1. Function Table

INPUTS			ON CHANNELS
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typical applications for the SN74LV4052A include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

9.2 Typical Application

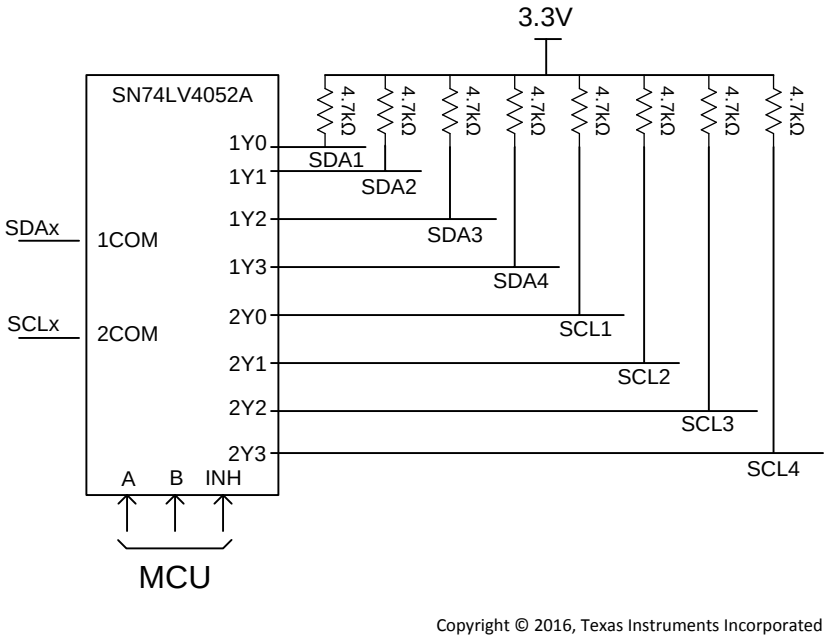


Figure 13. Typical I^2C Multiplexing Application

9.2.1 Design Requirements

Designing with the SN74LV4052A device requires a stable input voltage between 2 V and 5.5 V (see *Recommended Operating Conditions* for details). Another important design consideration are the characteristics of the signal being multiplexed which ensures no important information is lost due to timing or incompatibility with this device.

9.2.2 Detailed Design Procedure

The SN74LV4052A dual 1- to 4-channel multiplexer is ideal for I^2C selection. The I^2C data and clock lines are selected using A,B select lines from the MCU. The pullup resistors are selected based on the capability of the driver. Low pullup resistor results in faster rise time; however, it generates additional current during the low state into the driver. See to the *Recommended Operating Conditions* of the datasheet for the input transition rates (V_{IH} and V_{IL}) of the CMOS inputs.

Typical Application (continued)

9.2.3 Application Curve

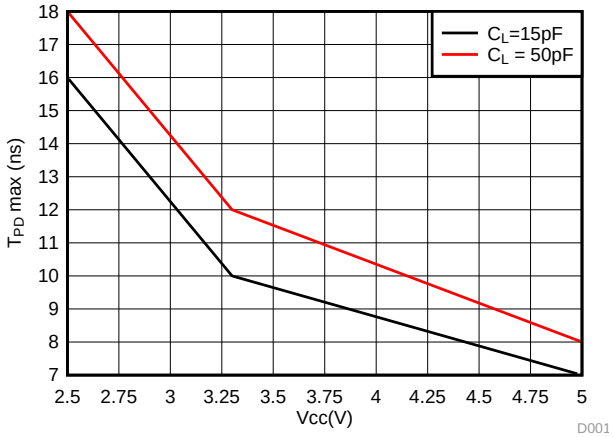


Figure 14. Maximum Propagation Delay vs V_{cc}

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10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

See the *Recommended Operating Conditions* for operating voltage range for this device. Having bypass capacitors of 0.1 µF is highly recommended.

11 Layout

11.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible (see Figure 15). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1 in. long. These traces must be designed with a characteristic impedance of either 50-Ω or 75-Ω as required by the application. Do not place this device too close to high-voltage switching components because they may cause interference. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 16 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

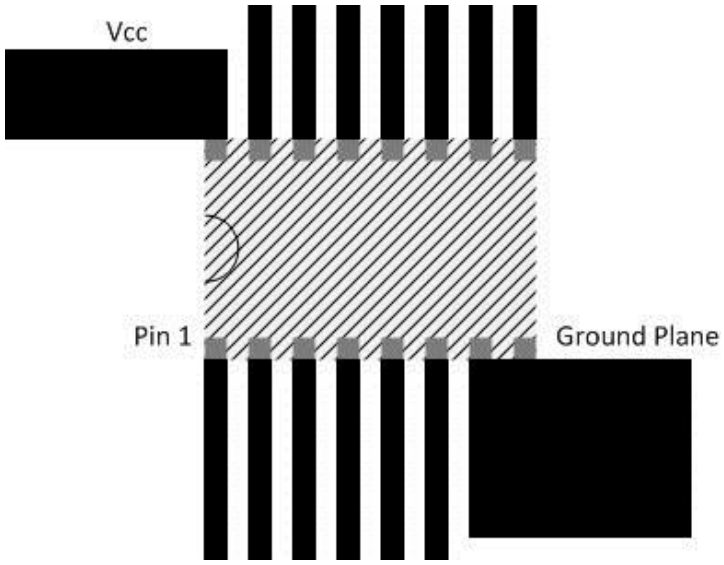


Figure 15. Layout Schematic

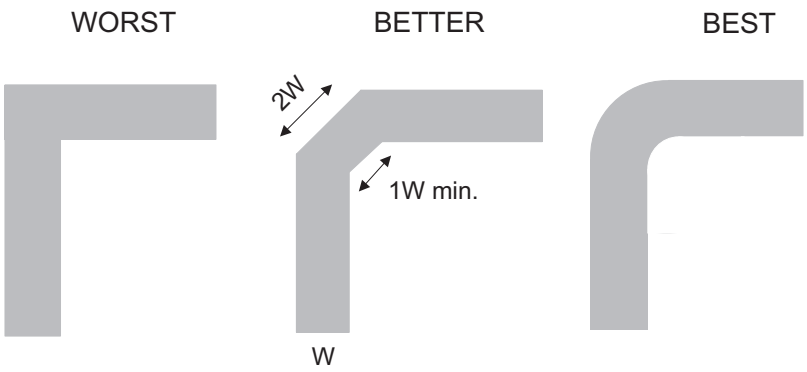


Figure 16. Trace Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4052AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A	Samples
SN74LV4052ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ADBRE4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV4052A	Samples
SN74LV4052AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4052AN	Samples
SN74LV4052ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A	Samples
SN74LV4052APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW052A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV4052A :

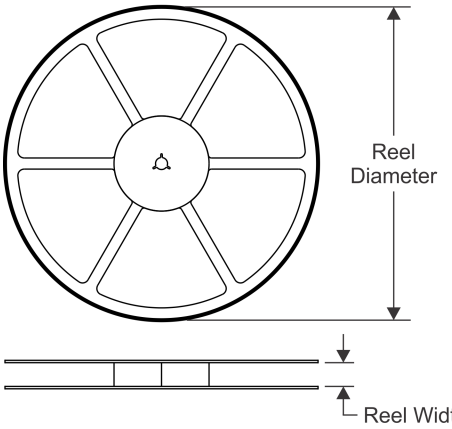
- Automotive : SN74LV4052A-Q1
- Enhanced Product : SN74LV4052A-EP

NOTE: Qualified Version Definitions:

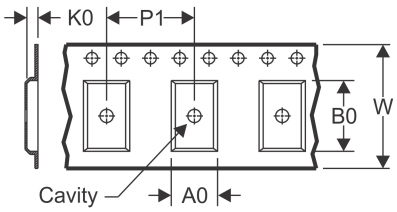
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

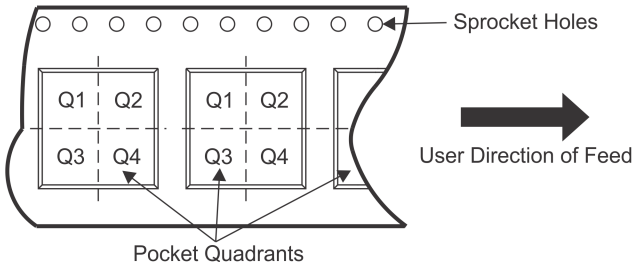


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

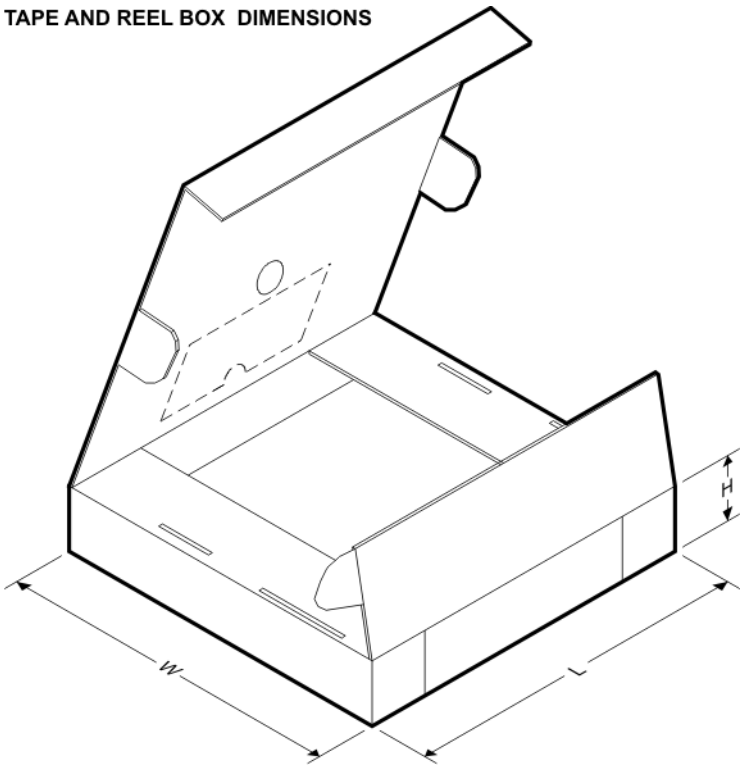
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4052ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4052ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4052ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4052ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4052ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

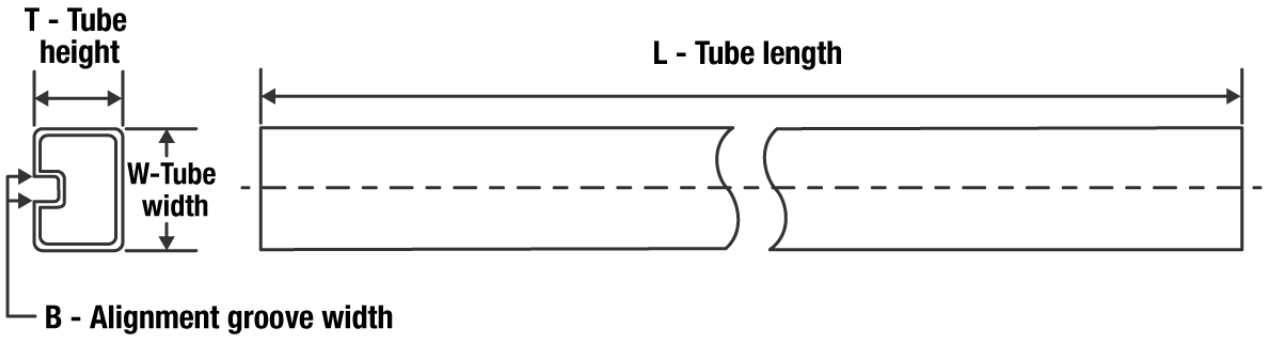
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4052ADBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74LV4052ADGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
SN74LV4052ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV4052ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV4052ANSR	SO	NS	16	2000	853.0	449.0	35.0
SN74LV4052APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV4052APWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74LV4052APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4052APWT	TSSOP	PW	16	250	853.0	449.0	35.0
SN74LV4052ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

TUBE

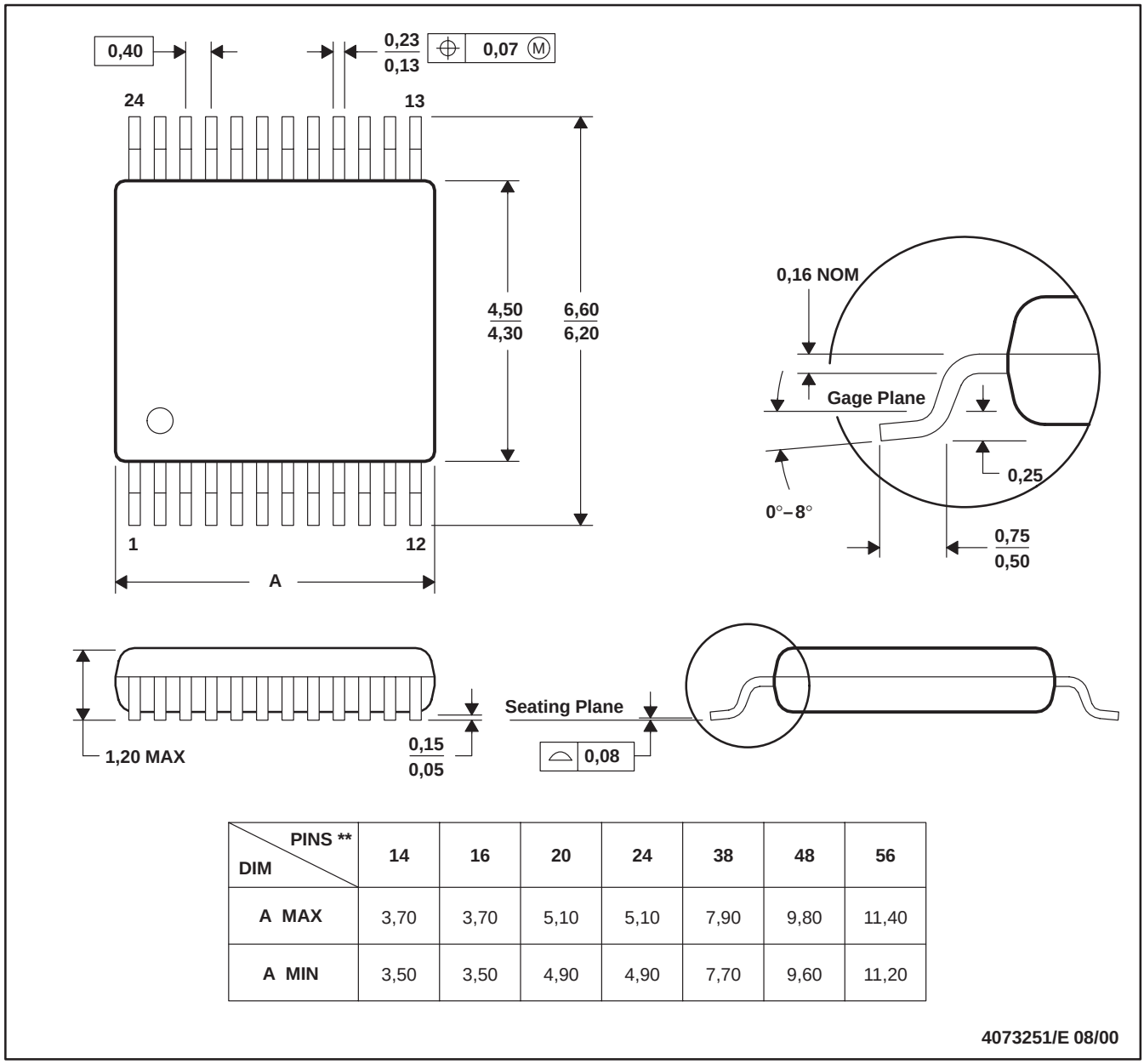


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV4052AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV4052AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4052APWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4052APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

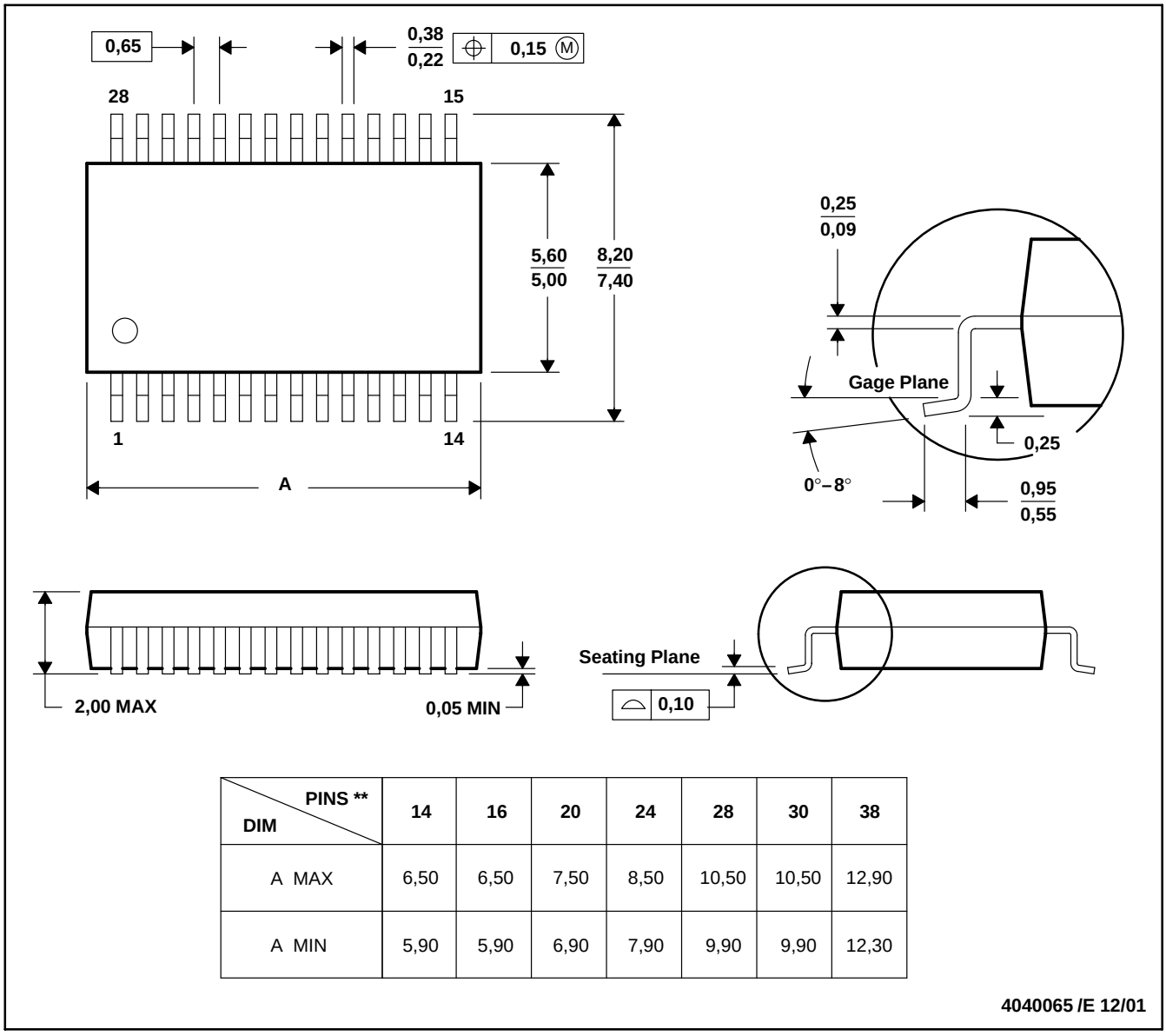
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

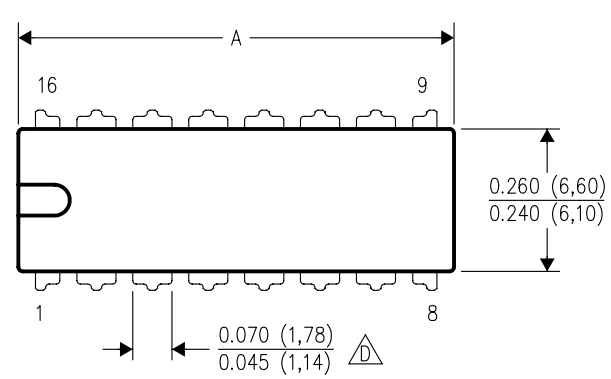
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

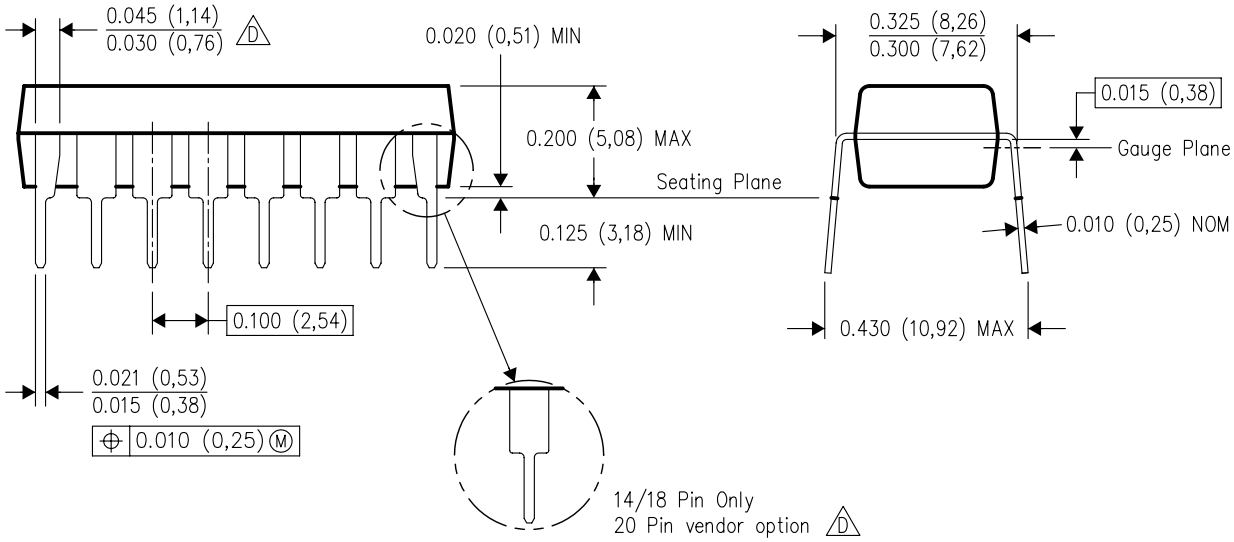
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



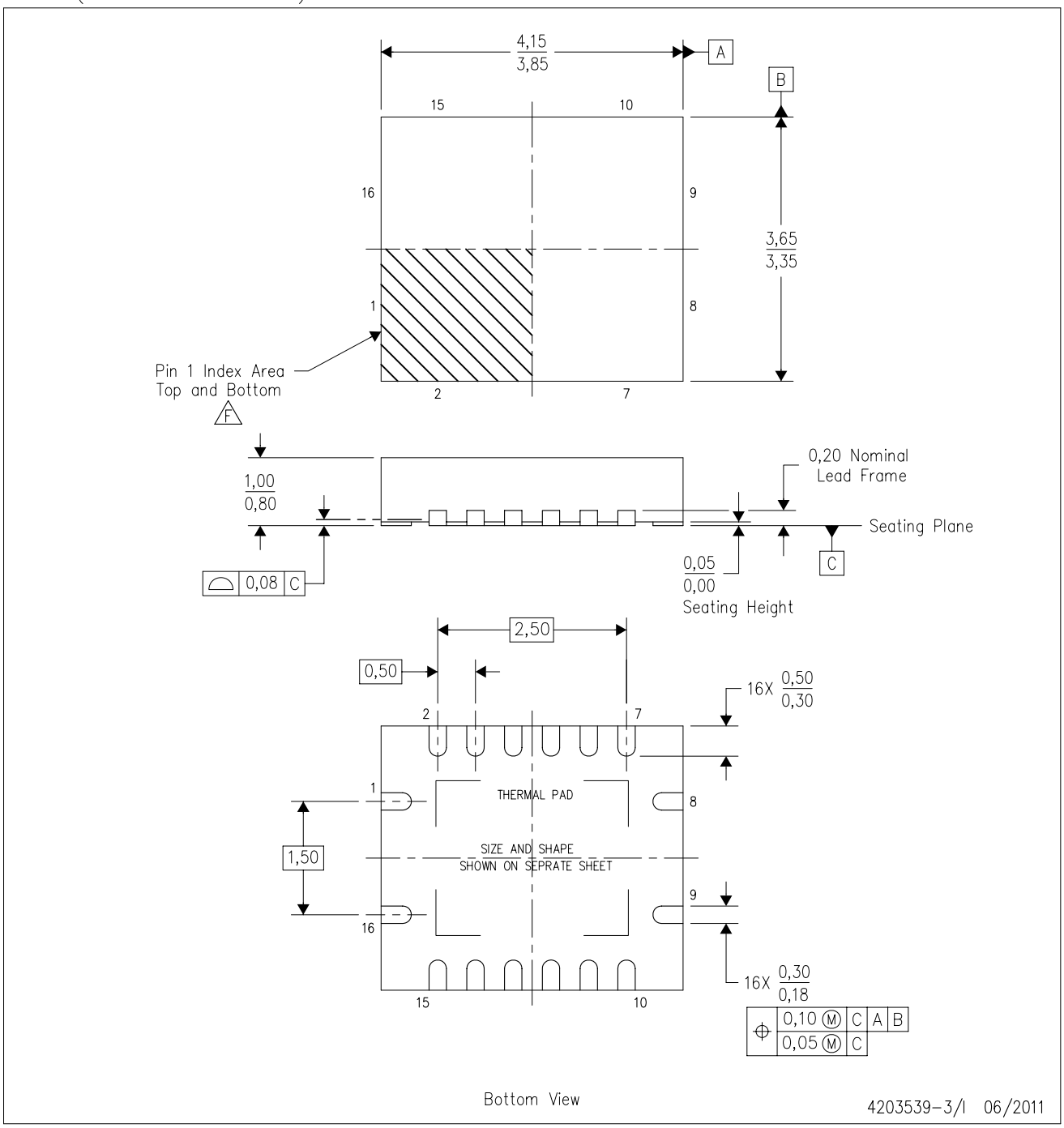
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

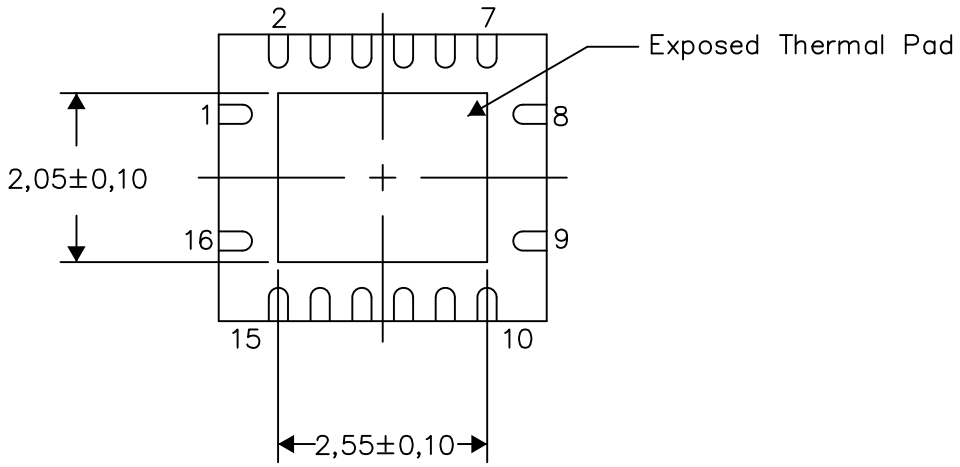
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



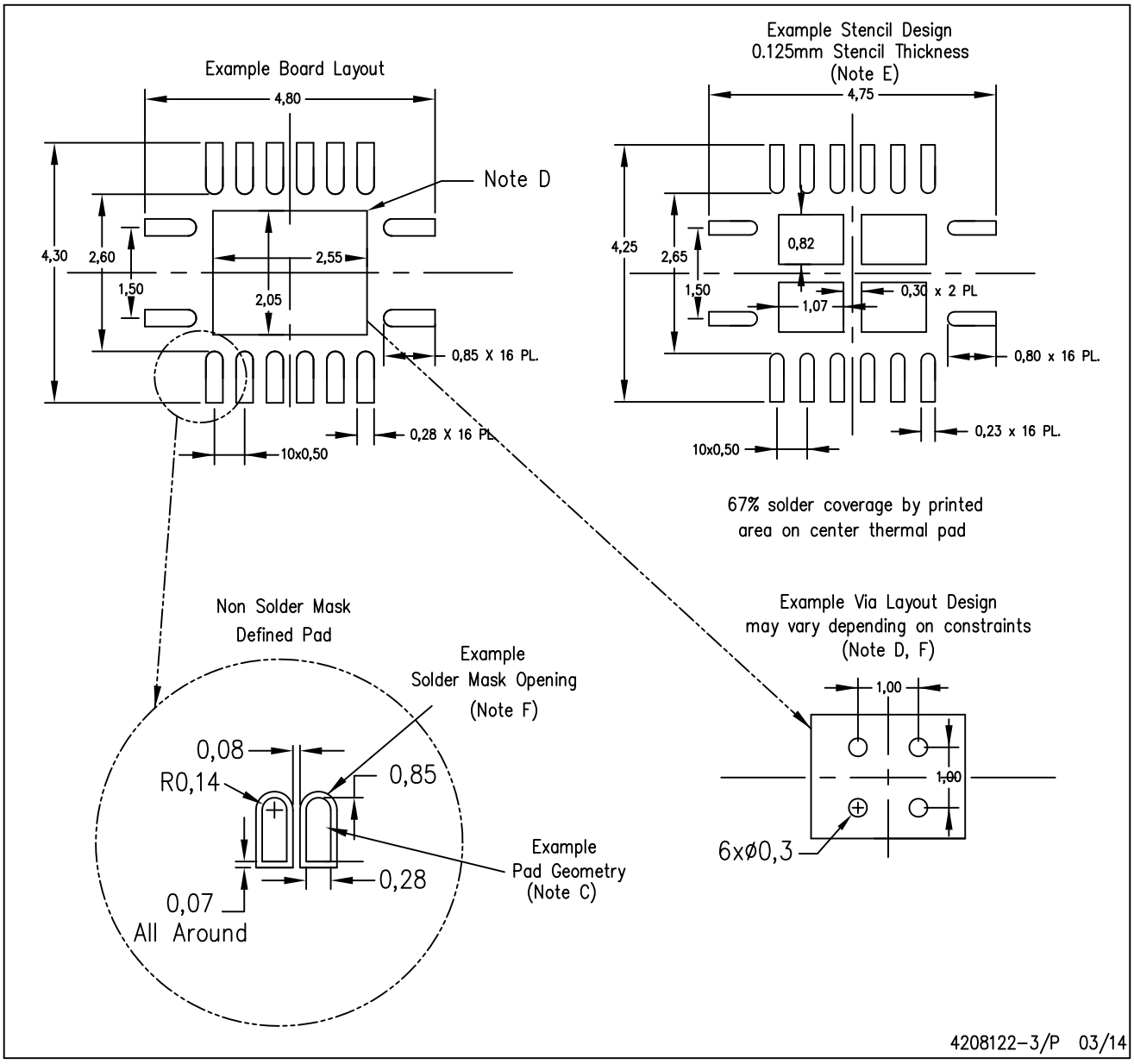
Bottom View

Exposed Thermal Pad Dimensions

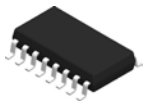
4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

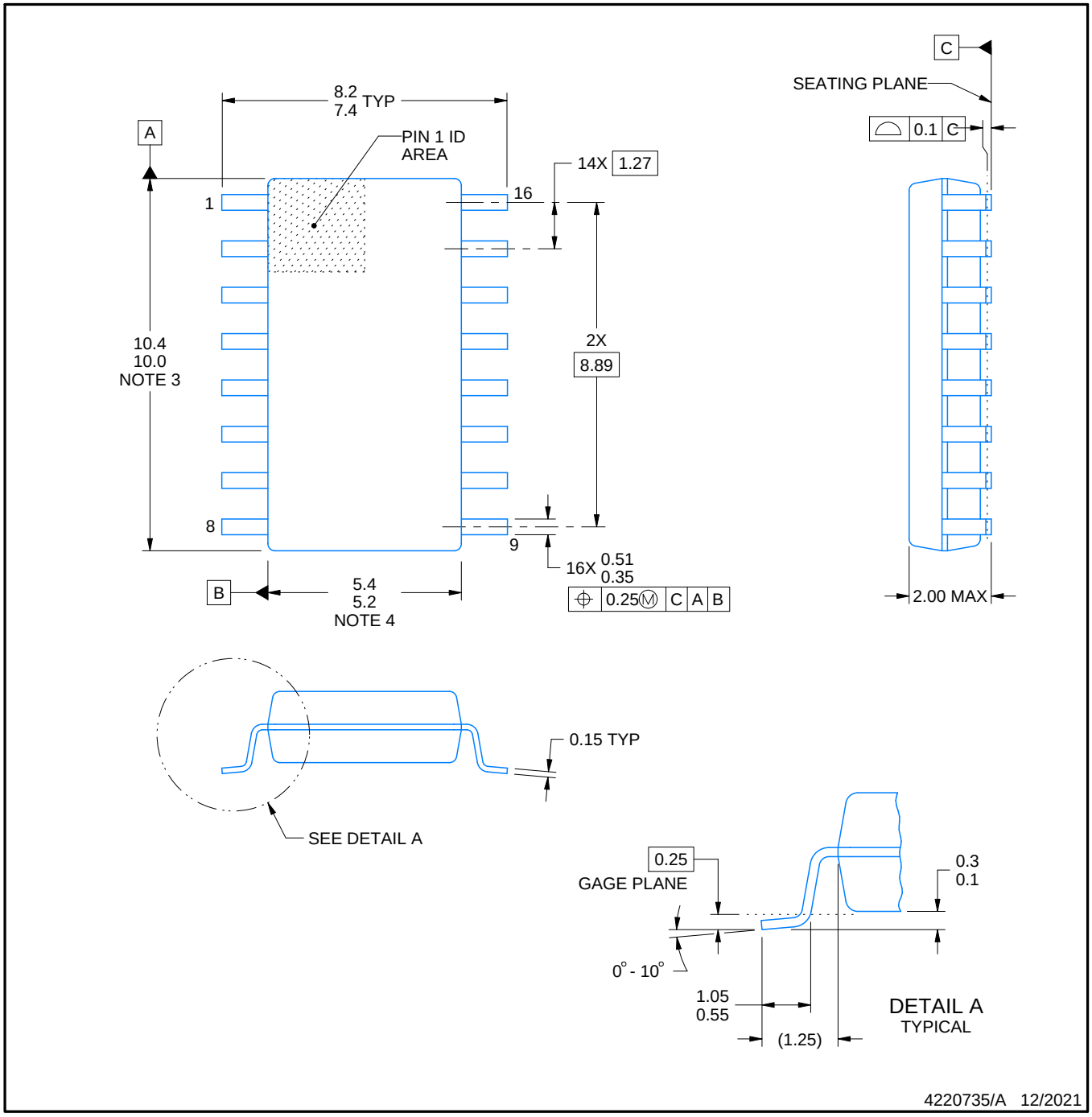


PACKAGE OUTLINE

NS0016A

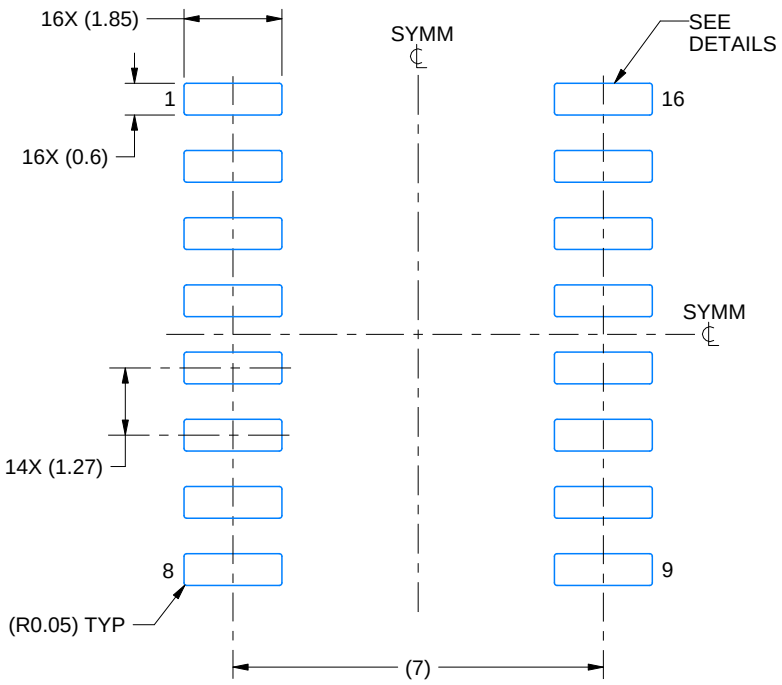
SOP - 2.00 mm max height

SOP

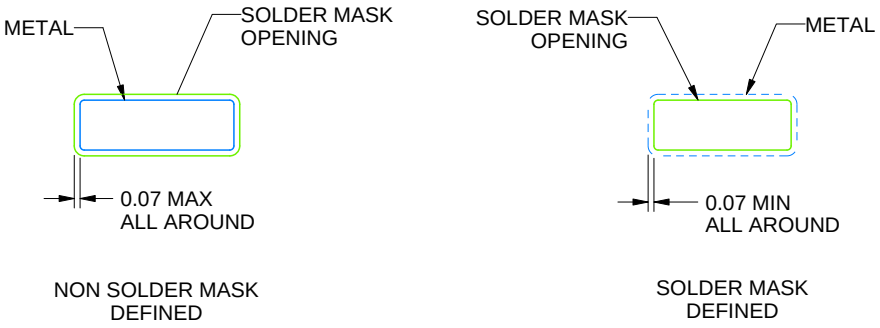


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

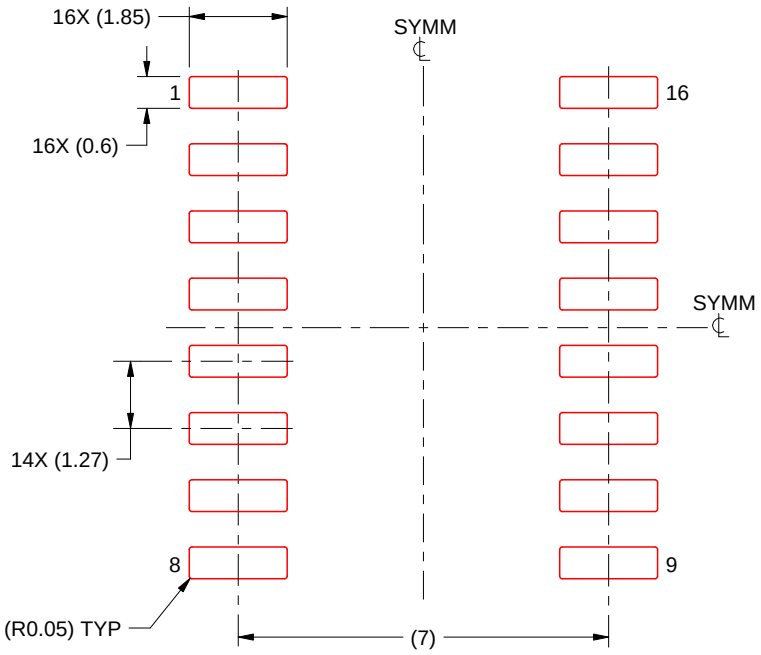
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



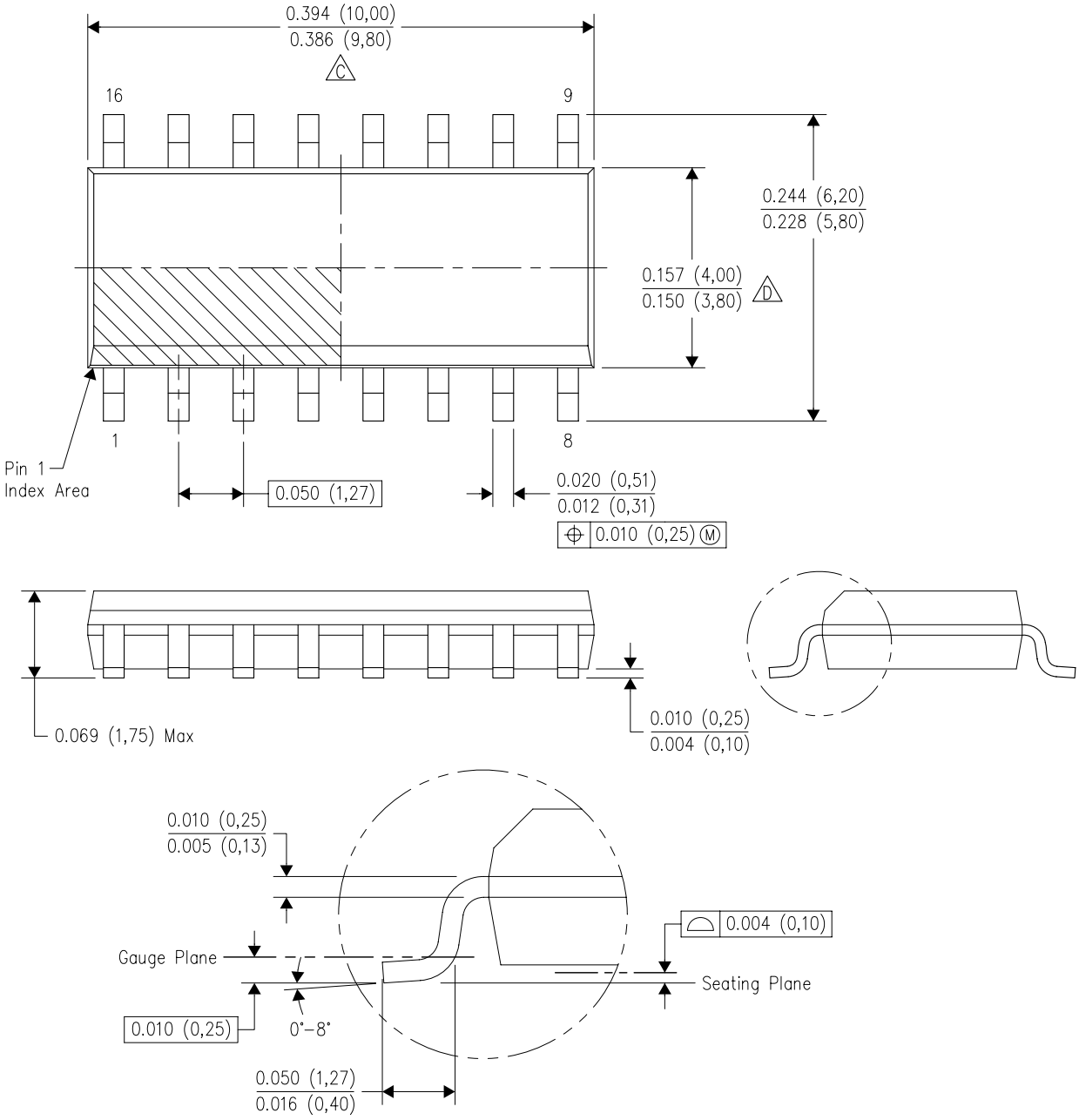
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

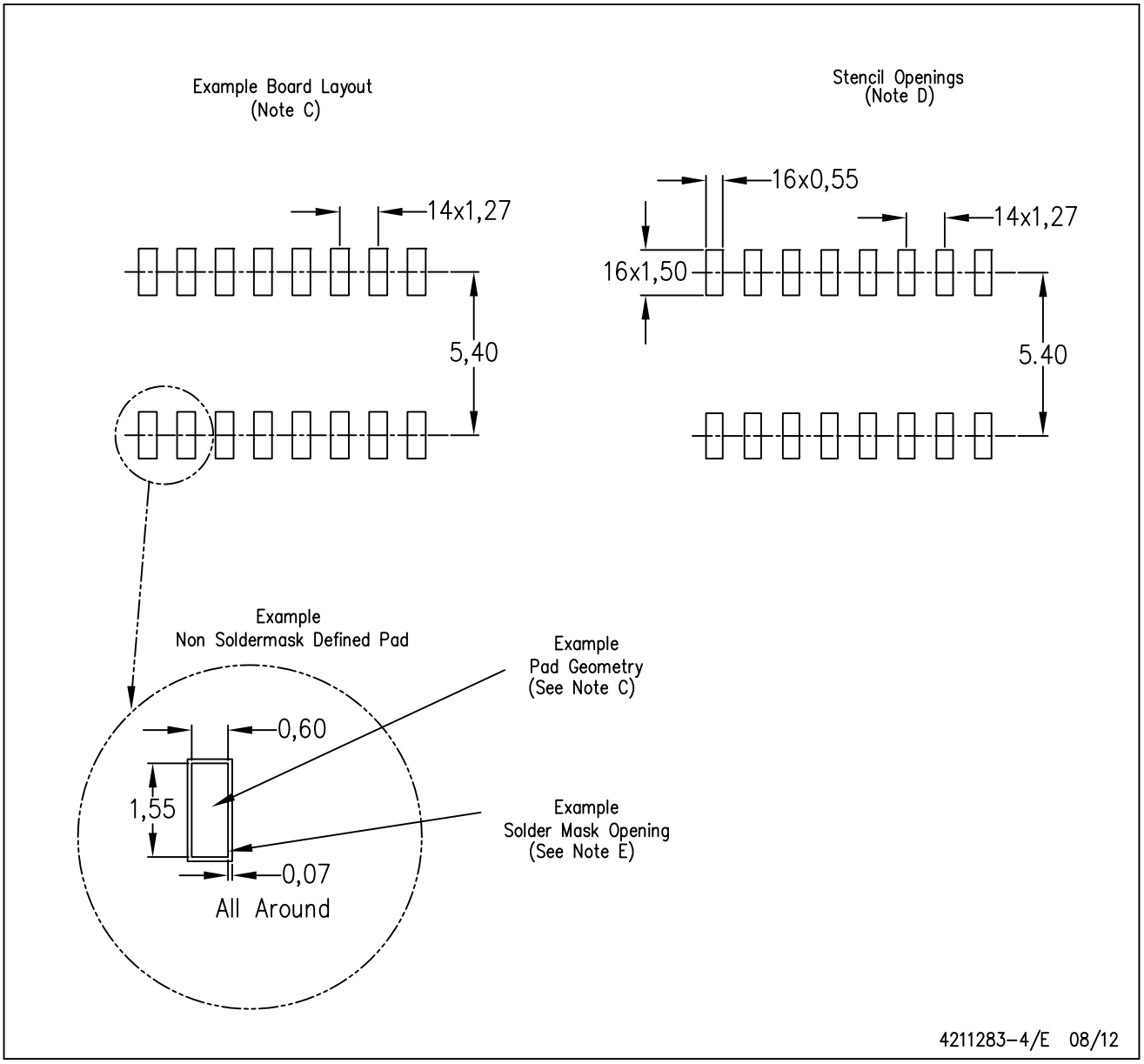
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



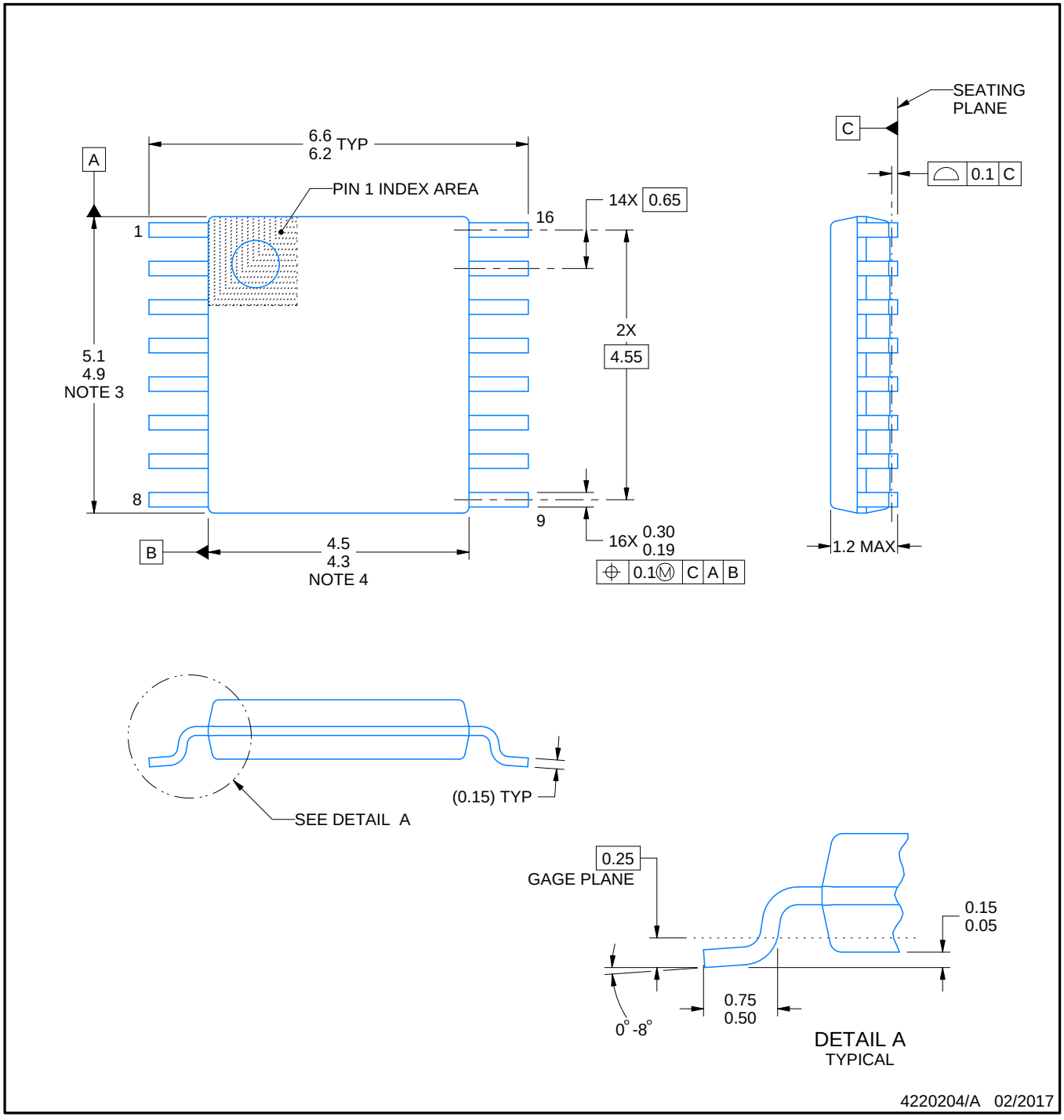
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

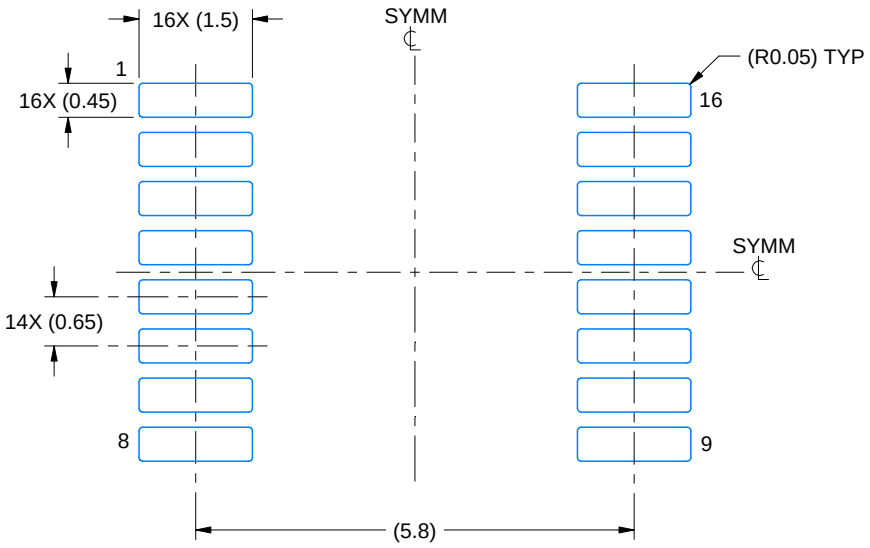
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

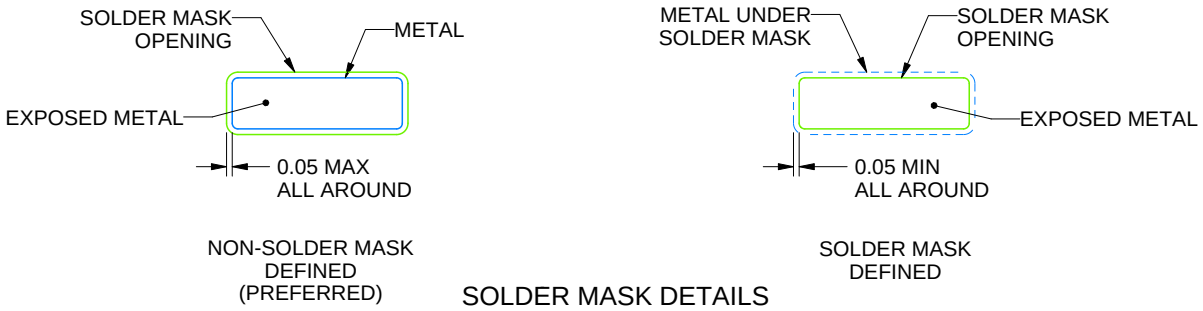


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

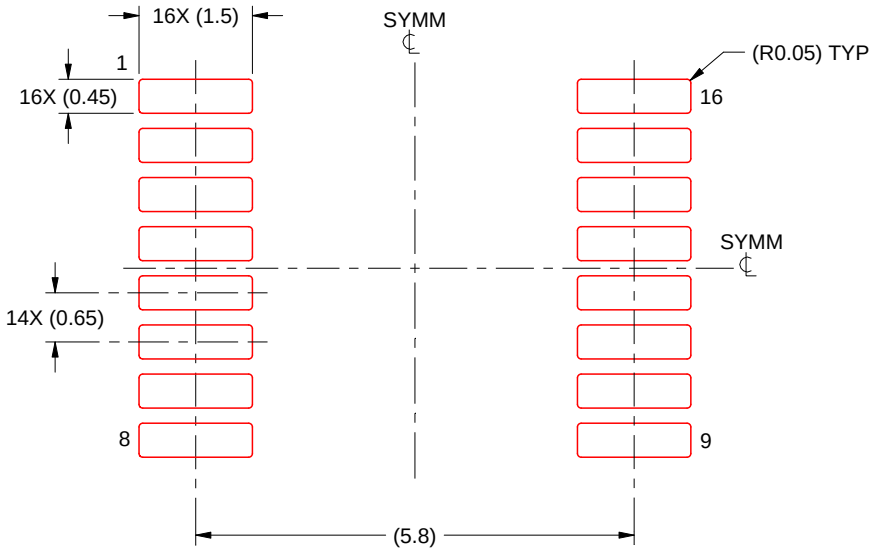


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

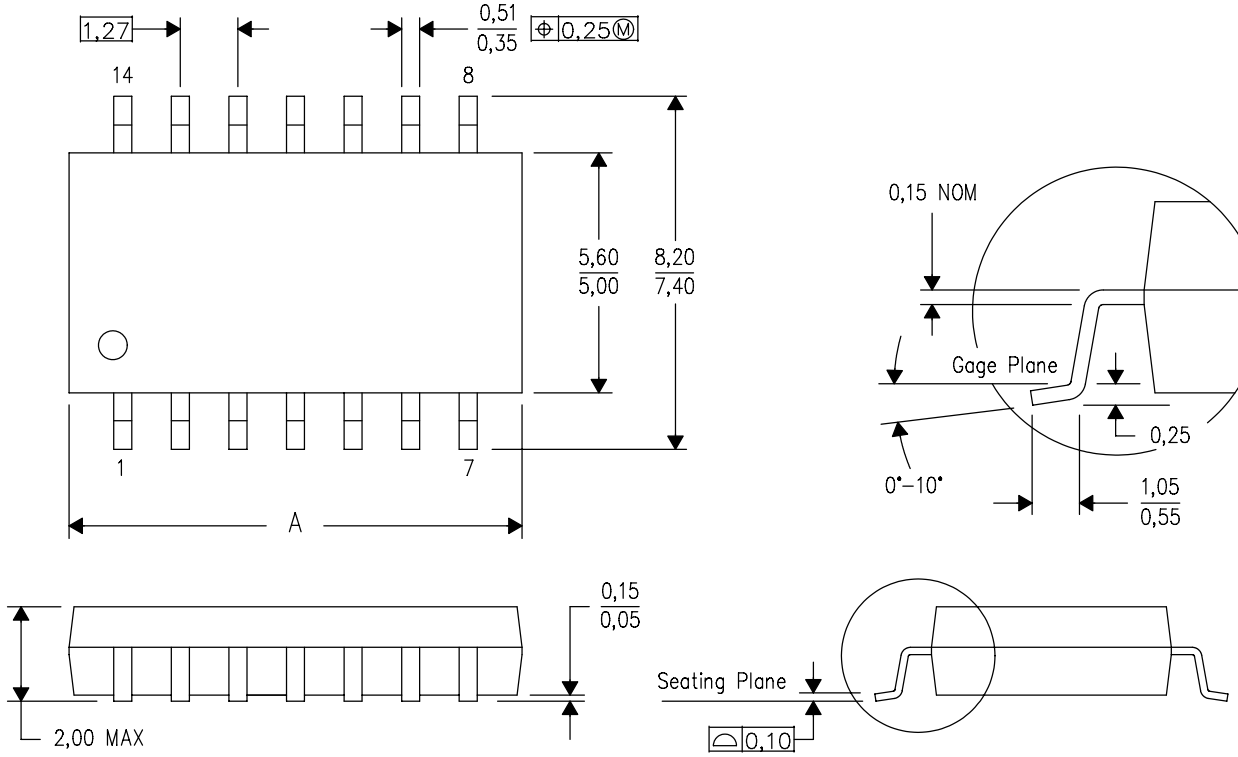
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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