

SNx4LV240A Octal Inverting Buffers/Drivers With 3-State Outputs

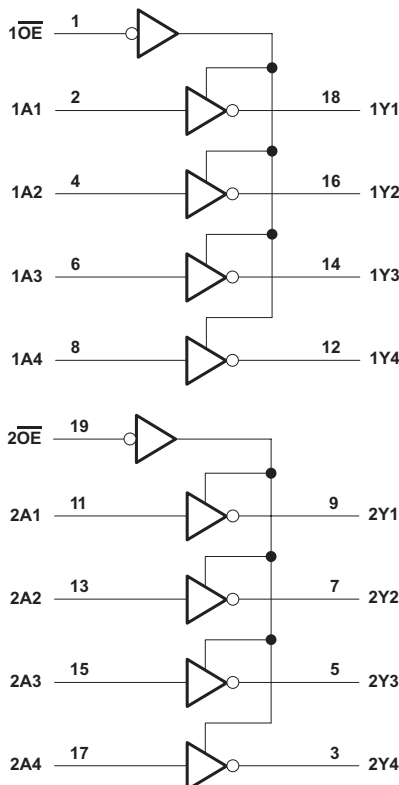
1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA per JESD 17
- I_{off} Supports Live Insertion, Partial Power-Down Mode, and Back Drive Protection
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Handset: Smartphone
- Network Switch
- Health and Fitness / Wearables

4 Logic Diagram (Positive Logic)



3 Description

These octal buffers/drivers with inverted outputs are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| LV240A | TVSOP (14) | 3.60 mm x 4.40 mm |
| | SOIC (14) | 8.65 mm x 3.91 mm |
| | SOP (14) | 10.30 mm x 5.30 mm |
| | SSOP (14) | 6.20 mm x 5.30 mm |
| | TSSOP (14) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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5 Revision History

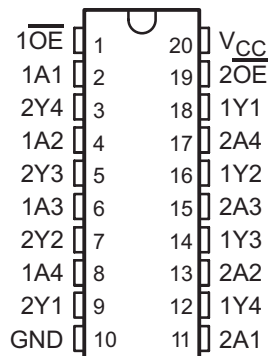
Changes from Revision H (April 2005) to Revision I

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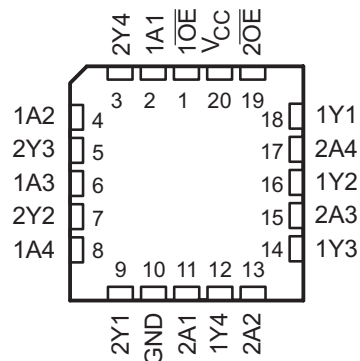
- | | | |
|---|--|---|
| • | Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • | Updated operating free-air temperature maximum from 85°C to 125°C for SN74LV240A | 5 |

6 Pin Configuration and Functions

SN54LV240A: J or W Package
SN74LV240A: DB, DGV, DW, NS, or PW Package
(Top View)



SN54LV240A: FK Package
(Top View)



Pin Functions

| PIN | I/O | DESCRIPTION |
|-----|-----|-----------------|
| 1 | 1OE | Output enable 1 |
| 2 | 1A1 | 1A1 input |
| 3 | 2Y4 | 2Y4 output |
| 4 | 1A2 | 1A2 input |
| 5 | 2Y3 | 2Y3 output |
| 6 | 1A3 | 1A3 input |
| 7 | 2Y2 | 2Y2 output |
| 8 | 1A4 | 1A4 input |
| 9 | 2Y1 | 2Y1 output |
| 10 | GND | Ground pin |
| 11 | 2A1 | 2A1 input |
| 12 | 1Y4 | 1Y4 output |
| 13 | 2A2 | 2A2 input |
| 14 | 1Y3 | 1Y3 output |
| 15 | 2A3 | 2A3 input |
| 16 | 1Y2 | 1Y2 output |
| 17 | 2A4 | 2A4 input |
| 18 | 1Y1 | 1Y1 output |
| 19 | 2OE | Output enable 2 |
| 20 | VCC | Power pin |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|-----------|---|-----------------------|----------------|------|----|
| V_{CC} | Supply voltage | -0.5 | 7 | V | |
| V_I | Input voltage ⁽²⁾ | -0.5 | 7 | V | |
| V_O | Voltage applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V | |
| V_O | Output voltage ^{(2) (3)} | -0.5 | $V_{CC} + 0.5$ | V | |
| I_{IK} | Input clamp current | $V_I < 0$ | -20 | mA | |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA | |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | -35 | 35 | mA |
| | Continuous current through V_{CC} or GND | | -70 | 70 | mA |
| T_{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value is limited to 5.5-V maximum.

7.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 |
| | | Machine model (A115-A) | 200 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 see ⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|--------------------------------|-----------------------|-----------------|----|
| V _{CC} | Supply voltage | 2 | 5.5 | V | |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | V | |
| | | V _{CC} = 2.3 to 2.7 V | V _{CC} × 0.7 | | |
| | | V _{CC} = 3 to 3.6 V | V _{CC} × 0.7 | | |
| | | V _{CC} = 4.5 to 5.5 V | V _{CC} × 0.7 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | 0.5 | V | |
| | | V _{CC} = 2.3 to 2.7 V | V _{CC} × 0.3 | | |
| | | V _{CC} = 3 to 3.6 V | V _{CC} × 0.3 | | |
| | | V _{CC} = 4.5 to 5.5 V | V _{CC} × 0.3 | | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 2 V | –50 | μA | |
| | | V _{CC} = 2.3 to 2.7 V | –2 | | |
| | | V _{CC} = 3 to 3.6 V | –8 | mA | |
| | | V _{CC} = 4.5 to 5.5 V | –16 | | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | 50 | μA | |
| | | V _{CC} = 2.3 to 2.7 V | 2 | | |
| | | V _{CC} = 3 to 3.6 V | 8 | mA | |
| | | V _{CC} = 4.5 to 5.5 V | 16 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 2.3 to 2.7 V | 200 | ns/V | |
| | | V _{CC} = 3 to 3.6 V | 100 | | |
| | | V _{CC} = 4.5 to 5.5 V | 20 | | |
| T _A | Operating free-air temperature | SN54LV240A | –55 | 125 | °C |
| | | SN74LV240A | –40 | 125 | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | DW | DB | DGV | NS | PW | UNIT | |
|-------------------------------|---|------|------|-------|------|-------|------|
| | 20 PINS | | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽²⁾ | 79.2 | 94.5 | 116.2 | 76.7 | 102.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 43.7 | 56.4 | 31.2 | 43.2 | 36.5 | |
| R _{θJB} | Junction-to-board thermal resistance | 47.0 | 49.7 | 57.7 | 44.2 | 53.6 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 18.6 | 18.5 | 0.9 | 16.8 | 2.4 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 46.5 | 49.3 | 57.0 | 43.8 | 52.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|---|------------|----------------|-----|-----|---------|
| V_{OH} | $I_{OH} = -50 \mu A$ | 2 to 5.5 V | $V_{CC} - 0.1$ | | | V |
| | $I_{OH} = -2 \text{ mA}$ | 2.3 V | 2 | | | |
| | $I_{OH} = -8 \text{ mA}$ | 3 V | 2.48 | | | |
| | $I_{OH} = -16 \text{ mA}$ | 4.5 V | 3.8 | | | |
| V_{OL} | $I_{OL} = 50 \mu A$ | 2 to 5.5 V | 0.1 | | | V |
| | $I_{OL} = 2 \text{ mA}$ | 2.3 V | 0.4 | | | |
| | $I_{OL} = 8 \text{ mA}$ | 3 V | 0.44 | | | |
| | $I_{OL} = 16 \text{ mA}$ | 4.5 V | 0.55 | | | |
| I_I | $V_I = 5.5 \text{ V or GND}$ | 0 to 5.5 V | ± 1 | | | μA |
| I_{OZ} | $V_O = V_{CC} \text{ or GND}$ | 5.5 V | ± 5 | | | μA |
| I_{CC} | $V_I = V_{CC} \text{ or GND, } I_O = 0$ | 5.5 V | 20 | | | μA |
| I_{off} | $V_I \text{ or } V_O = 0 \text{ to } 5.5 \text{ V}$ | 0 | 5 | | | μA |
| C_i | $V_I = V_{CC} \text{ or GND}$ | 3.3 V | 2.3 | | | pF |

7.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|---------------------|------------------|-------------------|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t_{pd} | A | Y | $C_L = 15\text{ pF}$ | 6.3 ⁽¹⁾ | 11.6 ⁽¹⁾ | 1 ⁽²⁾ | 14 ⁽²⁾ | ns | |
| t_{en} | \overline{OE} | | | 8.5 ⁽¹⁾ | 14.6 ⁽¹⁾ | 1 ⁽²⁾ | 17 ⁽²⁾ | | |
| t_{dis} | \overline{OE} | | | 9.7 ⁽¹⁾ | 14.1 ⁽¹⁾ | 1 ⁽²⁾ | 16 ⁽²⁾ | | |
| t_{pd} | A | Y | $C_L = 50\text{ pF}$ | 8.2 | 14.4 | 1 | 17 | ns | |
| t_{en} | \overline{OE} | | | 10.3 | 17.8 | 1 | 21 | | |
| t_{dis} | \overline{OE} | | | 14.2 | 19.2 | 1 | 21 | | |
| $t_{sk(o)}$ | | | | | 2 | | 2 ⁽³⁾ | | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) Value applies for SN74LV240A only

7.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|---------------------|------------------|---------------------|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t_{pd} | A | Y | $C_L = 15\text{ pF}$ | 4.6 ⁽¹⁾ | 7.5 ⁽¹⁾ | 1 ⁽²⁾ | 9 ⁽²⁾ | ns | |
| t_{en} | \overline{OE} | | | 6.2 ⁽¹⁾ | 10.6 ⁽¹⁾ | 1 ⁽²⁾ | 12.5 ⁽²⁾ | | |
| t_{dis} | \overline{OE} | | | 8.3 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 ⁽²⁾ | 13.5 ⁽²⁾ | | |
| t_{pd} | A | Y | $C_L = 50\text{ pF}$ | 5.9 | 11 | 1 | 12.5 | ns | |
| t_{en} | \overline{OE} | | | 7.5 | 14.1 | 1 | 16 | | |
| t_{dis} | \overline{OE} | | | 11.8 | 15 | 1 | 17 | | |
| $t_{sk(o)}$ | | | | | 1.5 | | 1.5 ⁽³⁾ | | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) Value applies for SN74LV240A only

7.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|---------------------|------------------|---------------------|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t_{pd} | A | Y | $C_L = 15\text{ pF}$ | 3.4 ⁽¹⁾ | 5.5 ⁽¹⁾ | 1 ⁽²⁾ | 6.5 ⁽²⁾ | ns | |
| t_{en} | \overline{OE} | | | 4.6 ⁽¹⁾ | 7.3 ⁽¹⁾ | 1 ⁽²⁾ | 8.5 ⁽²⁾ | | |
| t_{dis} | \overline{OE} | | | 7.4 ⁽¹⁾ | 12.2 ⁽¹⁾ | 1 ⁽²⁾ | 13.5 ⁽²⁾ | | |
| t_{pd} | A | Y | $C_L = 50\text{ pF}$ | 4.4 | 7.5 | 1 | 8.5 | ns | |
| t_{en} | \overline{OE} | | | 5.6 | 9.3 | 1 | 10.5 | | |
| t_{dis} | \overline{OE} | | | 9.7 | 14.2 | 1 | 15.5 | | |
| $t_{sk(o)}$ | | | | | 1 | | 1 ⁽³⁾ | | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) This values applies for SN74LV240A only

7.9 Noise Characteristics for SN74LV240A

 $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see ⁽¹⁾)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------|--|------|-------|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.56 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.49 | | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 2.82 | | |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | |

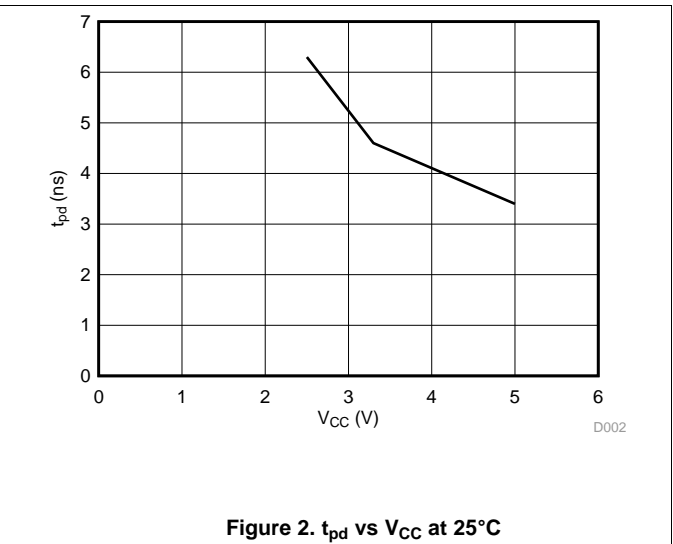
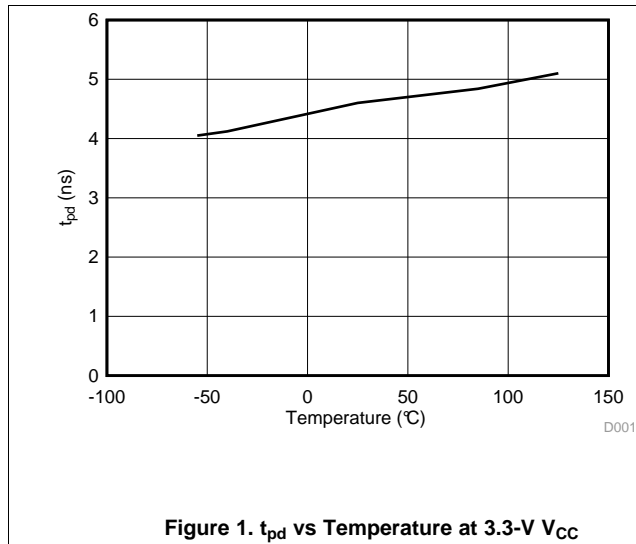
(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

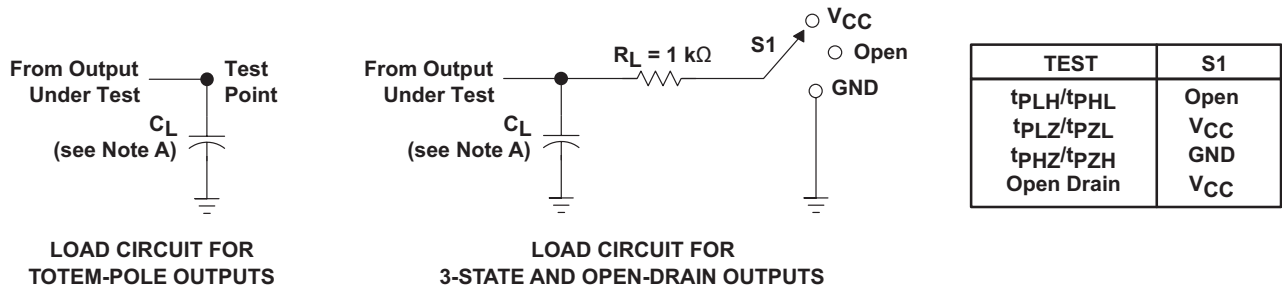
 $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------|-------------------------------|--|----------|------|------|
| C_{pd} | Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 14 | pF |
| | | | 5 V | 16.4 | |

7.11 Typical Characteristics

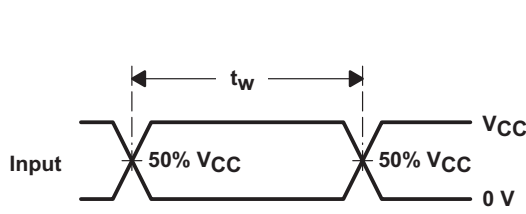


8 Parameter Measurement Information

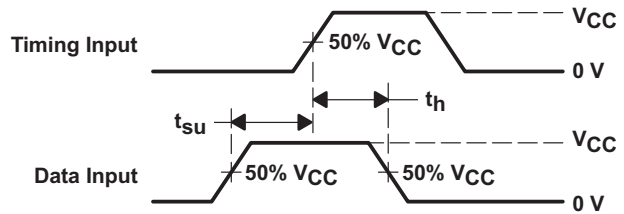


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

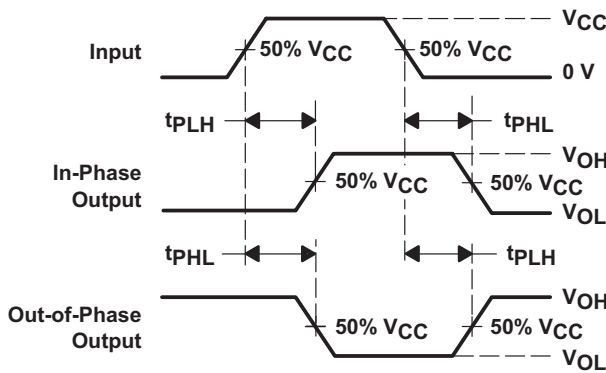
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



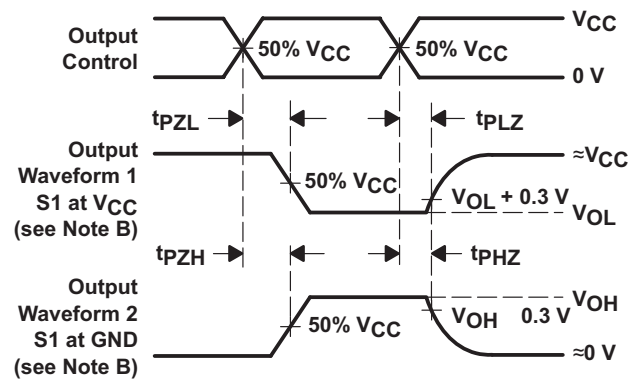
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

These octal buffers/drivers with inverted outputs are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

9.2 Functional Block Diagram

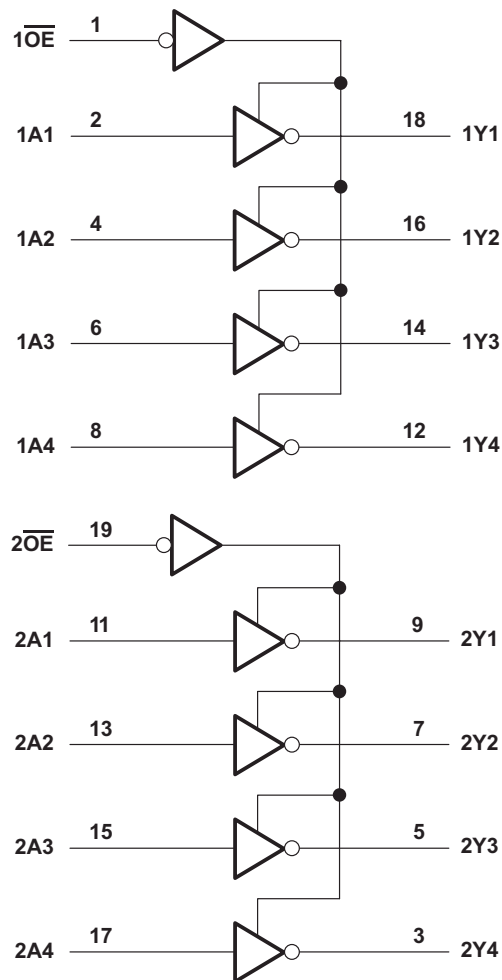


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

- Wide operating voltage range operates from 2-V to 5.5-V operation
- Allow down voltage translation inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

**Table 1. Function Table
(Each Buffer)**

| INPUTS | | OUTPUT |
|------------------------|---|--------|
| $\overline{\text{OE}}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LV240A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 8 mA of drive current at 3.3 V making it ideal for driving multiple outputs and low-noise applications. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application

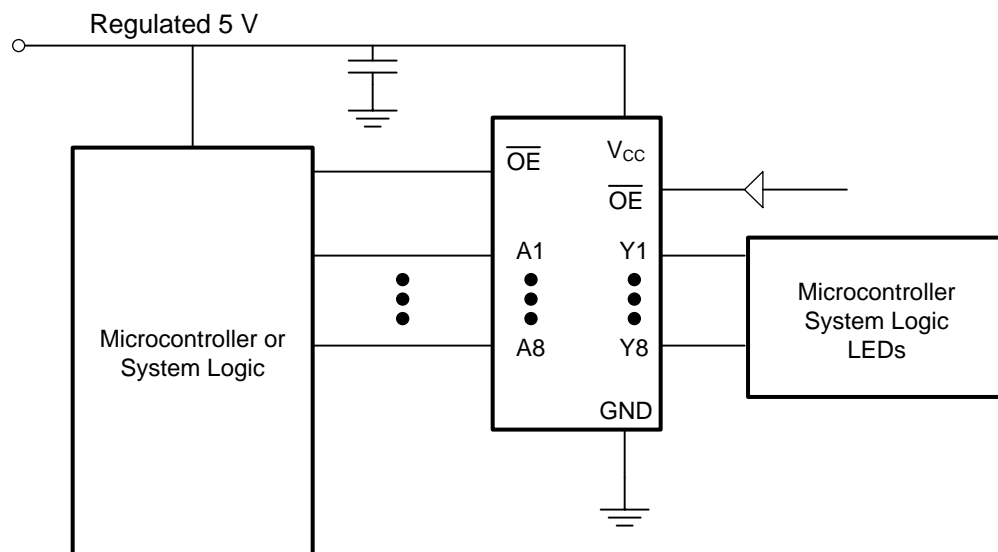


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
 - Rise time and fall time specifications see $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#).
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#).
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part
 - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curve

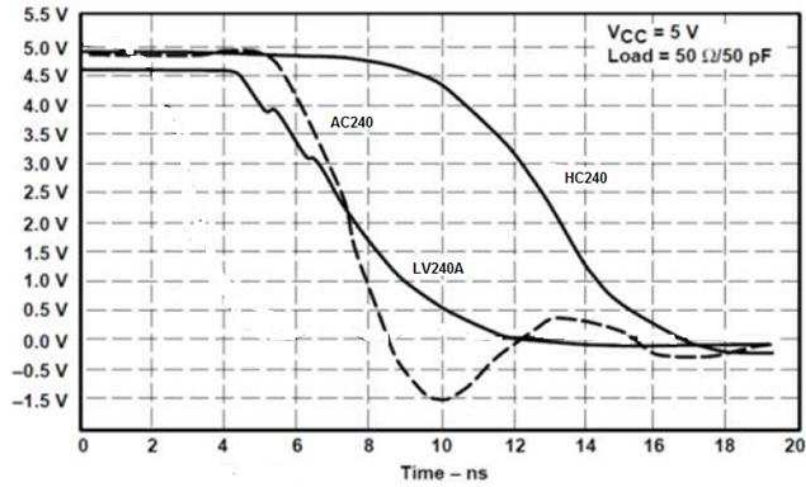


Figure 6. Switching Characteristics Comparison

11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 μF and if there are multiple V_{CC} terminals, then TI recommends .01 μF or .022 μF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

12.2 Layout Example

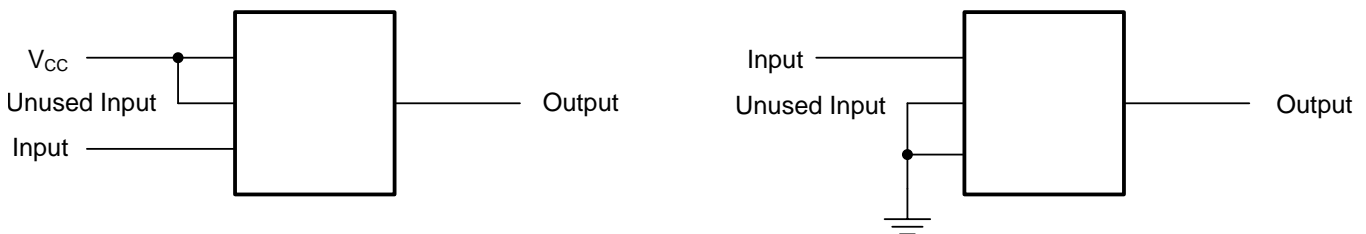


Figure 7. Layout Recommendation

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LV240A | Click here | Click here | Click here | Click here | Click here |
| SN74LV240A | Click here | Click here | Click here | Click here | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV240ADBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240ADW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240ADWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240ANSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV240A | Samples |
| SN74LV240APW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |
| SN74LV240APWT | ACTIVE | TSSOP | PW | 20 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV240A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

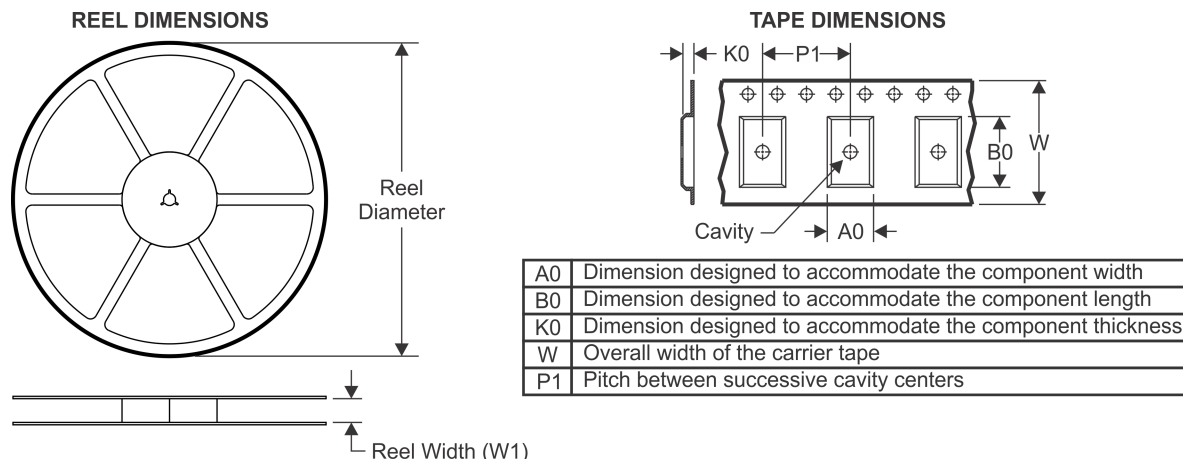
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



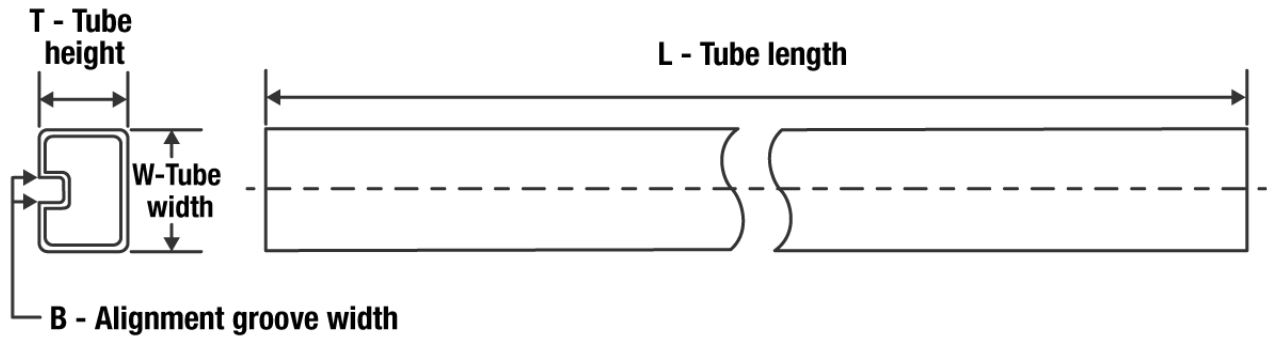
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV240ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV240ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV240ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV240ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LV240APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV240APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LV240APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LV240APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV240ADBR | SSOP | DB | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV240ADGVR | TVSOP | DGV | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV240ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV240ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV240APWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV240APWR | TSSOP | PW | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV240APWRG4 | TSSOP | PW | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV240APWT | TSSOP | PW | 20 | 250 | 853.0 | 449.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV240ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LV240APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LV240APWG4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

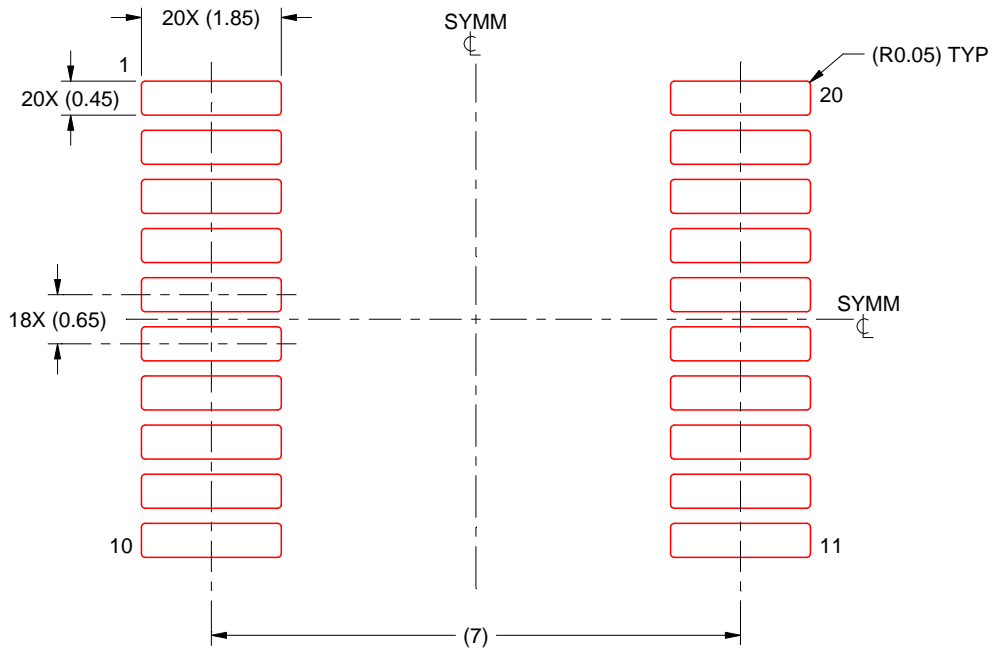
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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