SNx4LVC04A Hex Inverters

1 Features

- Operate From 1.65 V to 3.6 V
- Specified From –40°C to 85°C, –40°C to 125°C, and –55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Maximum t_{pd} of 4.5 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Power Sub-Station Controls
- Ethernet Switches
- Flow Meters
- I/O Modules and Digital PLC/DCS Inputs
- Servers
- Tests and Measurement

3 Description

The SNx4LVC04A hex inverters contains six independent inverters designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC04A hex inverter contains six independent inverters designed for 1.65-V to 3.6-V V_{CC} operation. The SNx4LVC04A devices perform the Boolean function $Y = \overline{A}$.

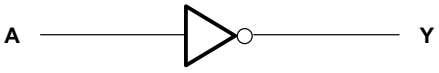
Inputs can be driven from 1.8-V or 3.3-V devices. This feature allows the use of these devices as translators in a mixed 1.8-V or 3.3-V system environment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54LVC04A	CDIP (14)	19.56 mm × 6.67 mm
	CFP (14)	9.21 mm × 5.97 mm
	LCCC (20)	8.89 mm × 8.89 mm
SN74LVC04A	SOIC (14)	8.65 mm × 3.91 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TVSOP (14)	3.60 mm × 4.40 mm
	SOP (14)	6.20 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Inverter (Positive Logic)



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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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4 Revision History

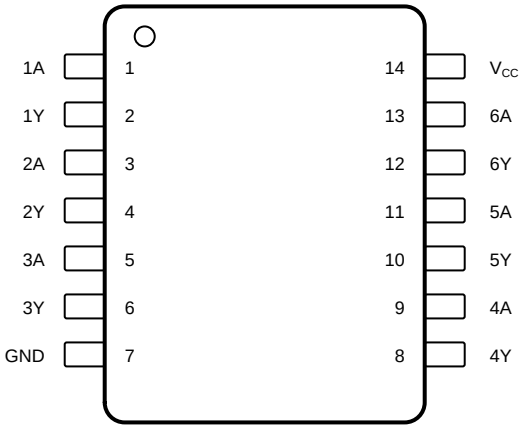
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (October 2010) to Revision T	Page
• Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet	1
• Added *Thermal Information Table – SN54LVC04A*	6
• Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information – SN74LVC04A* From: 96 To: 113.1 (DB), From: 127 To: 142.7 (DGV), From: 76 To: 95.4 (NS), From: 113 To: 129.5 (PW), and From: 47 To: 63.2 (RGY)	6

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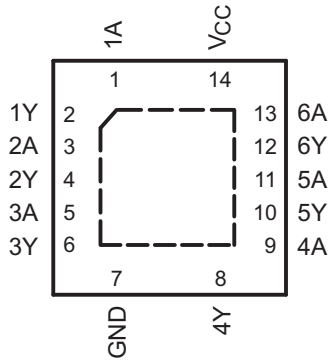
5 Pin Configuration and Functions

D, DB, DGV, J, NS, PW, or W Package
14-Pin SOIC, SSOP, TVSOP, CDIP, SOP, TSSOP, or CFP
Top View

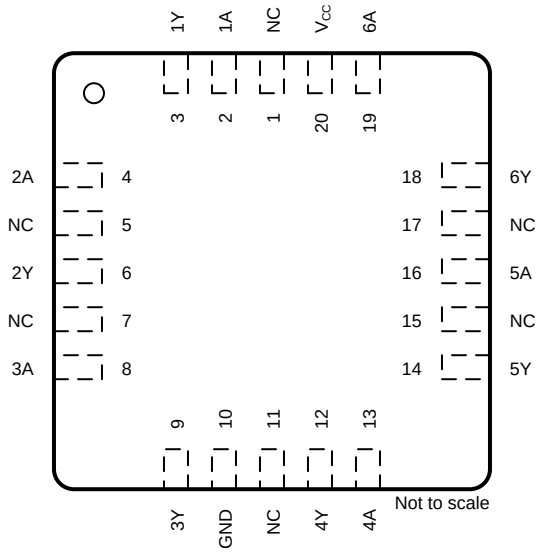


Not to scale

RGY Package
14-Pin VQFN With Exposed Thermal Pad
Top View



FK Package
20-Pin LCCC
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D, DB, DGV, J, NS, PW, RGY, W	FK, LCCC		
1A	1	2	I	Channel 1 input
1Y	2	3	O	Channel 1 output
2A	3	4	I	Channel 2 input
2Y	4	6	O	Channel 2 output
3A	5	8	I	Channel 3 input
3Y	6	9	O	Channel 3 output
4A	9	13	I	Channel 4 input
4Y	8	12	O	Channel 4 output
5A	11	16	I	Channel 5 input
5Y	10	14	O	Channel 5 output
6A	13	19	I	Channel 6 input
6Y	12	18	O	Channel 6 output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V_{CC}	14	20	—	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	6.5	V
Input voltage, V_I(2)		–0.5	6.5	V
Output voltage, V_O(2)(3)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Power dissipation, P_{tot}	T_A = –40°C to 125°C(4)(5)		500	mW
Maximum virtual junction temperature, $T_{J(MAX)}$			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.
(4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
(5) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	SN54LVC04A	2	3.6	V
			SN74LVC04A	1.65	3.6	
		Data retention only		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V, SN74LVC04A only		0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V, SN74LVC04A only		1.7		
		V_{CC} = 2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V, SN74LVC04A only			0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V, SN74LVC04A only			0.7	
		V_{CC} = 2.7 V to 3.6 V			0.8	
V_I	Input voltage			0	5.5	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V, SN74LVC04A only			–4	mA
		V_{CC} = 2.3 V, SN74LVC04A only			–8	
		V_{CC} = 2.7 V			–12	
		V_{CC} = 3 V			–24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V, SN74LVC04A only		4	mA
		V_{CC} = 2.3 V, SN74LVC04A only		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	

6.4 Thermal Information – SN54LVC04A

THERMAL METRIC(1)		SN54LVC04A			UNIT
		J (CDIP)	W (CFP)	FK (LCCC)	
		14 PINS	14 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92	158.2	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	88.7	62.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.5	156.5	61.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.2	58.5	55.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.2	135.5	61.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	25.3	15.3	10.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information – SN74LVC04A

THERMAL METRIC(1)		SN74LVC04A						UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.7	113.1	142.7	95.4	129.5	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	65.1	61.9	53.2	57.9	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.1	60.5	72.1	54.2	71.3	39.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	29.1	10.1	21.9	9.9	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.6	60	71.4	53.8	70.7	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	20.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics – SN54LVC04A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA, V_{CC} = 2.7 V to 3.6 V		V_{CC} – 0.2			V
		I_{OH} = –12 mA	V_{CC} = 2.7 V	2.2			
			V_{CC} = 3 V	2.4			
		I_{OH} = –24 mA, V_{CC} = 3 V		2.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, V_{CC} = 2.7 V to 3.6 V				0.2	V
		I_{OL} = 12 mA, V_{CC} = 2.7 V				0.4	
		I_{OL} = 24 mA, V_{CC} = 3 V				0.55	
I_I	Input current	V_I = 5.5 V or GND, V_{CC} = 3.6 V				±5	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 3.6 V				10	µA
ΔI_{CC}	Change in supply current	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND, V_{CC} = 2.7 V to 3.6 V				500	µA

6.7 Electrical Characteristics – SN74LVC04A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA, V_{CC} = 1.65 V to 3.6 V	T_A = 25°C		V_{CC} – 0.2			V
			T_A = –40°C to 125°C		V_{CC} – 0.3			
		I_{OH} = –4 mA, V_{CC} = 1.65 V	T_A = 25°C		1.29			
			T_A = –40°C to 85°C		1.2			
			T_A = –40°C to 125°C		1.05			
		I_{OH} = –8 mA, V_{CC} = 2.3 V	T_A = 25°C		1.9			
			T_A = –40°C to 85°C		1.7			
			T_A = –40°C to 125°C		1.55			
		I_{OH} = –12 mA	V_{CC} = 2.7 V	T_A = 25°C	2.2			
				T_A = –40°C to 125°C	2.05			
			V_{CC} = 3 V	T_A = 25°C	2.4			
				T_A = –40°C to 125°C	2.25			
		I_{OH} = –24 mA, V_{CC} = 3 V	T_A = 25°C		2.3			
			T_A = –40°C to 85°C		2.2			
			T_A = –40°C to 125°C		2			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, V_{CC} = 1.65 V to 3.6 V	T_A = 25°C				0.1	V
			T_A = –40°C to 85°C				0.2	
			T_A = –40°C to 125°C				0.3	
		I_{OL} = 4 mA, V_{CC} = 1.65 V	T_A = 25°C				0.24	
			T_A = –40°C to 85°C				0.45	
			T_A = –40°C to 125°C				0.6	
		I_{OL} = 8 mA, V_{CC} = 2.3 V	T_A = 25°C				0.3	
			T_A = –40°C to 85°C				0.7	
			T_A = –40°C to 125°C				0.85	
		I_{OL} = 12 mA, V_{CC} = 2.7 V	T_A = 25°C				0.4	
			T_A = –40°C to 125°C				0.6	
		I_{OL} = 24 mA, V_{CC} = 3 V	T_A = 25°C				0.55	
			T_A = –40°C to 125°C				0.8	
I_I	Input current	V_I = 5.5 V or GND, V_{CC} = 3.6 V	T_A = 25°C				±1	µA
			T_A = –40°C to 85°C				±5	
			T_A = –40°C to 125°C				±20	

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Electrical Characteristics – SN74LVC04A (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$, $V_{CC} = 3.6$ V	$T_A = 25°C$			1	µA
			$T_A = –40°C$ to 85°C			10	
			$T_A = –40°C$ to 125°C			40	
ΔI_{CC}	Change in supply current	One input at $V_{CC} – 0.6$ V, other inputs at V_{CC} or GND, $V_{CC} = 2.7$ V to 3.6 V	$T_A = 25°C$			500	µA
			$T_A = –40°C$ to 125°C			5000	
C_i	Input capacitance	$V_I = V_{CC}$ or GND, $V_{CC} = 3.3$ V			5		pF

6.8 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted; see Figure 2)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	Propagation (delay) time	From A (input) to Y (output)	$V_{CC} = 1.8$ V ±0.15 V, SN74LVC04A only	$T_A = 25°C$	1	4.1	7.5	ns
				$T_A = –40°C$ to 85°C	1		8	
				$T_A = –40°C$ to 125°C	1		9.5	
			$V_{CC} = 2.5$ V ±0.2 V, SN74LVC04A only	$T_A = 25°C$	1	3.6	7	
				$T_A = –40°C$ to 85°C	1		7.5	
				$T_A = –40°C$ to 125°C	1		9	
			$V_{CC} = 2.7$ V	$T_A = –55°C$ to 125°C, SN54LVC04A			5.5	
				$T_A = 25°C$, SN74LVC04A	1	3	5.3	
				$T_A = –40°C$ to 85°C, SN74LVC04A	1		5.5	
				$T_A = –40°C$ to 125°C, SN74LVC04A	1		7	
			$V_{CC} = 3.3$ V ±0.3 V	$T_A = –55°C$ to 125°C, SN54LVC04A	0.5		4.5	
				$T_A = 25°C$, SN74LVC04A	1	2.5	4.3	
				$T_A = –40°C$ to 85°C, SN74LVC04A	1		4.5	
				$T_A = –40°C$ to 125°C, SN74LVC04A	1		6	
$t_{sk(o)}$	Skew (time), output	$V_{CC} = 3.3$ V ±0.3 V, SN74LVC04A only	$T_A = –40°C$ to 85°C				1	ns
			$T_A = –40°C$ to 125°C				1.5	

6.9 Operating Characteristics

$T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	f = 10 MHz, $T_A = 25°C$	$V_{CC} = 1.8$ V		6		pF
			$V_{CC} = 2.5$ V		7		
			$V_{CC} = 3.3$ V		8		

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6.10 Typical Characteristics

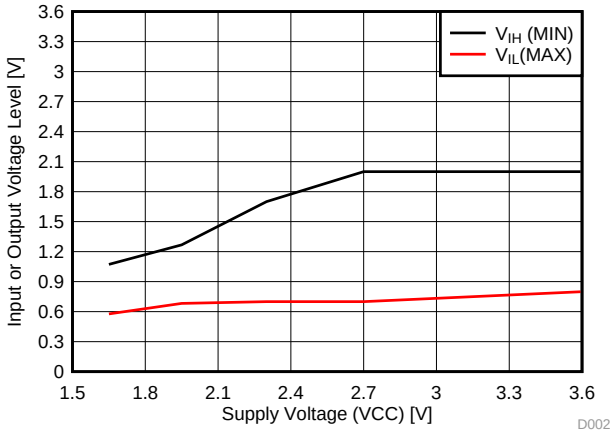
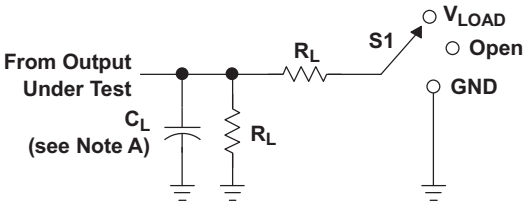


Figure 1. V_{IH} Minimum and V_{IL} Maximum vs Supply Voltage

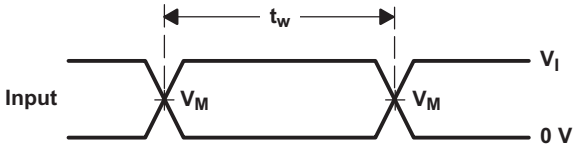
7 Parameter Measurement Information



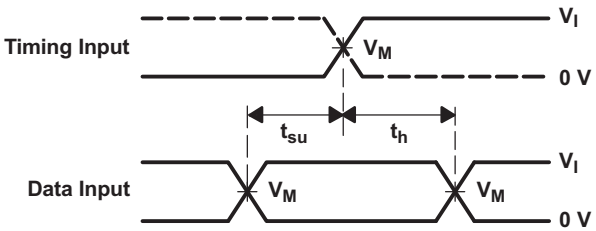
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

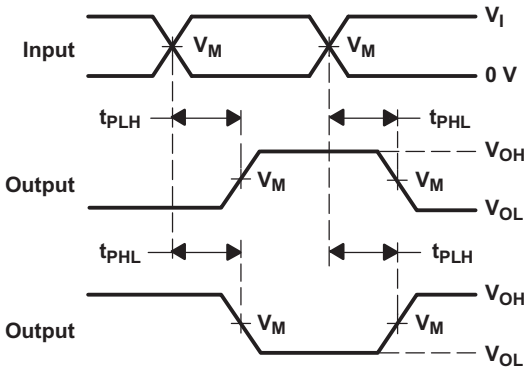
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



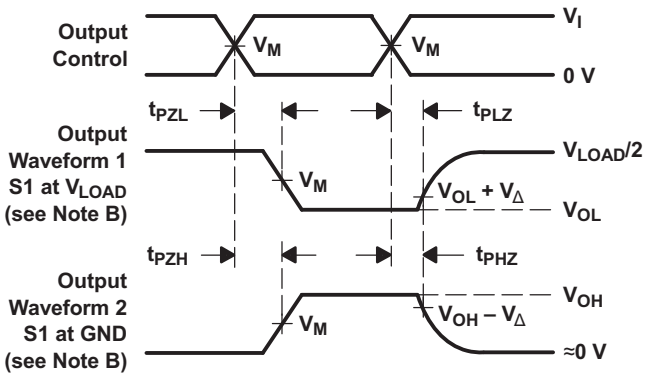
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

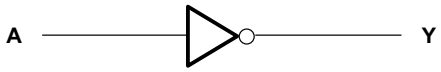
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8 Detailed Description

8.1 Overview

These hex inverters are designed for 1.65-V to 3.6-V V_{CC} operation. The SN74LVC04A devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. These devices are fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The inputs are high impedance when V_{CC} = 0V.

8.2 Functional Block Diagram



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8.3 Feature Description

Wide operating voltage range from 1.65 V to 3.6 V. Allows down-voltage translation with inputs accept voltages to 3.6 V. I_{OFF} feature supports live insertion, partial power down mode, and back drive protection.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4LVC04A.

Table 1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

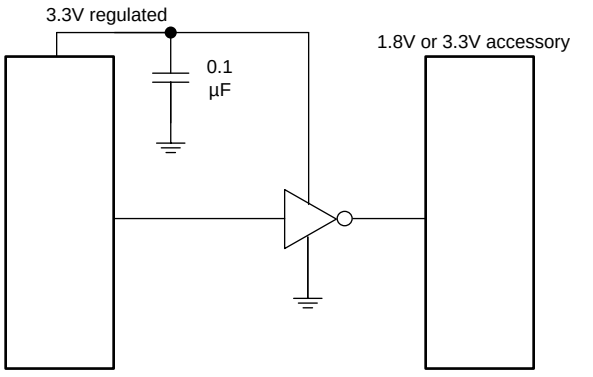
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SN74LVC04A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 3.6 V at any valid V_{CC} making it Ideal for down translation.

9.2 Typical Application



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Figure 3. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention, because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

Recommended Input Conditions:

- For rise time and fall time specifications, see $\Delta t/\Delta V$ in *Recommended Operating Conditions*.
- For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
- Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}.

Recommend Output Conditions:

- Load currents must not exceed 25 mA per output and 50 mA total for the part.
- Outputs must not be pulled above V_{CC}.

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Typical Application (continued)

9.2.3 Application Curves

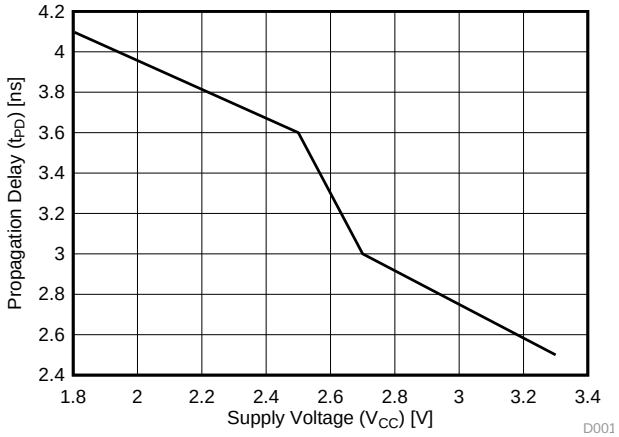


Figure 4. Typical Application Curve

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 5 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

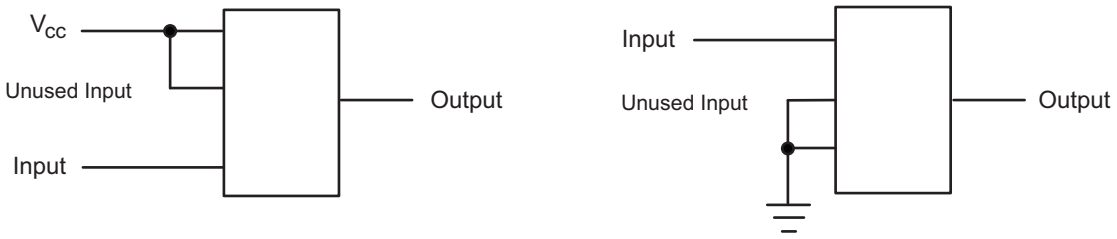


Figure 5. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC04A	Click here	Click here	Click here	Click here	Click here
SN74LVC04A	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9760501Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760501Q2A SNJ54LVC 04AFK	Samples
5962-9760501QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760501QC A SNJ54LVC04AJ	Samples
5962-9760501QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760501QD A SNJ54LVC04AW	Samples
SN74LVC04AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC04A	Samples
SN74LVC04ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04ADBRG4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LVC04A	Samples
SN74LVC04ADRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LVC04A	Samples
SN74LVC04ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC04A	Samples
SN74LVC04ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC04A	Samples
SN74LVC04ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC04A	Samples
SN74LVC04APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC04APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04APWTG4	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC04A	Samples
SN74LVC04ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC04A	Samples
SN74LVC04ARGYRG4	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC04A	Samples
SNJ54LVC04AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760501Q2A SNJ54LVC 04AFK	Samples
SNJ54LVC04AJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760501QC A SNJ54LVC04AJ	Samples
SNJ54LVC04AW	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9760501QD A SNJ54LVC04AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC04A, SN74LVC04A :

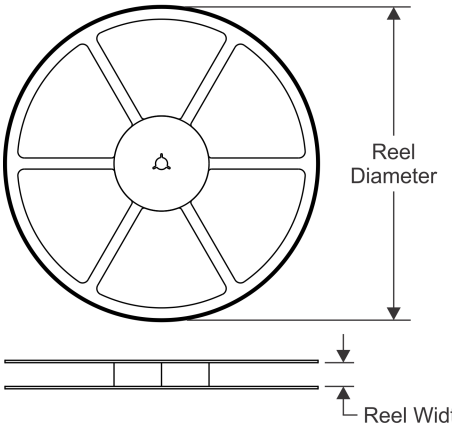
- Catalog : SN74LVC04A
- Automotive : SN74LVC04A-Q1, SN74LVC04A-Q1
- Enhanced Product : SN74LVC04A-EP, SN74LVC04A-EP
- Military : SN54LVC04A

NOTE: Qualified Version Definitions:

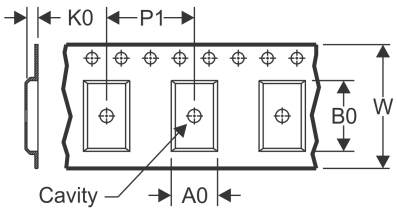
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

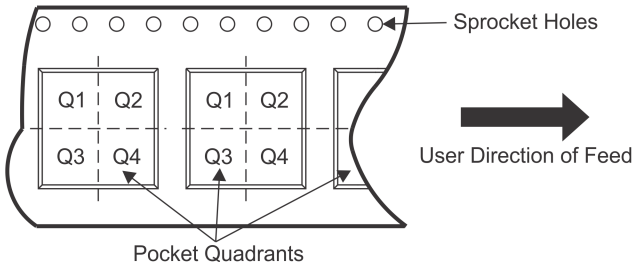


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

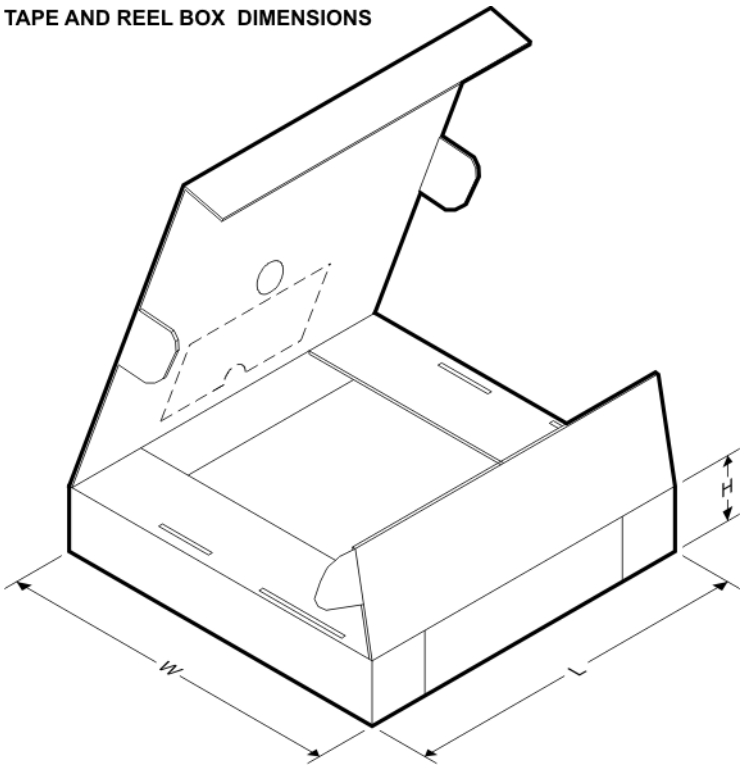
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC04ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC04ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC04ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74LVC04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC04ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74LVC04ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC04ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC04ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC04ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC04APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC04APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC04APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC04ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

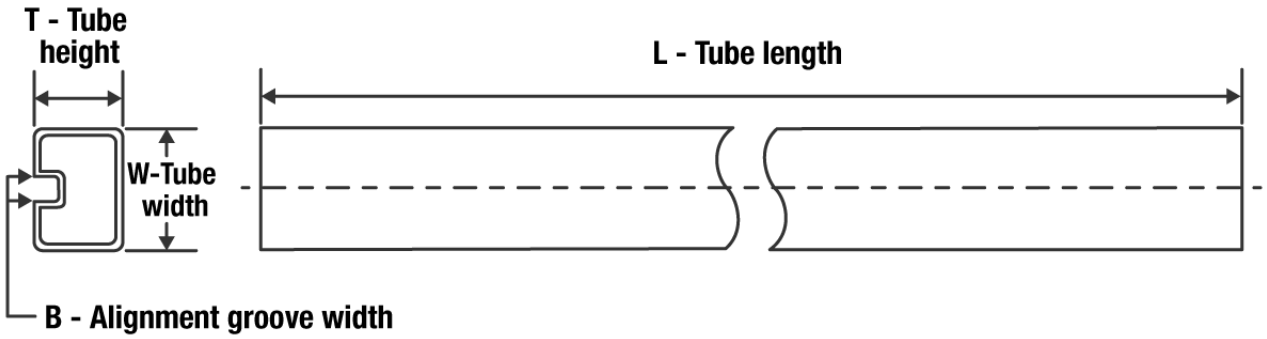
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC04ADBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74LVC04ADGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74LVC04ADR	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC04ADR	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVC04ADR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LVC04ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC04ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVC04ADRG4	SOIC	D	14	2500	853.0	449.0	35.0
SN74LVC04ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC04ANSR	SO	NS	14	2000	853.0	449.0	35.0
SN74LVC04APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC04APWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74LVC04APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC04APWRG4	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74LVC04APWT	TSSOP	PW	14	250	853.0	449.0	35.0
SN74LVC04ARGYR	VQFN	RGY	14	3000	853.0	449.0	35.0

TUBE

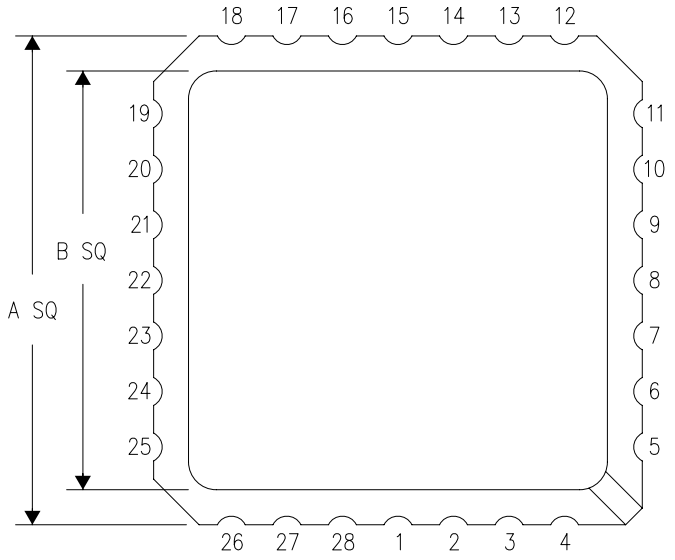


*All dimensions are nominal

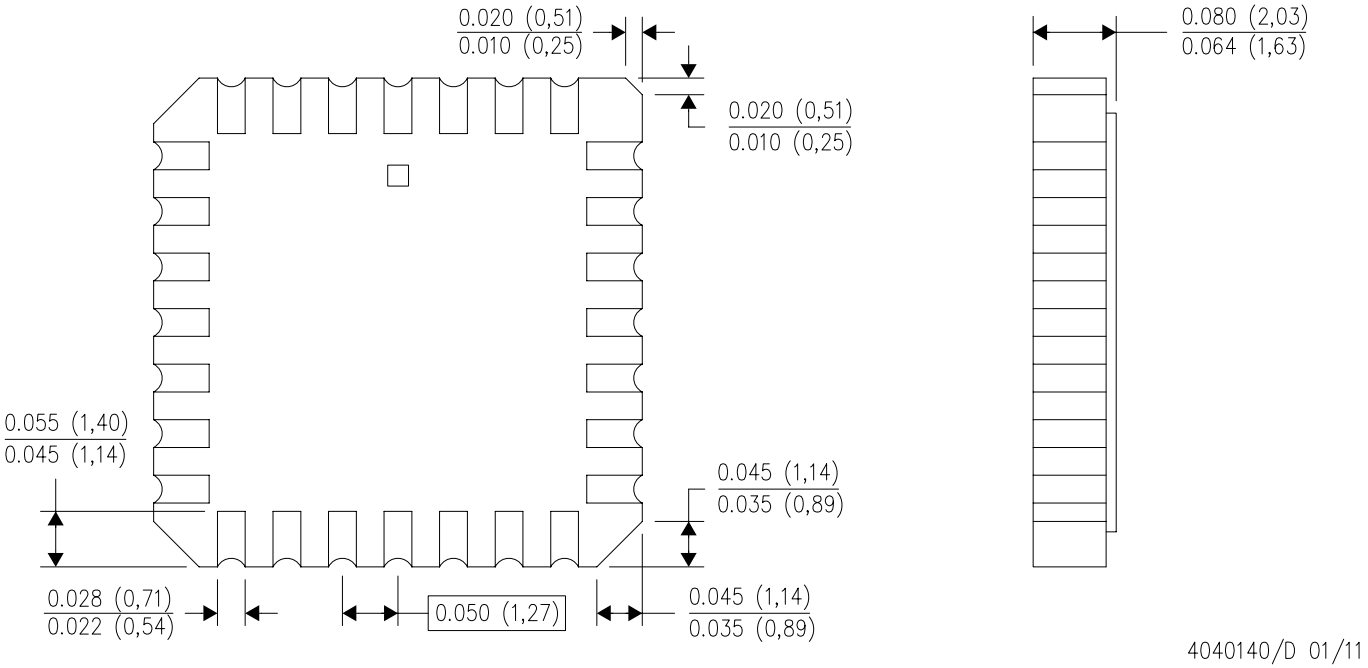
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9760501Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74LVC04AD	D	SOIC	14	50	507	8	3940	4.32
SN74LVC04AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC04APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC04APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC04APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC04AFK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



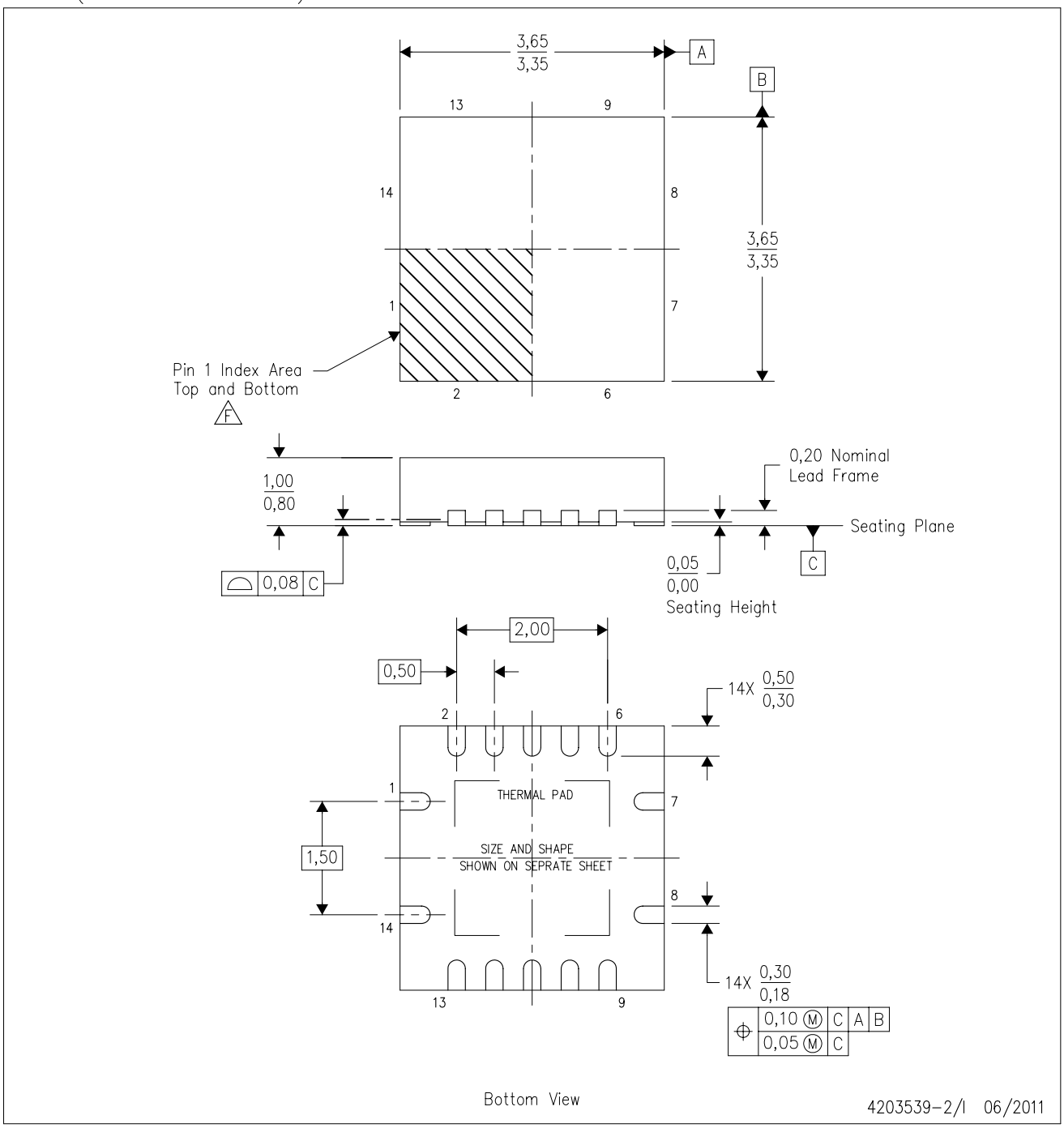
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

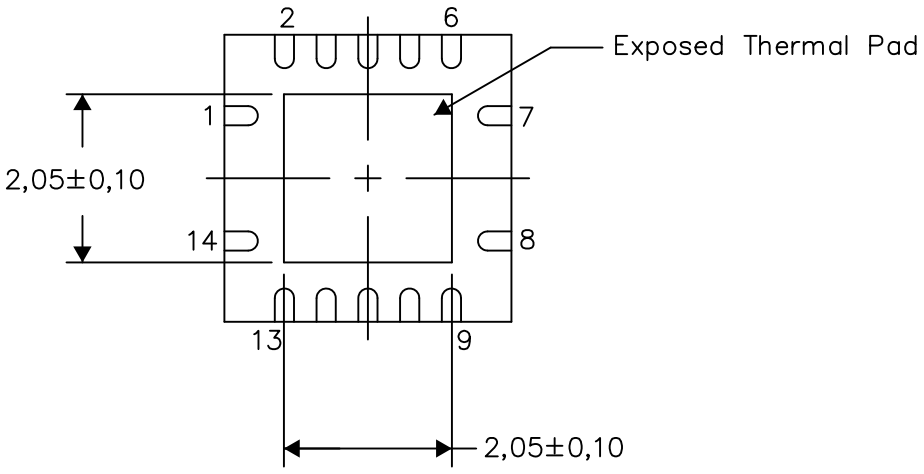
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



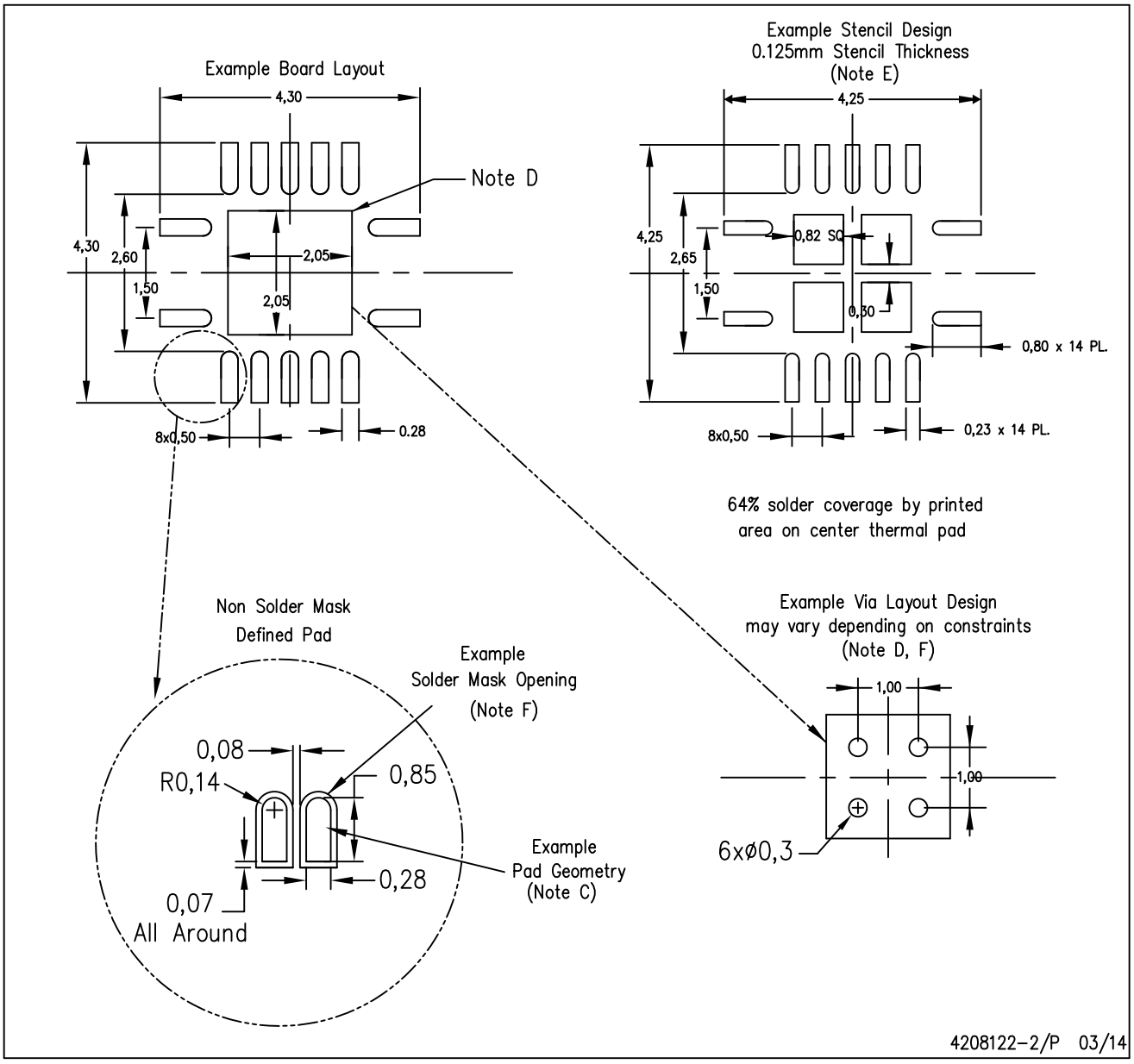
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

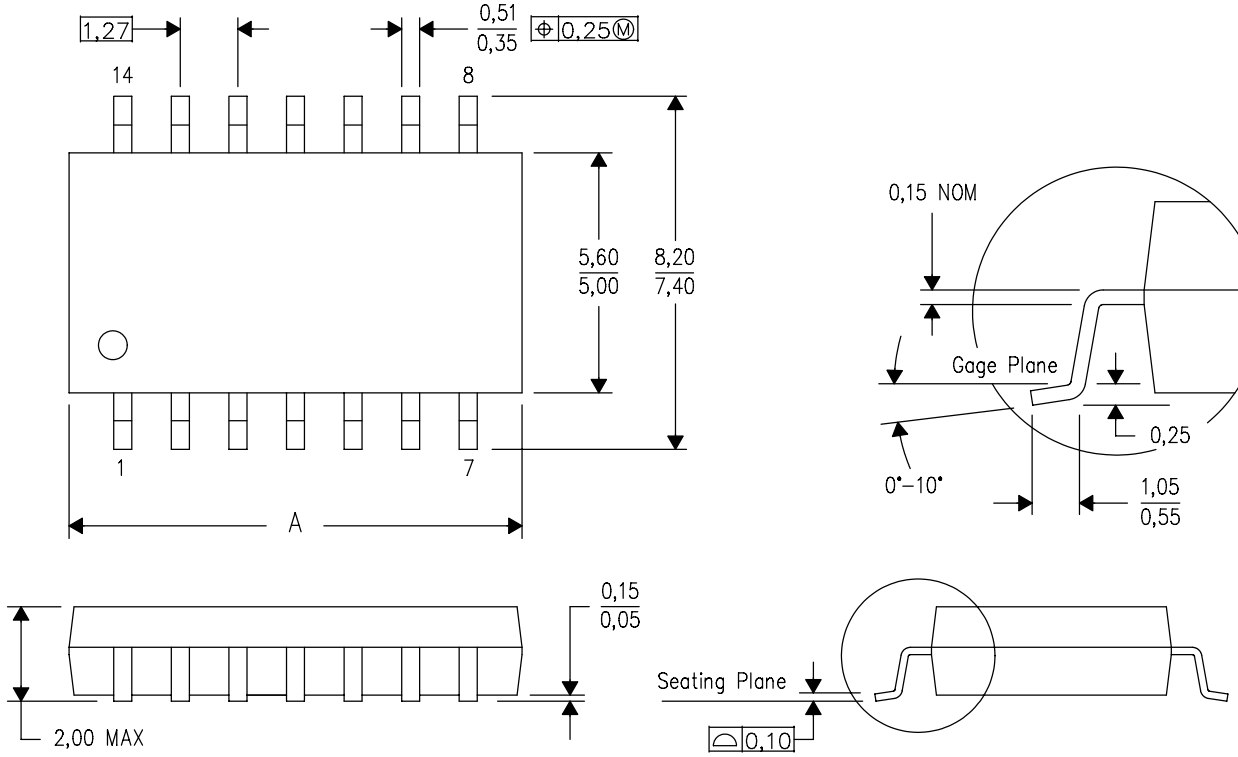


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

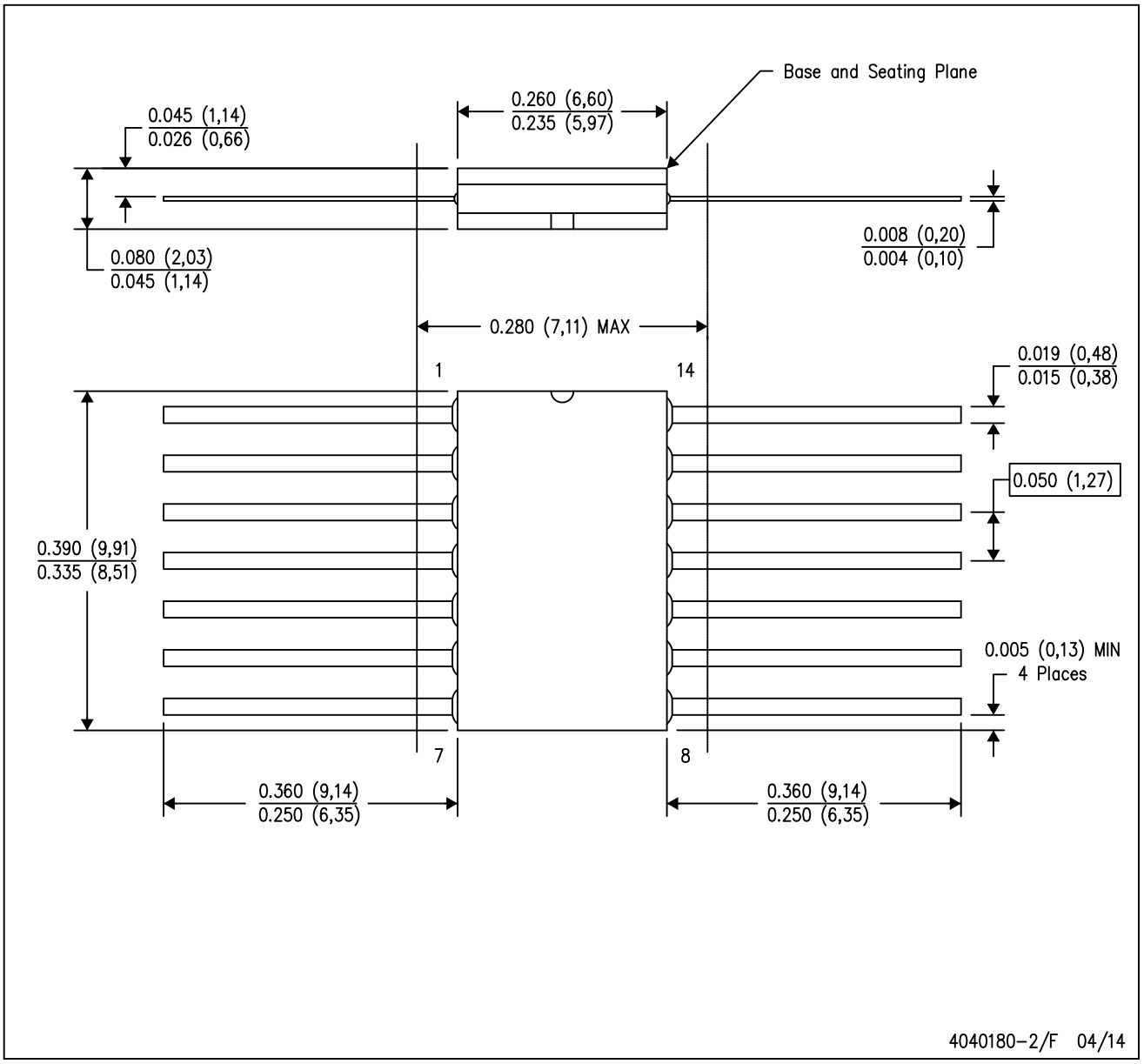


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

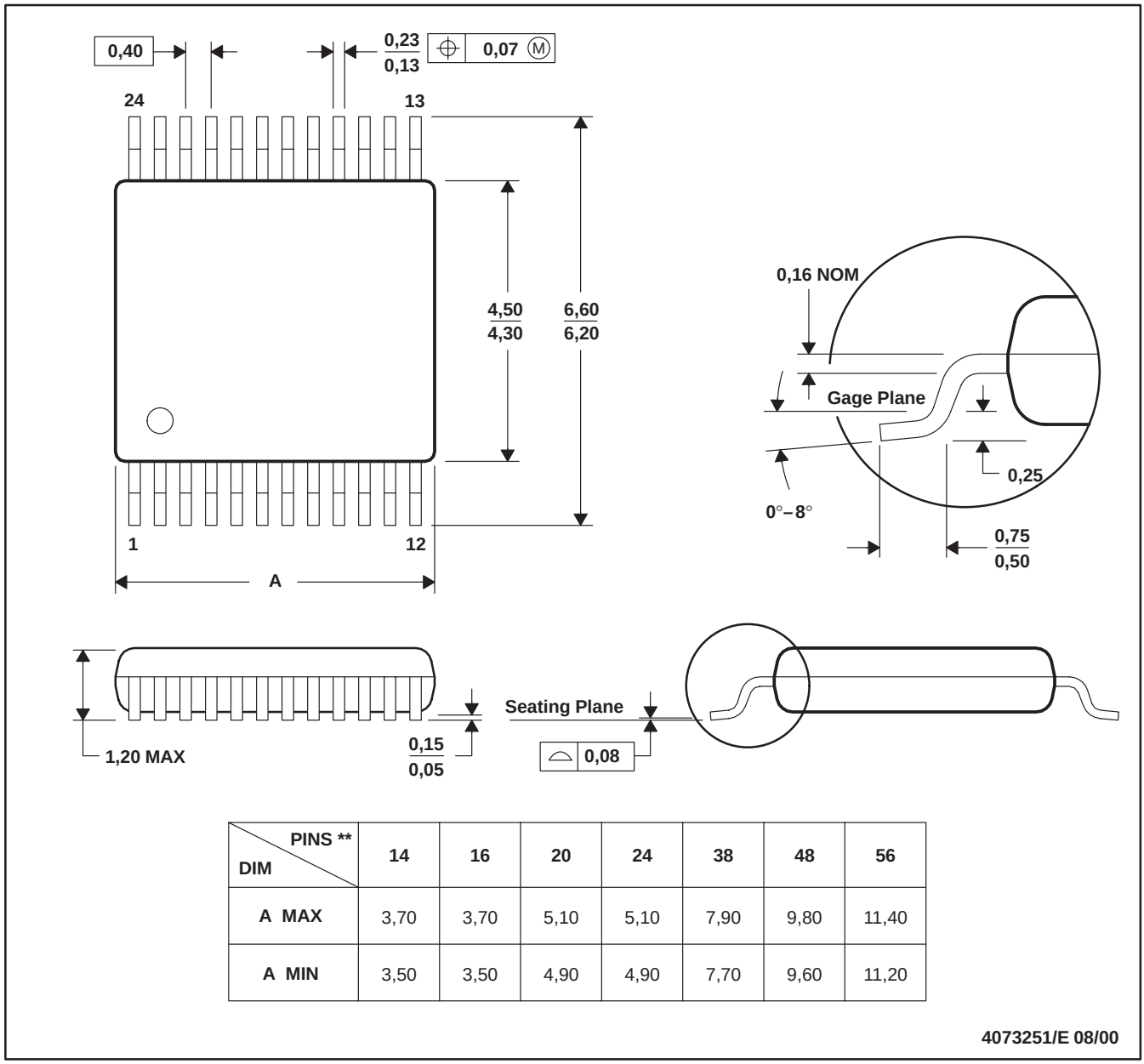
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

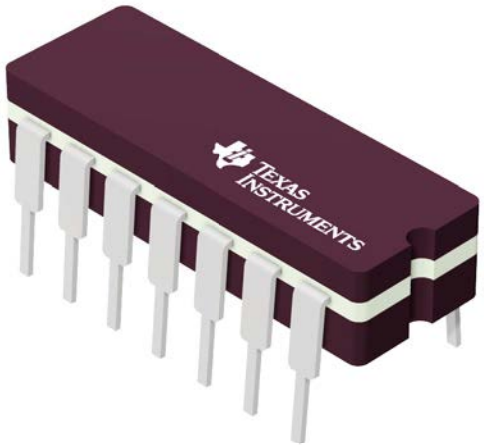
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

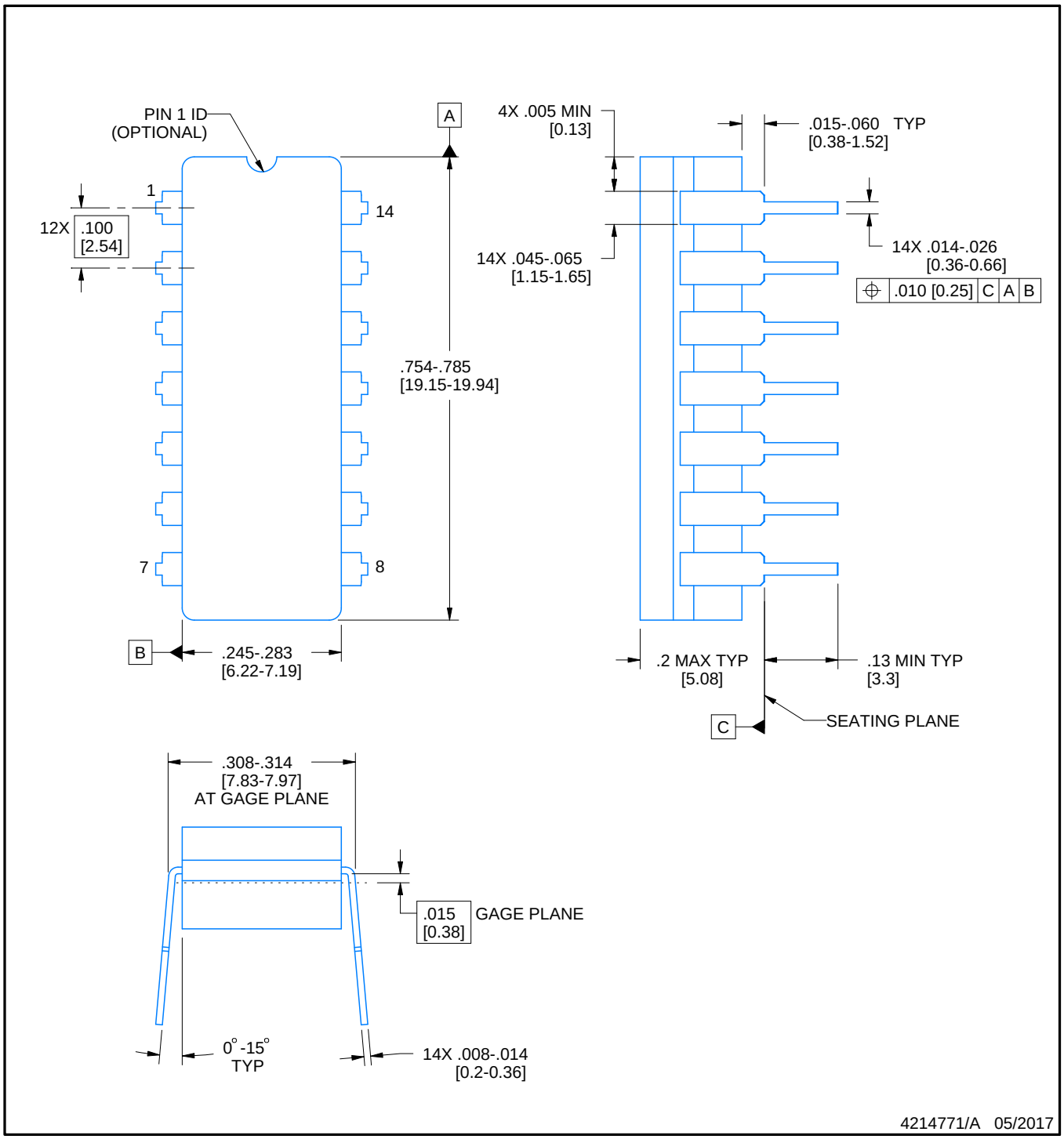


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

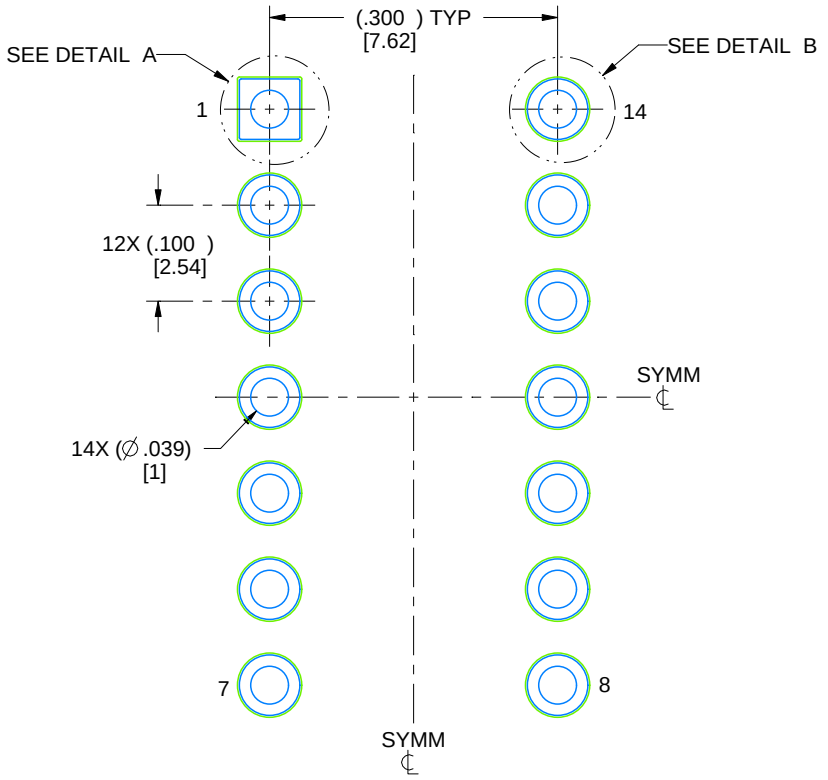
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

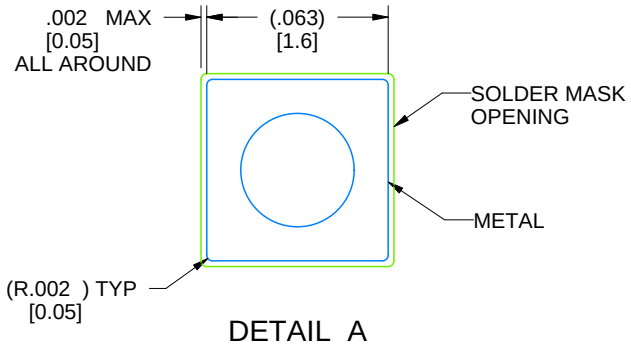
J0014A

CDIP - 5.08 mm max height

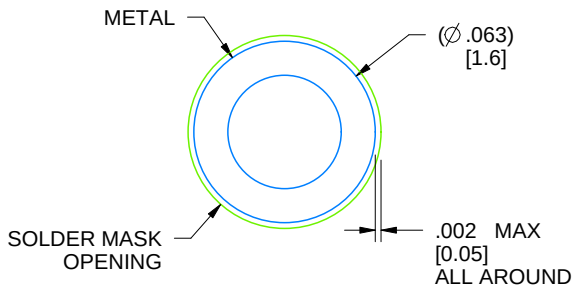
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



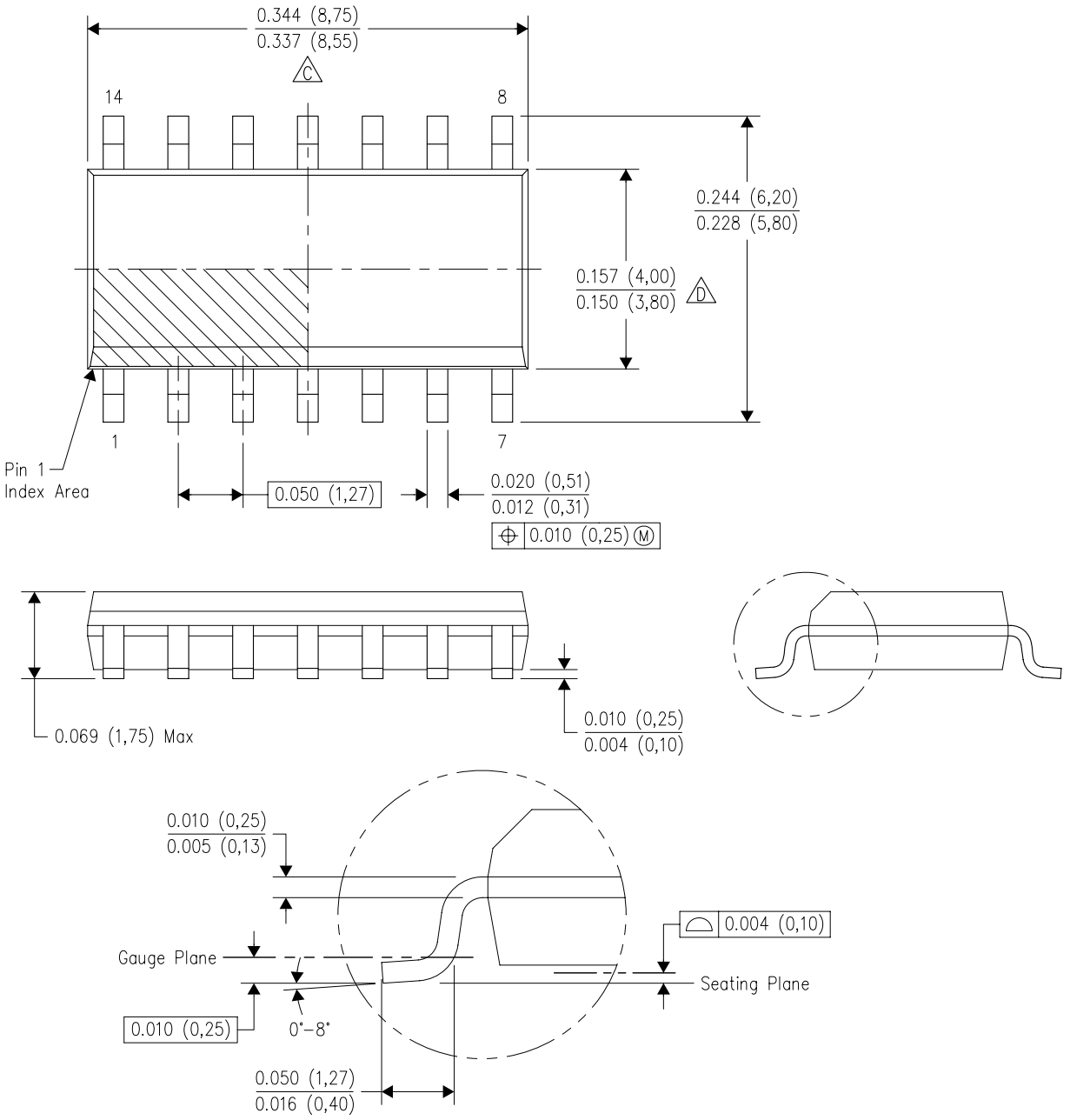
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

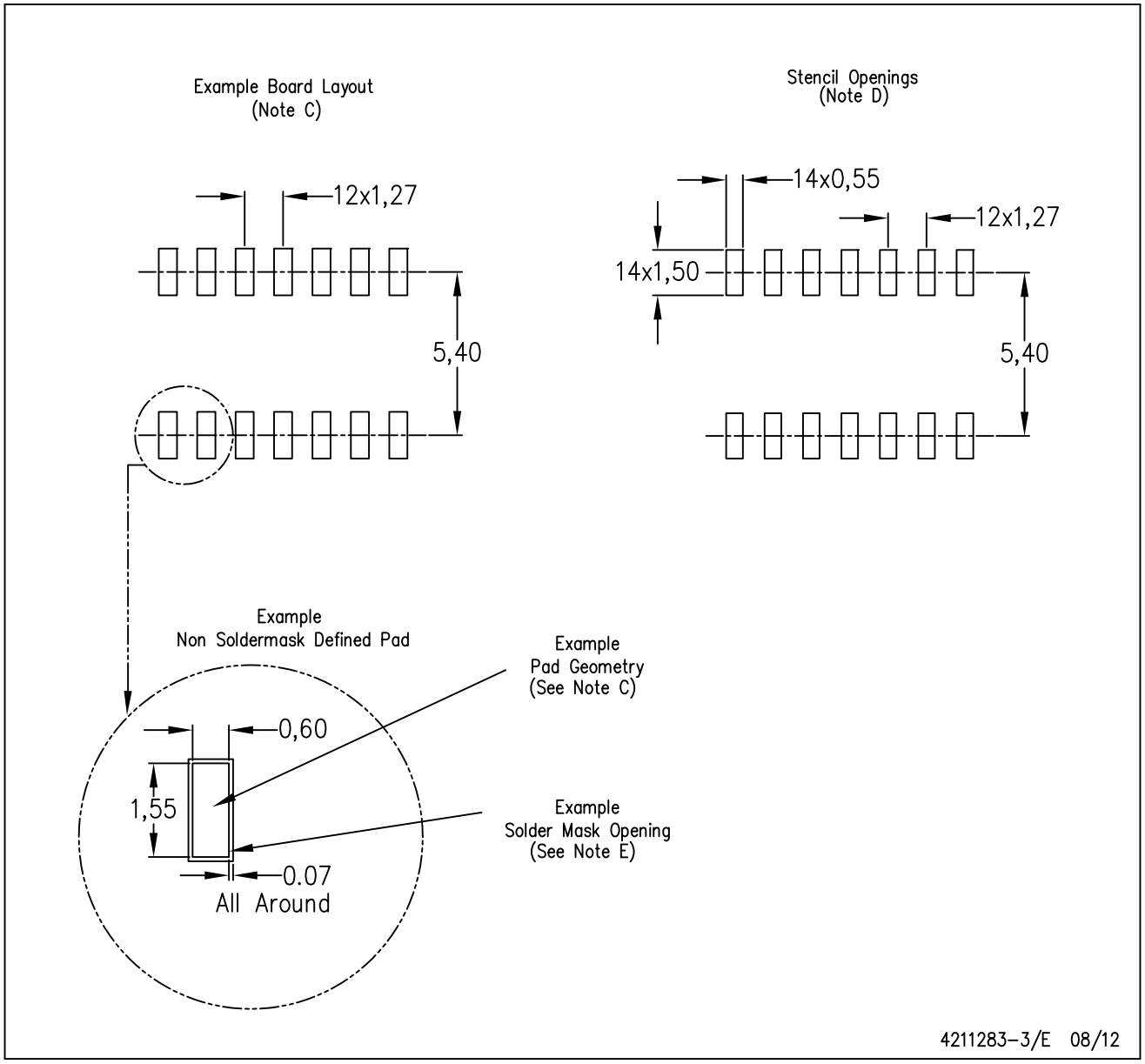
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

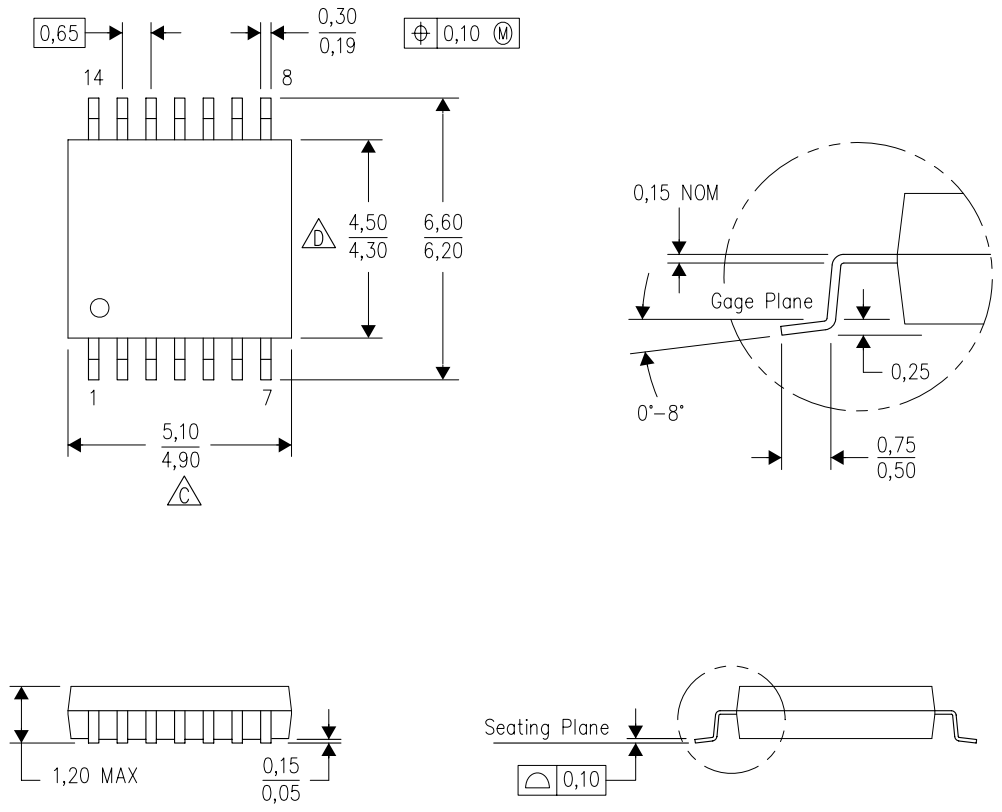
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

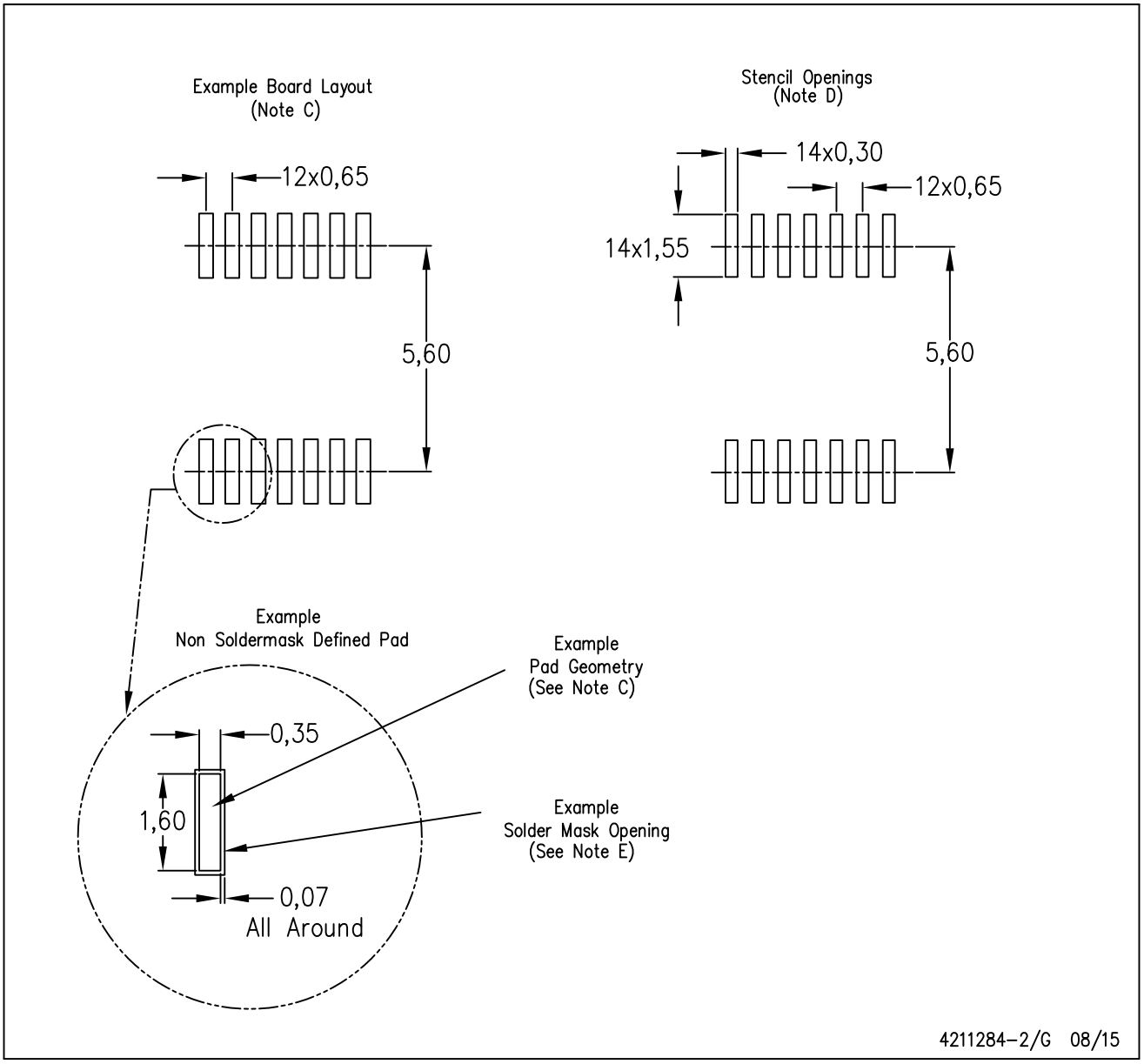
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

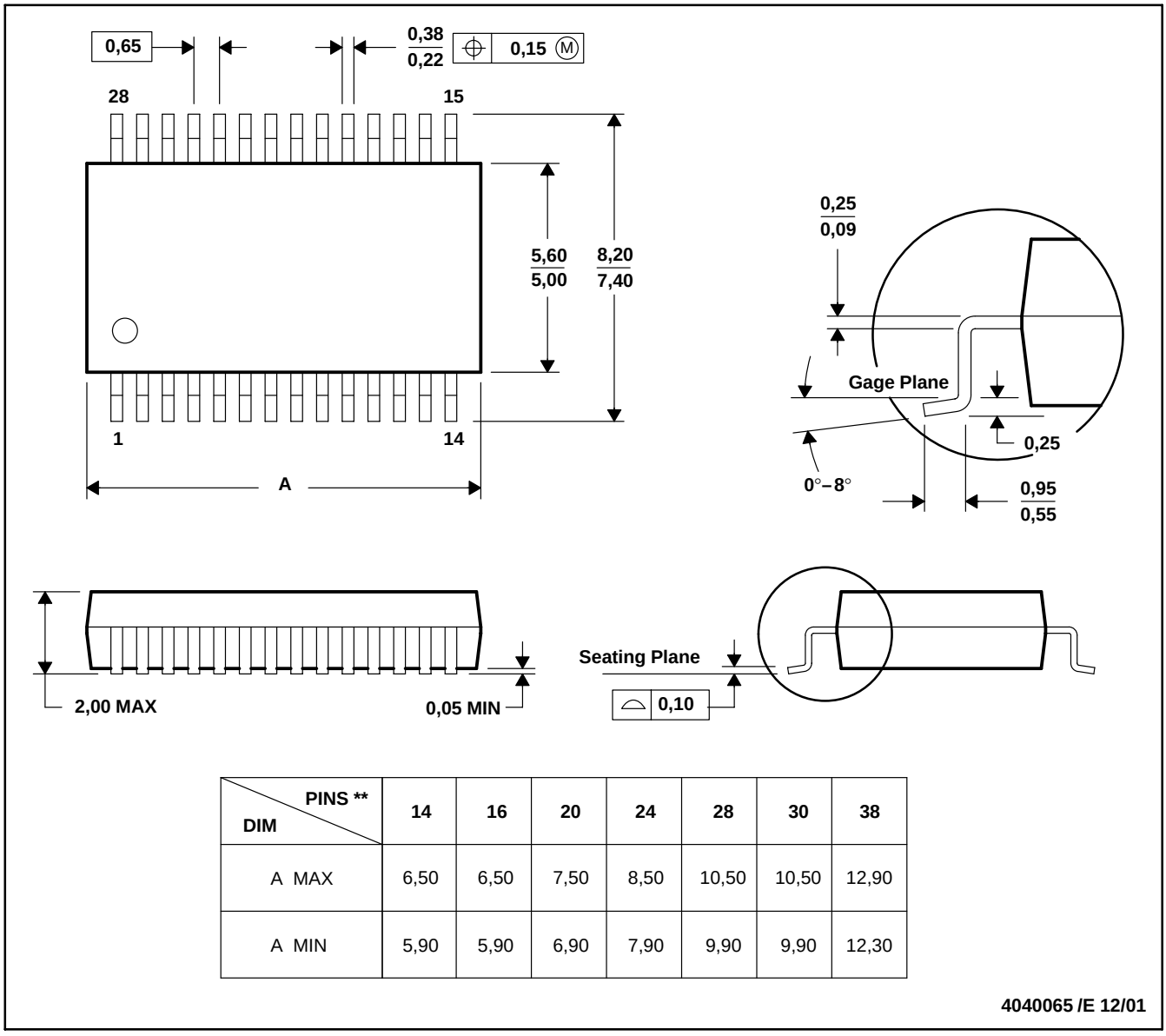


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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