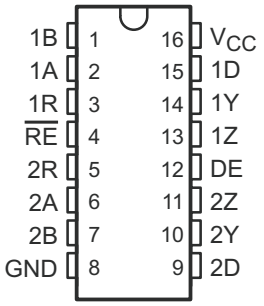
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

Check for Samples: SN65C1167 SN75C1167 SN65C1168 SN75C1168

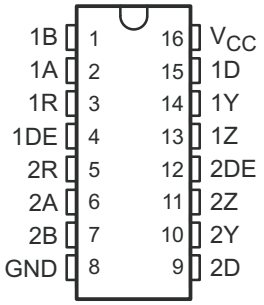
FEATURES

- **Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11**
- **BiCMOS Process Technology**
- **Low Supply-Current Requirements: 9 mA Max**
- **Low Pulse Skew**
- **Receiver Input Impedance . . . 17 kΩ Typ**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Common-Mode Input Voltage Range of −7 V to 7 V**
- **Operate From Single 5-V Power Supply**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Receiver 3-State Outputs Active-Low Enable for SN65C1167 and SN75C1167 Only**
- **Improved Replacements for the MC34050 and MC34051**

SN65C1167 . . . DB OR NS PACKAGE
SN75C1167 . . . DB, N, OR NS PACKAGE
(TOP VIEW)



SN65C1168 . . . N, NS, OR PW PACKAGE
SN75C1168 . . . DB, N, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN75C1167N	SN75C1167N
			SN75C1168N	SN75C1168N
	SOP – NS	Tape and reel	SN75C1167NSR	75C1167
			SN75C1168NSR	75C1168
	SSOP – DB	Tape and reel	SN75C1167DBR	CA1167
			SN75C1168DBR	CA1168
	TSSOP – PW	Tube	SN75C1168PW	CA1168
		Tape and reel	SN75C1168PWR	
–40°C to 85°C	PDIP – N	Tube	SN65C1168N	SN65C1168N
	SOP – NS	Tape and reel	SN65C1167NSR	65C1167
			SN65C1168NSR	65C1168
	SSOP – DB	Tape and reel	SN65C1167DBR	CB1167
	TSSOP – PW	Tube	SN65C1168PW	CB1168
		Tape and reel	SN65C1168PWR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/sc/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLES

Each Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

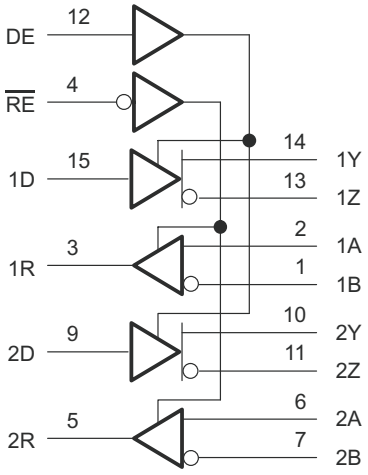
Each Receiver(1)

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

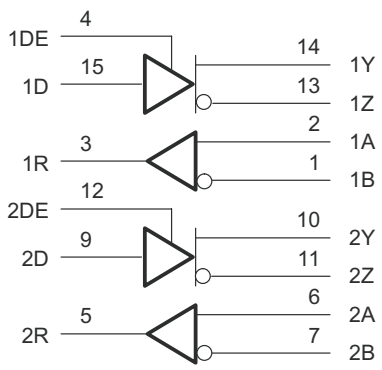
(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)

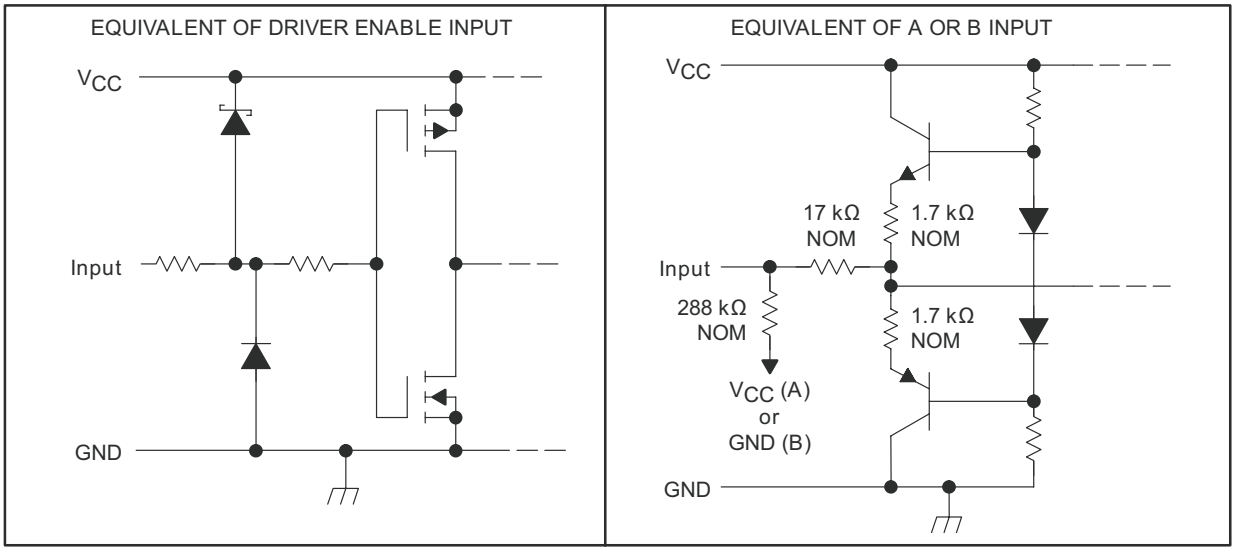
SN65C1167/SN75C1167



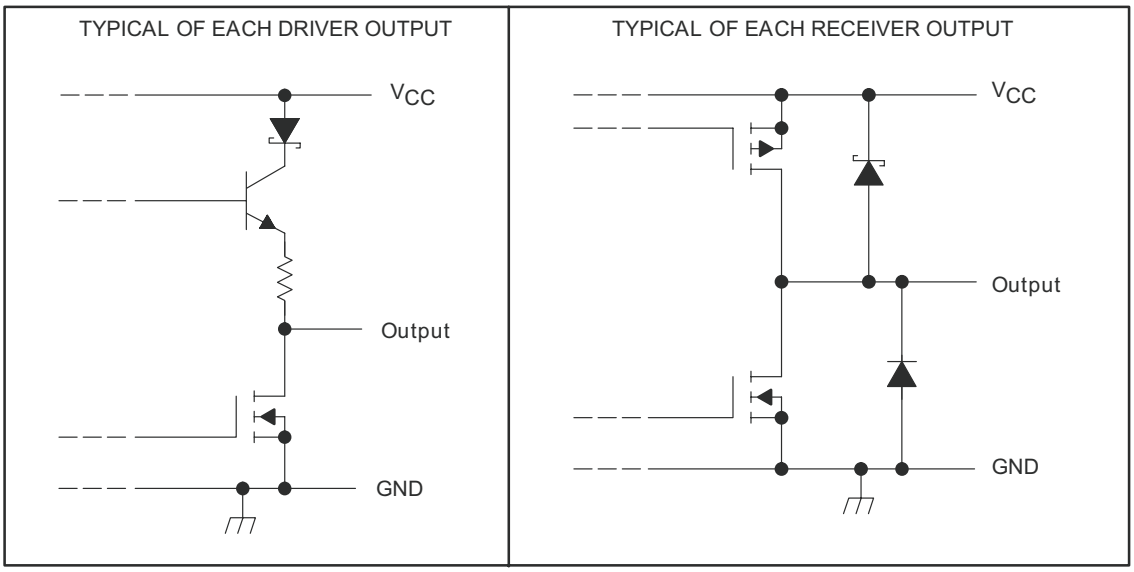
SN65C1168, SN75C1168



SCHEMATIC OF INPUTS



SCHEMATIC OF OUTPUTS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	7	V
V_I	Input voltage range	Driver	–0.5	V_{CC} + 0.5	V
		A or B, Receiver	–11	14	
V_{ID}	Differential input voltage range(3)	Receiver	–14	14	V
V_O	Output voltage range	Driver	–0.5	7	V
I_{IK} or I_{OK}	Clamp current range	Driver		±20	mA
I_O	Output current range	Driver		±150	mA
		Receiver		±25	
I_{CC}	Supply current			200	mA
	GND current			−200	mA
T_J	Operating virtual junction temperature			150	°C
θ_{JA}	Package thermal impedance(4) (5)	DB package		82	°C/W
		N package		67	
		NS package		64	
		PW package		108	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages values except differential input voltage are with respect to the network GND.
(3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
(4) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IC}	Common-mode input voltage(1)	Receiver				±7	V
V_{ID}	Differential input voltage	Receiver				±7	V
V_{IH}	High-level input voltage	Except A, B		2			V
V_{IL}	Low-level input voltage	Except A, B				0.8	V
I_{OH}	High-level output current	Receiver				−6	mA
		Driver				−20	
I_{OL}	Low-level output current	Receiver				6	mA
		Driver				20	
T_A	Operating free-air temperature		SN75C1167, SN75C1168	0		70	°C
			SN65C1167, SN65C1168	–40		85	

(1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −20 mA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0 mA		2		6	V
$\|V_{OD2}\|$	Differential output voltage [1]	R_L = 100 Ω, See Figure 1		2	3.1		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage					±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0 V	V_O = 6 V			100	µA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	V_O = 2.5 V				20	µA
		V_O = 5 V				−20	
I_{IH}	High-level input current	V_I = V_{CC} or V_{IH}				1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}				−1	µA
I_{OS}	Short-circuit output current[3]	V_O = V_{CC} or GND,		−30		−150	mA
I_{CC}	Supply current (total package)[4]	No load, Enabled	V_I = V_{CC} or GND		4	6	mA
			V_I = 2.4 or 0.5 V		5	3	
C_i	Input capacitance				6		pF

(1) Refer to TIA/EIA-422-B for exact conditions.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, See Figure 2		7	12	ns
t_{PLH}	Propagation delay time, low- to high-level output			7	12	ns
$t_{sk(p)}$	Pulse skew			0.5	4	ns
t_r	Rise time	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, SeeFigure 3		5	10	ns
t_f	Fall time			5	10	ns
t_{PZH}	Output enable time to high level	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level			10	19	ns
t_{PHZ}	Output disable time from low level	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, See Figure 4		7	16	ns
t_{PLZ}	Output disable time from high level			7	16	ns

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

RECEIVER SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input				−0.2(2)			V
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	SN75C1167	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −6 mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 6 mA		0.1	0.3	V
I_{OZ}	High-impedance-state output current	SN75C1167	VO = VCC or GND			±0.5	±5	µA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = −10 V			−2.5	
I_I	Enable input current, $\overline{RE}$	SN75C1167	V_I = V_{CC} or GND				±1	µA
r_i	Input resistance		V_{IC} = −7 V to 7 V,	Other input at 0 V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4 V or 0.5 V(3)		5	9	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B for exact conditions.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	ns
t_{TLH}	Transition time, low- to high-level output	V_{IC} = 0 V, See Figure 5		4	9	ns
t_{THL}	Transition time, high- to low-level output			4	9	ns
t_{PZH}	Output enable time to high level	R_L = 1 kW, See Figure 6		13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level			13	22	ns
t_{PLZ}	Output disable time from low level			13	22	ns

(1) Measured per input while the other inputs are at V_{CC} or GND
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

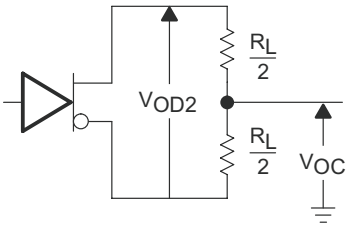


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r = t_f ≤ 6 ns.

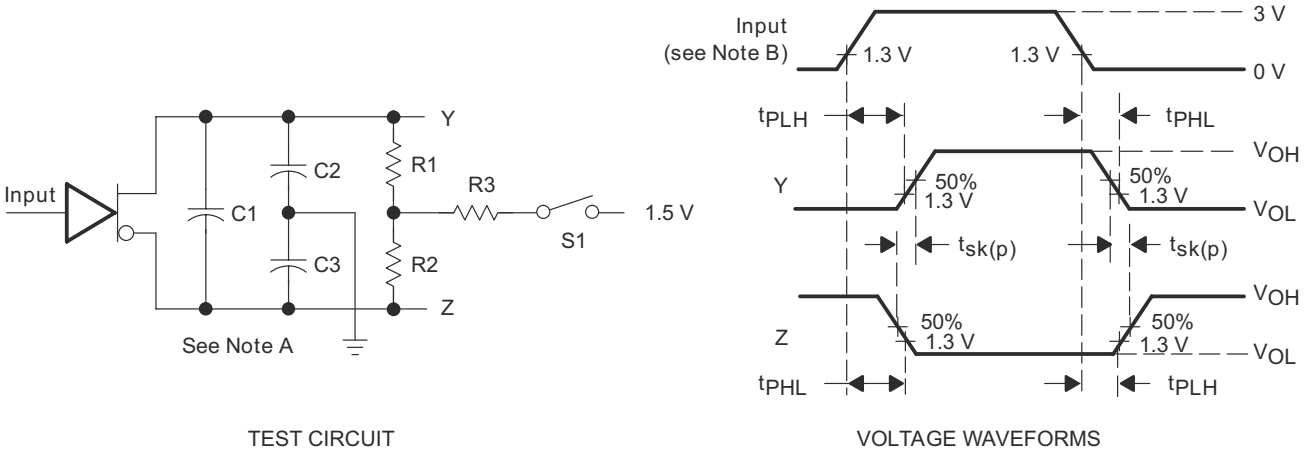


Figure 2. Driver Test Circuit and Voltage Waveforms

C. C1, C2, and C3 include probe and jig capacitance.

D. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r = t_f ≤ 6 ns.

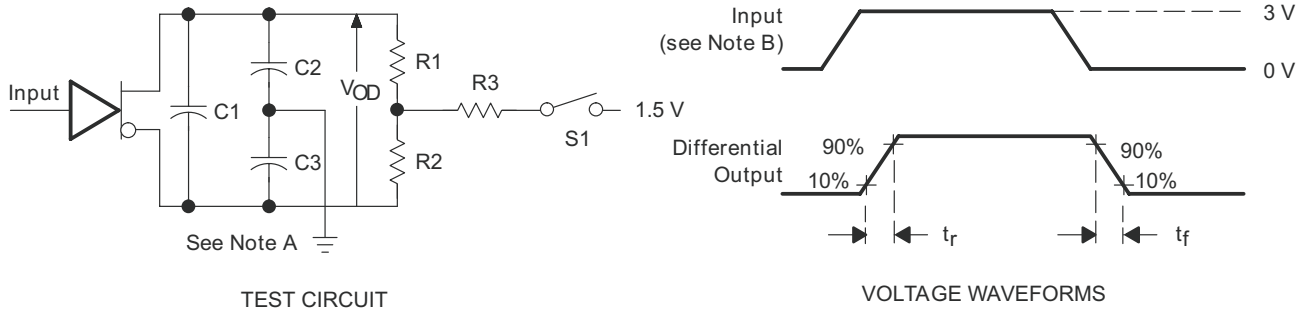
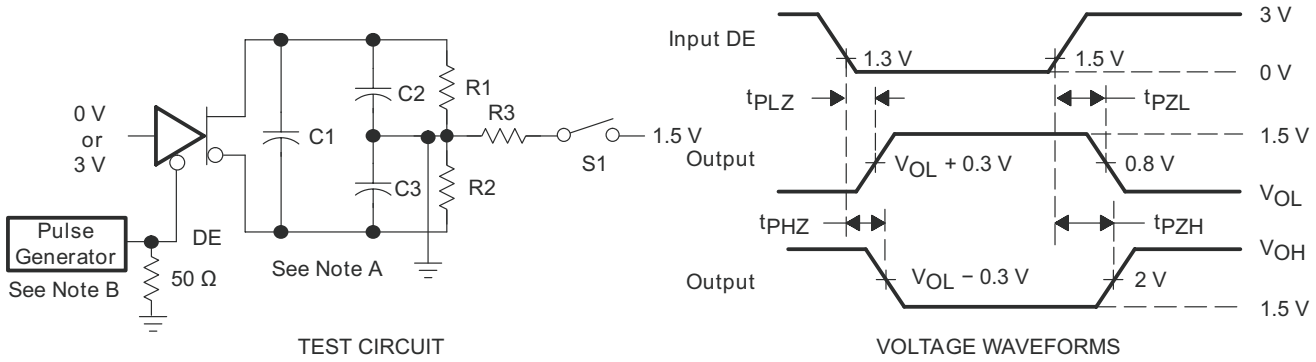


Figure 3. Driver Test Circuit and Voltage Waveforms

E. C1, C2, and C3 include probe and jig capacitance.

F. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r = t_f ≤ 6 ns.

PARAMETER MEASUREMENT INFORMATION (continued)

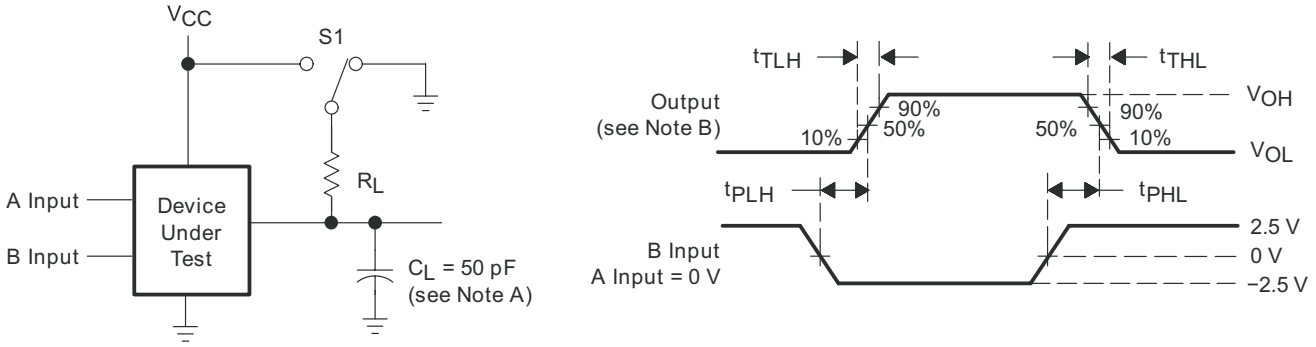


TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms

G. C_L includes probe and jig capacitance.

H. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r = t_f ≤ 6 ns.

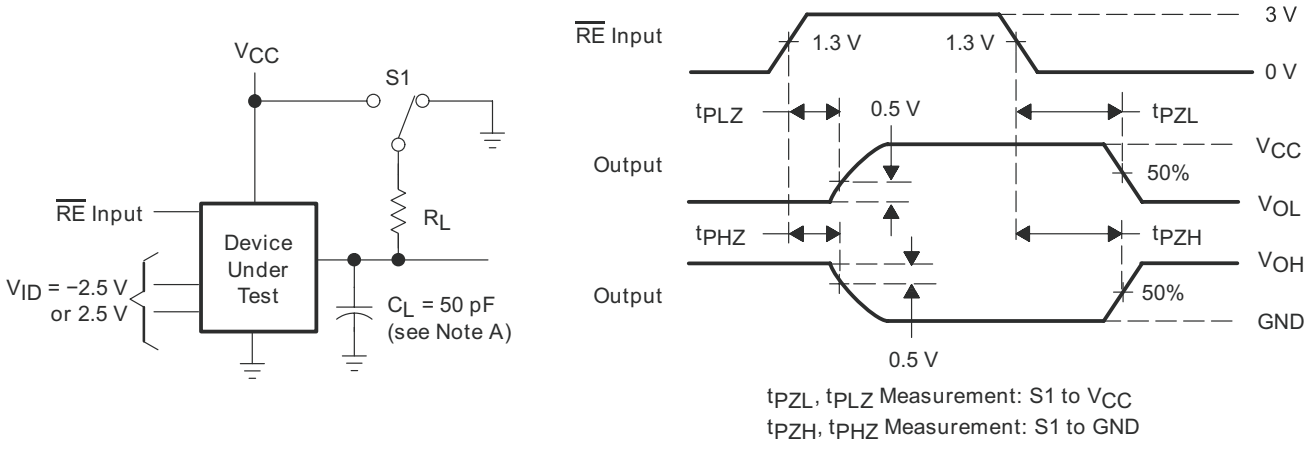


TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. Receiver Test Circuit and Voltage Waveforms

I. C_L includes probe and jig capacitance.

J. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r = t_f ≤ 6 ns.



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 6. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C1167NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1167NSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1168N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65C1168N	Samples
SN65C1168NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	Samples
SN65C1168NSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	Samples
SN65C1168PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN75C1167DB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		CA1167	Samples
SN75C1167DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167	Samples
SN75C1167N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C1167N	Samples
SN75C1167NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	Samples
SN75C1167NSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	Samples
SN75C1168DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C1168N	Samples
SN75C1168NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C1168N	Samples
SN75C1168NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples
SN75C1168NSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples
SN75C1168PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75C1168PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

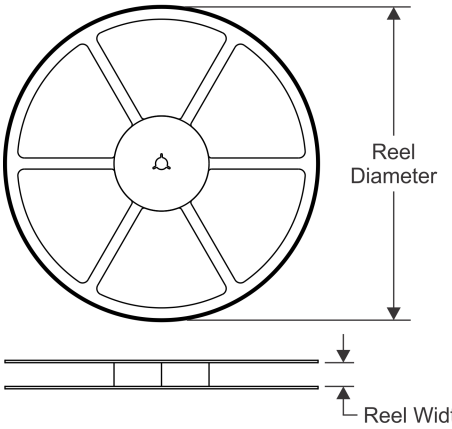
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

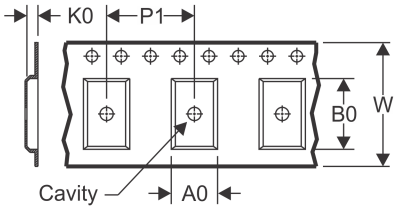
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

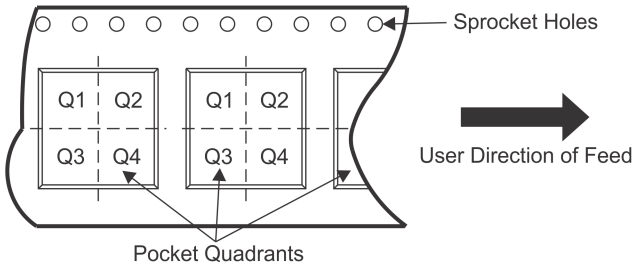


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

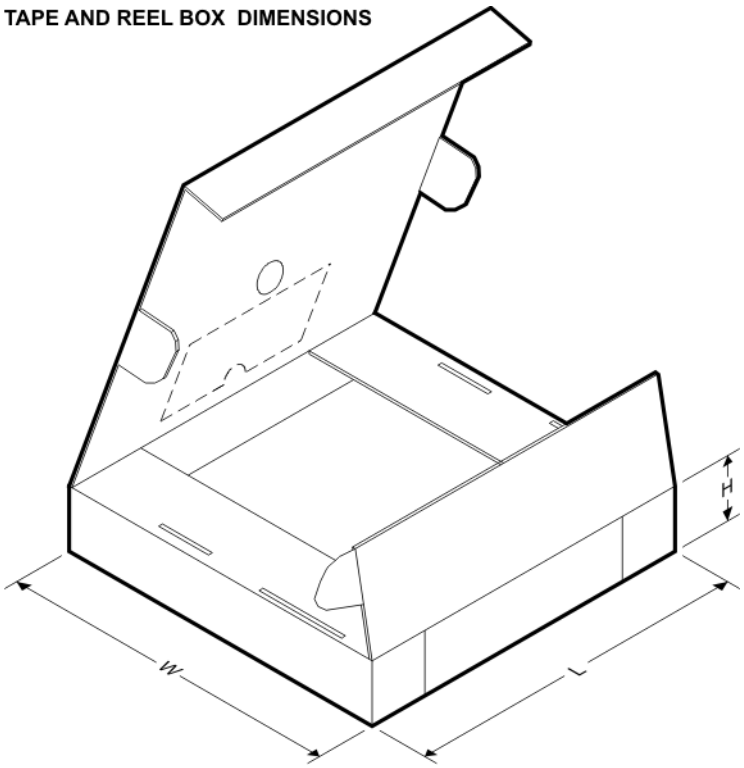
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C1167DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C1167NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C1168DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C1168NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

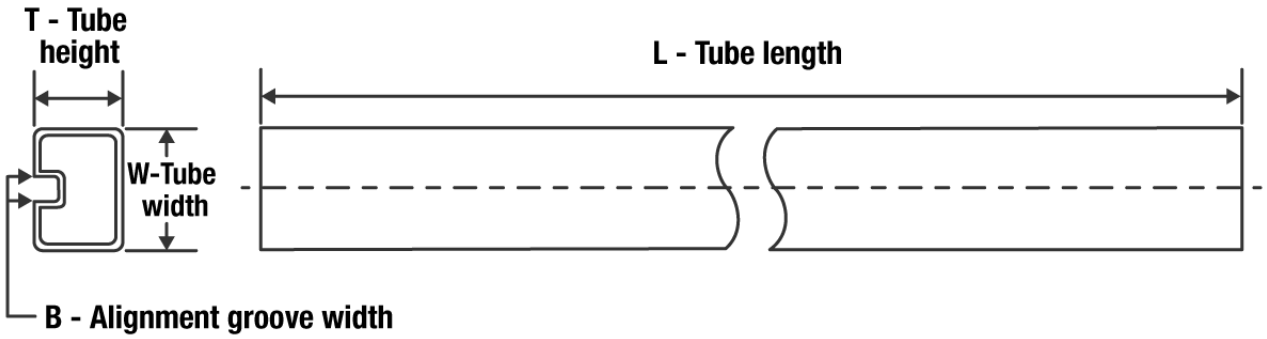
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

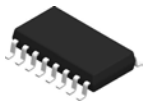
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167NSR	SO	NS	16	2000	853.0	449.0	35.0
SN65C1168NSR	SO	NS	16	2000	853.0	449.0	35.0
SN65C1168PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN75C1167DBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN75C1167NSR	SO	NS	16	2000	853.0	449.0	35.0
SN75C1168DBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN75C1168NSR	SO	NS	16	2000	367.0	367.0	38.0
SN75C1168PWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65C1168N	N	PDIP	16	25	506	13.97	11230	4.32
SN65C1168PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65C1168PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75C1167DB	DB	SSOP	16	80	530	10.5	4000	4.1
SN75C1167N	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168N	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75C1168PWE4	PW	TSSOP	16	90	530	10.2	3600	3.5

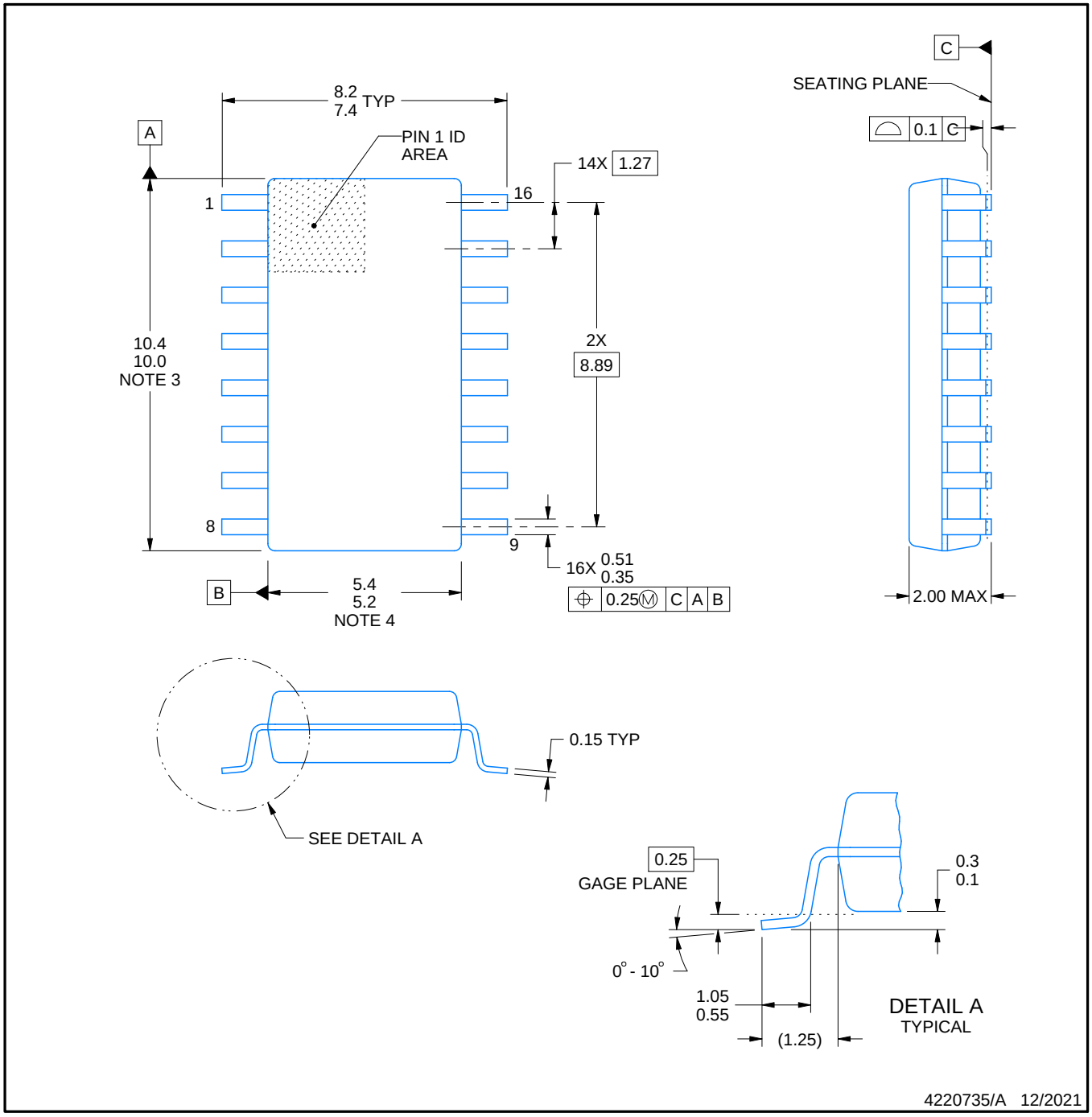


PACKAGE OUTLINE

NS0016A

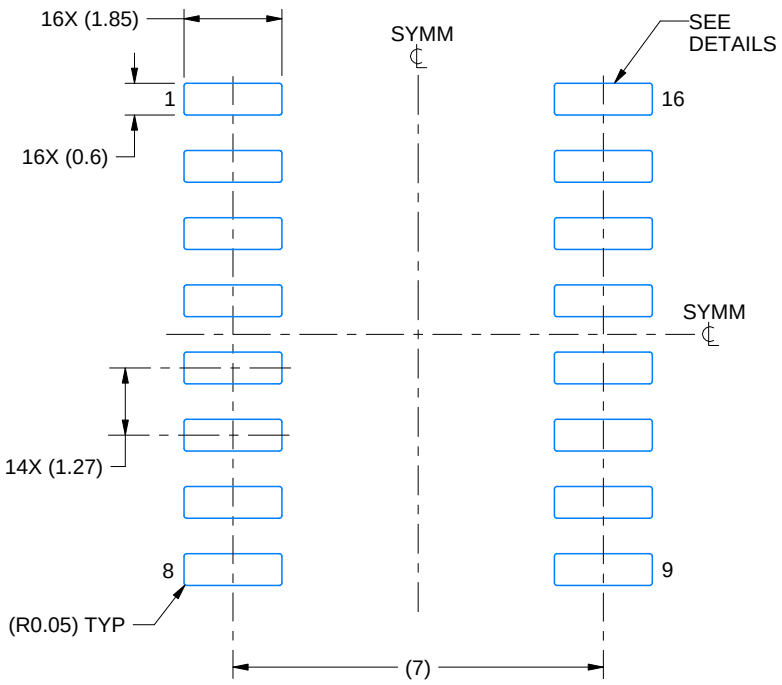
SOP - 2.00 mm max height

SOP

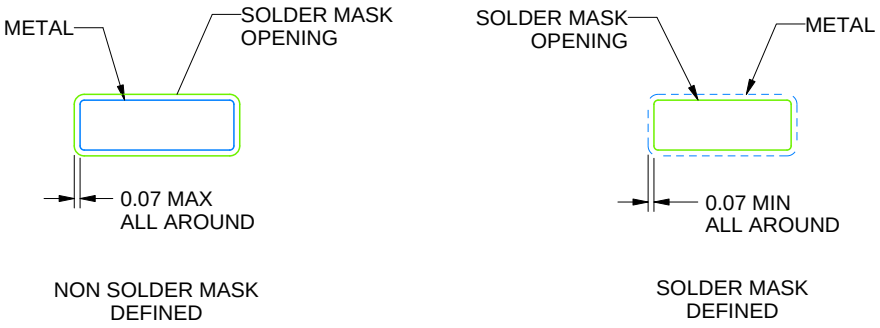


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

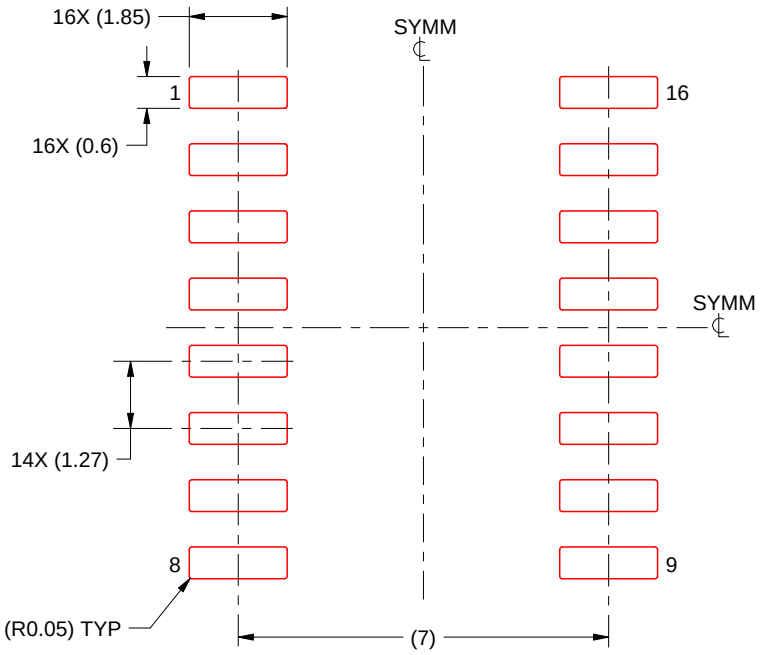
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

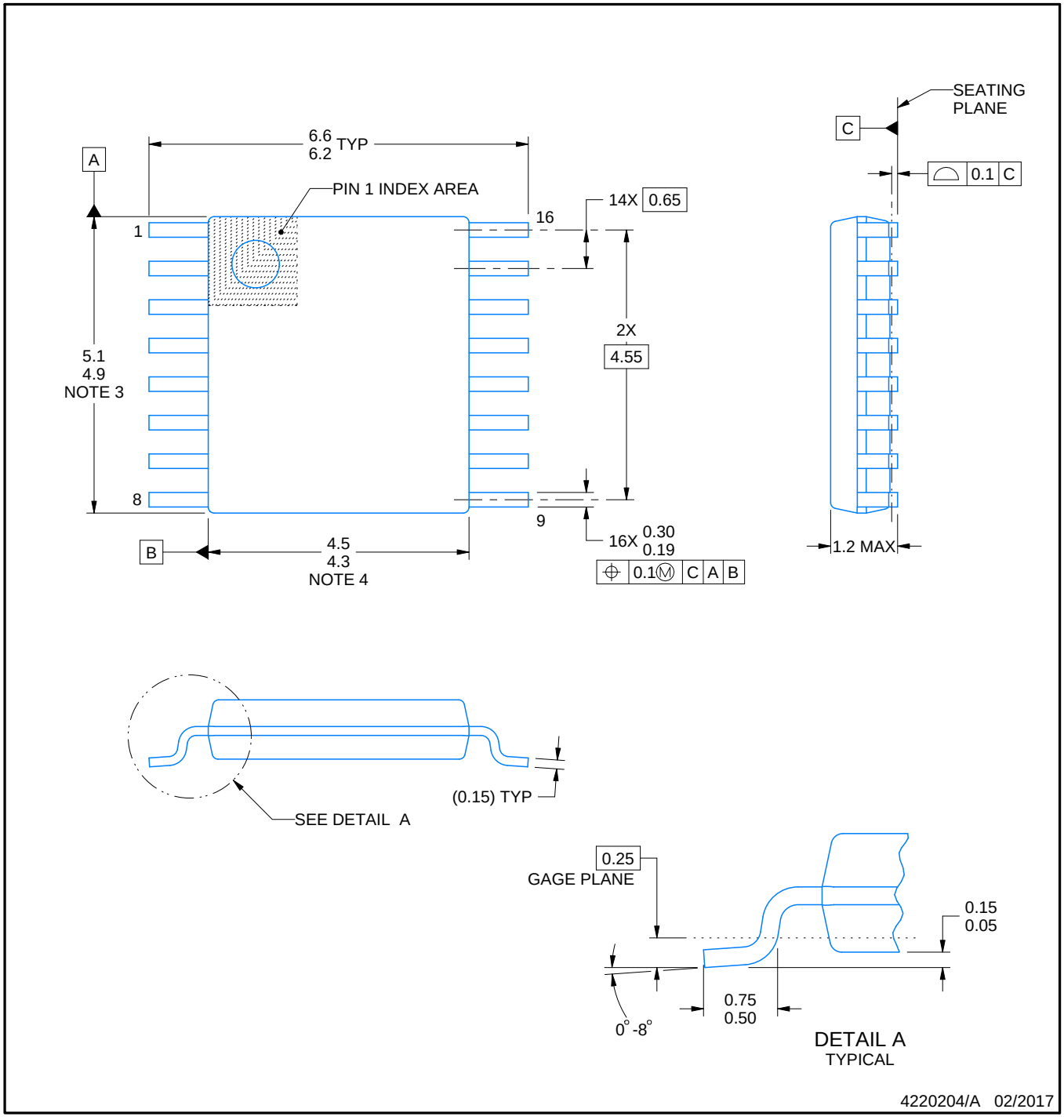
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

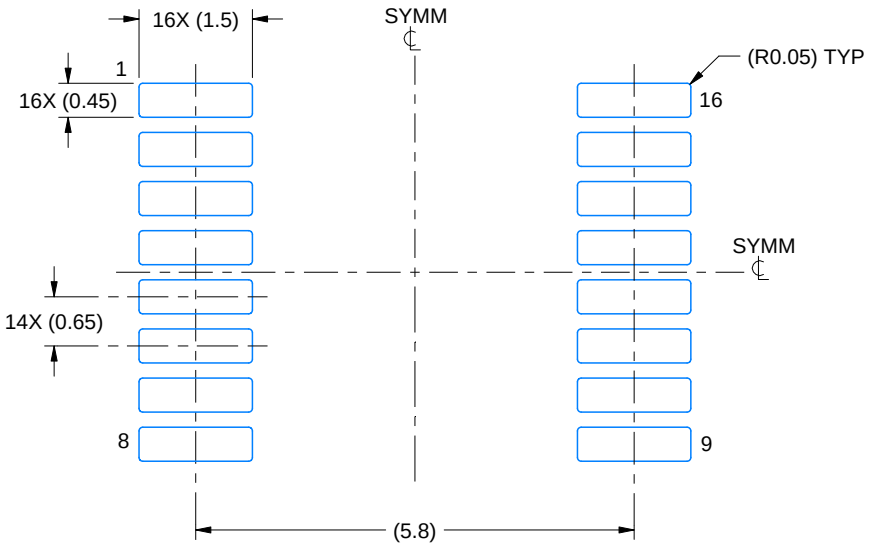
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

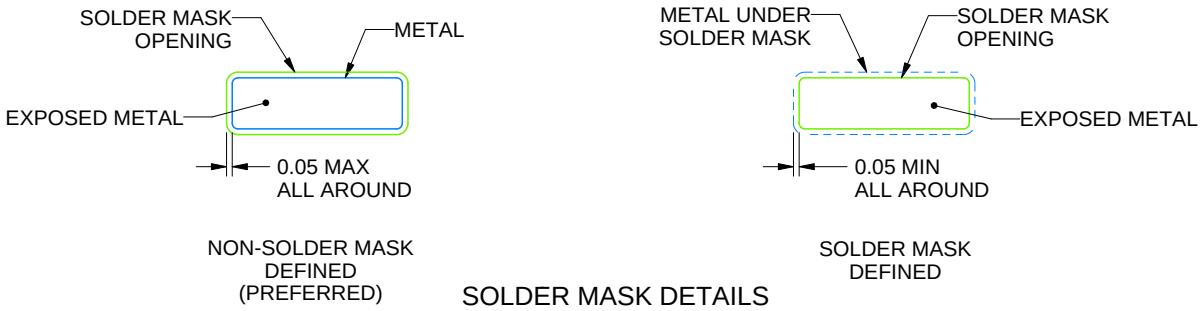


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

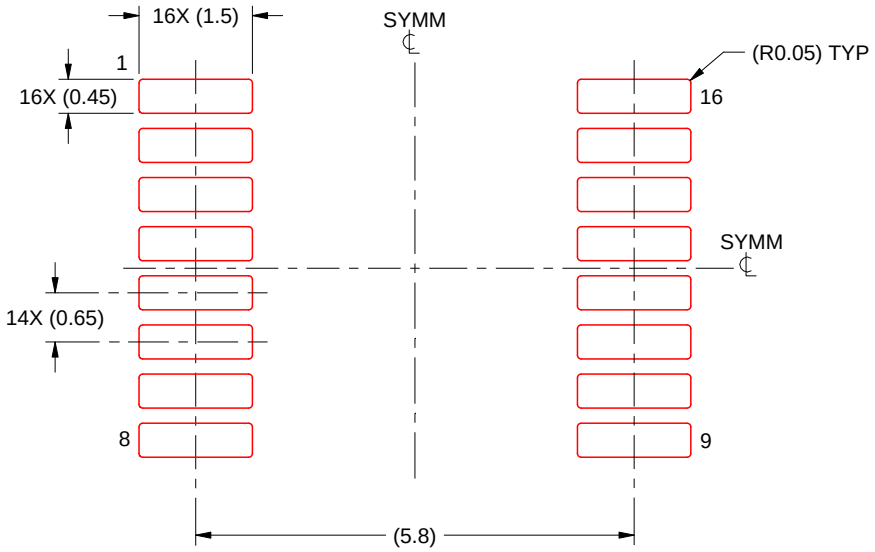


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

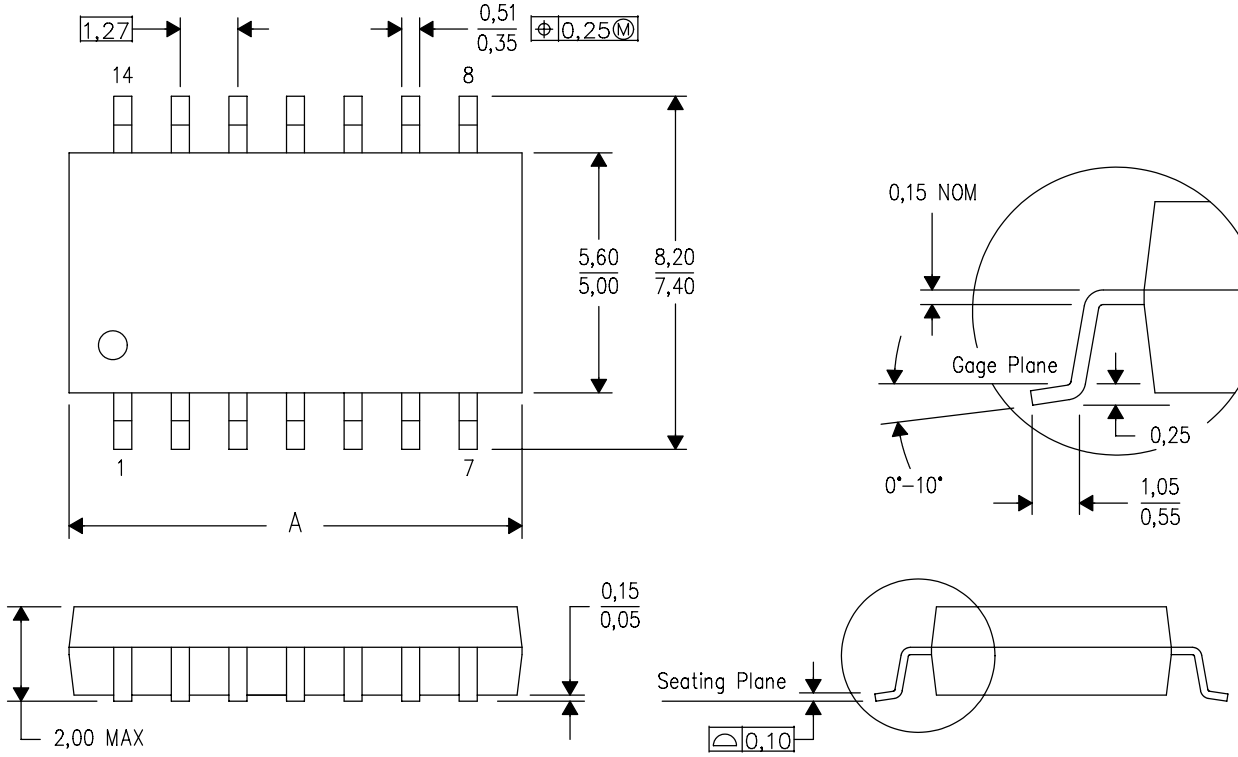
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

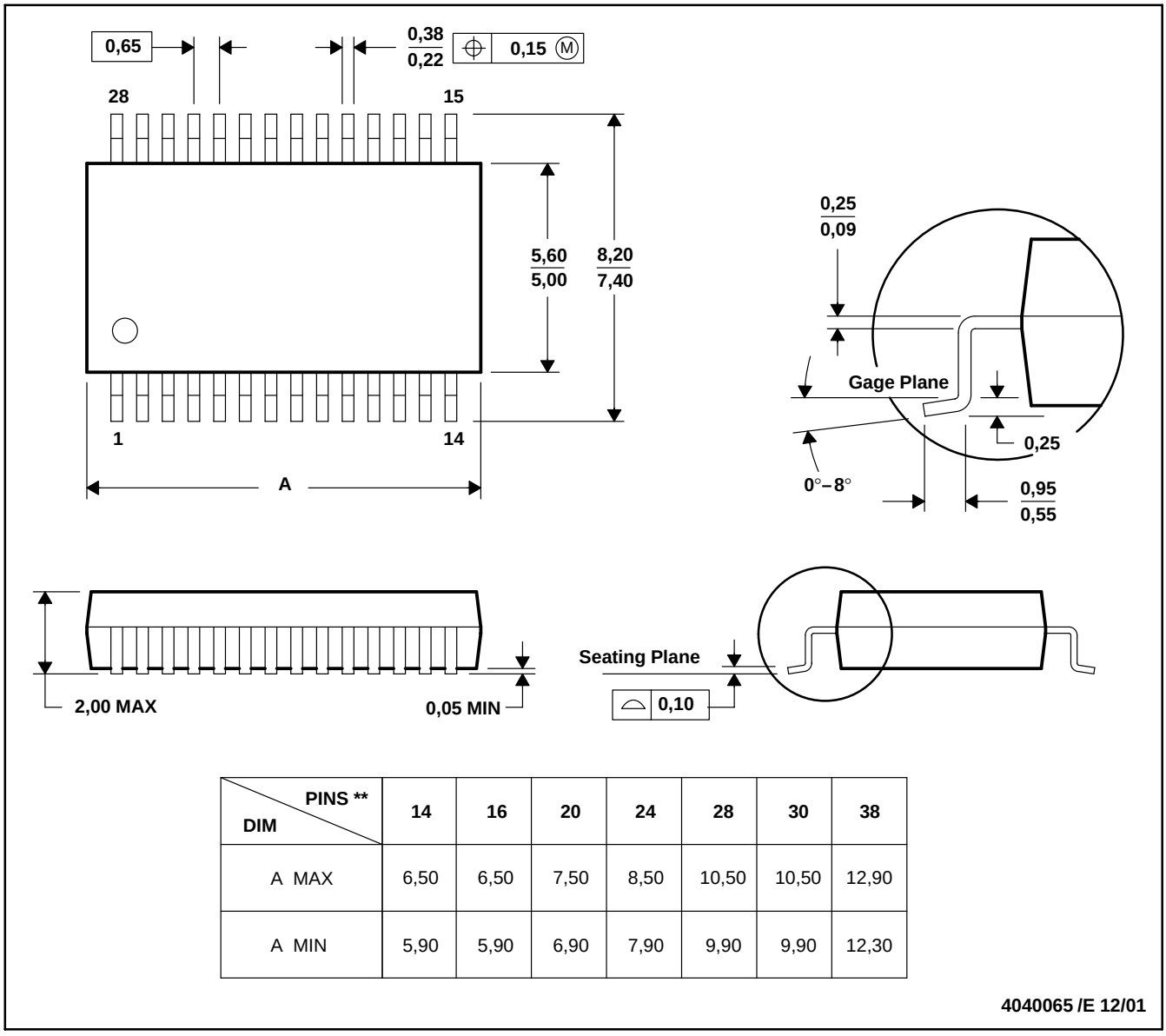
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

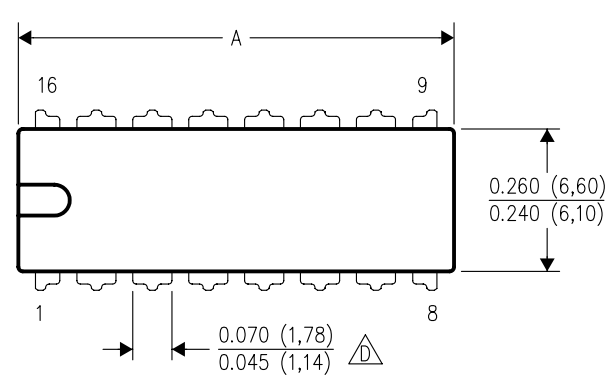
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

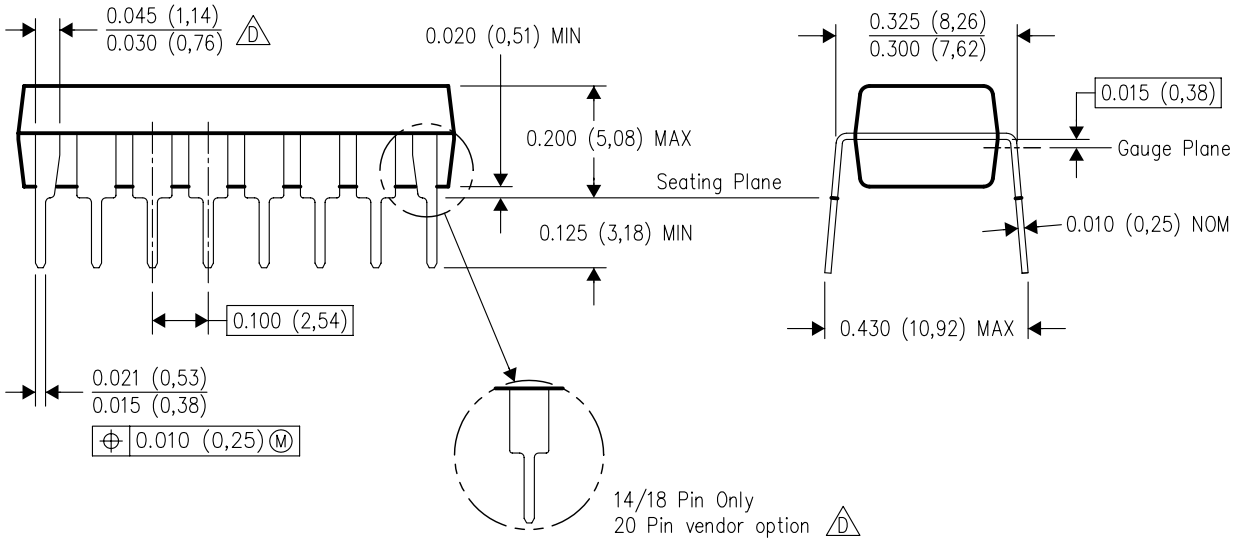
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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