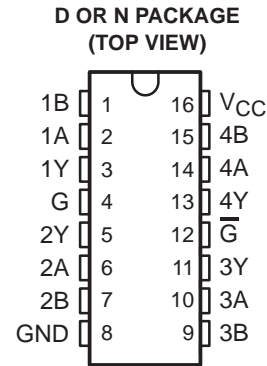


# SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS045B – JANUARY 1989 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Designed to Operate Up to 20 Mbaud
- 3-State Outputs
- Common-Mode Input Voltage Range – 7 V to 7 V
- Input Sensitivity . . .  $\pm 300$  mV
- Input Hysteresis . . . 120 mV Typ
- High-Input Impedance . . . 12 k $\Omega$  Min
- Operates from Single 5-V Supply
- Low Supply-Current Requirement 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A



## description

The SN75ALS197 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. The device meets the specifications of ITU Recommendations V.10, V.11, X.26, and X.27. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced, multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of  $\pm 300$  mV over a common-mode input voltage range of –7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES		OUTPUT Y
	G	$\bar{G}$	
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
$-0.3$ V < $V_{ID}$ < 0.3 V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

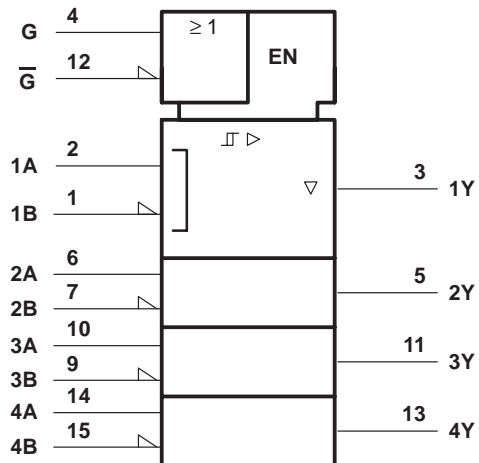
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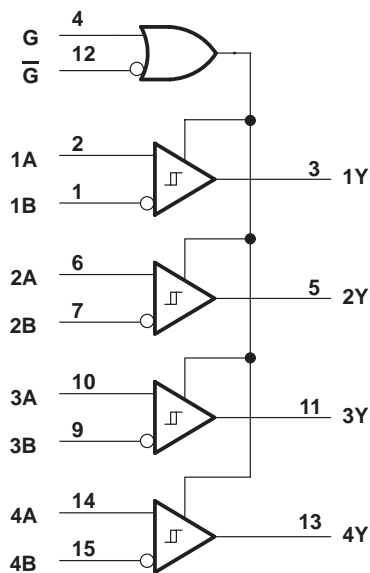
# SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS045B – JANUARY 1989 – REVISED MAY 1995

## logic symbol†

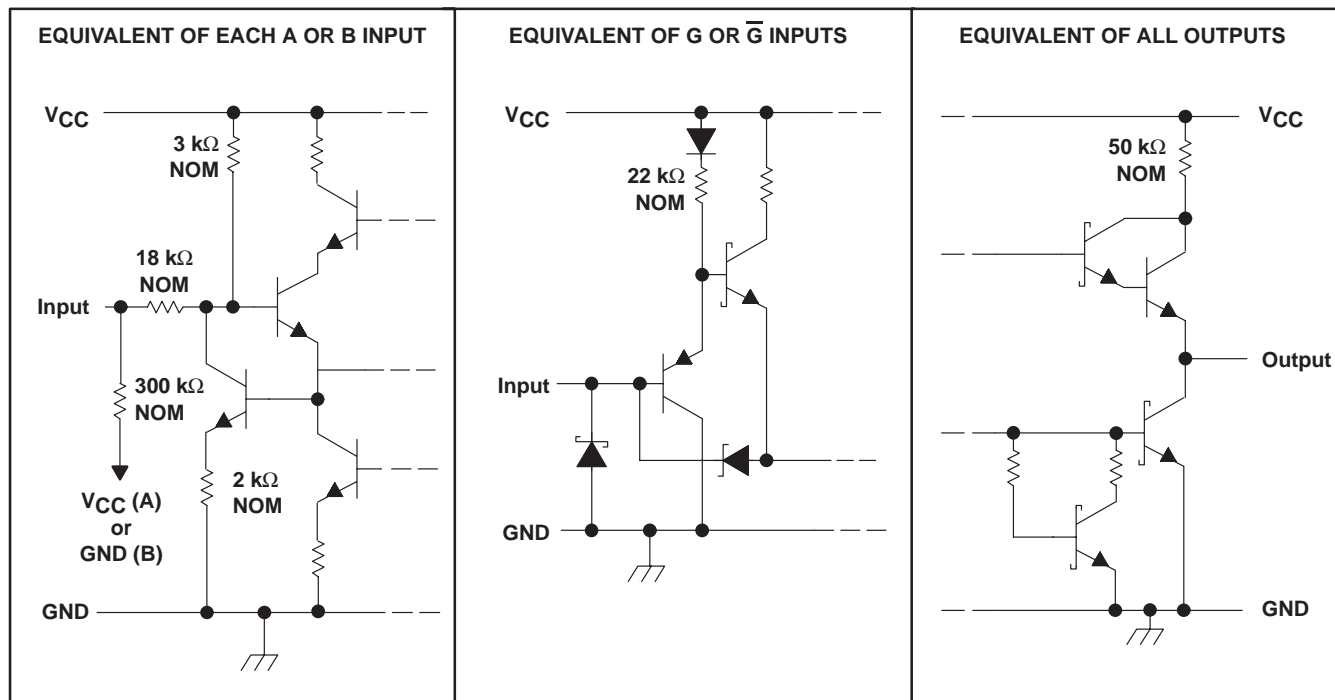


## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematics of inputs and outputs



# SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$ (A or B inputs)	$\pm 15$ V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 15$ V
Enable input voltage, $V_I$	7 V
Low-level output current, $I_{OL}$	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	$0^\circ\text{C}$ to $70^\circ\text{C}$
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.  
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/ $^\circ\text{C}$	608 mW
N	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$			$\pm 7$	V
Differential input voltage, $V_{ID}$			$\pm 12$	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
High-level output current, $I_{OH}$			-400	$\mu\text{A}$
Low-level output current, $I_{OL}$			16	mA
Operating free-air temperature, $T_A$	0		70	$^\circ\text{C}$

# SN75ALS197

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS045B – JANUARY 1989 – REVISED MAY 1995

**electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IT+</sub> Positive-going input threshold voltage				300	mV
V <sub>IT-</sub> Negative-going input threshold voltage		-300‡			mV
V <sub>hys</sub> Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )	See Figure 4		120		mV
V <sub>IK</sub> Enable-input clamp voltage	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 300 mV, I <sub>OH</sub> = -400 μA	2.7	3.6		V
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -300 mV			0.45	V
				0.5	
I <sub>OZ</sub> High-impedance-state output current	V <sub>CC</sub> = 5.25 V			20	μA
				-20	
I <sub>I</sub> Line input current	Other input at 0 V, See Note 3			0.7	mA
				-1.0	
I <sub>H</sub> High-level enable-input current				20	μA
				100	
I <sub>IL</sub> Low-level enable-input current	V <sub>IL</sub> = 0.4 V			-100	μA
	Input resistance	12	18		kΩ
I <sub>OS</sub> Short-circuit output current§	V <sub>ID</sub> = 3 V, V <sub>O</sub> = 0	-15	-78	-130	mA
I <sub>CC</sub> Supply current	Outputs disabled		22	35	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low- to high-level output	V <sub>ID</sub> = -2.5 V to 2.5 V, C <sub>L</sub> = 15 pF, See Figure 2		15	22	ns
t <sub>PHL</sub> Propagation delay time, high- to low-level output			15	22	
t <sub>PZH</sub> Output enable time to high level	C <sub>L</sub> = 15 pF, See Figure 3		13	25	ns
t <sub>PZL</sub> Output enable time to low level			11	25	
t <sub>PHZ</sub> Output disable time from high level	C <sub>L</sub> = 15 pF, See Figure 3		13	25	ns
t <sub>PLZ</sub> Output disable time from low level			15	22	



PARAMETER MEASUREMENT INFORMATION

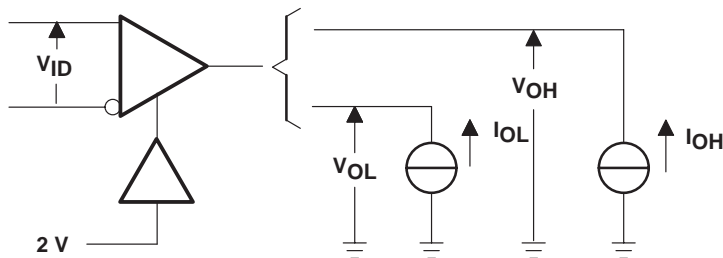
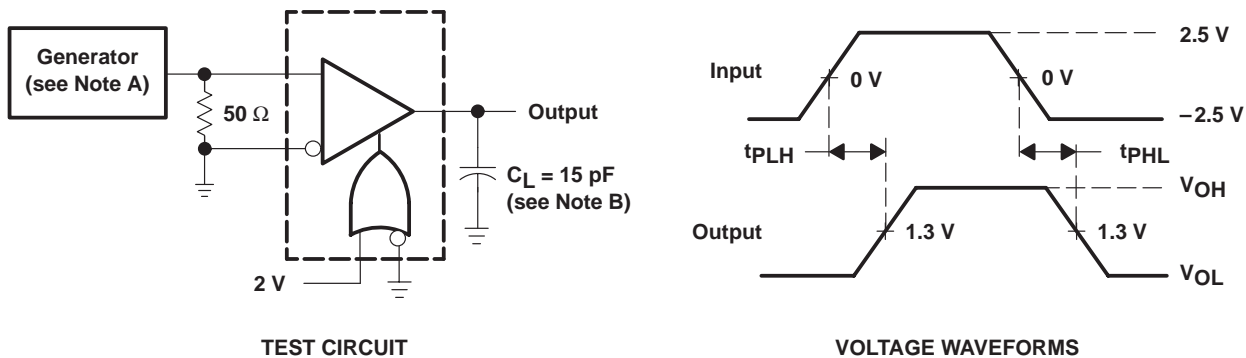


Figure 1.  $V_{OH}$  and  $V_{OL}$  Test Circuit



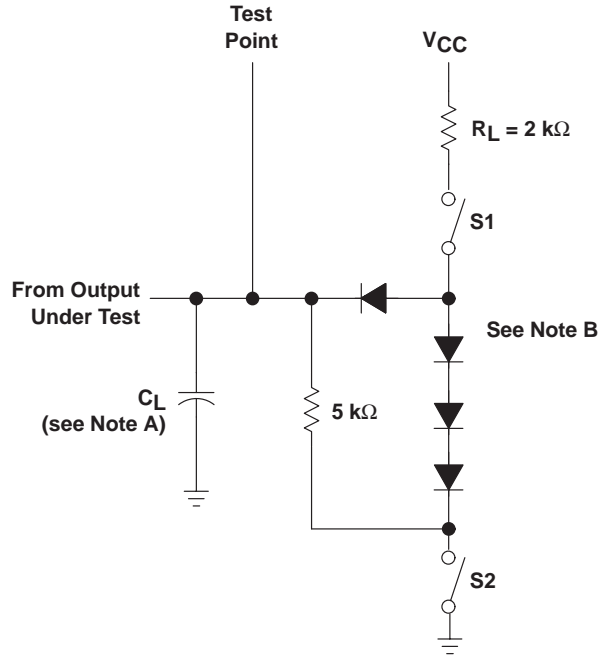
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, duty cycle  $\leq 50\%$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns.  
 B.  $C_L$  includes probe and jig capacitance.

Figure 2.  $t_{pLH}$  and  $t_{pHL}$  Test Circuit and Voltage Waveforms

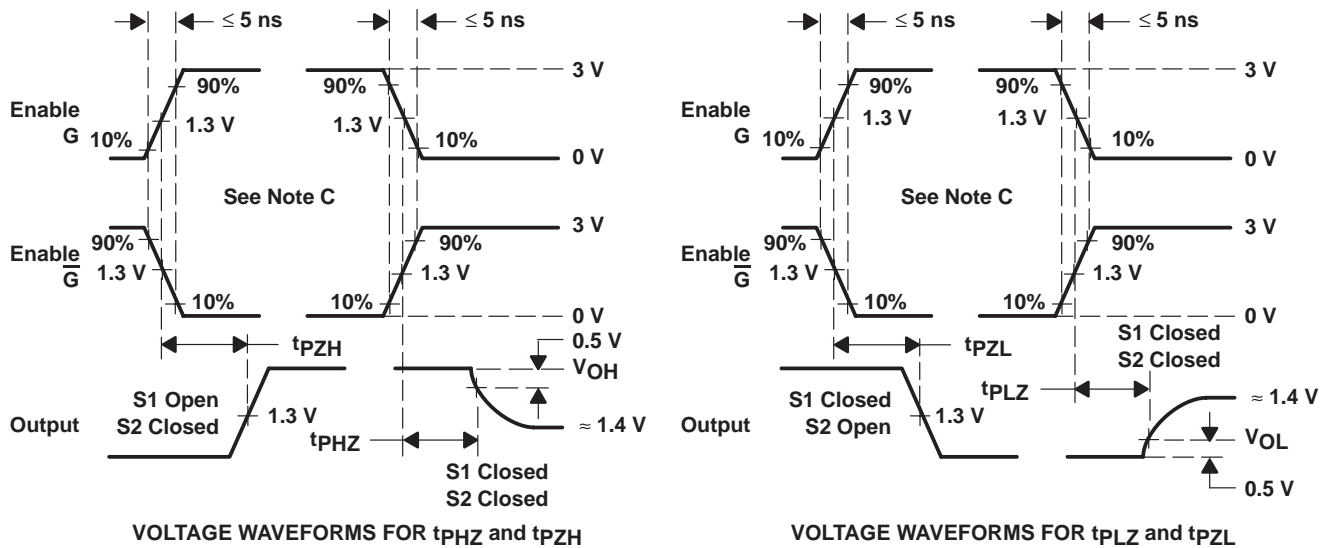
# SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Enable G is tested with G high;  $\bar{G}$  is tested with G low.

Figure 3.  $t_{pZH}$ ,  $t_{pZH}$ ,  $t_{pLZ}$ , and  $t_{pLZ}$  Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

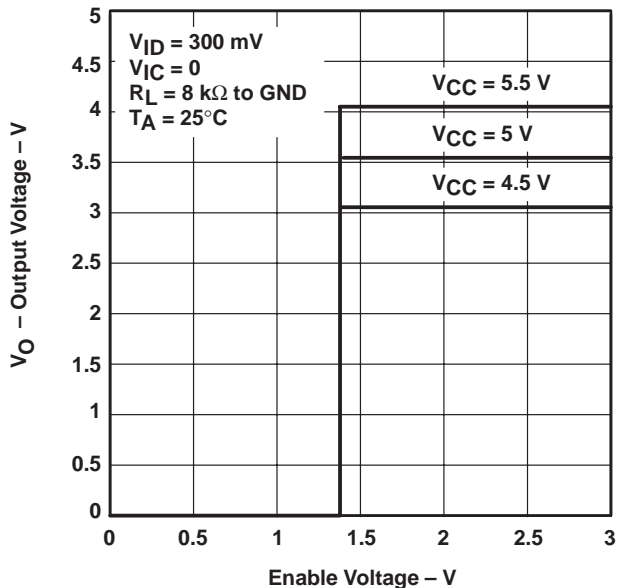


Figure 4

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

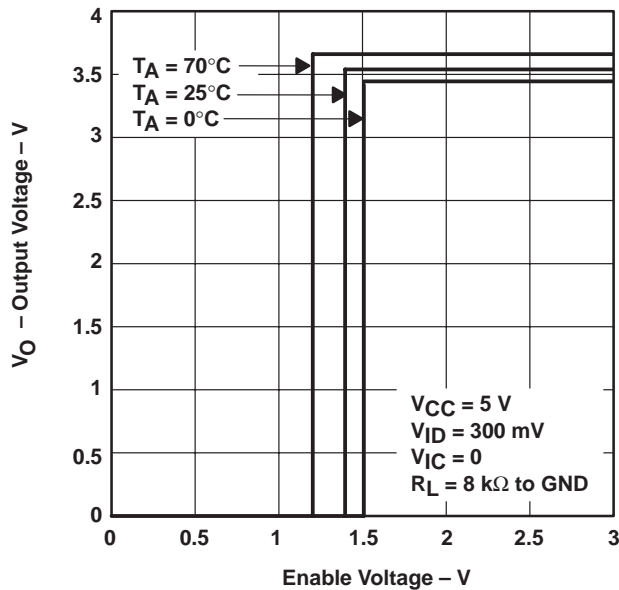


Figure 5

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

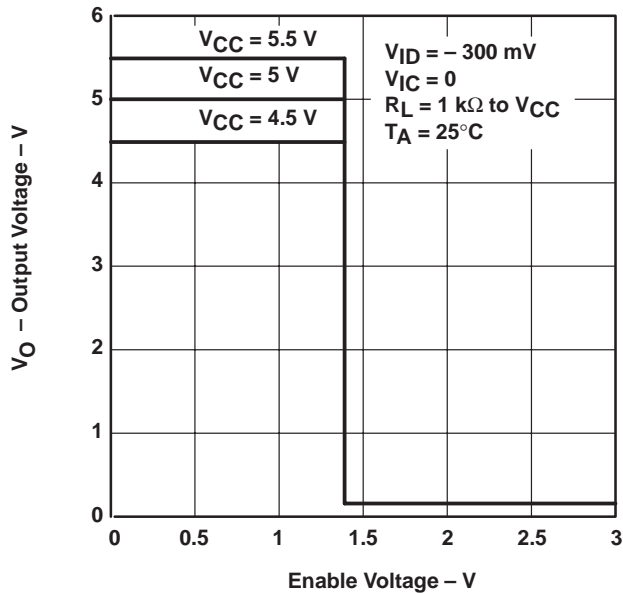


Figure 6

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

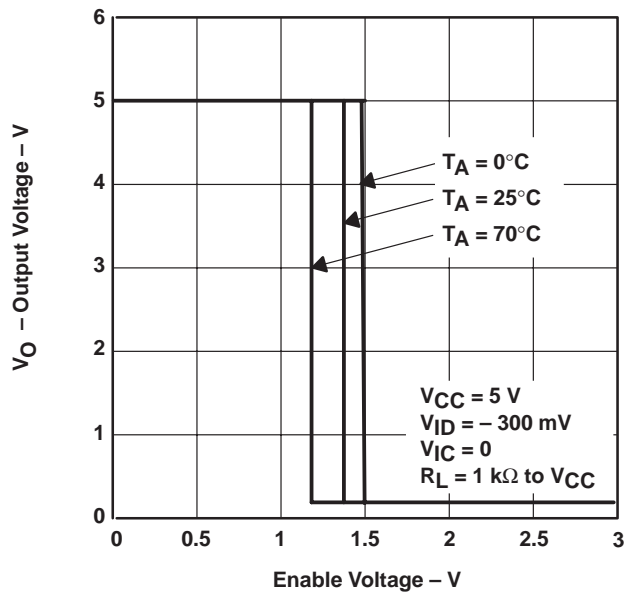
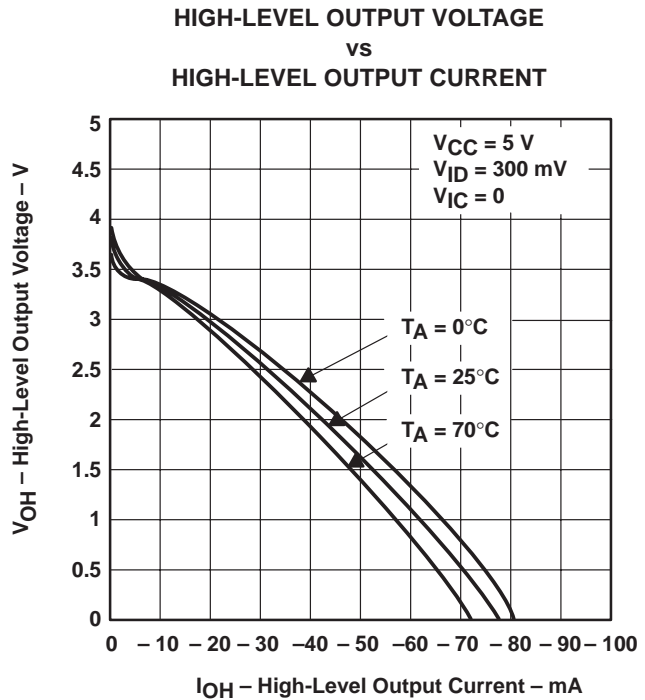
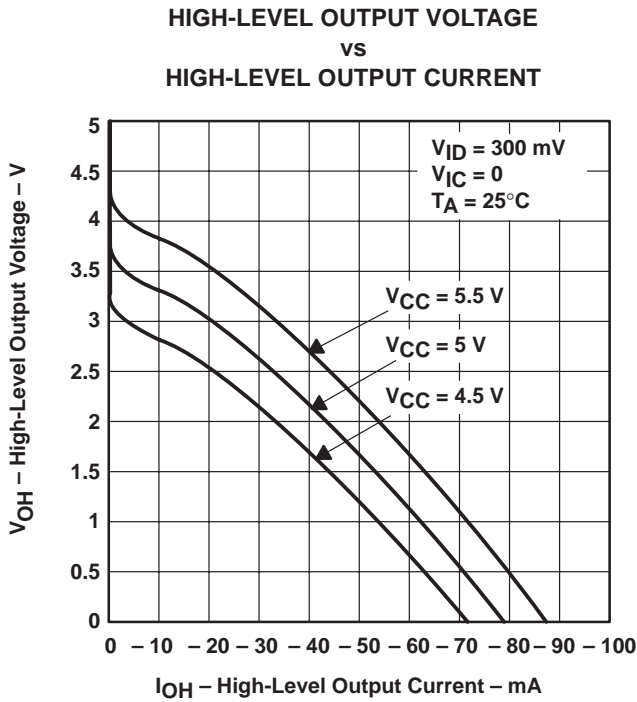
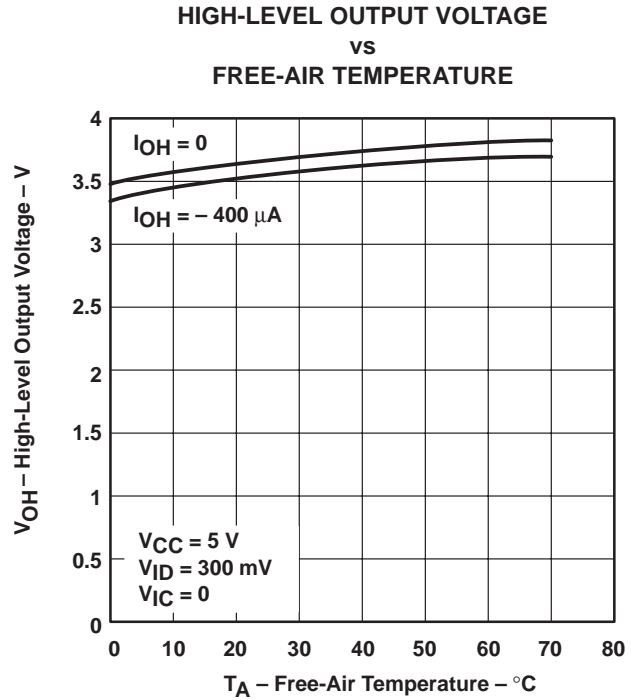
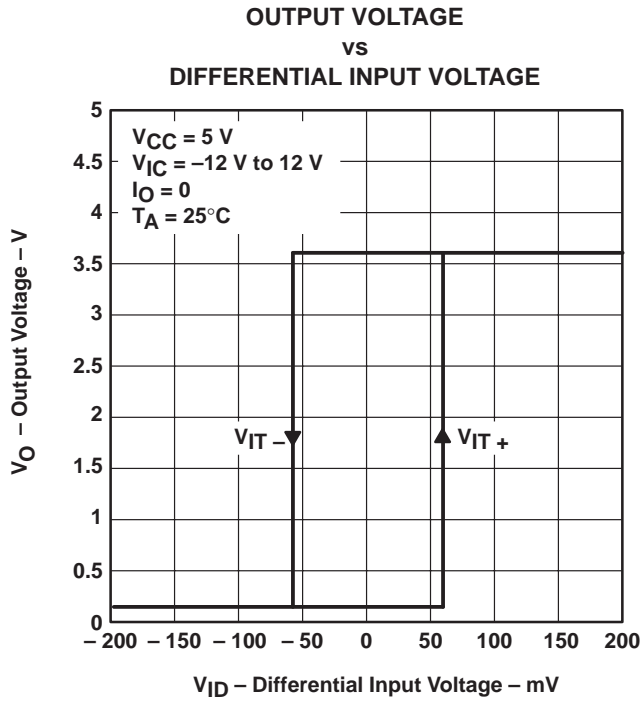


Figure 7

# SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE

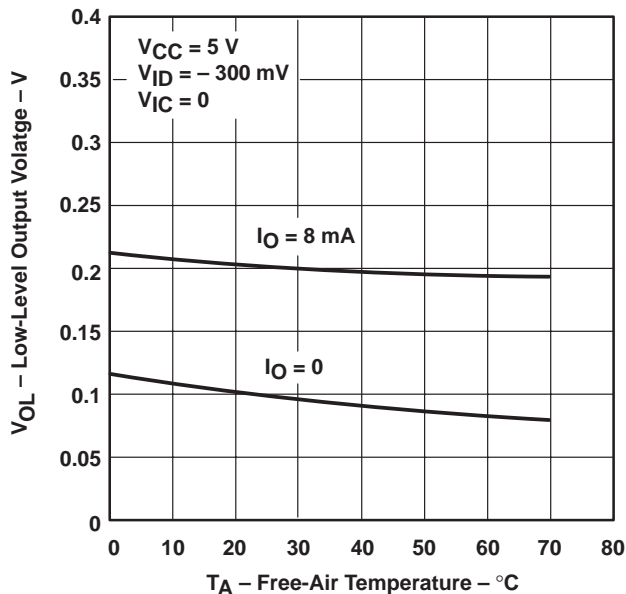


Figure 12

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

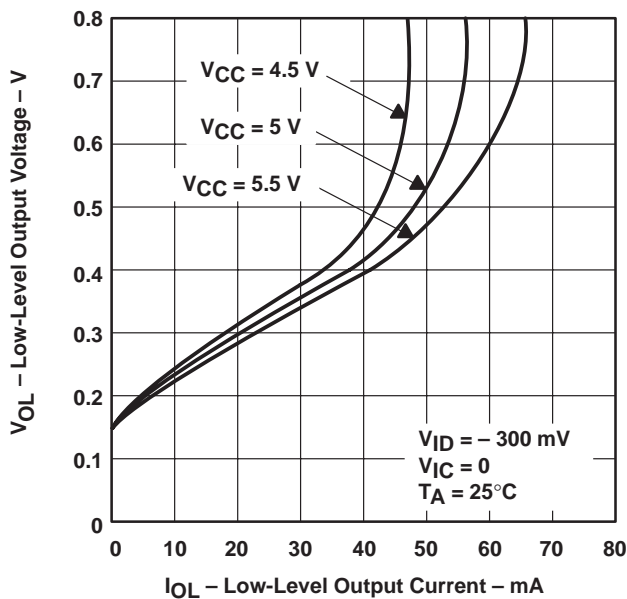


Figure 13

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

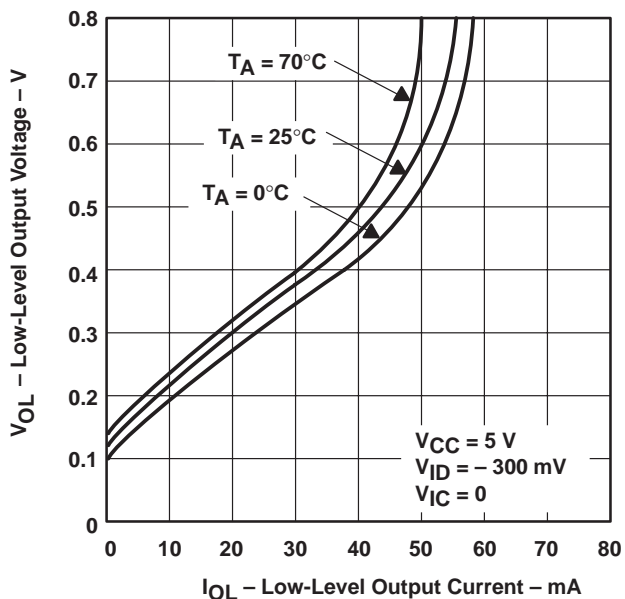


Figure 14

# SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

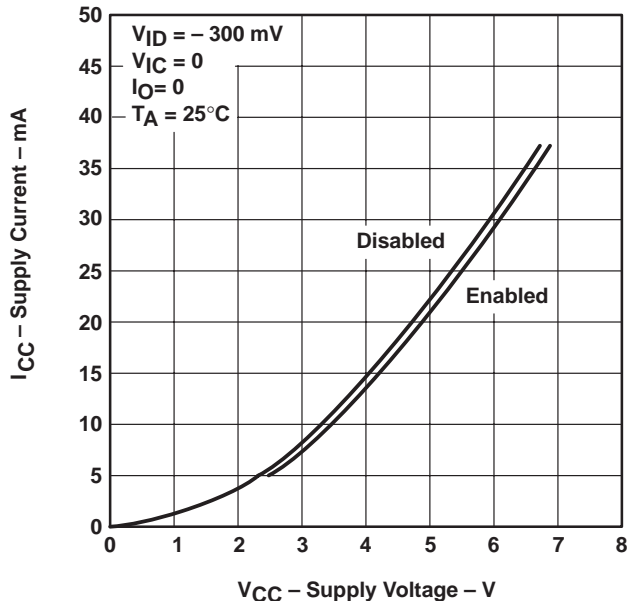


Figure 15

**SUPPLY CURRENT  
vs  
FREE-AIR TEMPERATURE**

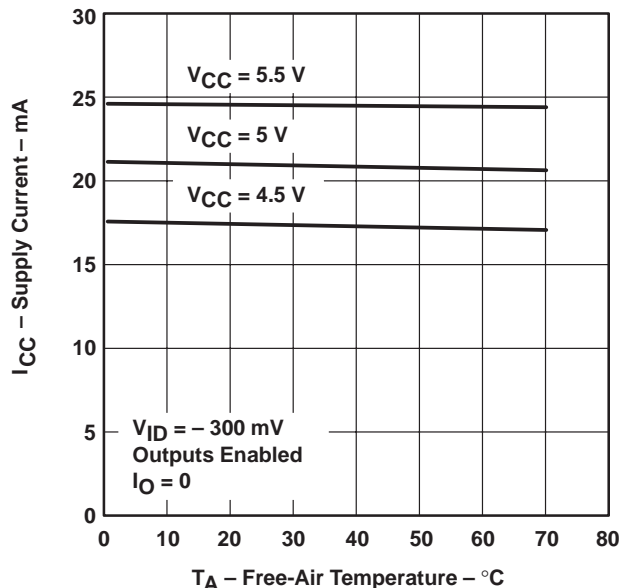


Figure 16

**SUPPLY CURRENT  
vs  
DIFFERENTIAL INPUT VOLTAGE**

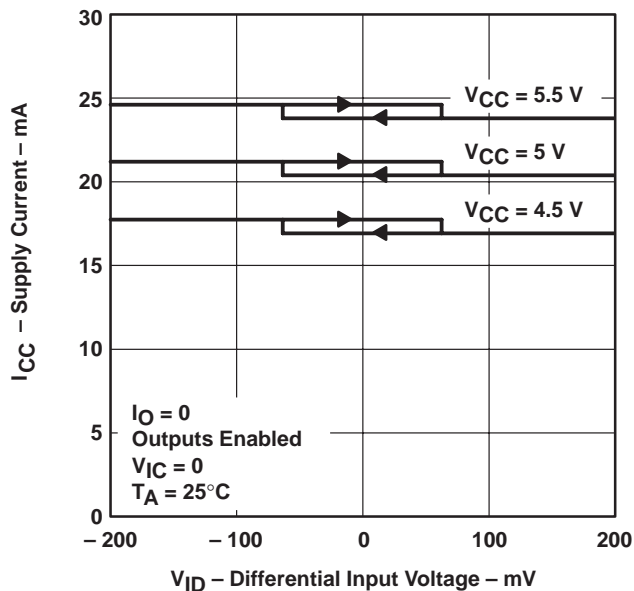


Figure 17

**SUPPLY CURRENT  
vs  
FREQUENCY**

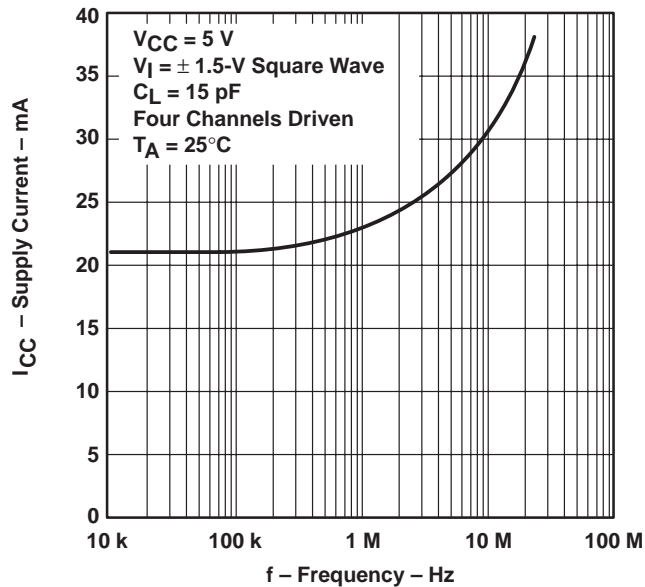


Figure 18



TYPICAL CHARACTERISTICS

INPUT RESISTANCE  
 vs  
 FREE-AIR TEMPERATURE

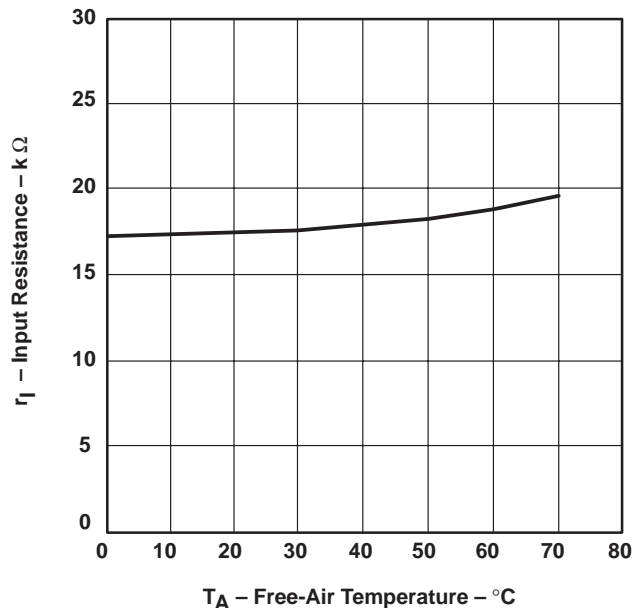


Figure 19

INPUT CURRENT  
 vs  
 INPUT VOLTAGE TO GND

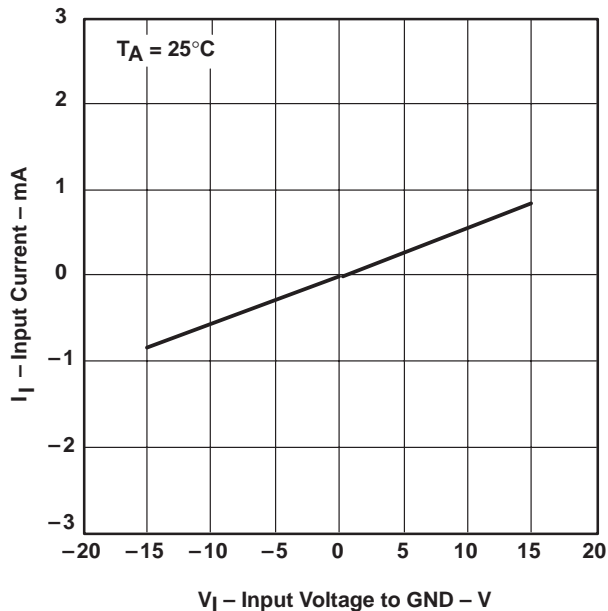


Figure 20

SWITCHING TIME  
 vs  
 FREE-AIR TEMPERATURE

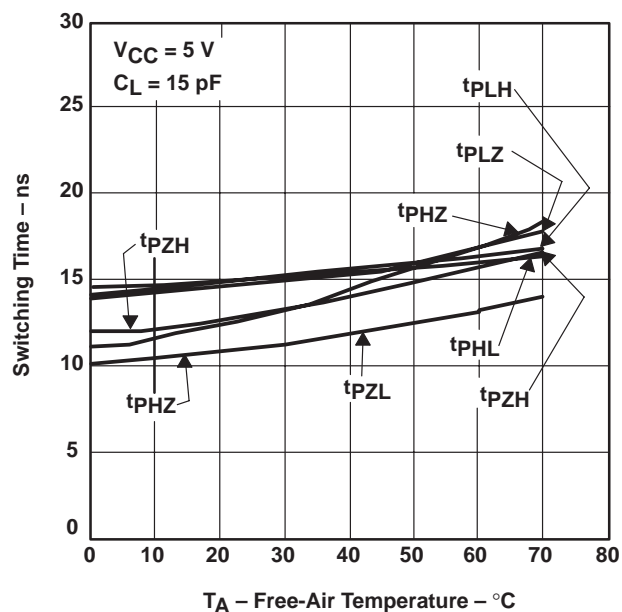


Figure 21

PROPAGATION DELAY TIME  
 vs  
 SUPPLY VOLTAGE

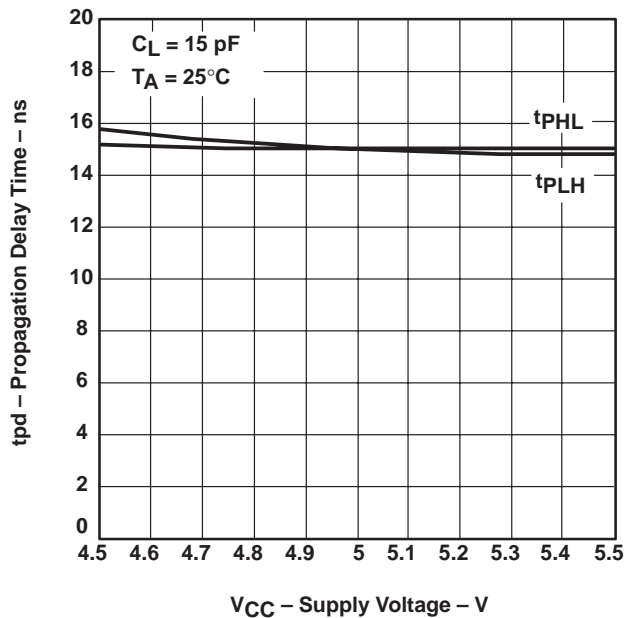


Figure 22

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS197D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS197	<a href="#">Samples</a>
SN75ALS197DE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS197	<a href="#">Samples</a>
SN75ALS197DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS197	<a href="#">Samples</a>
SN75ALS197N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS197N	<a href="#">Samples</a>
SN75ALS197NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS197	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS197DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS197NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS197DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75ALS197NSR	SO	NS	16	2000	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS197D	D	SOIC	16	40	507	8	3940	4.32
SN75ALS197DE4	D	SOIC	16	40	507	8	3940	4.32
SN75ALS197N	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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