

- Supports a 9-Pin GeoPort™ Host Interface Standard for the Intelligent Network Port
- Designed to Operate up to 4-Mbit/s Full Duplex
- ±5 V Supply Operation
- Provides 6 kV ESD Protection
- Has Driver Short-Circuit Protection
- Includes Failsafe Mechanism for Open Inputs
- Is Backward Compatible with AppleTalk™ and LocalTalk™
- Combines Multiple Components into a Single Chip Solution
- Complements the SN75LBC772 9-Pin GeoPort Peripheral (DCE) Interface Device
- Uses LinBiCMOS™ Process Technology

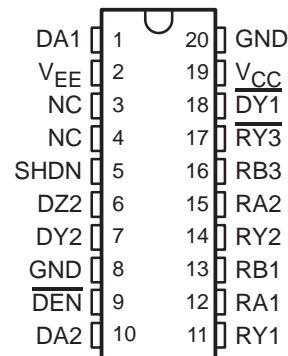
description

The SN75LBC771 is a low-power LinBiCMOS™ device that incorporates the drivers and receivers for a 9-pin GeoPort host interface. GeoPort combines hybrid EIA/TIA-422-B and EIA/TIA-423-B drivers and receivers to transmit data up to four-Mbit/s full duplex. GeoPort is a serial communications standard that is intended to replace the RS-232, AppleTalk, and printer ports all in one connector in addition to providing real-time data transfer capability. The SN75LBC771 provides point-to-point connections between GeoPort-compatible devices with data transmission rates up to 4-Mbit/s full duplex featuring a hot-plug capability. Applications include connection to telephone, ISDN, digital sound and imaging, fax-data modems, and other traditional serial and parallel connections. The GeoPort is backwardly compatible to both LocalTalk and AppleTalk.

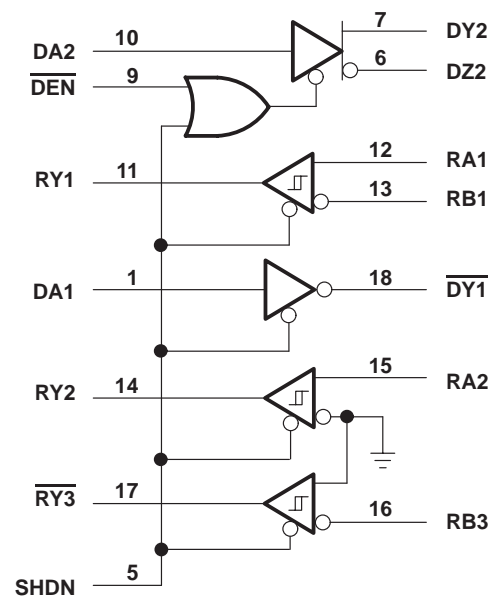
While the SN75LBC771 is powered off (V_{CC} and $V_{EE} = 0$), the outputs are in a high-impedance state. Also, when the shutdown (SHDN) terminal is high, all outputs go into a high-impedance state. A logic high on the driver enable (\overline{DEN}) terminal places the outputs of the differential driver into a high-impedance state. All drivers and receivers have fail-safe mechanisms that ensure a high output state when the inputs are left open.

The SN75LBC771 is characterized for operation over the 0°C to 70°C temperature range.

**DW PACKAGE
(TOP VIEW)**



logic diagram (positive logic)



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SN75LBC771 GEOPORT™ TRANSCEIVER

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FUNCTION TABLES†

SINGLE-ENDED DRIVER		
INPUT (DA1)	ENABLE (SHDN)	OUTPUT (DY1)
H	L	L
L	L	H
OPEN	L	L
X	H	Z
X	OPEN	Z

DIFFERENTIAL DRIVER				
INPUT (DA2)	ENABLE (SHDN) ($\overline{\text{DEN}}$)		OUTPUT (DY2) (DZ2)	
H	L	L	H	L
L	L	L	L	H
OPEN	L	L	H	L
X	H	X	Z	Z
X	OPEN	X	Z	Z
X	X	H	Z	Z
X	X	OPEN	Z	Z

SINGLED-ENDED RECEIVER			
INPUT (RA2, RA3)	ENABLE (SHDN)	OUTPUT (RY2) (RY3)	
H	L	H	L
L	L	L	H
OPEN	L	H	H
SHORT‡	L	?	?
X	H	Z	Z
X	OPEN	Z	Z

DIFFERENTIAL RECEIVER			
INPUT (RA1) (RB1)		ENABLE (SHDN)	OUTPUT (RY1)
H	L	L	H
L	H	L	L
OPEN		L	H
SHORT‡		L	?
X	X	H	Z
X	X	OPEN	Z

† H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

‡ $-0.2\text{ V} < V_{\text{ID}} < 0.2\text{ V}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Positive supply voltage range, V_{CC} (see Note 1)	–0.5 to 7 V
Negative supply voltage range, V_{EE} (see Note 1)	–7 to 0.5 V
Receiver input voltage range (RA, RB)	–15 V to 15 V
Receiver differential input voltage range, V_{ID}	–12 V to 12 V
Receiver output voltage range (RY)	–0.5 V to 5.5 V
Driver output voltage range (Power Off) ($\overline{\text{DY1}}$, DY2, DZ2)	–15 V to 15 V
Driver output voltage range (Power On) ($\overline{\text{DY1}}$, DY2, DZ2)	–11 V to 11 V
Driver input voltage range (DA, SHDN, $\overline{\text{DEN}}$)	–0.5 V to $V_{\text{CC}} + 0.4\text{ V}$
Electrostatic Discharge (see Note 2)	
(All pins) Class 3, A	6 kV
(All pins) Class 3, B	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_{A}	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating is per MIL-STD-883C, Method 3015.7.



DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC}	4.75	5	5.25	V
Negative supply voltage, V_{EE}	-5.25	-5	-4.75	V
High-level input voltage, V_{IH} (DA, SHDN, \overline{DEN})	2			V
Low-level input voltage, V_{IL} (DA, SHDN, \overline{DEN})				0.8
Receiver common-mode input voltage, V_{IC}	-7			7
Receiver differential input voltage, V_{ID}	-12		12	V
Operating free-air temperature, T_A	0		70	°C

driver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V_{OH}	High-level output voltage	Single-ended, See Figure 1	$R_L = 12\text{ k}\Omega$		3.6	4.5	V	
			$R_L = 120\ \Omega$		2	3.6	V	
V_{OL}	Low-level output voltage	Single-ended, See Figure 1	$R_L = 12\text{ k}\Omega$		-4.5		-3.6	V
			$R_L = 120\ \Omega$		-3.6		-2	V
$ V_{OD} $	Magnitude of differential output voltage $ V_{DY} - V_{DZ} $		$R_L = 120\ \Omega$, See Figure 2		4		V	
$\Delta V_{OD} $	Change in differential voltage magnitude				250		mV	
V_{OC}	Common-mode output voltage				-2	2	V	
$ \Delta V_{OC(SS)} $	Magnitude of change, common-mode steady-state output voltage		See Figure 3		200		mV	
$ \Delta V_{OC(PP)} $	Magnitude of change, common-mode peak-to-peak output voltage				700		mV	
I_{CC}	Positive supply current		SHDN = $\overline{DEN} = 0\text{ V}$, No Load		4	10	mA	
I_{EE}	Negative supply current				-2		-5	mA
I_{CC}	Positive supply current		SHDN = $\overline{DEN} = 5\text{ V}$, No Load		100		μA	
I_{EE}	Negative supply current				-100		μA	
I_{OZ}	High-impedance output current		$V_{CC} = 0\text{ or }5\text{ V}$, $-10\text{ V} \leq V_O \leq 10\text{ V}$		± 100		μA	
I_{OS}	Short-circuit output current		$V_{CC} = 5.25\text{ V}$, See Note 3		± 170	± 450	mA	

NOTE 3: Not more than one output should be shorted at one time.

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driver switching characteristics over operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{PHL}	Propagation delay time, high-to-low level output	Single ended, See Figure 4	42	75		ns	
t _{PLH}	Propagation delay time, low-to-high level output		41	75		ns	
t _{PZL}	Driver output enable time to low-level output		SHDN	25	100		μs
t _{PZH}	Driver output enable time to high-level output			25	100		μs
t _{PLZ}	Driver output disable time from low-level output			28	100		ns
t _{PHZ}	Driver output disable time from high-level output			37	100		ns
t _r	Rise time		10	25	75		ns
t _f	Fall time		10	23	75		ns
t _{PHL}	Propagation delay time, high-to-low level output		Differential, See Figure 5	40	75		ns
t _{PLH}	Propagation delay time, low-to-high level output			42	75		ns
t _{PZL}	Driver output enable time to low-level output	SHDN		25	100		μs
		DEN		29	150		ns
t _{PZH}	Driver output enable time to high-level output	SHDN		25	100		μs
		DEN		35	150		ns
t _{PLZ}	Driver output disable time from low-level output	SHDN		28	100		ns
		DEN		34	100		ns
t _{PHZ}	Driver output disable time from high-level output	SHDN		37	100		ns
		DEN		34	100		ns
t _r	Rise time	10		27	75		ns
t _f	Fall time	10		26	75		ns
t _{SK(p)}	Pulse skew, t _{PLH} - t _{PHL}					22	ns



receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

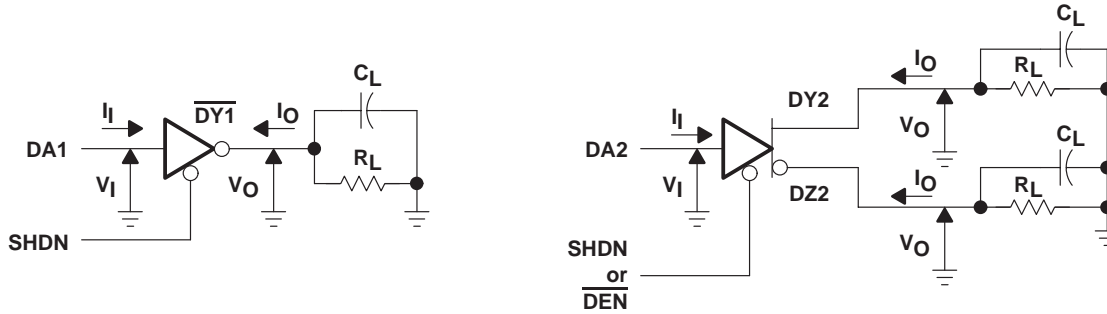
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 6			200	mV
V_{IT-}	Negative-going input threshold voltage		-200			mV
V_{hys}	Differential input voltage hysteresis ($V_{IT+} - V_{IT-}$)			50		mV
V_{OH}	High-level output voltage (see Note 4)	$V_{IC} = 0$, See Figure 6	$I_{OH} = -2$ mA,	2	4.5	V
V_{OL}	Low-level output voltage	$V_{IC} = 0$, See Figure 6	$I_{OL} = 2$ mA,	0.4	0.8	V
I_{OS}	Short-circuit output current	$V_O = 0$		-45	-85	mA
		$V_O = 5.25$ V		45	85	mA
R_{IN}	Input resistance	$V_{CC} = 0$ or 5.25 V, -12 V $\leq V_I \leq 12$ V	6	30		k Ω

NOTE 4: If the inputs are left unconnected, receivers one and two interpret this as a high-level input and receiver three interprets this as a low-level input so that all outputs are at the high level.

receiver switching characteristics over recommended conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
t_{PHL}	Propagation delay time, high-to-low level output	$R_L = 2$ k Ω , $C_L = 15$ pF, See Figure 6		30	75	ns		
t_{PLH}	Propagation delay time, low-to-high level output			30	75	ns		
t_r	Rise time			15	30	ns		
t_f	Fall time			15	30	ns		
$t_{SK(P)}$	Pulse skew $ t_{PLH} - t_{PHL} $				20	ns		
t_{PZL}	Receiver output enable time to low-level output	$C_L = 50$ pF, See Figure 7		35	100	ns		
t_{PZH}	Receiver output enable time to high-level output			35	100	ns		
t_{PLZ}	Receiver output disable time from low-level output		Differential		20	100	ns	
t_{PHZ}	Receiver output disable time from high-level output				20	100	ns	
t_{PZL}	Receiver output enable time to low-level output		Single-ended		12	25	ns	
t_{PZH}	Receiver output enable time to high-level output				12	25	μ s	
t_{PLZ}	Receiver output disable time from low-level output					25	100	μ s
t_{PHZ}	Receiver output disable time from high-level output					125	400	ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: $C_L = 50 \text{ pF}$

Figure 1. Single-Ended Driver DC Parameter Test Circuits

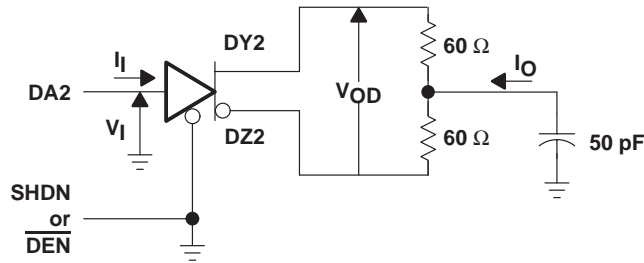
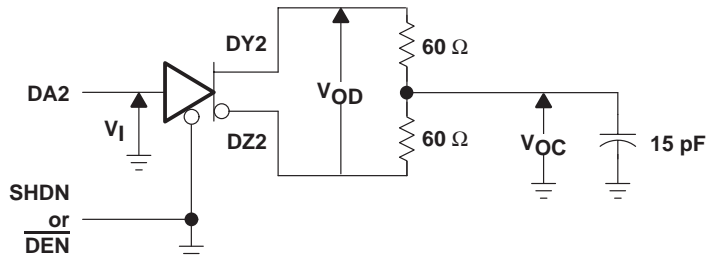
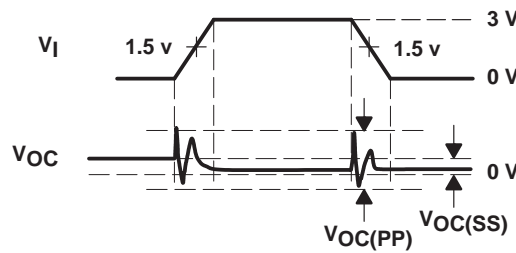


Figure 2. Differential Driver DC Parameter Test Circuit



TEST CIRCUIT

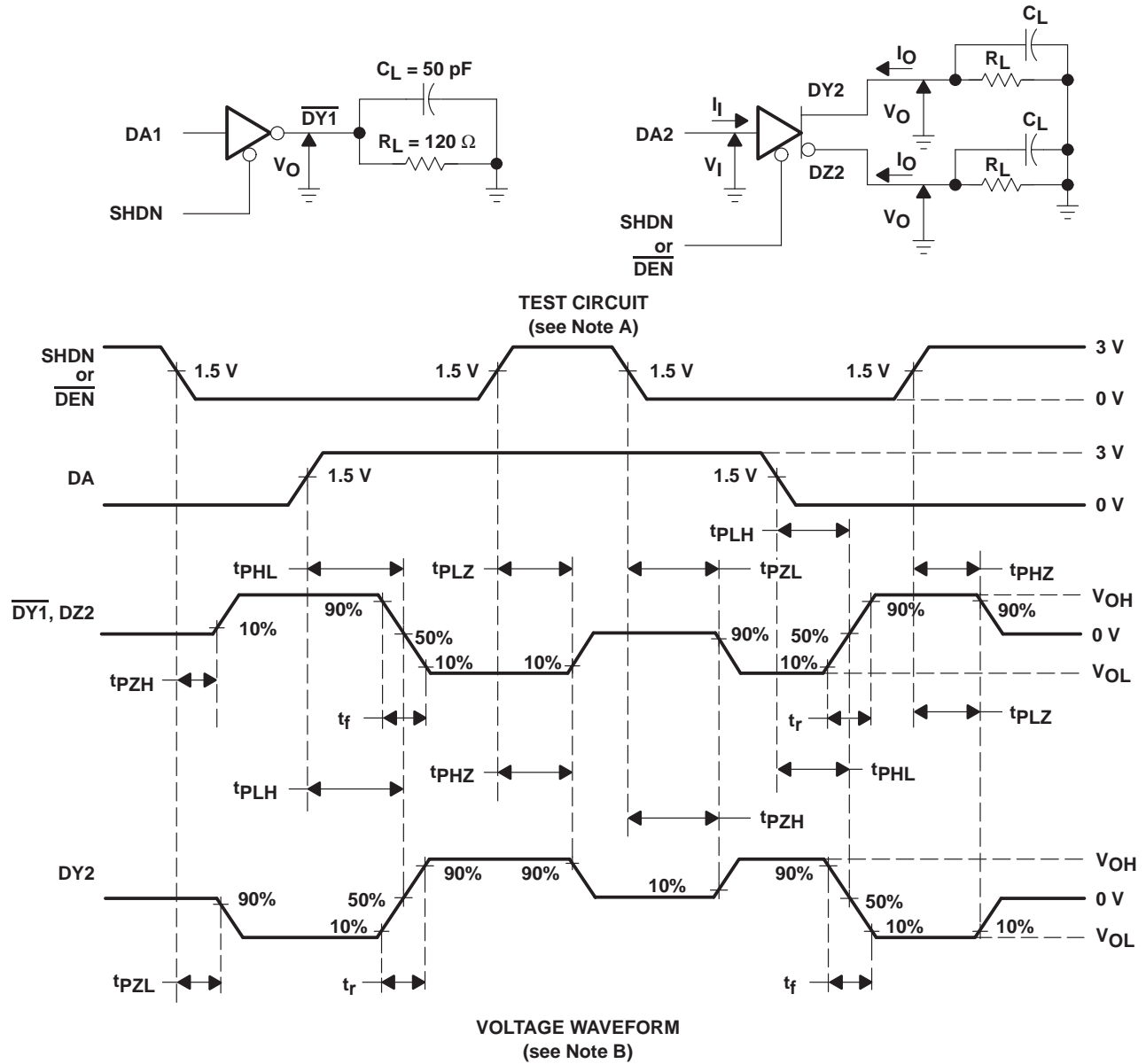


VOLTAGE WAVEFORM

NOTE A: Measured 3dB Bandwidth = 300 MHz

Figure 3. Differential Driver Common-Mode Output Voltage Test Circuit

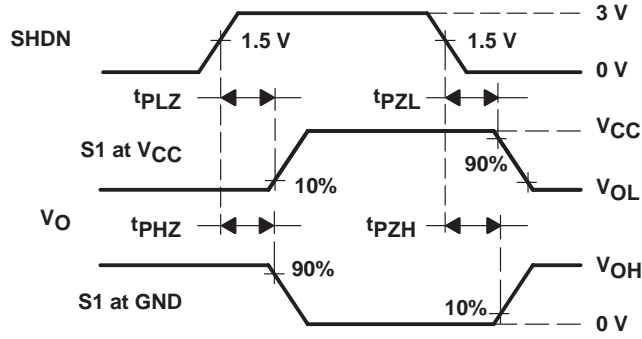
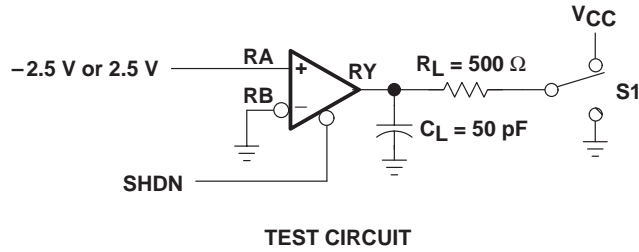
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. $C_L = 50 \text{ pF}$, $R_L = 120 \Omega$
B. The input waveform t_r , $t_f \leq 10 \text{ ns}$.

Figure 4. Single-Ended Driver Propagation and Transition Times Test Circuits and Waveform

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
 (see Note A)

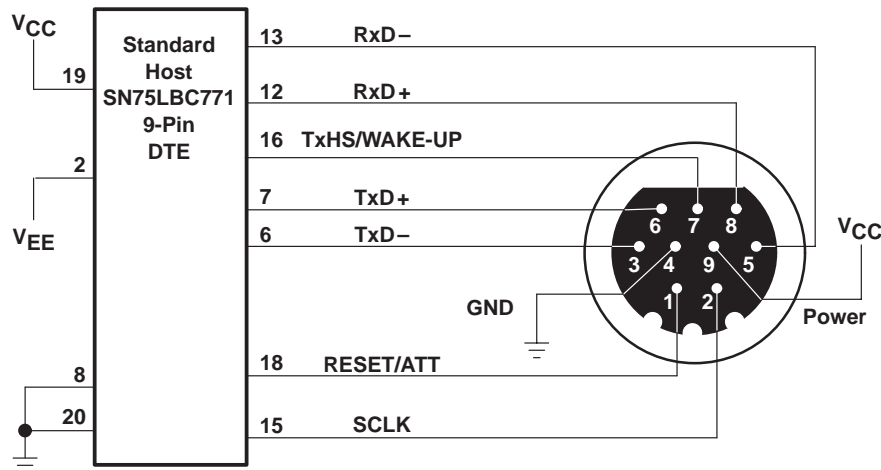
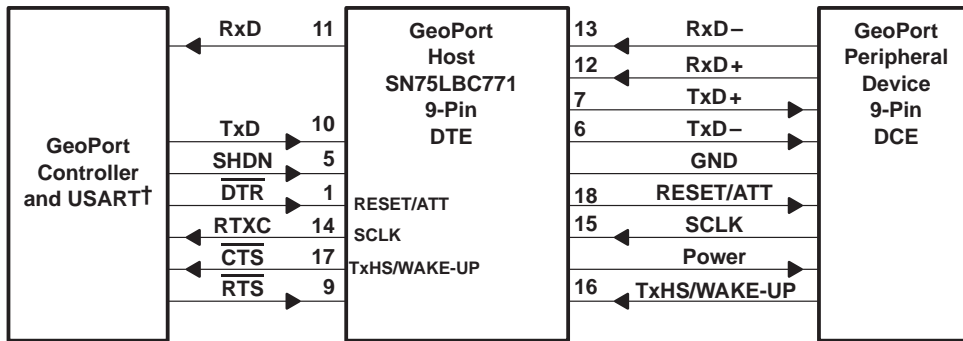
NOTE A: For the input waveform $t_r, t_f \leq 10$ ns

Figure 7. Receiver Enable and Disable Test Circuit and Waveforms

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APPLICATION INFORMATION



† USART = universal synchronous asynchronous receiver transmitter

Figure 8. GeoPort 9-Pin DTE Connection Application

generator characteristics

PARAMETER	TEST CONDITIONS	232/V.28		423/V.10		562		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
V _O	Output voltage magnitude	Open circuit		25		4 6		13.2	V
		3 kΩ ≤ R _L ≤ 7 kΩ		5 15		NA		3.7	V
		R _L = 450 Ω		NA		3.6		NA	V
I _{OS}	Short-circuit output current	V _O = 0		100		150		60	mA
R _(OFF)	Power-off source resistance	V _{CC} = 0, V _O < 2 V		300		NA		300	Ω
I _{O(OFF)}	Power-off output current	V _{CC} = 0, V _O < 6 V		NA		±100		NA	μA
SR	Output voltage slew rate			30		NA		4 30	V/μs
t _t	Output transition time	±3.3 V to ±3.3 V		NA		NA		0.22 2.1	μs
		±3 V to ±3 V		0.04		NA		NA	ui [‡]
		10% to 90%		NA		0.3		NA	ui [‡]
V _{O(RING)}	Output voltage ring			NA		10%		5%	

[‡] ui is the unit interval and is the inverse of the signaling rate (bit time).

APPLICATION INFORMATION

receiver characteristics

PARAMETER	TEST CONDITIONS	232/V.28		423/V.10		562		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
V _I	Input voltage		25		10		25	V	
V _{IT}	Input voltage threshold	V _I < 15 V		-3	3	NA	-3	3	V
		V _I < 10 V		NA		-0.2	0.2	NA	V
R _I	Input resistance	3 V < V _I < 15 V		3	7	NA	3	7	kΩ
		V _I < 10 V		NA		4	NA		kΩ

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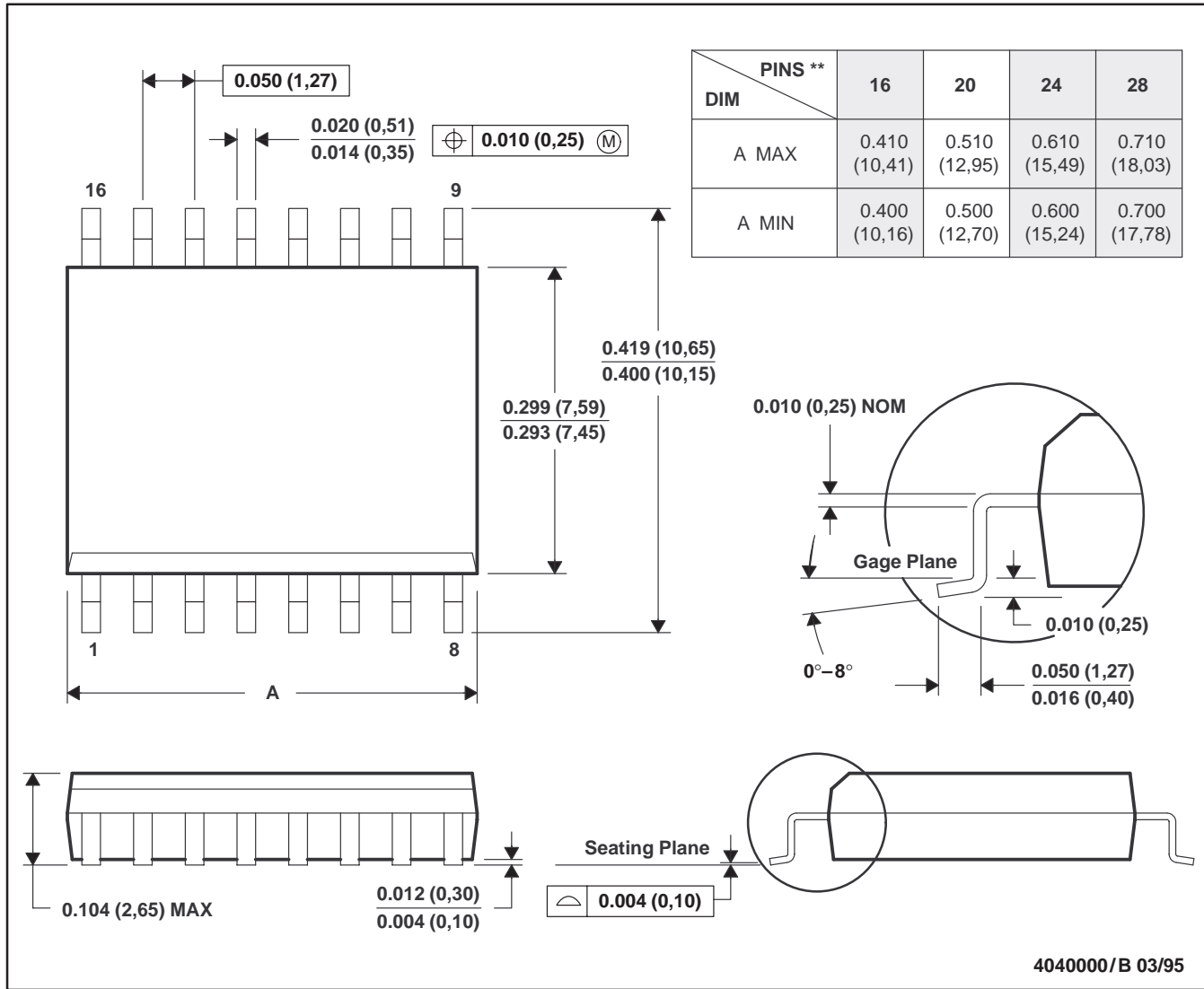
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MECHANICAL INFORMATION

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LBC771DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC771	Samples
SN75LBC771DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC771	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75LBC771DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75LBC771DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC771DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC771DWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6

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