SN65LVDS386, SN65LVDS388A
SN65LVDS390, SN65LVDT386, SN65LVDT388A, SN65LVDT390, SN75LVDS386
SN75LVDS388A, SN75LVDS390, SN75LVDT386, SN75LVDT388A, SN75LVDT390
SLLS394I – SEPTEMBER 1999 – REVISED DECEMBER 2014

SNx5LVDx3xx High-Speed Differential Line Receivers

1 Features

- Four- ('390), Eight- ('388A), or Sixteen- ('386) Line Receivers Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Integrated 110-Ω Line Termination Resistors on LVDT Products
- Designed for Signaling Rates Up to 250 Mbps
- SN65 Versions Bus-Terminal ESD Exceeds 15 kV
- Operates From a Single 3.3-V Supply
- Typical Propagation Delay Time of 2.6 ns
- Output Skew 100 ps (Typical) Part-To-Part Skew Is Less Than 1 ns
- LVTTL Levels Are 5-V Tolerant
- Open-Circuit Fail Safe
- Flow-Through Pinout
- Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch

2 Applications

- Wireless Infrastructure
- Telecom Infrastructure
- Printer

3 Description

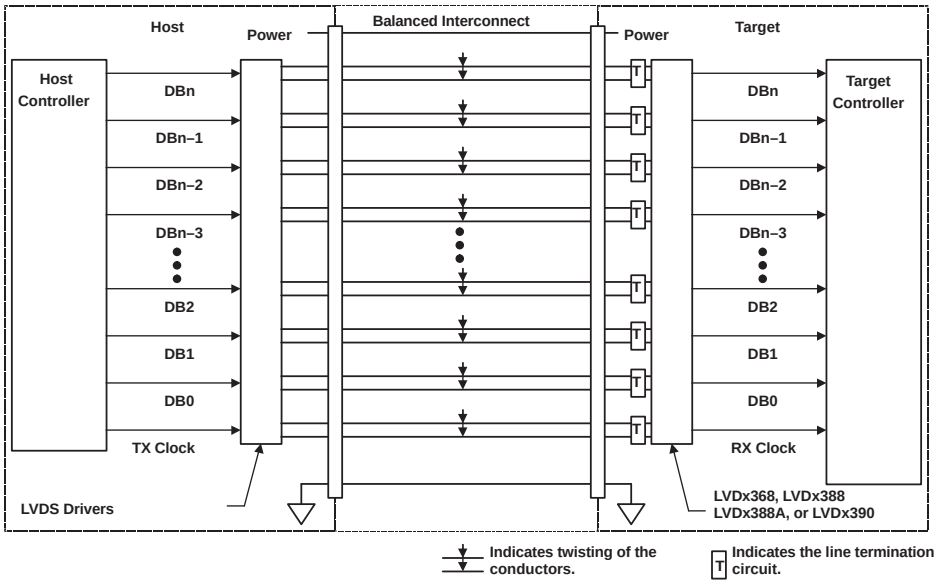
This family of 4-, 8-, or 16-differential line receivers (with optional integrated termination) implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3-V supply rail.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS386	TSSOP (64)	17.00 mm × 6.10 mm
SN65LVDT386		
SN75LVDS386		
SN75LVDT386		
SN65LVDS388A	TSSOP (38)	9.70 mm × 4.40 mm
SN65LVDT388A		
SN75LVDS388A		
SN75LVDT388A		
SN65LVDS390	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm
SN65LVDT390	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm
SN75LVDS390	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm
SN75LVDT390	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (Continued) ... 3
6 Device Options ... 3
7 Pin Configuration and Functions ... 4
8 Specifications ... 8
8.1 Absolute Maximum Ratings ... 8
8.2 ESD Ratings ... 8
8.3 Recommended Operating Conditions ... 8
8.4 Thermal Information ... 8
8.5 Electrical Characteristics ... 9
8.6 Switching Characteristics ... 10
8.7 Typical Characteristics ... 11
9 Parameter Measurement Information ... 13
10 Detailed Description ... 16
10.1 Overview ... 16
10.2 Functional Block Diagram ... 16
10.3 Feature Description ... 16
10.4 Device Functional Modes ... 18
11 Application and Implementation ... 19
11.1 Application Information ... 19
11.2 Typical Application ... 19
12 Power Supply Recommendations ... 25
13 Layout ... 25
13.1 Layout Guidelines ... 25
13.2 Layout Example ... 27
14 Device and Documentation Support ... 29
14.1 Device Support ... 29
14.2 Documentation Support ... 29
14.3 Related Links ... 29
14.4 Trademarks ... 29
14.5 Electrostatic Discharge Caution ... 30
14.6 Glossary ... 30
15 Mechanical, Packaging, and Orderable Information ... 30

4 Revision History

Changes from Revision H (May 2007) to Revision I — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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5 Description (Continued)

Any of the differential receivers provides a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. Additionally, the high-speed switching of LVDS signals almost always requires the use of a line impedance matching resistor at the receiving end of the cable or transmission media. The LVDT products eliminate this external resistor by integrating it with the receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of receivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion, the 8- or 16-channel driver (the SN65LVDS389 or SN65LVDS387, respectively), over 200 million data transfers per second in single-edge clocked systems are possible with little power.

NOTE

The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

6 Device Options

PART NUMBER (1)	TEMPERATURE RANGE	NUMBER OF RECEIVERS	BUS-PIN ESD	SYMBOLIZATION
SN65LVDS386DGG	–40°C to 85°C	16	15 kV	LVDS386
SN65LVDT386DGG	–40°C to 85°C	16	15 kV	LVDT386
SN75LVDS386DGG	0°C to 70°C	16	4 kV	75LVDS386
SN75LVDT386DGG	0°C to 70°C	16	4 kV	75LVDT386
SN65LVDS388ADBT	–40°C to 85°C	8	15 kV	LVDS388A
SN65LVDT388ADBT	–40°C to 85°C	8	15 kV	LVDT388A
SN75LVDS388ADBT	0°C to 70°C	8	4 kV	75LVDS388A
SN75LVDT388ADBT	0°C to 70°C	8	4 kV	75LVDT388A
SN65LVDS390D (PW)	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDT390D (PW)	–40°C to 85°C	4	15 kV	LVDT390
SN75LVDS390D (PW)	0°C to 70°C	4	4 kV	75LVDS390
SN75LVDT390D (PW)	0°C to 70°C	4	4 kV	75LVDT390

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, SN65LVDS386DGGR).

Maximum Recommended Operating Speeds

PART NUMBER	ALL BUFFERS ACTIVE
SN65LVDS386, SN75LVDS386	250 Mbps
SN65LVDS388A, SN75LVDS388A	200 Mbps
SN65LVDS390, SN75LVDS390	200 Mbps

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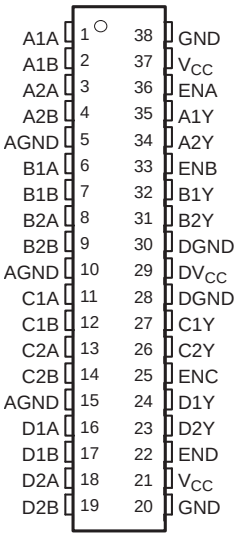
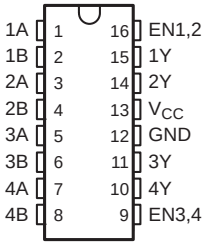
7 Pin Configuration and Functions

'LVDS388A, 'LVDT388A
DBT PACKAGE
(TOP VIEW)

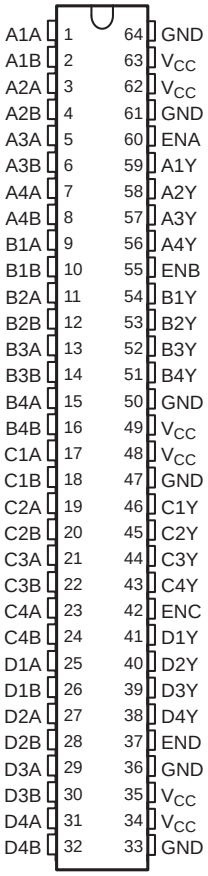


See application section for V_{CC} and GND description.

'LVDS390, 'LVDT390
D OR PW PACKAGE
(TOP VIEW)



'LVDS386, 'LVDT386
DGG PACKAGE
(TOP VIEW)



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Pin Functions: SNx5LVDx390

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	13	–	Supply voltage
GND	12	–	Ground
1A	1	I	Differential (LVDS) non-inverting input
1B	2	I	Differential (LVDS) inverting input
1Y	15	O	LVTTL output signal
2A	3	I	Differential (LVDS) non-inverting input
2B	4	I	Differential (LVDS) inverting input
2Y	14	O	LVTTL output signal
3A	5	I	Differential (LVDS) non-inverting input
3B	6	I	Differential (LVDS) inverting input
3Y	11	O	LVTTL output signal
4A	7	I	Differential (LVDS) non-inverting input
4B	8	I	Differential (LVDS) inverting input
4Y	10	O	LVTTL output signal
EN1, 2	16	I	Enable for channels 1 and 2
EN3, 4	9	I	Enable for channels 3 and 4

Pin Functions: SNx5LVDx388A

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	21, 37	–	Supply voltage
DVCC	29	–	Digital supply voltage
GND	20, 38	–	Ground
DGND	28, 30	–	Digital ground
AGND	5, 10, 15	–	Analog ground
A1A	1	I	Differential (LVDS) non-inverting input
A1B	2	I	Differential (LVDS) inverting input
A1Y	35	O	LVTTL output signal
A2A	3	I	Differential (LVDS) non-inverting input
A2B	4	I	Differential (LVDS) inverting input
A2Y	34	O	LVTTL output signal
B1A	6	I	Differential (LVDS) non-inverting input
B1B	7	I	Differential (LVDS) inverting input
B1Y	32	O	LVTTL output signal
B2A	8	I	Differential (LVDS) non-inverting input
B2B	9	I	Differential (LVDS) inverting input
B2Y	31	O	LVTTL output signal
C1A	11	I	Differential (LVDS) non-inverting input
C1B	12	I	Differential (LVDS) inverting input
C1Y	27	O	LVTTL output signal
C2A	13	I	Differential (LVDS) non-inverting input
C2B	14	I	Differential (LVDS) inverting input
C2Y	26	O	LVTTL output signal
D1A	16	I	Differential (LVDS) non-inverting input
D1B	17	I	Differential (LVDS) inverting input
D1Y	24	O	LVTTL output signal
D2A	18	I	Differential (LVDS) non-inverting input

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Pin Functions: SNx5LVDx388A (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
D2B	19	I	Differential (LVDS) inverting input
D2Y	23	O	LVTTL output signal
ENA	36	I	Enable for channel A
ENB	33	I	Enable for channel B
ENC	25	I	Enable for channel C
END	22	I	Enable for channel D

Pin Functions: SNx5LVDx386

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	34, 35, 48, 49, 62, 63	–	Supply voltage
GND	33, 36, 47, 50, 61, 64	–	Ground
A1A	1	I	Differential (LVDS) non-inverting input
A1B	2	I	Differential (LVDS) inverting input
A1Y	59	O	LVTTL output signal
A2A	3	I	Differential (LVDS) non-inverting input
A2B	4	I	Differential (LVDS) inverting input
A2Y	58	O	LVTTL output signal
A3A	5	I	Differential (LVDS) non-inverting input
A3B	6	I	Differential (LVDS) inverting input
A3Y	57	O	LVTTL output signal
A4A	7	I	Differential (LVDS) non-inverting input
A4B	8	I	Differential (LVDS) inverting input
A4Y	56	O	LVTTL output signal
B1A	9	I	Differential (LVDS) non-inverting input
B1B	10	I	Differential (LVDS) inverting input
B1Y	54	O	LVTTL output signal
B2A	11	I	Differential (LVDS) non-inverting input
B2B	12	I	Differential (LVDS) inverting input
B2Y	53	O	LVTTL output signal
B3A	13	I	Differential (LVDS) non-inverting input
B3B	14	I	Differential (LVDS) inverting input
B4Y	52	O	LVTTL output signal
B4A	15	I	Differential (LVDS) non-inverting input
B4B	16	I	Differential (LVDS) inverting input
B2Y	51	O	LVTTL output signal
C1A	17	I	Differential (LVDS) non-inverting input
C1B	18	I	Differential (LVDS) inverting input
C1Y	46	O	LVTTL output signal
C2A	19	I	Differential (LVDS) non-inverting input
C2B	20	I	Differential (LVDS) inverting input
C2Y	45	O	LVTTL output signal
C3A	21	I	Differential (LVDS) non-inverting input
C3B	22	I	Differential (LVDS) inverting input
C3Y	44	O	LVTTL output signal

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Pin Functions: SNx5LVDx386 (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
C4A	23	I	Differential (LVDS) non-inverting input
C4B	24	I	Differential (LVDS) inverting input
C4Y	43	O	LVTTL output signal
D1A	25	I	Differential (LVDS) non-inverting input
D1B	26	I	Differential (LVDS) inverting input
D1Y	41	O	LVTTL output signal
D2A	27	I	Differential (LVDS) non-inverting input
D2B	28	I	Differential (LVDS) inverting input
D2Y	40	O	LVTTL output signal
D3A	29	I	Differential (LVDS) non-inverting input
D3B	30	I	Differential (LVDS) inverting input
D3Y	39	O	LVTTL output signal
D4A	31	I	Differential (LVDS) non-inverting input
D4B	32	I	Differential (LVDS) inverting input
D4Y	38	O	LVTTL output signal
ENA	60	I	Enable for channel A
ENB	55	I	Enable for channel B
ENC	42	I	Enable for channel C
END	37	I	Enable for channel D

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC} [2]	Supply voltage range		–0.5	4	V
V_I	Voltage range:	Enables or Y	–0.5	6	V
		A or B	–0.5	4	V
I_O	Output current	Y	–12	12	mA
$\|V_{ID}\|$	Differential input voltage magnitude	SN65LVDT' or SN75LVDT' only		1	V
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	SN65' (A, B, and GND)	Class 3, A	15000	V
			Class 3, B	400	V
		SN75' (A, B, and GND)	Class 2, A	4000	V
			Class 2, B	400	V
	Lead temperature 1.6 mm (1/16 in) from case for 10 seconds				°C

(1) Tested in accordance with MIL-STD-883C Method 3015.7.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_O	Output current	Y	–8		8	mA
$\|V_{ID}\|$	Magnitude of differential input voltage		0.1		0.6	V
V_{IC}	Common-mode input voltage, See Figure 1		$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	V
					$V_{CC} - 0.8$	
T_A	Operating free-air temperature	SN75'	0		70	°C
		SN65'	–40		85	°C

8.4 Thermal Information

THERMAL METRIC[1]		SN65LVDS386, SN65LVDT386, SN75LVDS386, SN75LVDT386	SN65LVDS388A, SN65LVDT388A, SN75LVDS388A, SN75LVDT388A	SN65LVDS390, SN65LVDT390, SN75LVDS390, SN75LVDT390		UNIT
		DGG	DBT	D	PW	
		64 PINS	38 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.3				mW/°C
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.2				
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7				
ψ_{JT}	Junction-to-top characterization parameter	0.4				
ψ_{JB}	Junction-to-board characterization parameter	27.4				

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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Thermal Information (continued)

THERMAL METRIC[1]	SN65LVDS386, SN65LVDT386, SN75LVDS386, SN75LVDT386	SN65LVDS388A, SN65LVDT388A, SN75LVDS388A, SN75LVDT388A	SN65LVDS390, SN65LVDT390, SN75LVDS390, SN75LVDT390		UNIT
	DGG	DBT	D	PW	
	64 PINS	38 PINS	16 PINS	16 PINS	
Power Rating: $T_A \leq 25°C$	2094	1071	950	774	mW
Power Rating: $T_A = 70°C$	1342	688	608	496	
Power Rating: $T_A = 85°C$	1089	556	494	402	

8.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 9 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold			–100			mV
V_{OH}	High-level output voltage		$I_{OH} = -8$ mA	2.4	3		V
V_{OL}	Low-level output voltage		$I_{OL} = 8$ mA		0.2	0.4	V
I_{CC}	Supply current	'LVDx386	Enabled, No load		50	70	mA
		'LVDx388A			22	40	
		'LVDx390			8	18	
		'LVDx386	Disabled			3	
		'LVDx388A				3	
		'LVDx390				1.5	
I_I	Input current (A or B inputs)	'LVDS	$V_I = 0$ V		–13	–20	µA
			$V_I = 2.4$ V	–1.2	–3		
		'LVDT	$V_I = 0$ V, other input open			–40	
			$V_I = 2.4$ V, other input open	–2.4			
I_{ID}	Differential input current $\lvert I_{IA} - I_{IB} \rvert$	'LVDS	$V_{IA} = 0$ V, $V_{IB} = 0.1$ V, $V_{IA} = 2.4$ V, $V_{IB} = 2.3$ V			±2	µA
I_{ID}	Differential input current $(I_{IA} - I_{IB})$	'LVDT	$V_{IA} = 0.2$ V, $V_{IB} = 0$ V, $V_{IA} = 2.4$ V, $V_{IB} = 2.2$ V	1.5		2.2	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	'LVDS	$V_{CC} = 0$ V, $V_I = 2.4$ V		12	±20	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	'LVDT	$V_{CC} = 0$ V, $V_I = 2.4$ V			±40	µA
I_{IH}	High-level input current (enables)		$V_{IH} = 2$ V			10	µA
I_{IL}	Low-level input current (enables)		$V_{IL} = 0.8$ V			10	µA
I_{OZ}	High-impedance output current		$V_O = 0$ V			±1	µA
			$V_O = 3.6$ V			10	
C_{IN}	Input capacitance, A or B input to GND		V_{ID} = 0.4sin2.5E09t V		5		pF
$Z_{(t)}$	Termination impedance		V_{ID} = 0.4sin2.5E09t V	88		132	Ω

(1) All typical values are at 25°C and with a 3.3-V supply.

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8.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 10	1	2.6	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	2.5	4	ns
t_r	Output signal rise time		500	800	1200	ps
t_f	Output signal fall time		500	800	1200	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			150	600	ps
$t_{sk(o)}$	Output skew(2)			100	400	ps
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 11		7	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			7	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

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8.7 Typical Characteristics

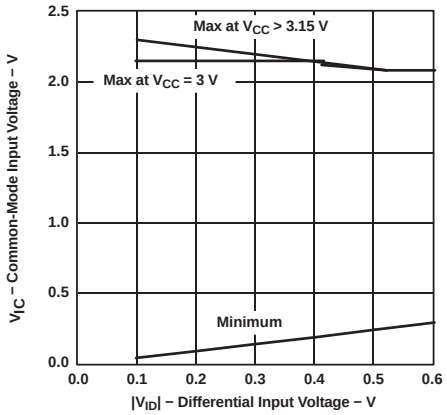

Figure 1. Common-Mode Input Voltage vs Differential Input Voltage

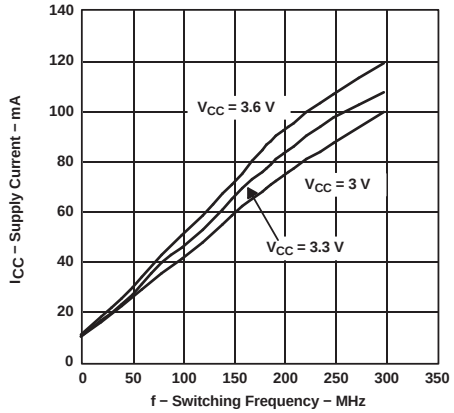

Figure 2. LVDX390 Supply Current vs Switching Frequency

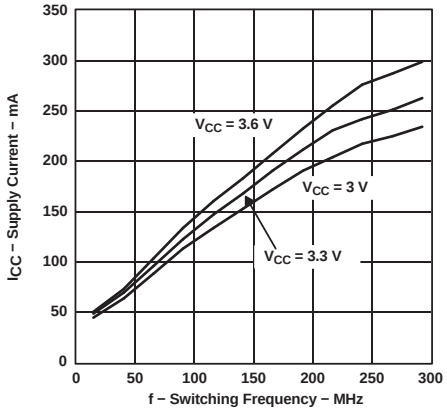

Figure 3. LVDX388A Supply Current vs Switching Frequency

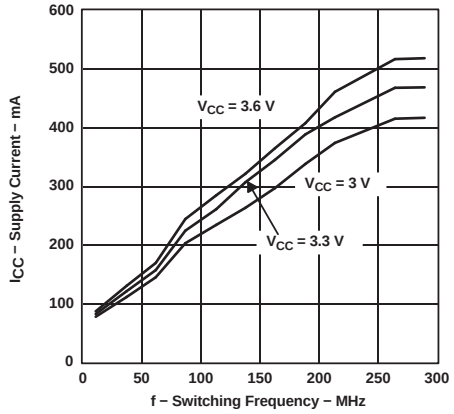

Figure 4. LVDX386 Supply Current vs Switching Frequency

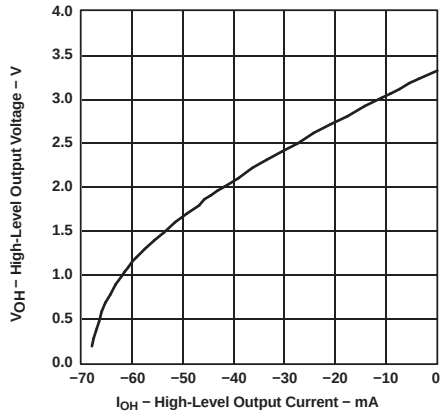

Figure 5. High-Level Output Voltage vs High-Level Output Current

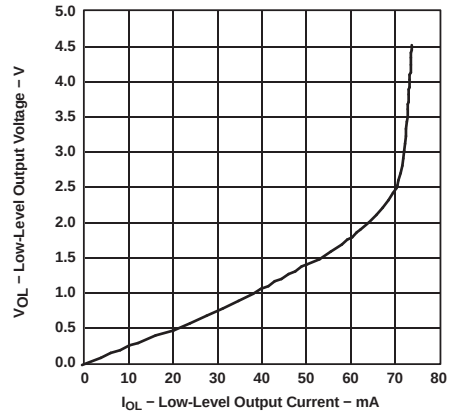

Figure 6. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

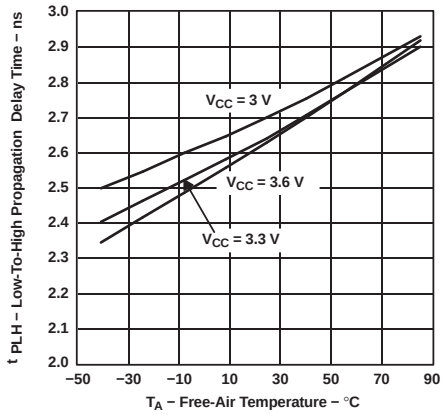

Figure 7. Low-to-High Propagation Delay Time vs Free-Air Temperature

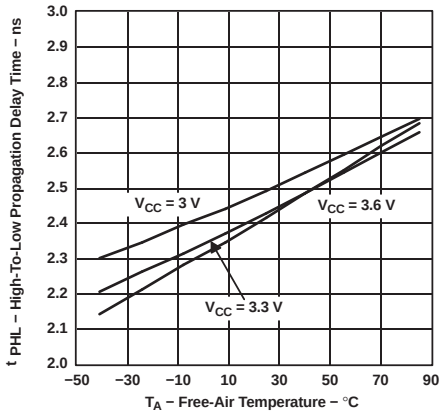

Figure 8. High-to-Low Propagation Delay Time vs Free-Air Temperature

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9 Parameter Measurement Information

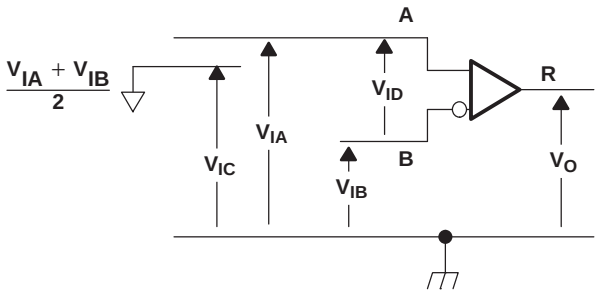

Figure 9. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

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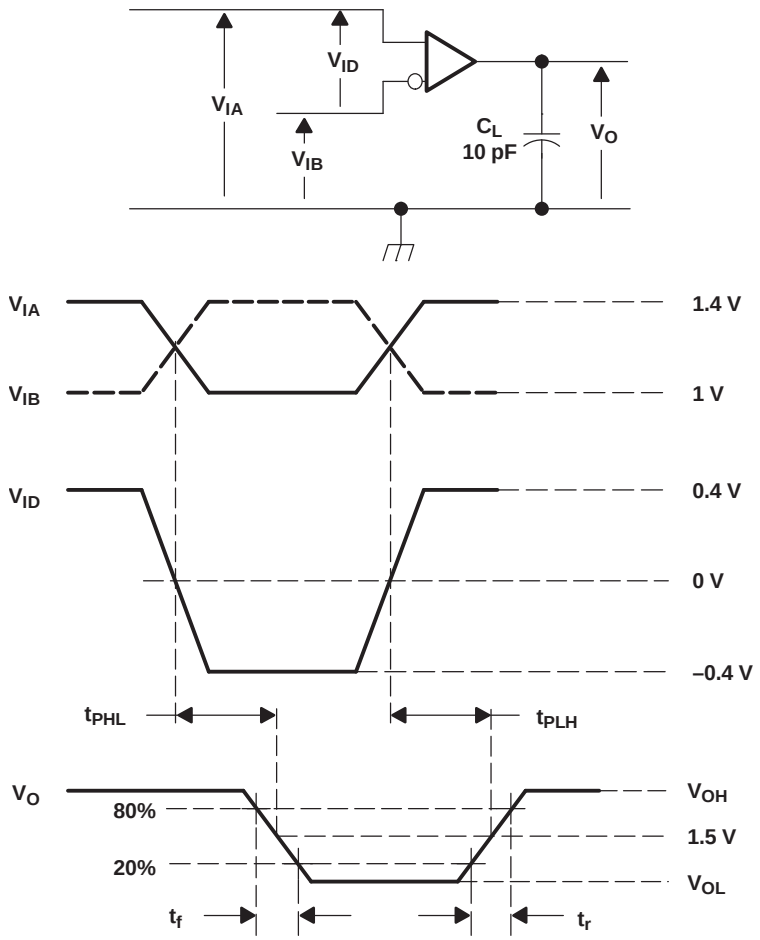

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test.

Figure 10. Timing Test Circuit and Wave Forms

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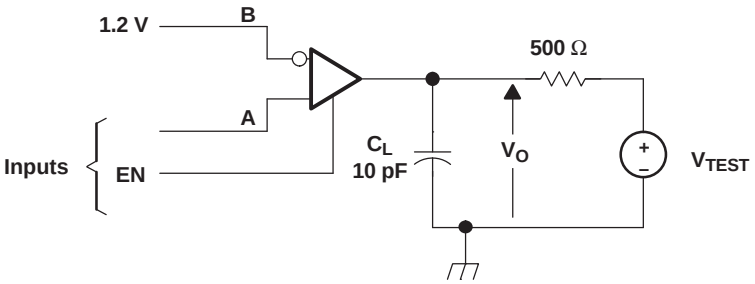


NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test.

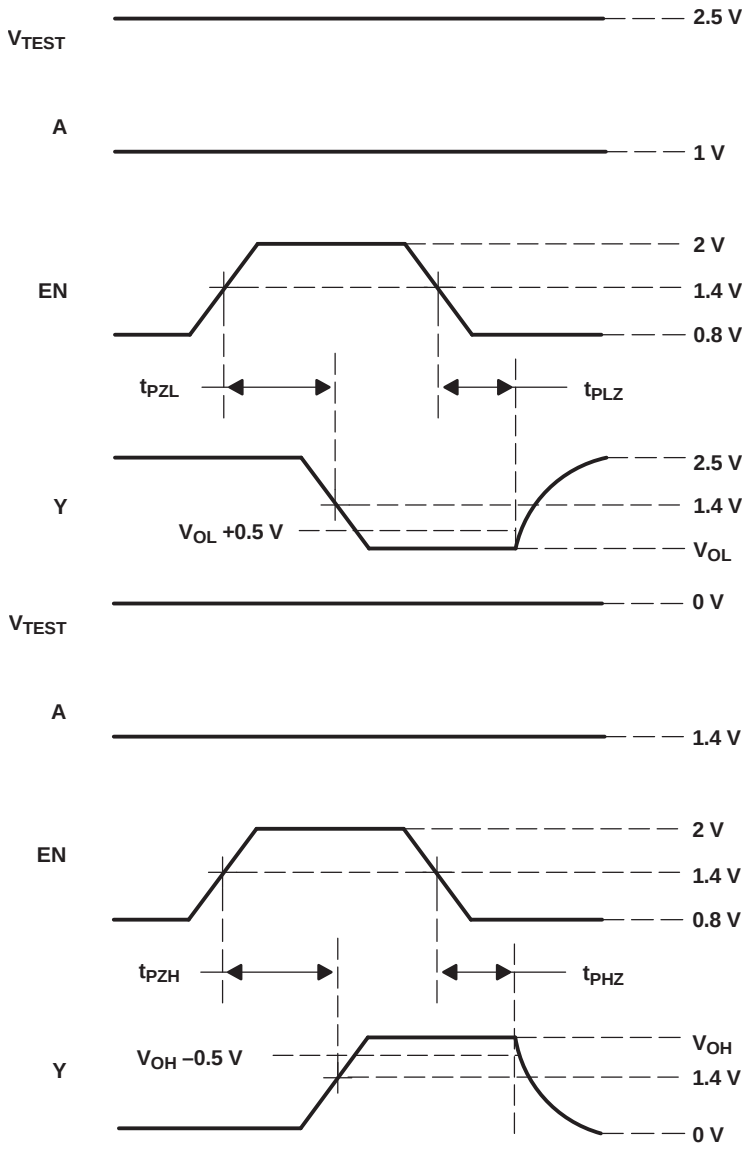


Figure 11. Enable and Disable Time Test Circuit and Waveforms

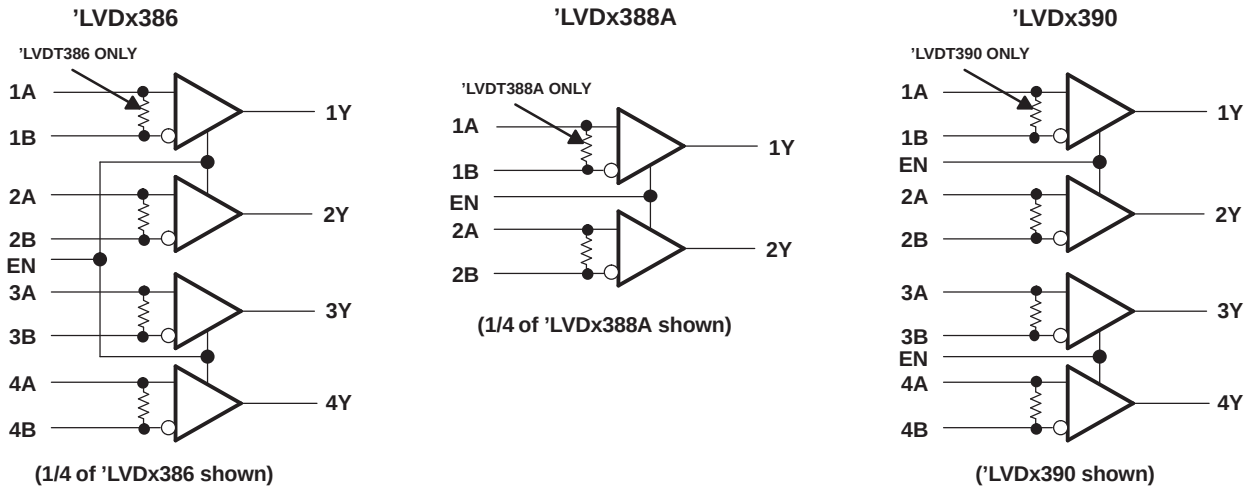
10 Detailed Description

10.1 Overview

The SNx5LVDS3xx devices are LVDS line receivers. They operate from a single supply that is nominally 3.3 V, but can be as low as 3.0 V and as high as 3.6 V. The input signals to the SNx5LVDS3xx are differential LVDS signals. The output of the device is a LVTTL digital signal. This LVDS receiver requires ±100 mV of input signal to determine the correct state of the received signal. Compliant LVDS receivers can accept input signals with a common-mode range between 0.05 V and 2.35 V. As the common-mode output voltage of an LVDS driver is 1.2 V, the SNx5LVDS3xx correctly determines the line state when operated with a 1-V ground shift between driver and receiver.

The SNx5LVDT3xx devices are also LVDS receivers. These devices differ from their LVDS variants in that they incorporate integrated termination resistors along with the receivers. These terminations would take the place of the matched-load line termination needed in any LVDS communication channel. The SNx5LVDT3xx can be used in a point-to-point system or in a multidrop system when it is the last receiver on the multidrop bus. The SNx5LVDT3xx should not be used at every node in a multidrop system as this would change the loaded bus impedance throughout the bus resulting in multiple reflections and signal distortion. While the integration of a bus terminating resistor is always attractive in a point-to-point LVDS communication channel, the value of 8- and 16-channel LVDS receivers with their 8 and 16 termination resistors is clear for many reasons: cost, signal integrity, manufacturing, and so on.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Receiver Output States

When the receiver differential input signal is greater than 100 mV, the receiver output is high; and when the differential input voltage is below –100 mV, the receiver output is low. When the input voltage is between these thresholds (example: between –100 mV and 100 mV), the receiver output is indeterminate. It may be high or low. A special case occurs when the input to the receiver is open-circuited, which is covered in *Receiver Open-Circuit Fail-safe*. When the receiver is disabled, the receiver outputs will be high-impedance.

10.3.2 Receiver Open-Circuit Fail-safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. The TI LVDS receiver is different in how it handles the open-input circuit situation, however.

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Feature Description (continued)

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors, as shown in Figure 12. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

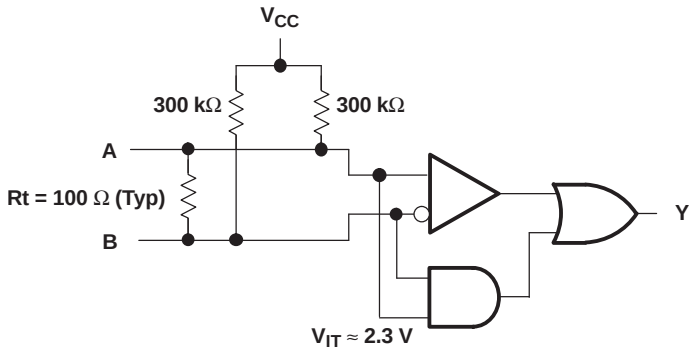

Figure 12. Open-Circuit Fail-Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 12. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

10.3.3 Common-Mode Range

The SNx5LVDx3xx receivers operate over an input common-mode range of ½ × V_{ID} V to 2.4 – ½ × V_{ID} V. If the input signal is anywhere within this range and has a differential magnitude greater than or equal to 100 mV, the receivers correctly output the LVDS bus state.

10.3.4 General Purpose Comparator

While the SNx5LVDx3xx receivers are LVDS standard-compliant receivers, their utility and applications extend to a wider range of signals. As long as the input signals are within the required differential and common-mode voltage ranges mentioned above, the receiver output will be a faithful representation of the input signal.

10.3.5 Receiver Equivalent Schematics

The receiver equivalent input and output schematic diagrams are shown in Figure 13. The receiver input is a high-impedance differential pair in the case of the SNx5LVDS3xx. The SNx5LVDT3xx receivers include internal termination resistor of 110 Ω across the input port. 7-V Zener diodes are included on each input to provide ESD protection. The receiver output structure shown is a CMOS inverter with an additional Zener diode, again for ESD protection.

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Feature Description (continued)

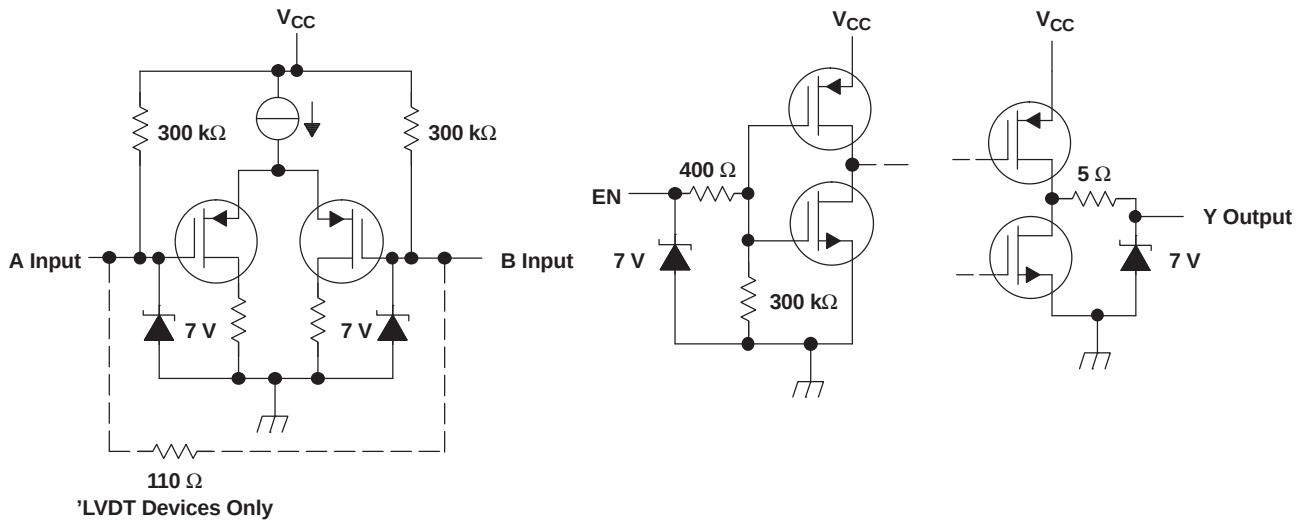

Figure 13. Equivalent Input and Output Schematic Diagrams

10.4 Device Functional Modes

Table 2. Function Table

SNx5LVD386/388A/390 and SNx5LVDT386/388A/390		
DIFFERENTIAL INPUT(1)	**ENABLES(1)**	**OUTPUT(1)**
A-B	**EN**	**Y**
$V_{ID} \geq 100$ mV	H	H
-100 mV $< V_{ID} \leq 100$ mV	H	?
$V_{ID} \leq -100$ mV	H	L
X	L	Z
Open	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high-impedance (off), ? = indeterminate

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The SNx5LVDx3xx devices are LVDS receivers. These devices are generally used as building blocks for high-speed, point-to-point data transmission where ground differences are less than 1 V. LVDS drivers and receivers provide high-speed signaling rates that are often implemented with ECL class devices without the ECL power and dual-supply requirements.

11.1.1 Analog and Digital Grounds and Power Supplies

Although it is not necessary to separate out the analog and digital supplies and grounds on the SN65LVDS/T388A and SN75LVDS/T388A devices, the pinout provides the user that option. To help minimize or perhaps eliminate switching noise being coupled between the two supplies, the user could lay out separate supply and ground planes for the designated pinout.

Most applications probably have all grounds connected together and all power supplies connected together. This configuration was used while characterizing and setting the data sheet parameters.

11.2 Typical Application

11.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 14.

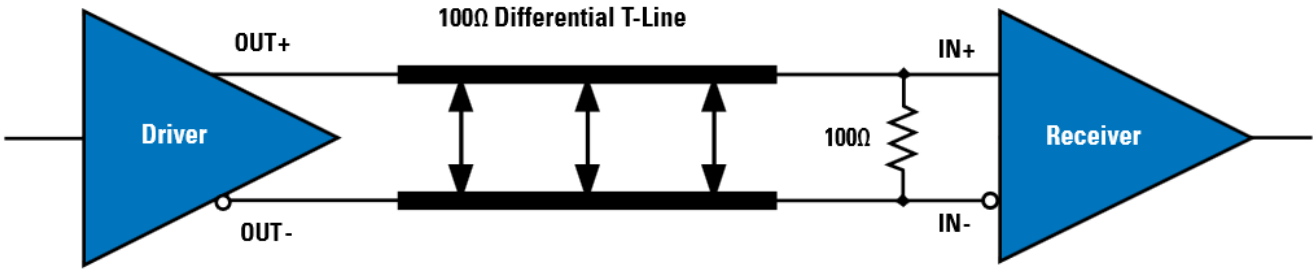

Figure 14. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 14 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

Typical Application (continued)

11.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 5.0 V
Driver Signaling Rate	DC to 200 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Driver Supply Voltage

An LVDS driver such as the SN65LVDS387 is operated from a single supply. The device can support operation with a supply as low as 3 V and as high as 3.6 V. The differential output voltage is nominally 340 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for a 3.3-V supply.

11.2.1.2.2 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very-low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson, equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. [(1)]

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}}\right) \times T_{\text{Rise Time}} \tag{1}$$

$$C_{LVDS} = \left(\frac{1A}{0.2V}\right) \times 200\ \text{ps} = 0.001\ \mu F \tag{2}$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

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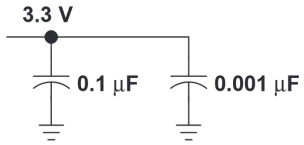

Figure 15. Recommended LVDS Bypass Capacitor Layout

11.2.1.2.3 Driver Output Voltage

The SNx5LVDSxx driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 340 mV. This 340 mV is the absolute value of the differential swing ($V_{OD} = |V^+ – V^–|$). The peak-to-peak differential voltage is twice this value, or 680 mV.

11.2.1.2.4 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect is between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

11.2.1.2.5 PCB Transmission Lines

As per SNLA187, Figure 16 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 16 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

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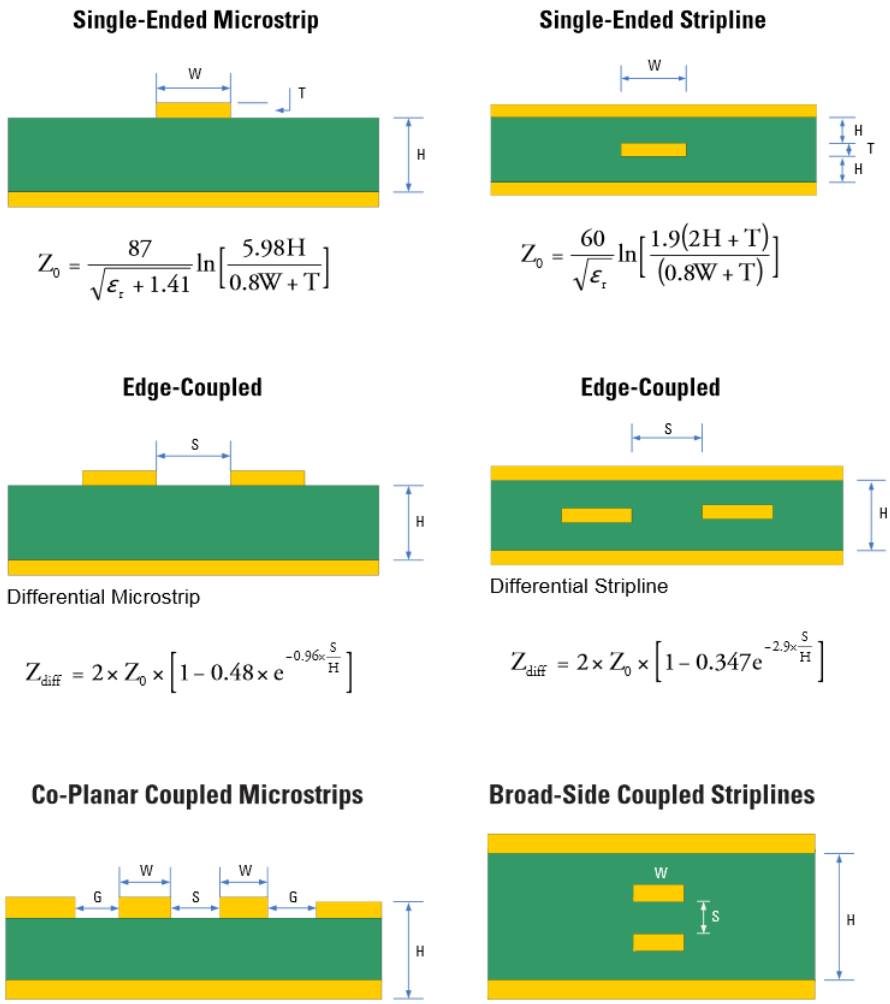

Figure 16. Controlled-Impedance Transmission Lines

11.2.1.2.6 Termination Resistor

As shown earlier, an LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 Ω and 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver, which is exactly what is offered with a device like the SN65LVDT386. The SN65LVDT386 provides all the functionality and performance of the SN65LVDT386 receiver, with the added feature of an integrated termination load.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line. In such an environment, SN65LVDT386 receivers could be used for loads branching off the main bus, with an SN65LVDT386 used only at the bus end.

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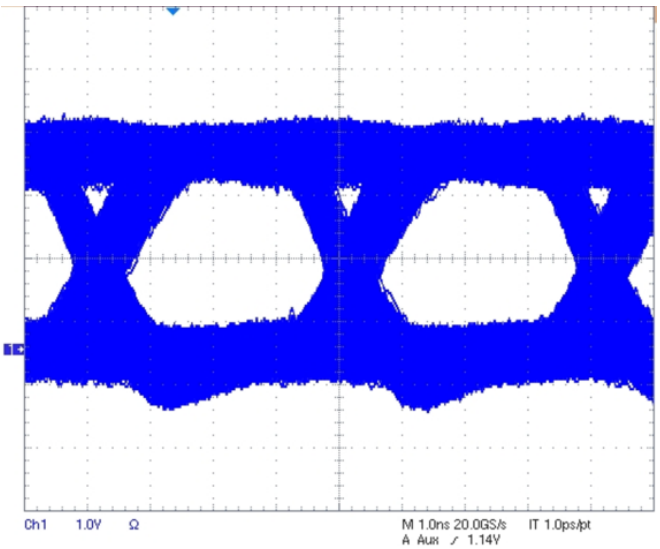
11.2.1.3 Application Curve

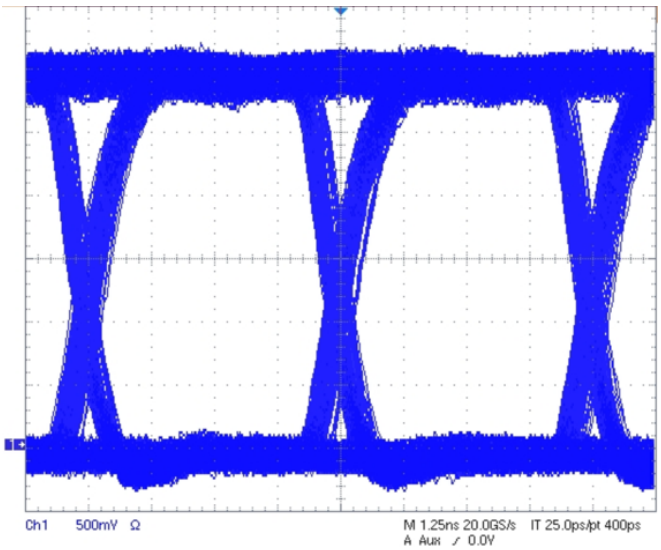


All 16 Rx Switching at 250 Mbps:

T_A = 25°C
V_{CC} = 3.6 V
PRBS = 2^{23-1}
Ch1 = Xyy

Where x represents the Rx Group: A, B, C, or D
y represents the Rx: 1, 2, 3, or 4

Figure 17. Typical Eye Pattern SN65LVDS386



All 8 Rx Switching at 200 Mbps:

T_A = 25°C
V_{CC} = 3.6 V
PRBS = 2^{23-1}
Ch1 = Xyy

Where: x represents the Rx Group: A, B, C, or D
y represents the Rx: 1 or 2

Figure 18. Typical Eye Pattern SN65LVDS388A

11.2.2 Multidrop Communications

A second common application of LVDS buffers is a multidrop topology. In a multidrop configuration, a single driver and a shared bus are present, along with two or more receivers (with a maximum permissible number of 32 receivers). Figure 19 below shows an example of a multidrop system.

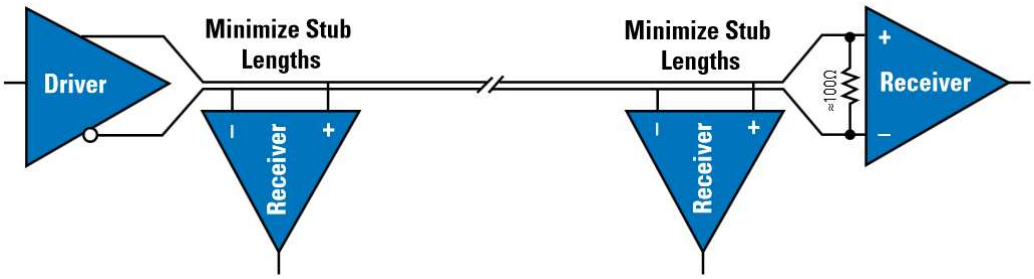


Figure 19. Multidrop Topology

11.2.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 200 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	2 to 32
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

11.2.2.2 Detailed Design Procedure

11.2.2.2.1 Interconnecting Media

The interconnect in a multidrop system differs considerably from a point-to-point system. While point-to-point interconnects are straightforward, and well understood, the bus type architecture encountered with multidrop systems requires more careful attention. We will use Figure 19 above to explore these details.

The most basic multidrop system would include a single driver, located at a bus origin, with multiple receiver nodes branching off the main line, and a final receiver at the end of the transmission line, co-located with a bus termination resistor. While this would be the most basic multidrop system, it has several considerations not yet explored.

The location of the transmitter at one bus end allows the design concerns to be simplified, but this comes at the cost of flexibility. With a transmitter located at the origin, a single bus termination at the far-end is required. The far-end termination absorbs the incident traveling wave. The flexibility lost with this arrangement is thus: if the single transmitter needed to be relocated on the bus, at any location other than the origin, we would be faced with a bus with one open-circuited end and one properly terminated end. Locating the transmitter say in the middle of the bus may be desired to reduce (by ½) the maximum flight time from the transmitter to receiver.

Another new feature in Figure 19 is clear in that every node branching off the main line results in stubs. The stubs should be minimized in any case, but have the unintended effect of locally changing the loaded impedance of the bus.

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded multipoint or multidrop bus is defined by $\sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching must be accounted for in the noise budget.

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12 Power Supply Recommendations

The LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 2.4 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used and are covered in *Driver Bypass Capacitance*.

13 Layout

13.1 Layout Guidelines

13.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 20.

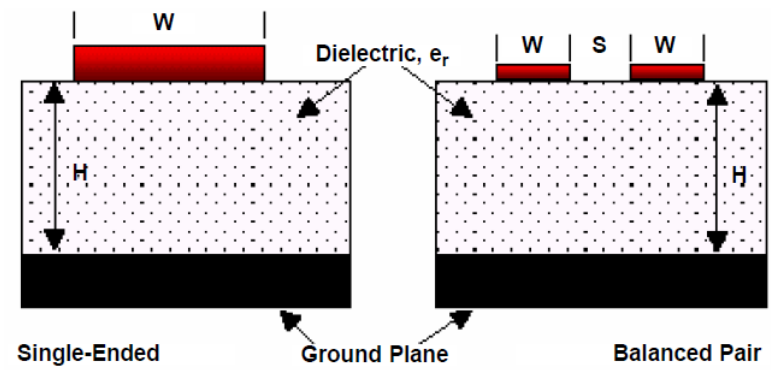

Figure 20. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1, 2, and 3 provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

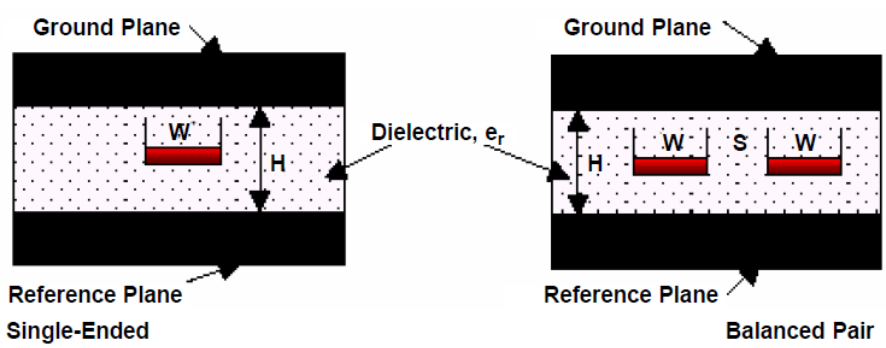

Figure 21. Stripline Topology

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

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Layout Guidelines (continued)

13.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise and fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

13.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 22.

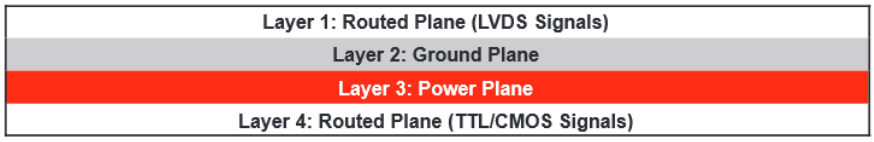

Figure 22. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 23.

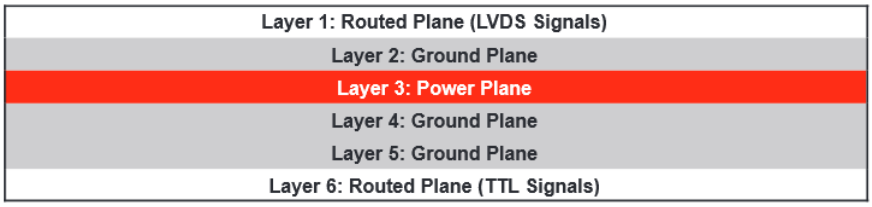

Figure 23. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

13.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

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Layout Guidelines (continued)

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

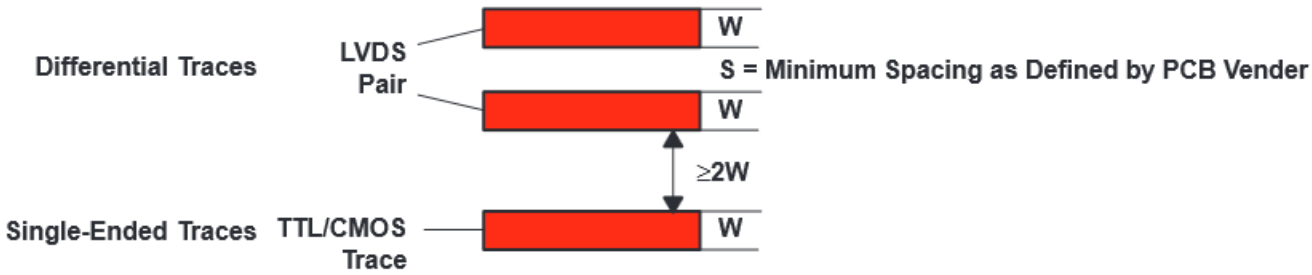

Figure 24. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

13.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

13.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 25.

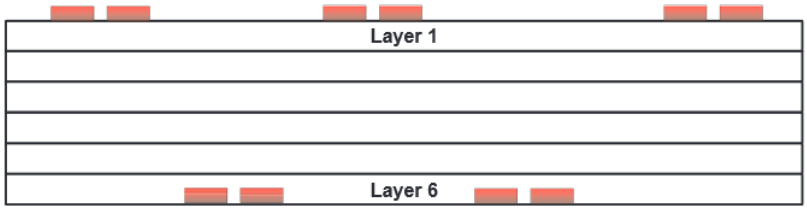

Figure 25. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 26. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

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Layout Example (continued)

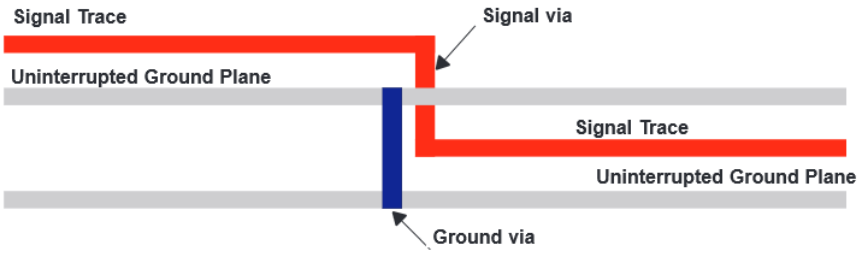

Figure 26. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

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14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

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14.1.2 Other LVDS Products

For other products and application notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

14.2 Documentation Support

14.2.1 Related Information

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

14.3 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65LVDS386	Click here	Click here	Click here	Click here	Click here
SN65LVDS388A	Click here	Click here	Click here	Click here	Click here
SN65LVDS390	Click here	Click here	Click here	Click here	Click here
SN65LVDT386	Click here	Click here	Click here	Click here	Click here
SN65LVDT388A	Click here	Click here	Click here	Click here	Click here
SN65LVDT390	Click here	Click here	Click here	Click here	Click here
SN75LVDS386	Click here	Click here	Click here	Click here	Click here
SN75LVDS388A	Click here	Click here	Click here	Click here	Click here
SN75LVDS390	Click here	Click here	Click here	Click here	Click here
SN75LVDT386	Click here	Click here	Click here	Click here	Click here
SN75LVDT388A	Click here	Click here	Click here	Click here	Click here
SN75LVDT390	Click here	Click here	Click here	Click here	Click here

14.4 Trademarks

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All other trademarks are the property of their respective owners.

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14.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS386DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS386DGGG4	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS386DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS388ADBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS388A	Samples
SN65LVDS388ADBTG4	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS388A	Samples
SN65LVDS388ADBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS388A	Samples
SN65LVDS390D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDT386DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT386DGGG4	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT386DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT386DGGRG4	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT388ADBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT388A	Samples
SN65LVDT388ADBTG4	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT388A	Samples
SN65LVDT388ADBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT388A	Samples
SN65LVDT390D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDT390PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN65LVDT390PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN75LVDS386DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS386	Samples
SN75LVDS386DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS386	Samples
SN75LVDS388ADBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS388A	Samples
SN75LVDS390D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS390	Samples
SN75LVDS390DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS390	Samples
SN75LVDS390PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDS390PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDS390PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDT386DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT386	Samples
SN75LVDT386DGGG4	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT386	Samples
SN75LVDT386DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT386	Samples
SN75LVDT388ADBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT388ADBTG4	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT388ADBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT388ADBTRG4	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT390D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDT390	Samples
SN75LVDT390DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDT390	Samples
SN75LVDT390PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples
SN75LVDT390PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDT390PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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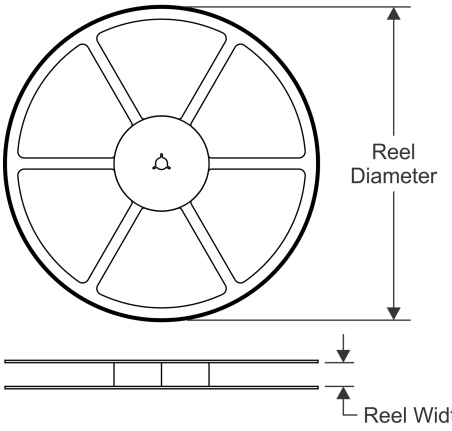
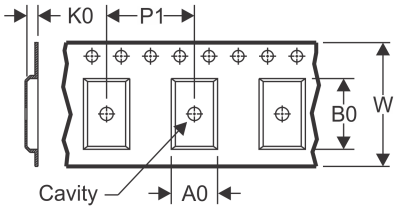
TAPE AND REEL INFORMATION

REEL DIMENSIONS

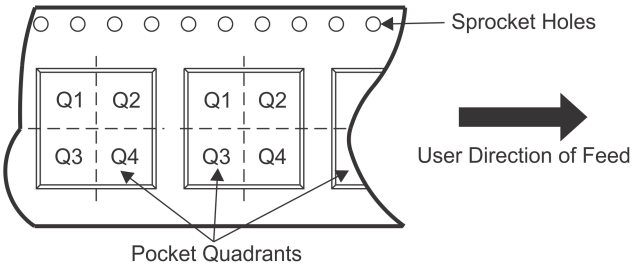


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

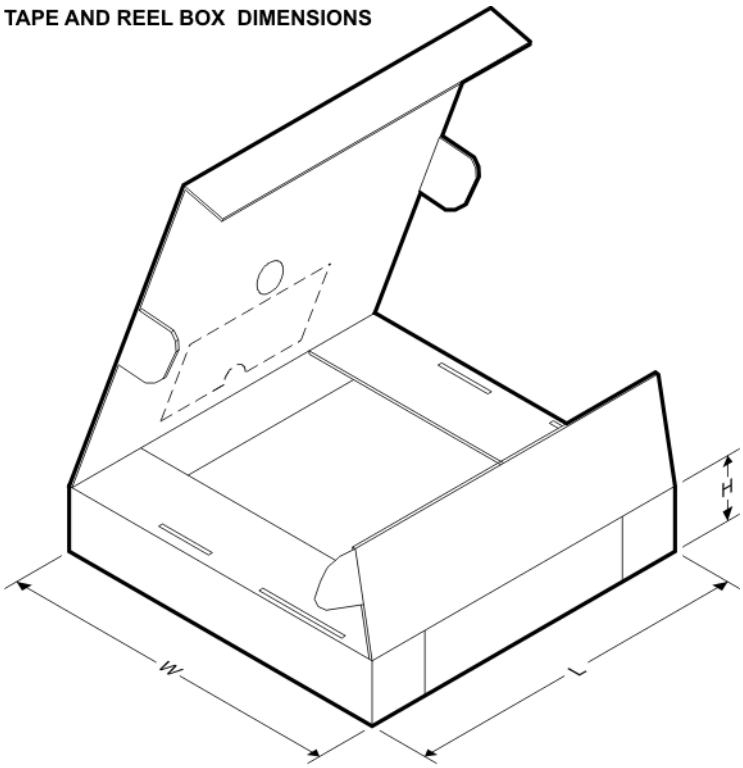
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDS388ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDS390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDT388ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDT390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75LVDS386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN75LVDS390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LVDS390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75LVDT386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN75LVDT388ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75LVDT390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LVDT390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

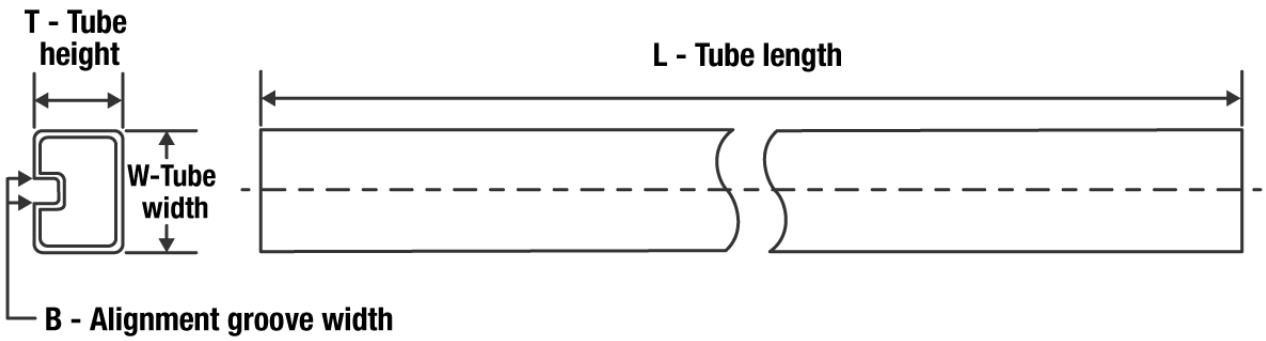
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDS388ADBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0
SN65LVDS390DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS390PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDT386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDT388ADBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0
SN65LVDT390PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN75LVDS386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN75LVDS390DR	SOIC	D	16	2500	350.0	350.0	43.0
SN75LVDS390PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN75LVDT386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN75LVDT388ADBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0
SN75LVDT390DR	SOIC	D	16	2500	350.0	350.0	43.0
SN75LVDT390PWR	TSSOP	PW	16	2000	350.0	350.0	43.0

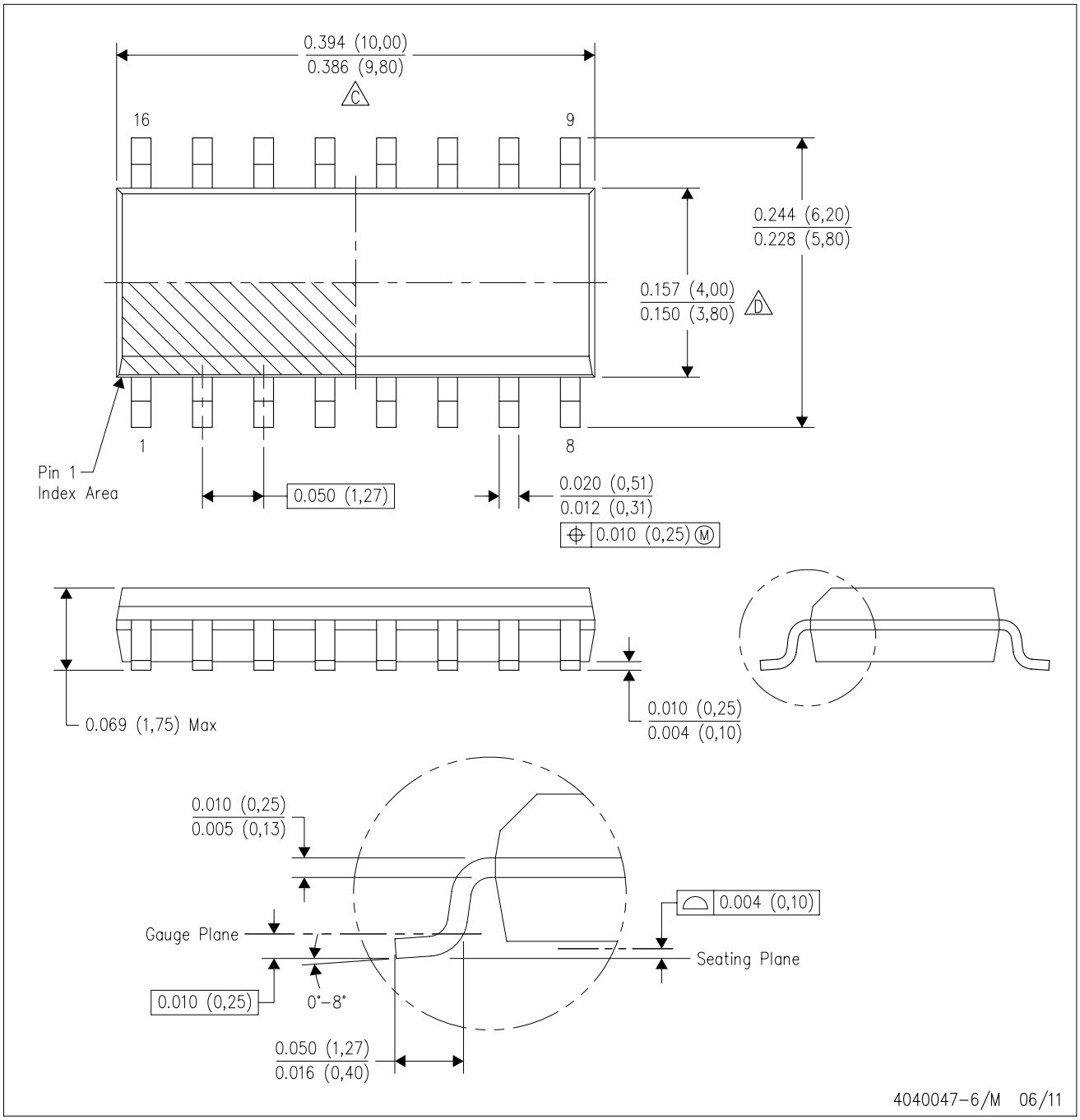
TUBE



*All dimensions are nominal

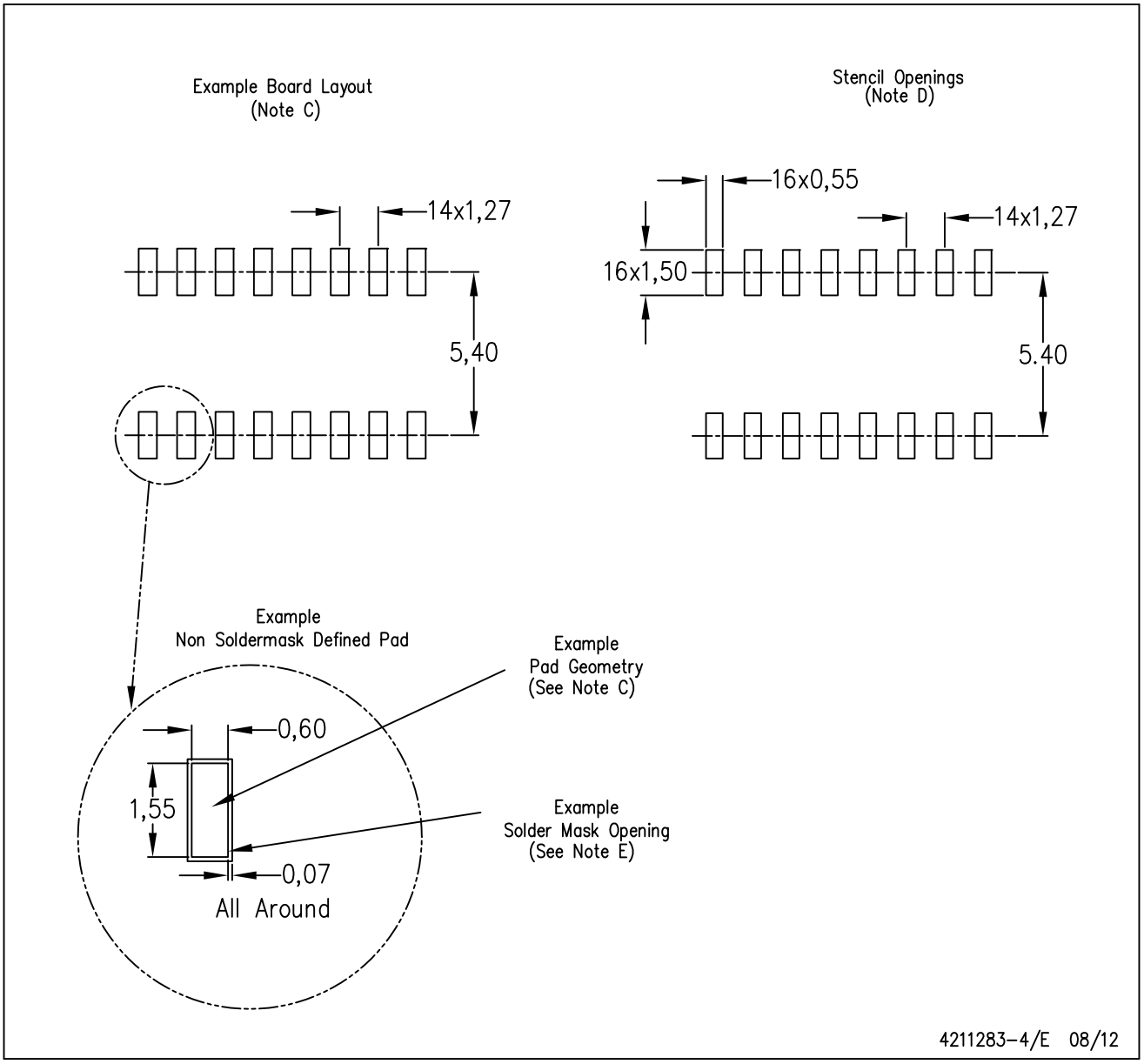
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS386DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDS386DGGG4	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDS388ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDS388ADBTG4	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDS390D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS390PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDT386DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDT386DGGG4	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDT388ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT388ADBTG4	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT390D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDT390PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDS386DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN75LVDS388ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN75LVDS390D	D	SOIC	16	40	505.46	6.76	3810	4
SN75LVDS390PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDS390PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDT386DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN75LVDT386DGGG4	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN75LVDT388ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN75LVDT388ADBTG4	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN75LVDT390D	D	SOIC	16	40	505.46	6.76	3810	4
SN75LVDT390PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDT390PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



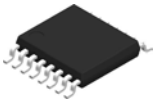
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

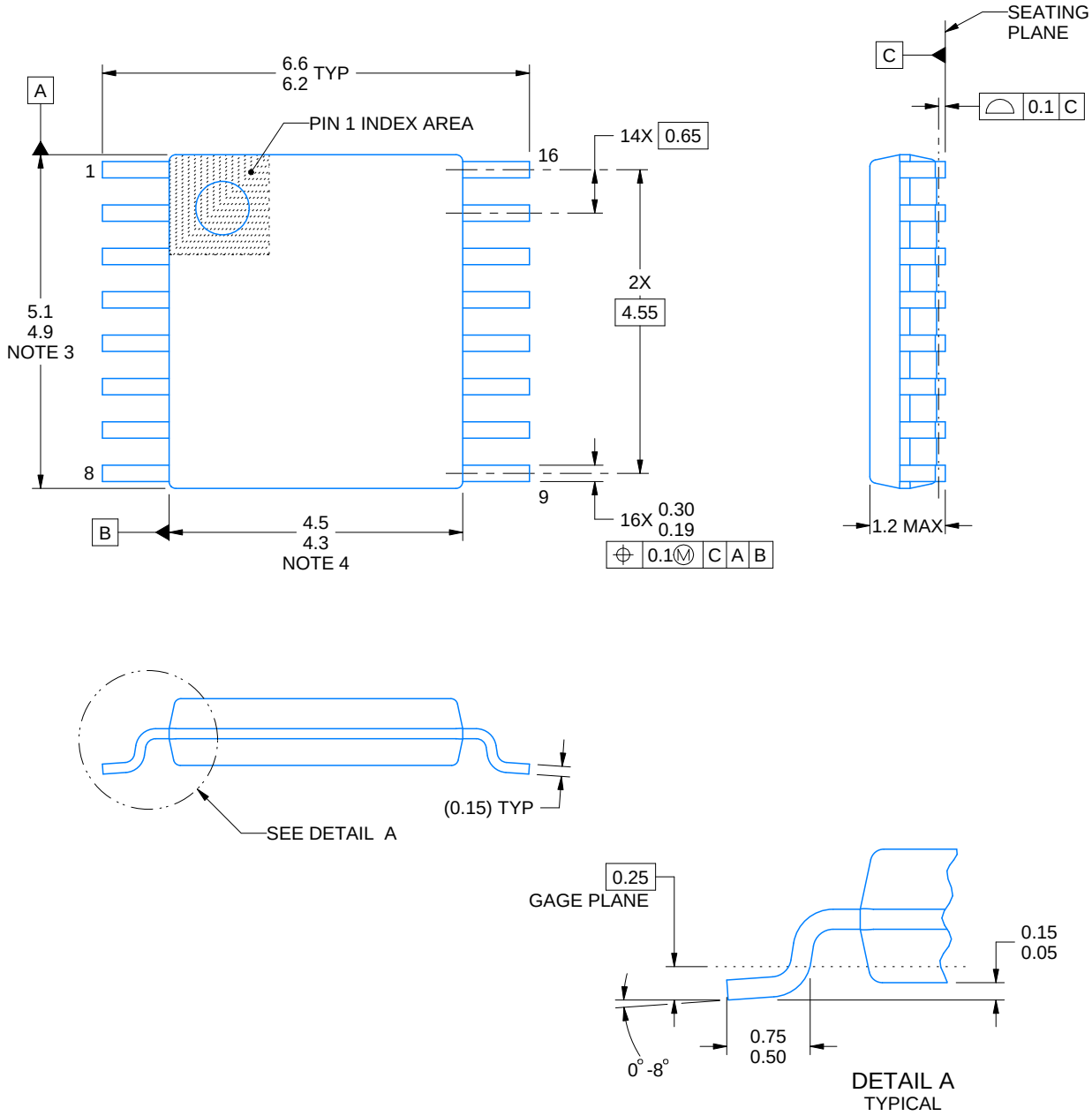
PW0016A



PACKAGE OUTLINE

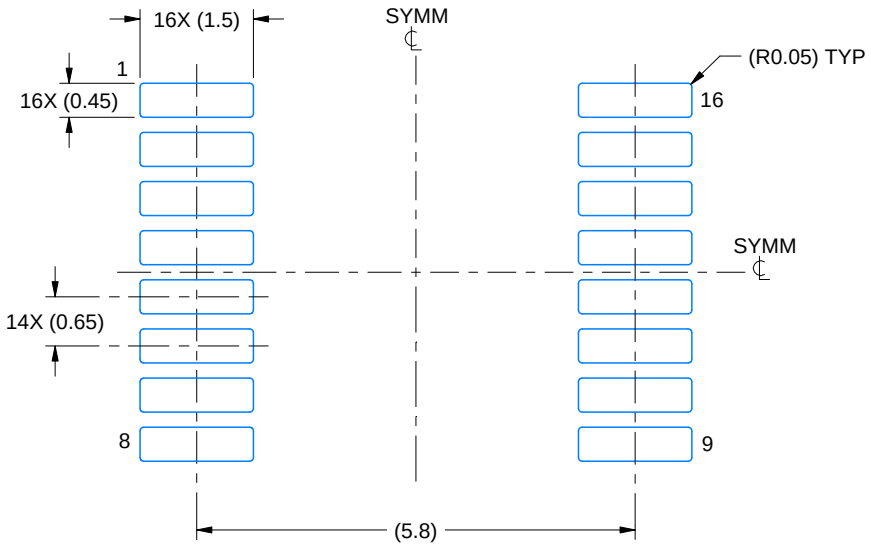
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

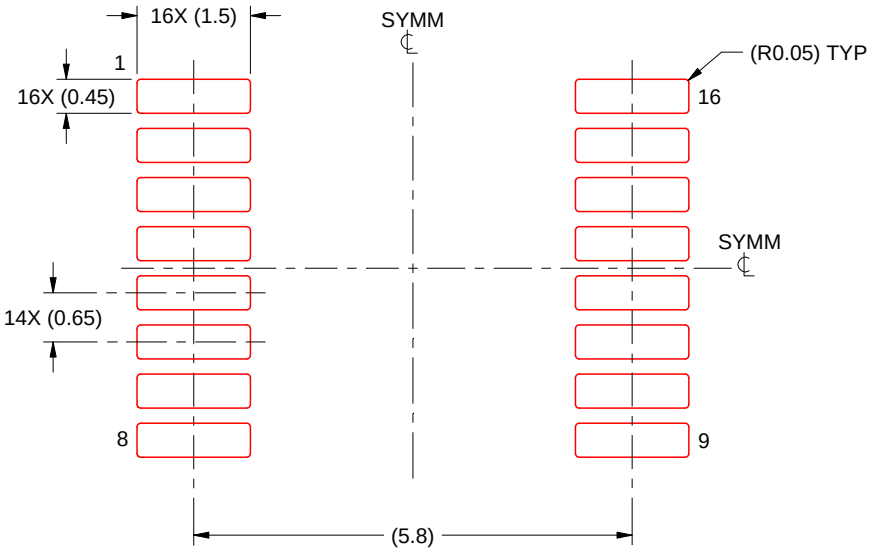
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

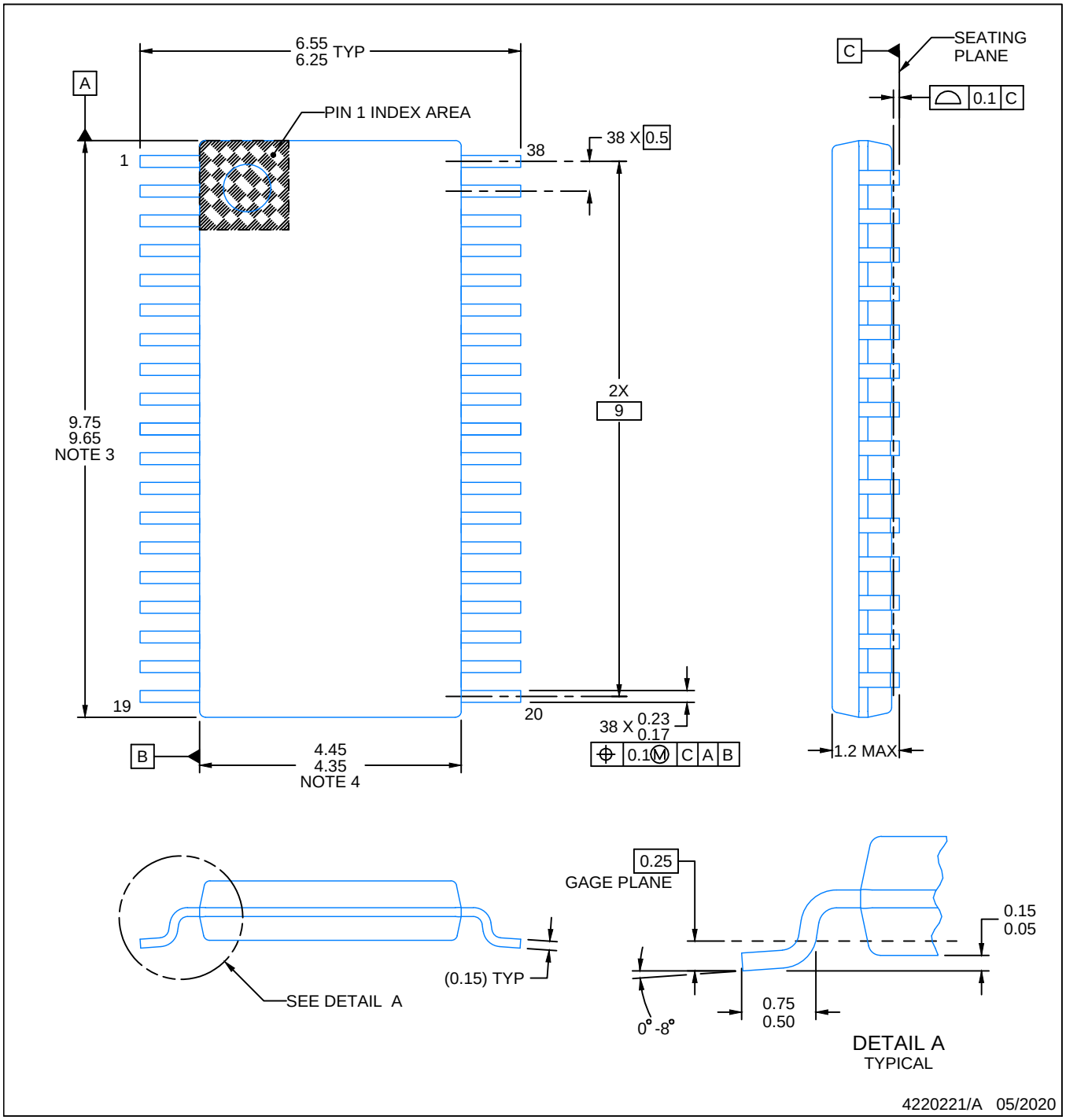
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBT0038A

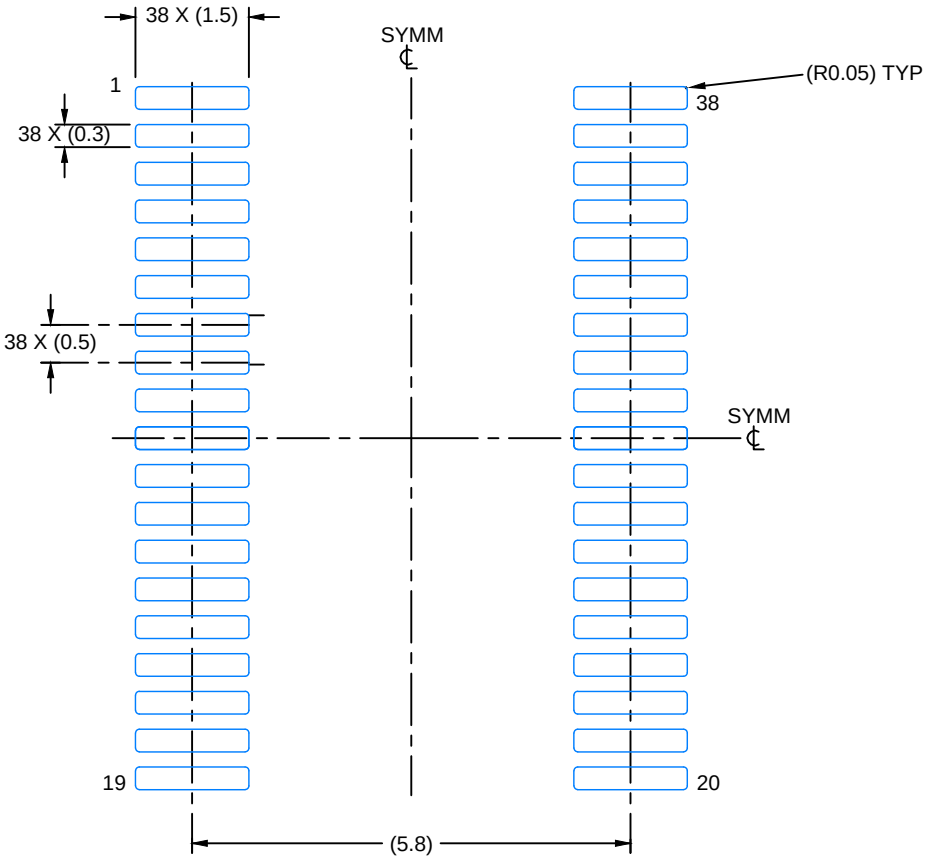
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



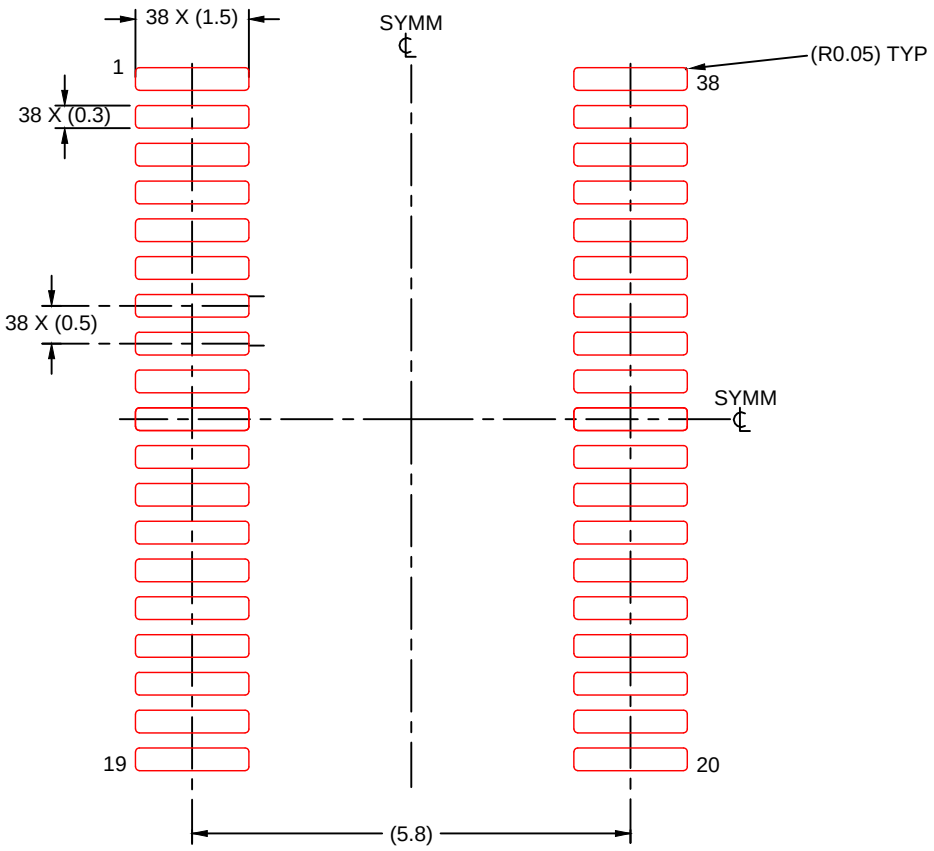
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

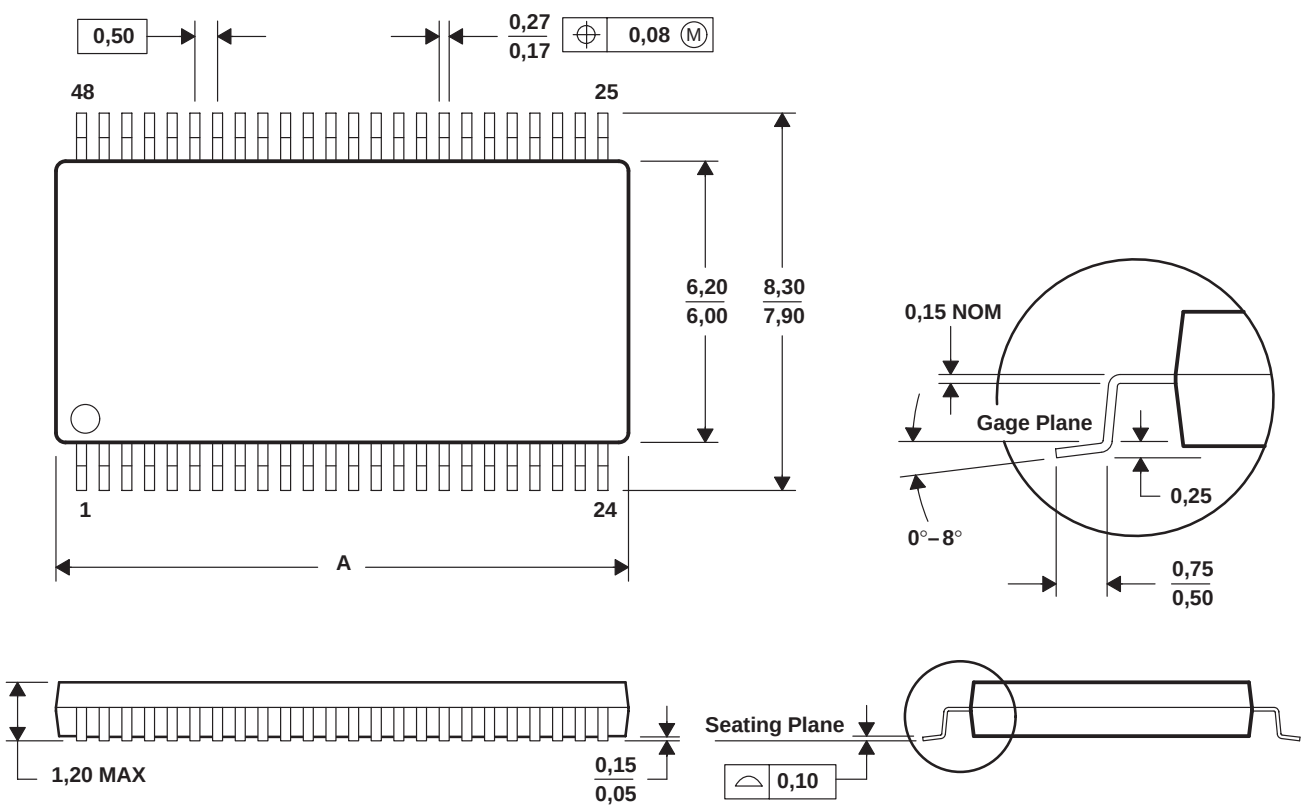
4220221/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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