LOW-DISTORTION, HIGH SLEW RATE, CURRENT-FEEDBACK AMPLIFIERS

Check for Samples: THS3061 THS3062

FEATURES

- **Unity Gain Bandwidth: 300 MHz**
- **0.1-dB Bandwidth: 120 MHz (G = 2)**
- **High Slew Rate: 7000 V/µs**
- **HD3 at 10 MHz: –81 dBc (G = 2, R_L = 150 Ω)**
- **High Output Current: ±145 mA into 50 Ω**
- **Power-Supply Voltage Range: ±5 V to ±15 V**

APPLICATIONS

- **High-Speed Signal Processing**
- **Test and Measurement Systems**
- **VDSL Line Driver**
- **High-Voltage ADC Preamplifier**
- **Video Line Driver**

DESCRIPTION

The THS3061 (single) and THS3062 (dual) are high-voltage, high slew-rate current feedback amplifiers utilizing Texas Instruments' BICOM-1 process. Designed for low-distortion with a high slew rate of 7000 V/µs, the THS306x amplifiers are ideally suited for applications requiring large, linear output signals such as video line drivers and VDSL line drivers.

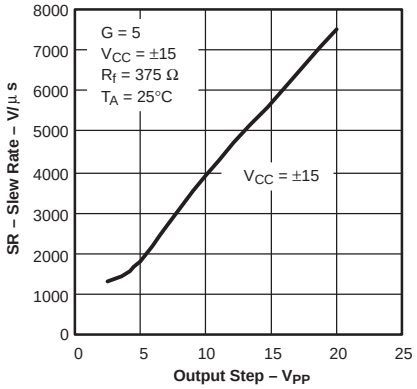
The THS3061 and THS3062 provide well-regulated ac performance characteristics with power supplies ranging from ±5-V operation up to ±15-V supplies. Most notably, the 0.1-dB flat bandwidth is exceedingly high, reaching beyond 100 MHz, and the THS306x has less than 0.3 dB of peaking in the frequency response when configured in unity gain. The unity-gain bandwidth of 300 MHz provides excellent distortion characteristics at 10 MHz. The flexibility of the current-feedback design allows a 220-MHz, –3-dB bandwidth in a gain of 10, indicating excellent performance even at high gains.

The THS306x consumes 8.3 mA per-channel quiescent current at room temperature, and has the capability of producing up to ±145 mA of output current. The THS3061 is packaged in an 8-pin SOIC and an 8-pin MSOP with PowerPAD™. The THS3062 is available in an 8-pin SOIC with PowerPAD and an 8-pin MSP with PowerPAD.

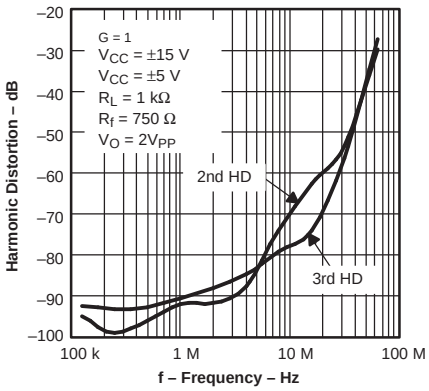
RELATED DEVICES AND DESCRIPTIONS

DEVICE	DESCRIPTION
THS3001	Low Distortion Current-Feedback Amplifier
THS3112	Dual Current-Feedback Amplifier With 175 mA Drive
THS3122	Dual Current-Feedback Amplifier With 350 mA Drive
OPA691	Wideband Current-Feedback Amplifier with 350 mA Drive

SLEW RATE vs OUTPUT STEP



HARMONIC DISTORTION vs FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted.(1)

V_S	Supply voltage	±16.5 V
V_I	Input voltage	$\pm V_S$
I_O	Output current	200 mA
V_{ID}	Differential input voltage	±3 V
	Continuous power dissipation	See Dissipation Ratings Table
T_J	Maximum junction temperature	+150°C
T_J (2)	Maximum junction temperature, continuous operation, long term reliability	+125°C
T_{stg}	Storage temperature range	–65°C to +150°C

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)(1)	POWER RATING (T_J = +125°C)(2)	
			$T_A \le$ +25°C	T_A = +85°C
D (8 pin)	38.3	97.5	1.02 W	410 mW
DDA (8 pin)(3)	9.2	45.8	2.18 W	873 mW
DGN (8 pin) (3)	4.7	58.4	1.71 W	680 mW

(1) This data was taken using the JEDEC High-K test PCB.
(2) This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in x 3 in PCB.
(3) The THS306x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage	Dual supply	±5	±15	V
	Single supply	10	30	

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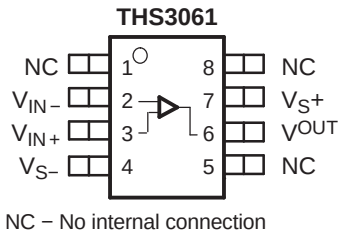
ORDERING INFORMATION(1)

PART NUMBER	PACKAGE TYPE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
Single			
THS3061D	SOIC-8	—	Rails, 75
THS3061DR			Tape and Reel, 2500
THS3061DGN	MSOP-8-PP(2)	BIB	Rails, 80
THS3061DGNR			Tape and Reel, 2500
Dual			
THS3062D	SOIC-8	—	Rails, 75
THS3062DR			Tape and Reel, 2500
THS3062DDA	SOIC-8-PP(2)	—	Rails, 75
THS3062DDAR			Tape and Reel, 2500
THS3062DGN	MSOP-8-PP(2)	BIC	Rails, 80
THS3062DGNR			Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The PowerPAD is electrically isolated from all other pins.

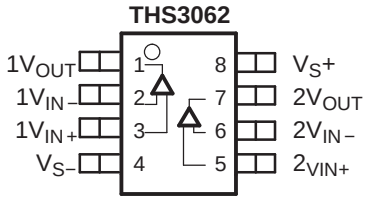
PIN ASSIGNMENTS

TOP VIEW D, DGN



NC − No internal connection

TOP VIEW D, DDA, DGN



PARAMETER MEASUREMENT INFORMATION

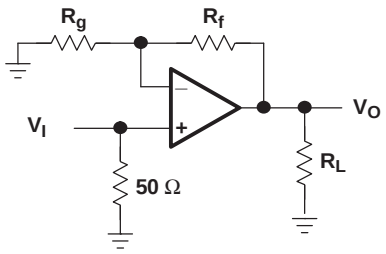


Figure 1. Noninverting Test Circuit

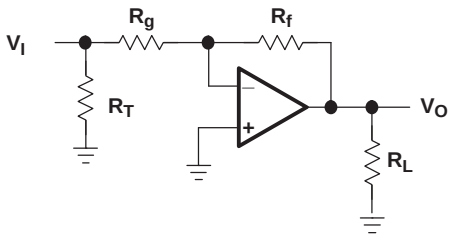


Figure 2. Inverting Test Circuit

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ELECTRICAL CHARACTERISTICS

At V_S = ±15 V: R_f = 560 Ω, R_L = 150 Ω, and G = 2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3061, THS3062					
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
AC PERFORMANCE							
Small-signal bandwidth (V_O = 100 mV_{PP}, Peaking < 0.3 dB)	G = 1, R_f = 750Ω	300				MHz	Typ
	G = 2, R_f = 560 Ω	275					
	G = 5, R_f = 357 Ω	260					
	G = 10, R_f = 200 Ω	220					
Bandwidth for 0.1-dB flatness	G = 2, V_O = 100mV_{PP}	120				MHz	Typ
Peaking at a gain of 1	V_O = 100 mV_{PP}	0.3				dB	Typ
Large-signal bandwidth	G = 2, V_O = 4 V_{PP}	120				MHz	Typ
Slew rate (25% to 75% level)	G = 5, 20 V-Step	7000				V/µs	Typ
	G = 2, 10 V-Step	5700					
Rise and fall time	G = 2, V_O = 10 V-Step	1				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2 V-Step	30				ns	Typ
Settling time to 0.01%		125				ns	Typ
Harmonic distortion							
2nd order harmonic	G = 2, f = 10 MHz, V_O = 2 V_{PP}, R_L = 150 Ω	–78				dBc	Typ
	R_L = 1 kΩ	–73					
3rd order harmonic	R_L = 150 Ω	–81				dBc	Typ
	R_L = 1 kΩ	–82					
3rd order intermodulation distortion	G = 2, f_c = 10 MHz, V_O = 2 $V_{PP(envelope)}$ Δf = 200 kHz	–93				dBc	Typ
Input voltage noise	f > 10 kHz	2.6				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 kHz	20				pA/√Hz	Typ
Input current noise (inverting)		36				pA/√Hz	Typ
Differential gain (NTSC, PAL)	G = 2, R_L = 150 Ω	0.02%					Typ
Differential phase (NTSC, PAL)		0.01°					Typ
DC PERFORMANCE							
Open-loop transimpedance gain	V_O = 0 V, R_L = 1 kΩ	1	0.7	0.6	0.6	MΩ	Min
Input offset voltage	V_{CM} = 0 V	±0.7	±3.5	±4.4	±4.5	mV	Max
Average offset voltage drift				±10	±10	µV/°C	Typ
Input bias current (inverting)		±2.0	±20	±32	±35	µA	Max
Average bias current drift (–)				±25	±30	nA/°C	Typ
Input bias current (noninverting)		±6.0	±25	±38	±40	A	Max
Average bias current drift (+)				±45	±50	nA/°C	Typ
INPUT							
Common-mode input range		±13.9	±13.1	±13.1	±13.1	V	Min
Common-mode rejection ratio	V_{CM} = ±0.5 V	72	60	58	58	dB	Min
Input resistance	Noninverting	518				kΩ	Typ
	Inverting	71				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ

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ELECTRICAL CHARACTERISTICS (continued)

At V_S = ±15 V: R_f = 560 Ω, R_L = 150 Ω, and G = 2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3061, THS3062					
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±13.7	±13.4	±13.4	±13.3	V	Min
	R_L = 150 Ω	±13	±12.6	±12.4	±12.3		
Current output, sourcing	R_L = 50 Ω	145	140	135	130	mA	Min
Current output, sinking	R_L = 50 Ω	–145	–140	–135	–130	mA	Min
POWER SUPPLY							
Closed-loop output impedance	G = 1, f = 1 MHz	0.1				Ω	Typ
Specified operating voltage		±15				V	Typ
Maximum operating voltage			±16.5	±16.5	±16.5	V	Max
Maximum quiescent current/channel		8.3	10	11.7	12	mA	Max
Minimum quiescent current/channel		8.3	6.1	6	6	mA	Min
Power-supply rejection (+PSRR)	V_{S+} = 14.50 V to 15.50 V	76	65	63	63	dB	Min
Power-supply rejection (–PSRR)	$V_{S–}$ = –14.50 V to –15.50 V	74	65	63	63	dB	Min

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ELECTRICAL CHARACTERISTICS

At V_S = ±5 V: R_f = 560 Ω, R_L = 150 Ω , and G = 2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3061, THS3062					
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
AC PERFORMANCE							
Small-signal bandwidth (V_O = 100 mV_{PP}, peaking < 0.3 dB)	G = 1, R_f = 750 Ω	275				MHz	Typ
	G = 2, R_f = 560 Ω	250					
	G = 5, R_f = 383 Ω	230					
	G = 10, R_f = 200 Ω	210					
Bandwidth for 0.1-dB flatness	G = 2, V_O = 100 mV_{PP}	100				MHz	Typ
Peaking at a gain of 1	V_O = 100 mV_{PP}	< 0.3				dB	Typ
Large-signal bandwidth	G = 2, V_O = 4 V_{PP}	100				MHz	Typ
Slew rate (25% to 75% level)	G = 1, 5-V Step, R_f = 750 Ω	2700				V/µs	Typ
	G = 5, 5-V Step, R_f = 357 Ω	1300					
Rise and fall time	G = 2, V_O = 5-V Step	2				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V Step	20				ns	Typ
Settling time to 0.01%		160					
Harmonic distortion							
2nd order harmonic	G = 2, f = 10 MHz, V_O = 2 V_{PP}, R_L = 150 Ω	–76				dBc	Typ
	R_L = 1 kΩ	–70					
3rd order harmonic	R_L = 150 Ω	–79				dBc	Typ
	R_L = 1 kΩ	–77					
3rd order intermodulation distortion	G = 2, f_c = 10 MHz, V_O = 2 $V_{PP(envelope)}$, Δf = 200 kHz	–91				dBc	Typ
Input voltage noise	f > 10 kHz	2.6				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 kHz	20				pA/√Hz	Typ
Input current noise (inverting)		36				pA/√Hz	Typ
Differential gain (NTSC, PAL)	G = 2, R_L = 150 Ω	0.025%					Typ
Differential phase (NTSC, PAL)		0.01°					Typ
DC PERFORMANCE							
Open-loop transimpedance gain	V_O = 0 V, R_L = 1 kΩ	0.8	0.6	0.5	0.5	MΩ	Min
Input offset voltage	V_{CM} = 0 V	±0.3	±3.5	±4.4	±4.5	mV	Max
Average offset voltage drift				±9	±9	µV/°C	Typ
Input bias current (inverting)		±2.0	±20	±32	±35	µA	Max
Average bias current drift (–)				±20	±25	nA/°C	Typ
Input bias current (noninverting)		±6.0	±25	±38	±40	µA	Max
Average bias current drift (+)				±30	±35	nA/°C	Typ
INPUT							
Common-mode input range		±3.9	±3.1	±3.1	±3.1	V	Min
Common-mode rejection ratio	V_{CM} = ±0.5 V	70	60	58	58	dB	Min
Input resistance	Noninverting	518				kΩ	Typ
	Inverting	71				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±4.1	±3.8	±3.8	±3.7	V	Min
	R_L = 150 Ω	±4.0	±3.6	±3.6	±3.5		

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ELECTRICAL CHARACTERISTICS (continued)

At V_S = ±5 V: R_f = 560 Ω, R_L = 150 Ω , and G = 2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3061, THS3062					
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
Current output, sourcing	R_L = 50 Ω	63	61	60	59	mA	Min
Current output, sinking		–63	–61	–60	–59	mA	Min
Closed-loop output impedance	G = 1, f = 1 MHz	0.1				Ω	Typ
POWER SUPPLY							
Specified operating voltage		±5				V	Typ
Minimum operating voltage			±4.5	±4.5	±4.5	V	Min
Maximum quiescent current		6.3	8.0	9.2	9.5	mA	Max
Minimum quiescent current		6.3	5.0	4.7	4.6	mA	Min
Power-supply rejection (+PSRR)	V_{S+} = 4.50 V to 5.50 V	73	65	63	63	dB	Min
Power-supply rejection (–PSRR)	$V_{S–}$ = –4.50 V to –5.50 V	75	65	63	63	dB	Min

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

SMALL-SIGNAL FREQUENCY RESPONSE

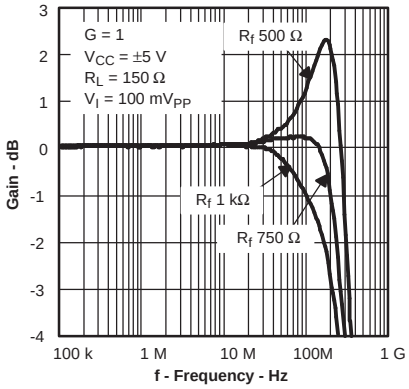


Figure 3.

SMALL-SIGNAL FREQUENCY RESPONSE

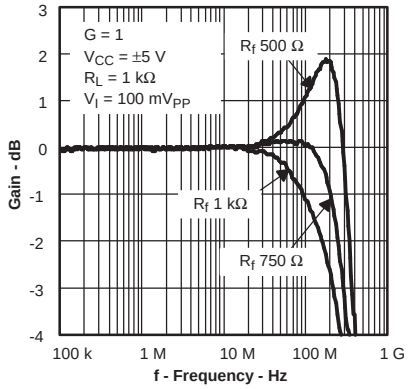


Figure 4.

SMALL-SIGNAL FREQUENCY RESPONSE

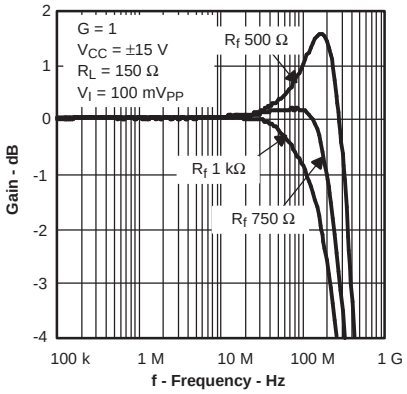


Figure 5.

SMALL-SIGNAL FREQUENCY RESPONSE

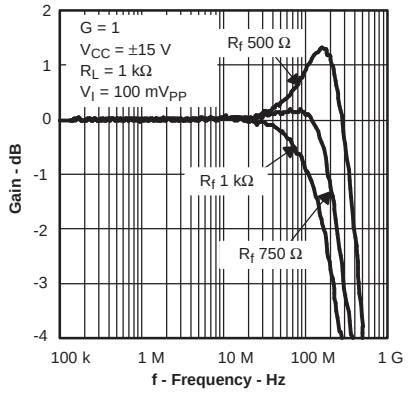


Figure 6.

SMALL-SIGNAL FREQUENCY RESPONSE

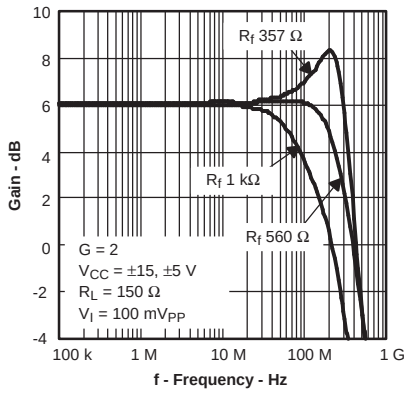


Figure 7.

SMALL-SIGNAL FREQUENCY RESPONSE

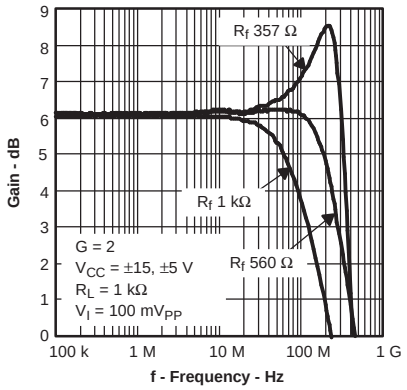


Figure 8.

SMALL-SIGNAL FREQUENCY RESPONSE

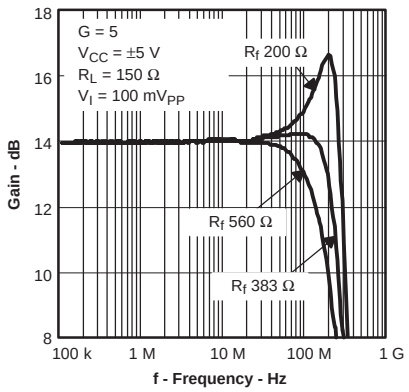


Figure 9.

SMALL-SIGNAL FREQUENCY RESPONSE

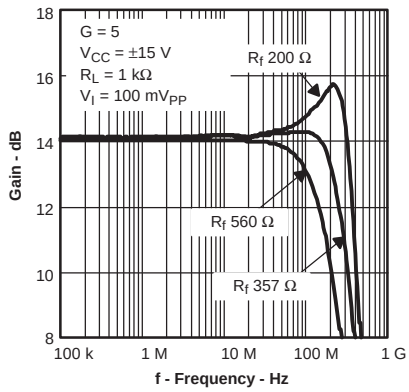


Figure 10.

SMALL-SIGNAL FREQUENCY RESPONSE

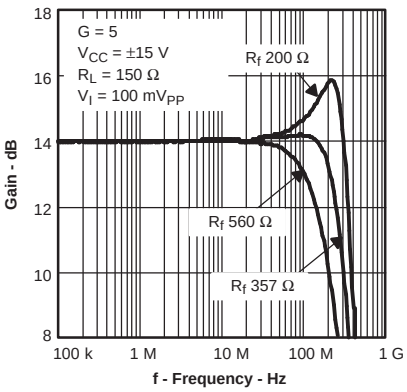


Figure 11.

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TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL FREQUENCY RESPONSE

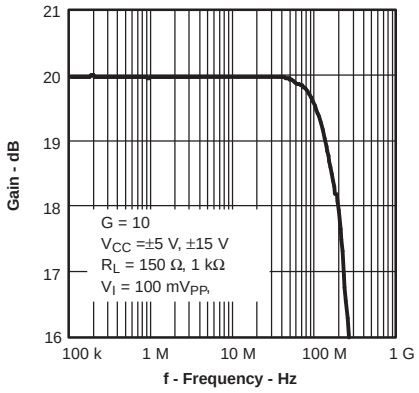


Figure 12.

SMALL-SIGNAL FREQUENCY RESPONSE

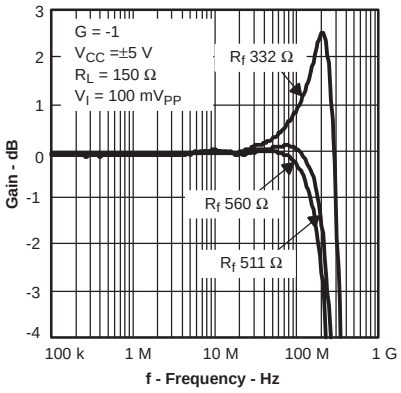


Figure 13.

SMALL-SIGNAL FREQUENCY RESPONSE

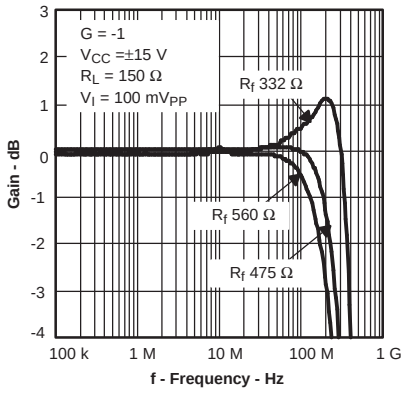


Figure 14.

LARGE-SIGNAL FREQUENCY RESPONSE

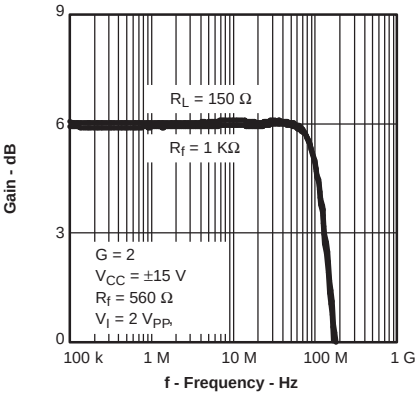


Figure 15.

LARGE-SIGNAL FREQUENCY RESPONSE

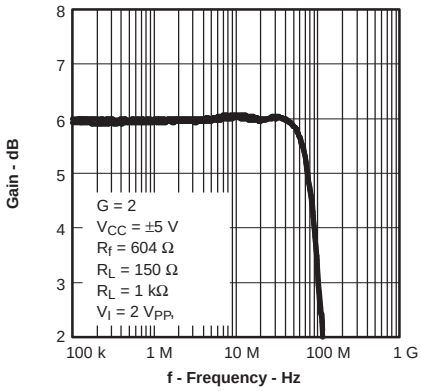


Figure 16.

THS3061 HARMONIC DISTORTION vs FREQUENCY

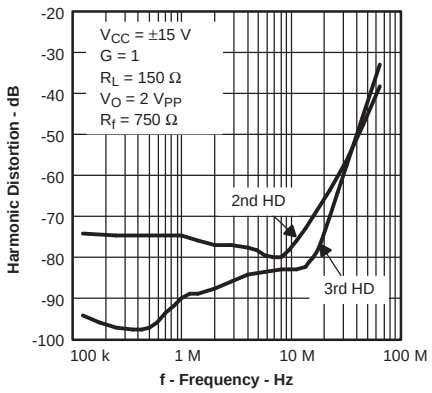


Figure 17.

THS3062 HARMONIC DISTORTION vs FREQUENCY

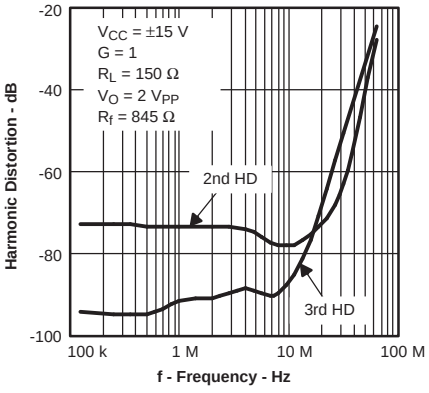


Figure 18.

HARMONIC DISTORTION vs FREQUENCY

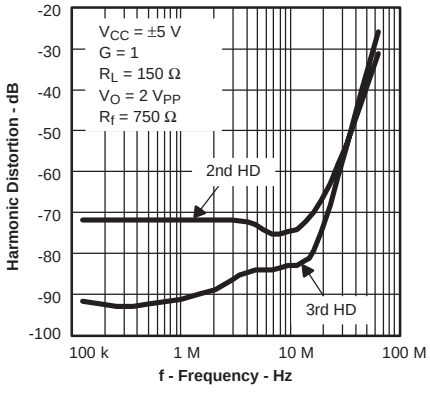


Figure 19.

HARMONIC DISTORTION vs FREQUENCY

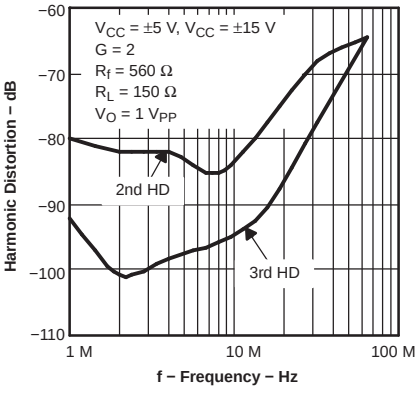


Figure 20.

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TYPICAL CHARACTERISTICS (continued)

HARMONIC DISTORTION vs FREQUENCY

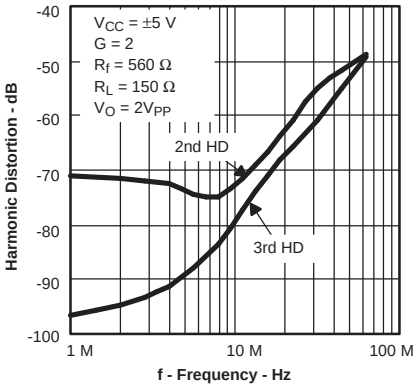


Figure 21.

HARMONIC DISTORTION vs FREQUENCY

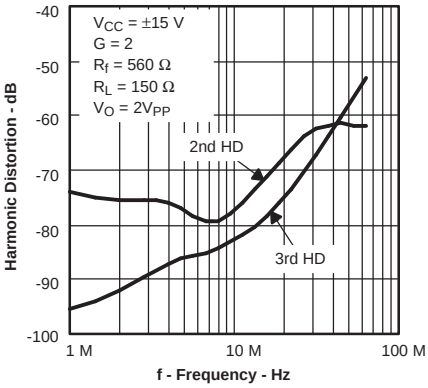


Figure 22.

HARMONIC DISTORTION vs FREQUENCY

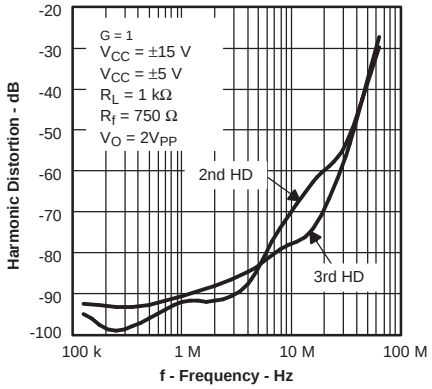


Figure 23.

THS3061 HARMONIC DISTORTION vs OUTPUT VOLTAGE

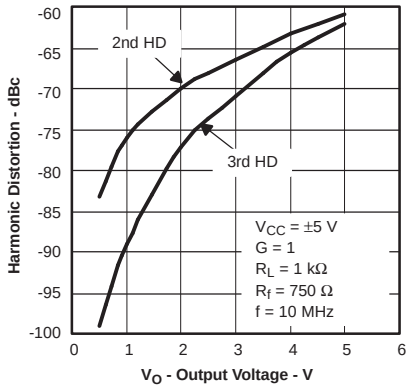


Figure 24.

THS3061 HARMONIC DISTORTION vs OUTPUT VOLTAGE

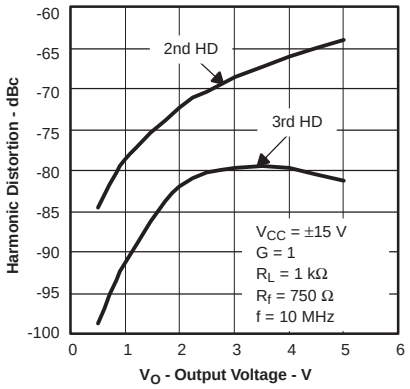


Figure 25.

THS3061 HARMONIC DISTORTION vs OUTPUT VOLTAGE

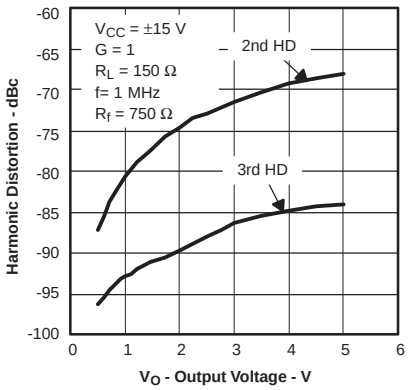


Figure 26.

THS3061 HARMONIC DISTORTION vs OUTPUT VOLTAGE

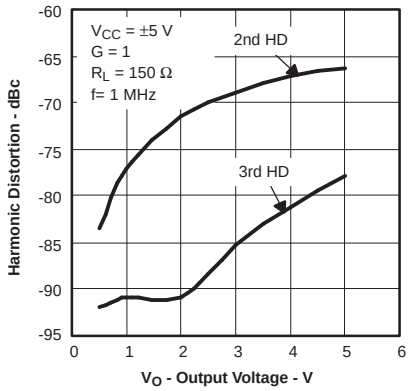


Figure 27.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

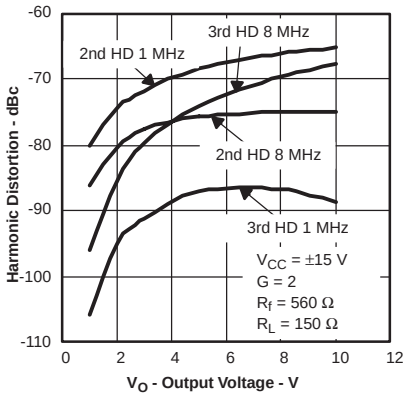


Figure 28.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

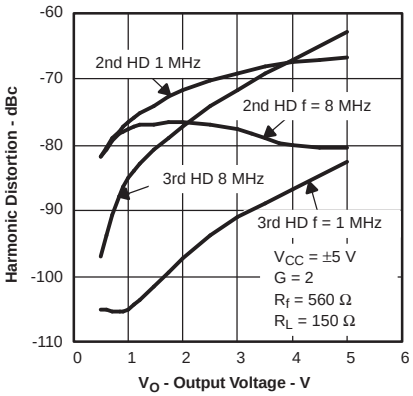


Figure 29.

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TYPICAL CHARACTERISTICS (continued)

OUTPUT IMPEDANCE vs FREQUENCY

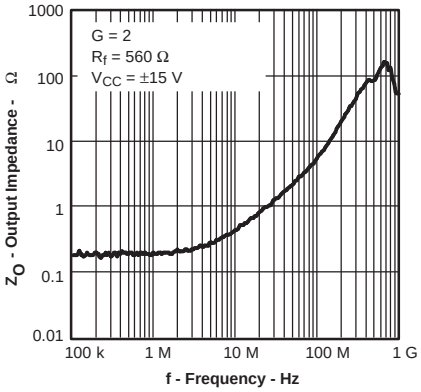


Figure 30.

COMMON-MODE REJECTION RATIO vs FREQUENCY

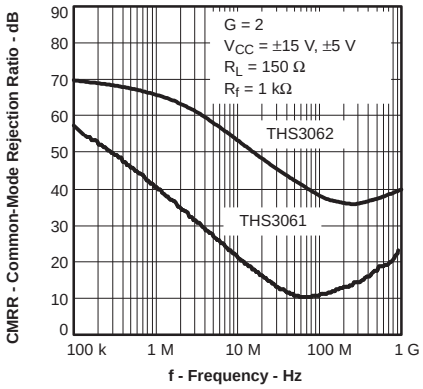


Figure 31.

INPUT CURRENT NOISE vs FREQUENCY

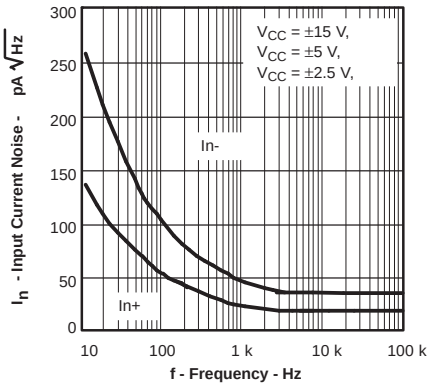


Figure 32.

VOLTAGE NOISE DENSITY vs FREQUENCY

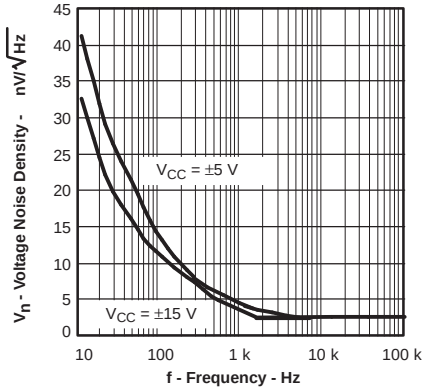


Figure 33.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

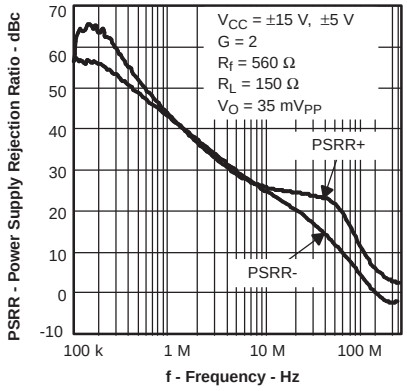


Figure 34.

COMMON-MODE REJECTION RATIO (DC) vs INPUT COMMON-MODE RANGE

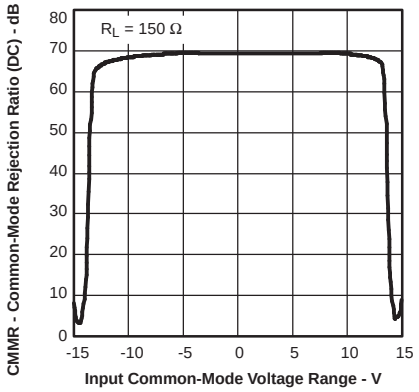


Figure 35.

THS3061 SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

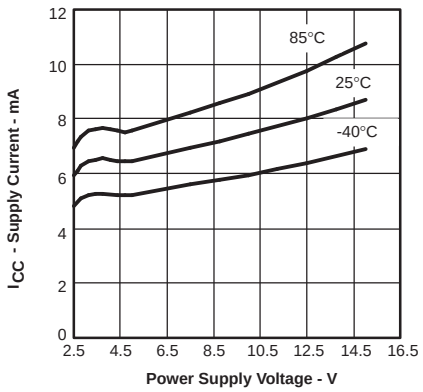


Figure 36.

THS3062 SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

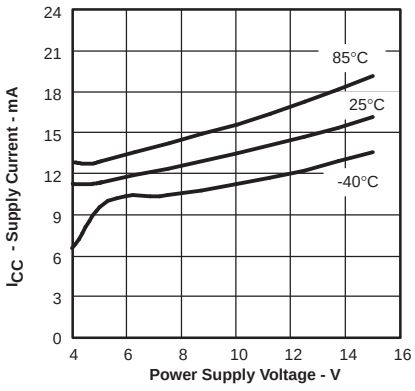


Figure 37.

SLEW RATE vs OUTPUT VOLTAGE

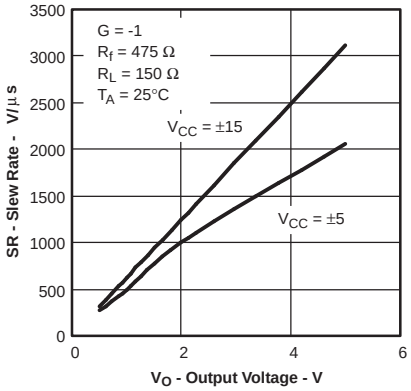


Figure 38.

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TYPICAL CHARACTERISTICS (continued)

SLEW RATE vs OUTPUT VOLTAGE

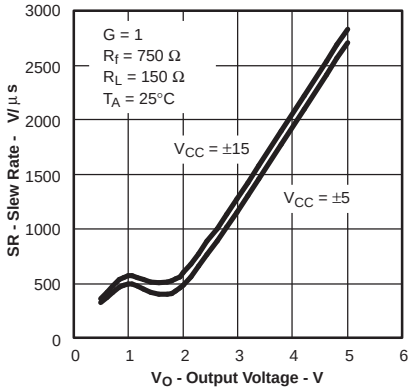


Figure 39.

SLEW RATE vs OUTPUT STEP

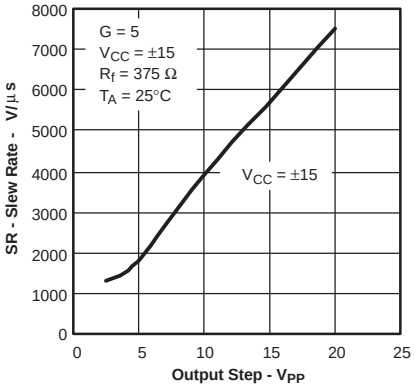


Figure 40.

INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE SWING

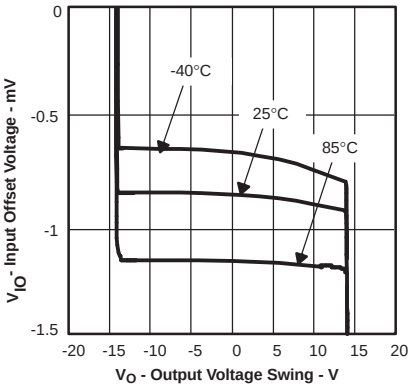


Figure 41.

OVERDRIVE RECOVERY TIME

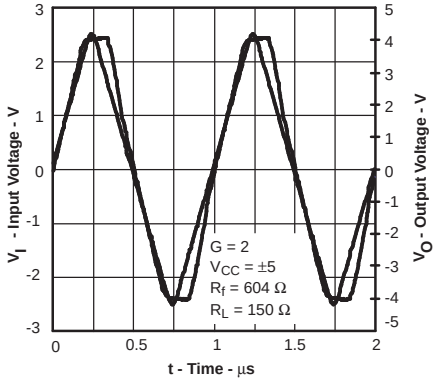


Figure 42.

OVERDRIVE RECOVERY TIME

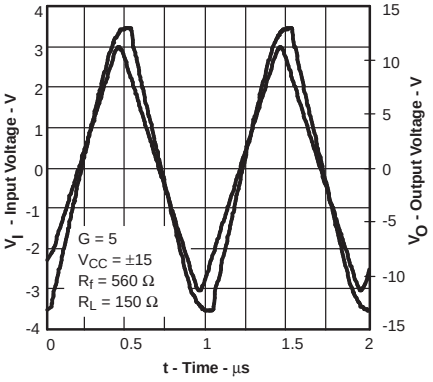


Figure 43.

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

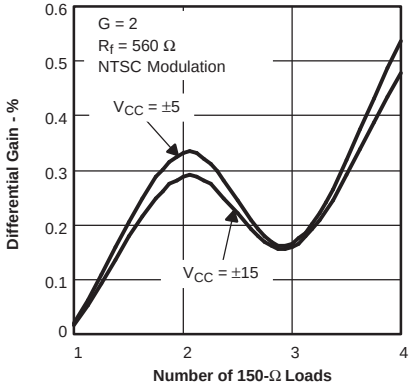


Figure 44.

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

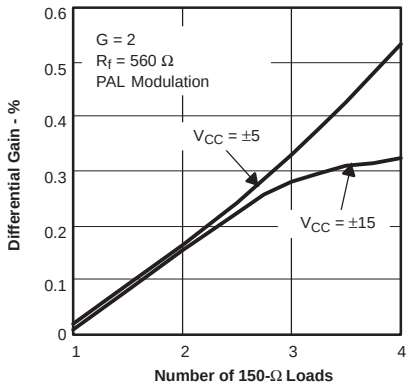


Figure 45.

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

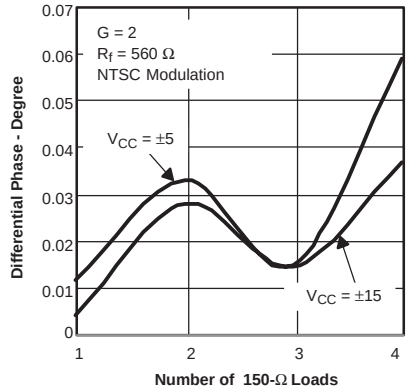


Figure 46.

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

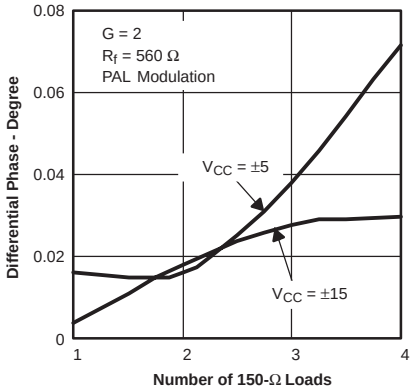


Figure 47.

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APPLICATION INFORMATION

INTRODUCTION

The THS306x is a high-speed operational amplifier configured in a current-feedback architecture. The device is built using Texas Instruments' BiCOM-I process, a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion.

MAXIMUM SLEW RATE FOR REPETITIVE SIGNALS

The THS3061 and THS3062 are recommended for high slew rate, pulsed applications where the internal nodes of the amplifier have time to stabilize between pulses.It is recommended to have at least a 20-ns delay between pulses.

The THS3061 and THS3062 are not recommended for applications with repetitive signals (sine, square, sawtooth, or other types) that exceed 900 V/µs. Using this device in these types of applications results in an excessive current draw from the power supply and possible device damage. For applications with a high slew rate and repetitive signals, the THS3091 and THS3095 (singles) or the THS3092 and THS3096 (duals) are recommended instead.

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current-feedback amplifiers, the bandwidth of the THS306x is an inversely proportional function of the value of the feedback resistor. The recommended resistors for optimum frequency response are shown in Table 1. These should be used as a starting point, and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback-resistor value of 750 Ω is recommended—a good compromise between bandwidth and phase margin that yields a very stable amplifier.

As shown in Table 1, to maintain the highest bandwidth with increasing gain, the feedback resistor is reduced. The advantage of dropping the feedback resistance (and the gain-resistor value) is that the noise of the system is also reduced compared to no reduction of these resistor values (see NOISE CALCULATIONS). Thus, keeping the bandwidth as high as possible maintains very good distortion performance of the amplifier by keeping the excess loop gain as high as possible.

Table 1. Recommended Resistor Values for Optimum Frequency Response

GAIN	R_F for V_{CC} = ±15 V	R_F for V_{CC} = ±5 V
1	750 Ω	750 Ω
2, –1	560 Ω	560 Ω
5	357 Ω	383 Ω
10	200 Ω	200 Ω

Care must be taken to not set these values too low. The amplifier's output must drive the feedback resistance (and gain resistance), and this may place a burden on the amplifier. The end result is that distortion may actually increase due to the low-impedance load presented to the amplifier. The designer must carefully manage the amplifier bandwidth and the associated loading effects for optimum performance.

The THS3061/62 amplifiers exhibit very good distortion performance and bandwidth, and can use power supplies up to 15 V. The excellent current-drive capability of up to 145 mA into a 50-Ω load allows many versatile applications. One application is driving a twisted pair line (that is, a telephone line). Figure 48 shows a simple circuit for driving a twisted pair differentially.

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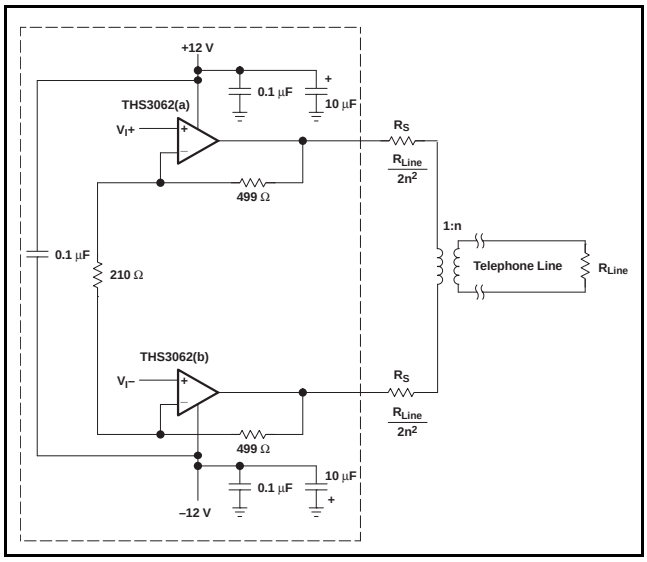


Figure 48. Simple Line Driver With THS3062

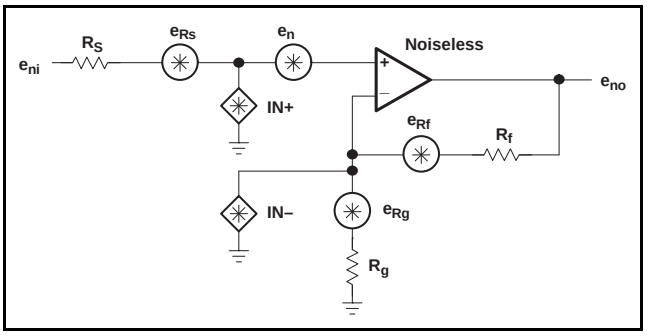


Figure 49. Noise Model

Due to the high supply voltages and the large current-drive capability, the power dissipation of the amplifier must be carefully considered. To have as much power dissipation as possible in a small package, the THS3062 is available only in a MSOP-8 PowerPAD package (DGN), and an even lower thermal-impedance SOIC-8 PowerPAD package (DDA). The thermal impedance of a standard SOIC package is too large to allow useful applications with up to 30 V across the power-supply terminals with this dual amplifier. But the THS3061 (a single amplifier) can be used in the standard SOIC package. Again, the amplifier power dissipation must be carefully examined, or else the amplifiers could overheat, severely degrading performance. See the *Power Dissipation and Thermal Considerations* section for more information on thermal management.

NOISE CALCULATIONS

Noise can cause errors on very small signals. This is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback amplifiers (CFB) is the same as for voltage feedback amplifiers (VFB). The only difference between the two is that CFB amplifiers generally specify different current-noise parameters for each input, while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 49. This model includes all of the noise sources as follows:

- en = Amplifier internal voltage noise (nV/$\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise (pA/$\sqrt{\text{Hz}}$)
- IN– = Inverting current noise (pA/$\sqrt{\text{Hz}}$)
- eRx = Thermal voltage noise associated with each resistor (eRx = 4 kTRx)

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + (IN+ \times R_S)^2 + (IN- \times (R_f \parallel R_g))^2 + 4\,kTR_S + 4\,kT(R_f \parallel R_g)}$$

where

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_f \parallel R_g$ = Parallel resistance of R_f and R_g

To calculate the equivalent output noise of the amplifier, multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni} A_V = e_{ni}\left(1 + \frac{R_f}{R_g}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_F and R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

PCB LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high-frequency devices in the THS306x family requires careful attention to board layout, parasitic effects, and external component types.

Recommendations to optimize performance include:

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- Minimize parasitic capacitance to any ac ground for all signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 µF or more) tantalum decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the printed circuit board (PCB). The primary goal is to minimize the impedance in the differential-current return paths. For driving differential loads with the THS3062, adding a capacitor between the power-supply pins improves 2nd-order harmonic-distortion performance. This also minimizes the current loop formed by the differential drive.
- Careful selection and placement of external components preserve the high frequency performance of the THS306x family. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep leads and PCB trace lengths as short as possible. Never use wirebound-type resistors in a high-frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series-output resistors, if any, as close as possible to the inverting-input pins and output pins. Other network components, such as input-termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can affect circuit operation. Keep resistor values as low as possible, consistent with load-driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S since the THS306x family is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).

  A 50-Ω environment is not necessary onboard, and in fact, a higher-impedance environment improves distortion as shown in the distortion-versus-load plots. With a characteristic board-trace impedance based on board material and trace dimensions, a matching series resistor is used in the trace from the output of the THS306x, as well as a terminating shunt resistor at the input of the destination device.

  Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high speed part like the THS306x family is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS306x family parts directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS306x family is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset

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leadframe upon which the die is mounted [see Figure 50(a) and Figure 50(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 50(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount, compared with awkward mechanical methods of heatsinking.

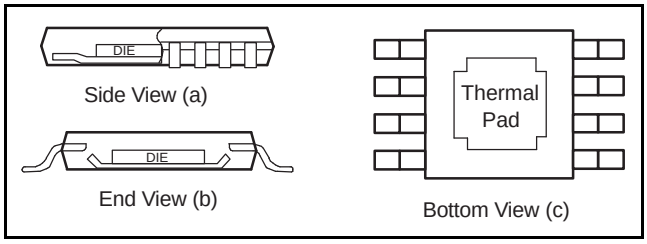


Figure 50. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top-side etch pattern as shown in Figure 51. There should be etch for the leads as well as etch for the thermal pad.

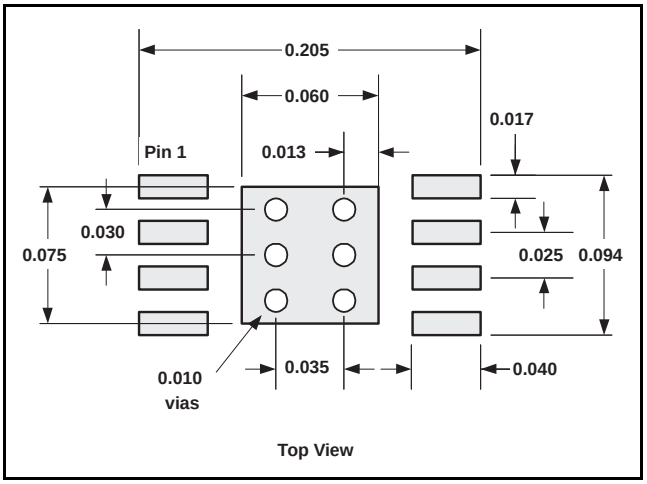


Figure 51. DGN PowerPAD PCB Etch and Via Pattern

2. Place five holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS306x-family IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS306x family PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the

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solder reflow operation as any standard surface-mount component. This results in a properly-installed device.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

To maintain maximum output capability, the THS360x does not incorporate automatic thermal shutoff protection. The designer must ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of +150°C is exceeded. For best performance, design for a maximum junction temperature of +125°C. Between +125°C and +150°C, damage does not occur, but the performance of the amplifier begins to degrade.

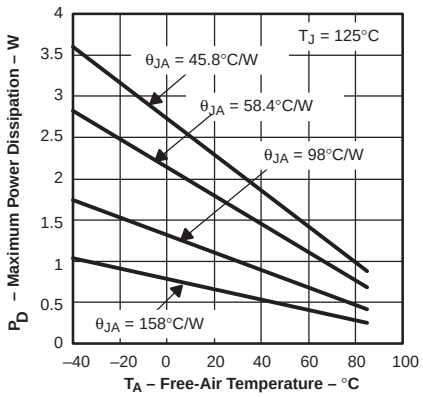
The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using Equation 1.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

(1)

For systems where heat dissipation is more critical, the THS306x family of devices is offered in an 8-pin MSOP with PowerPAD, and the THS3062 is available in the SOIC-8 PowerPAD package offering even better thermal performance. The thermal coefficients for the PowerPAD packages are substantially improved over traditional SOICs. Maximum power dissipation levels are given in the graph for the available packages. Data for the PowerPAD packages assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note number SLMA002. The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially, which can cause serious heat and performance issues. Always be sure to solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3"x3"
θ_{JA} = 45.8°C/W for 8-Pin SOIC w/PowerPad (DDA)
θ_{JA} = 58.4°C/W for 8-Pin MSOP w/PowerPad (DGN)
θ_{JA} = 98°C/W for 8-Pin SOIC High Test PCB (D)
θ_{JA} = 158°C/W for 8-Pin MSOP w/PowerPad w/o Solder

Figure 52. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important not only to consider quiescent power dissipation, but also dynamic power dissipation. Often, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS306x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier as shown in Figure 53. A minimum value of 10 Ω works well for most applications. For example, in 75-Ω transmission systems, setting the series-resistor value to 75 Ω both isolates any capacitive loading and provides the proper line impedance matching at the source end.

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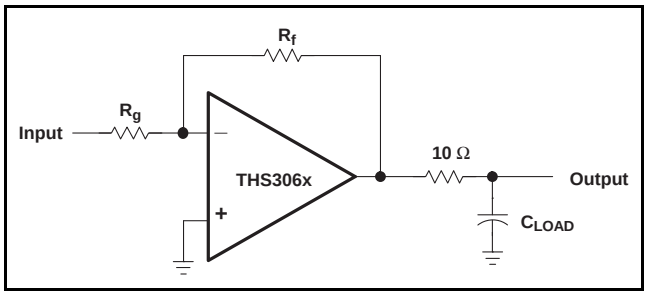


Figure 53. Driving a Capacitive Load

General Configurations

A common error for the first-time CFB-amplifier user is creating a unity gain buffer amplifier by shorting the output directly to the inverting input. In this configuration, a CFB amplifier oscillates, and is *not* recommended. The THS306x, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended, because at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, must be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 54).

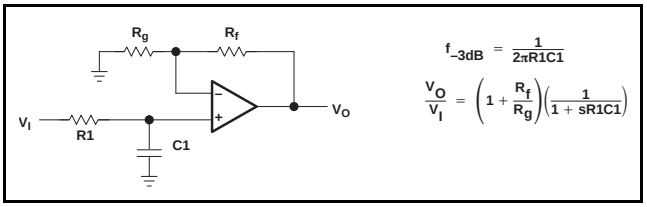


Figure 54. Single-Pole Low-Pass Filter

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If a multiple-pole filter is required, a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew rates and high bandwidths, CFB amplifiers can pass very accurate signals and help minimize distortion. An example is shown in Figure 55.

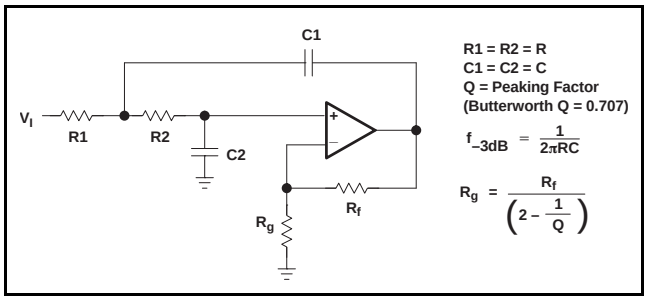


Figure 55. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in Figure 56, adds a resistor in series with the capacitor. This is acceptable, because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in Figure 57, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.

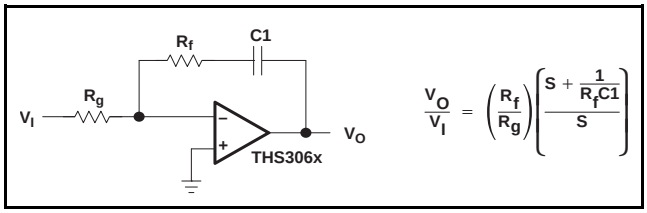


Figure 56. Inverting CFB Integrator

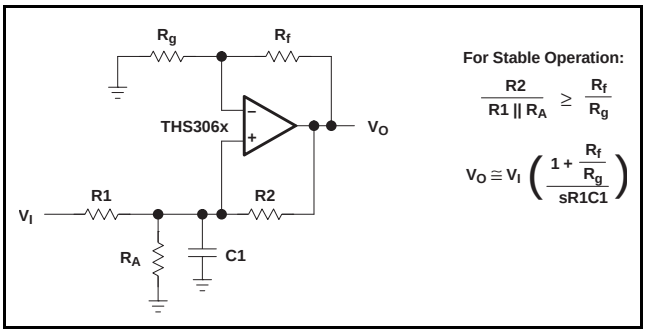


Figure 57. Noninverting CFB Integrator

The THS306x may also be employed as a very good video-distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (dP) and the differential gain (dG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

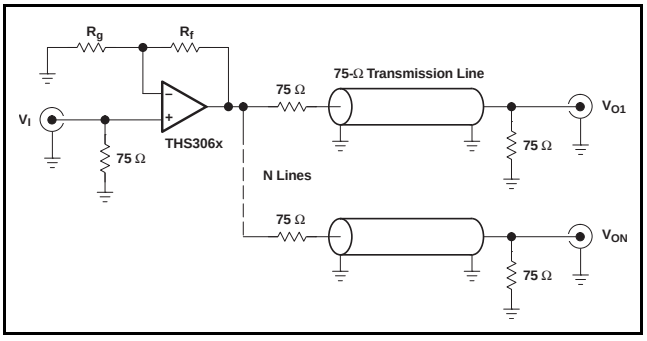


Figure 58. Video Distribution Amplifier Application

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October, 2002) to Revision B	Page
• Updated document format to current standards	1
• Deleted *lead temperature* specification from Absolute Maximum Ratings table	2
• Added *Maximum Slew Rate for Repetitive Signals* section	13

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3061D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3061	Samples
THS3061DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BIB	Samples
THS3061DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BIB	Samples
THS3061DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BIB	Samples
THS3061DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3061	Samples
THS3062D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3062	Samples
THS3062DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3062	Samples
THS3062DDAG3	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3062	Samples
THS3062DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BIC	Samples
THS3062DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BIC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

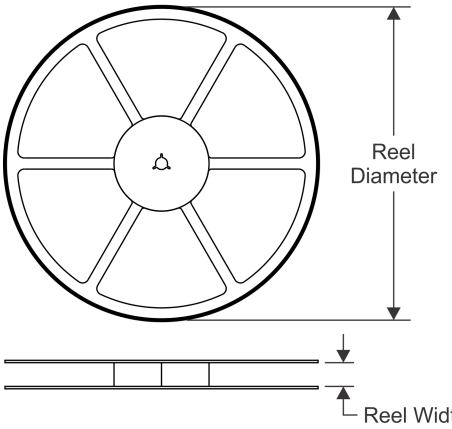
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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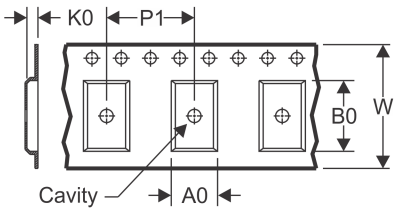
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

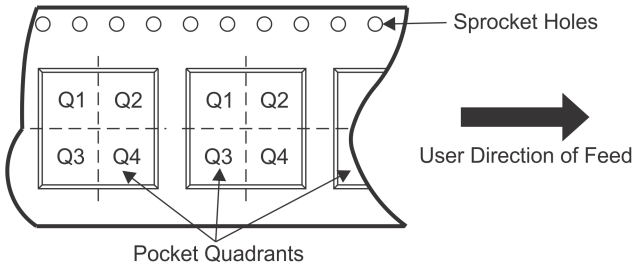


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

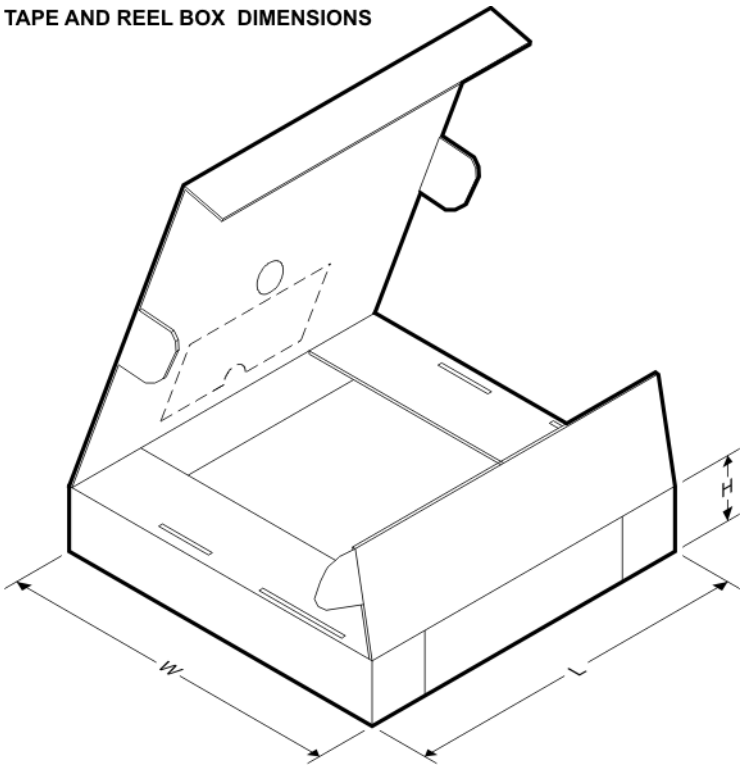
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3061DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3061DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

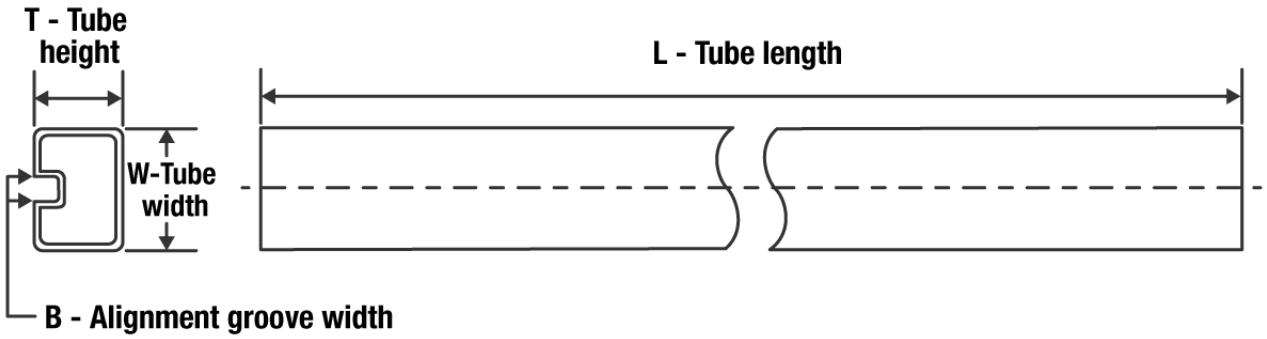
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3061DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS3061DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS3061D	D	SOIC	8	75	505.46	6.76	3810	4
THS3062D	D	SOIC	8	75	505.46	6.76	3810	4
THS3062DDA	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS3062DDAG3	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS3062DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS3062DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

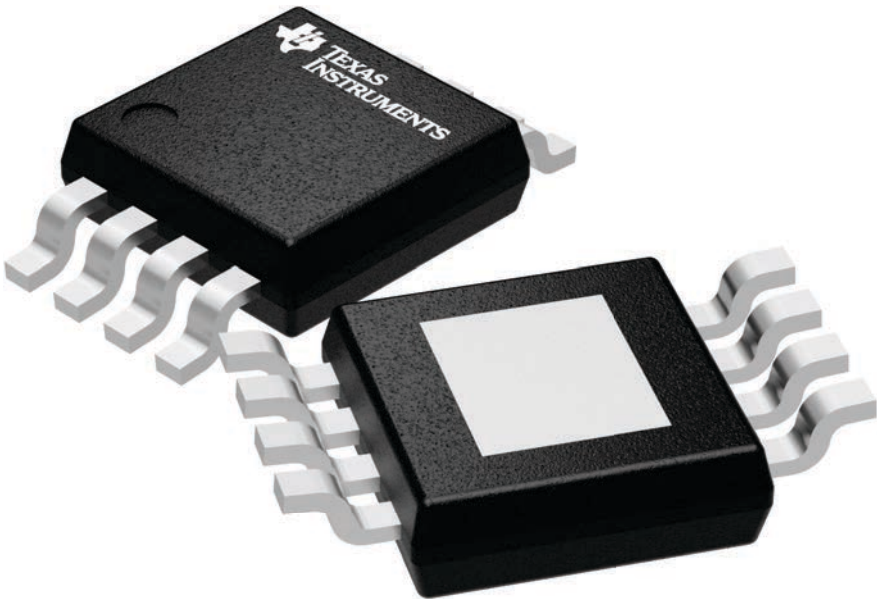
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

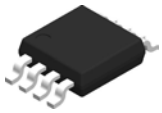
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

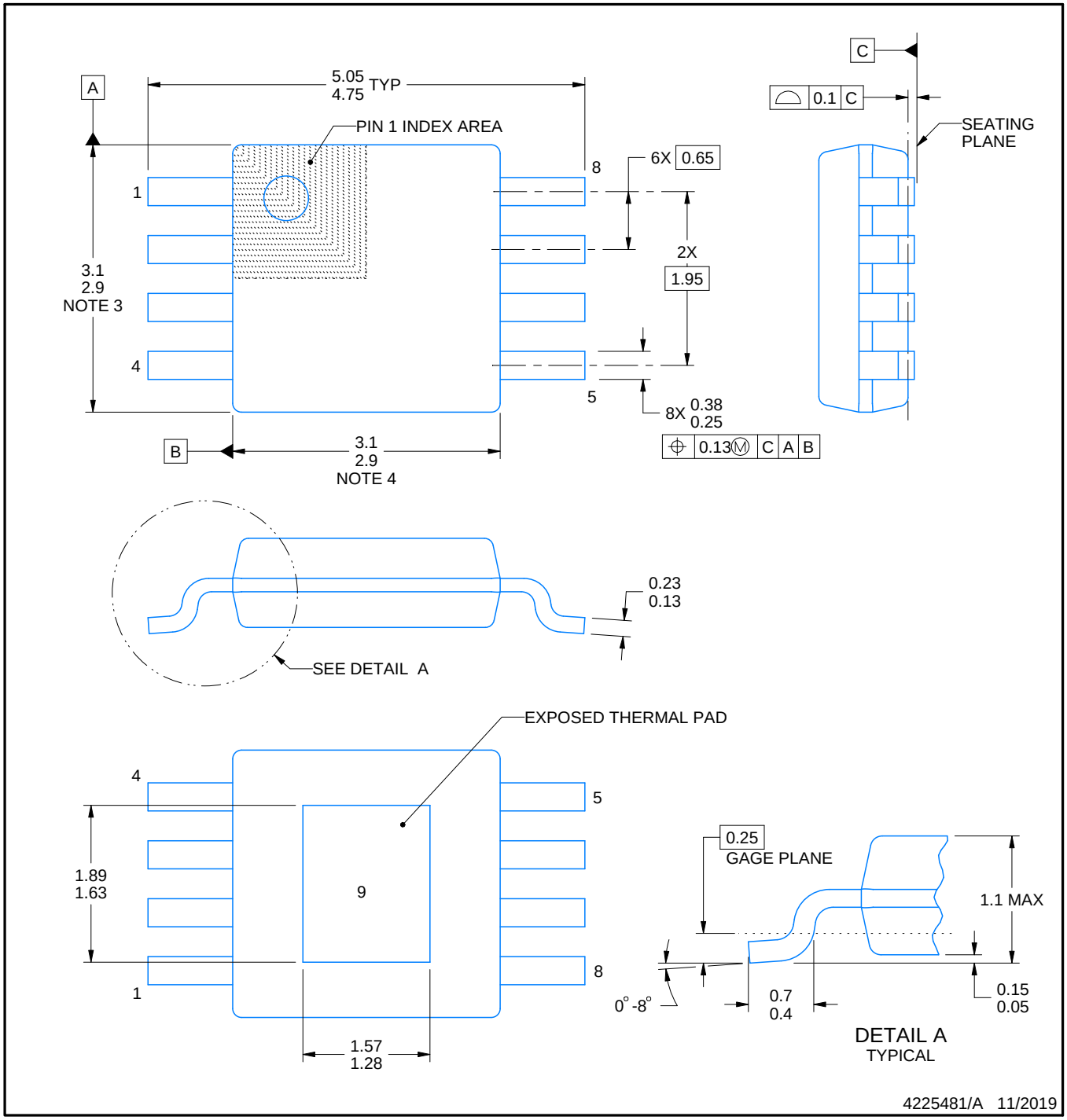
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

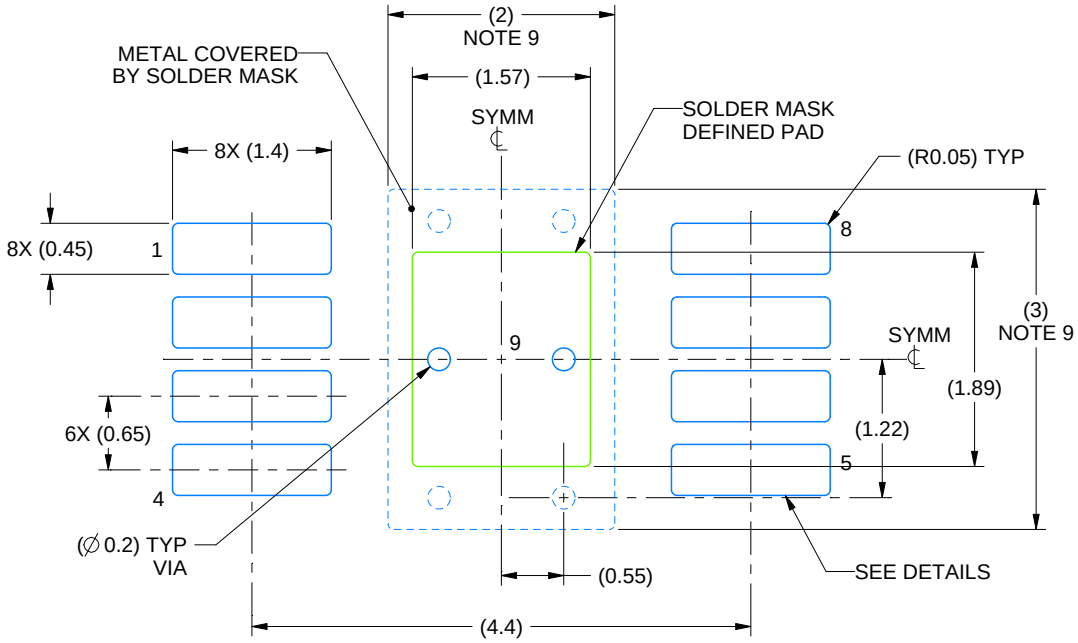
SMALL OUTLINE PACKAGE



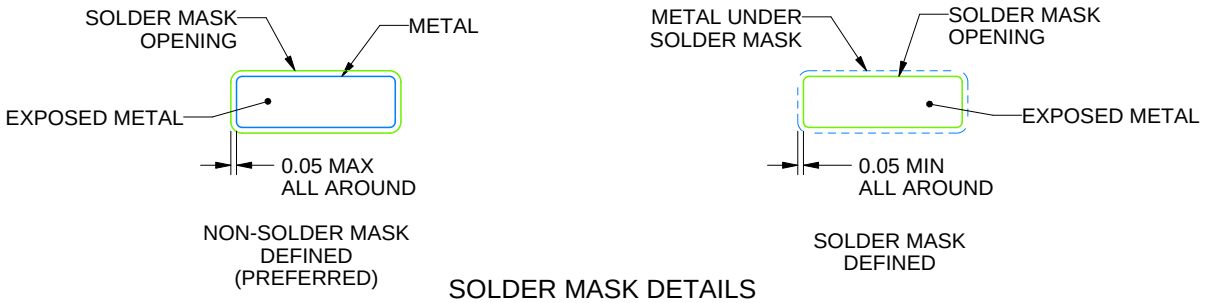
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

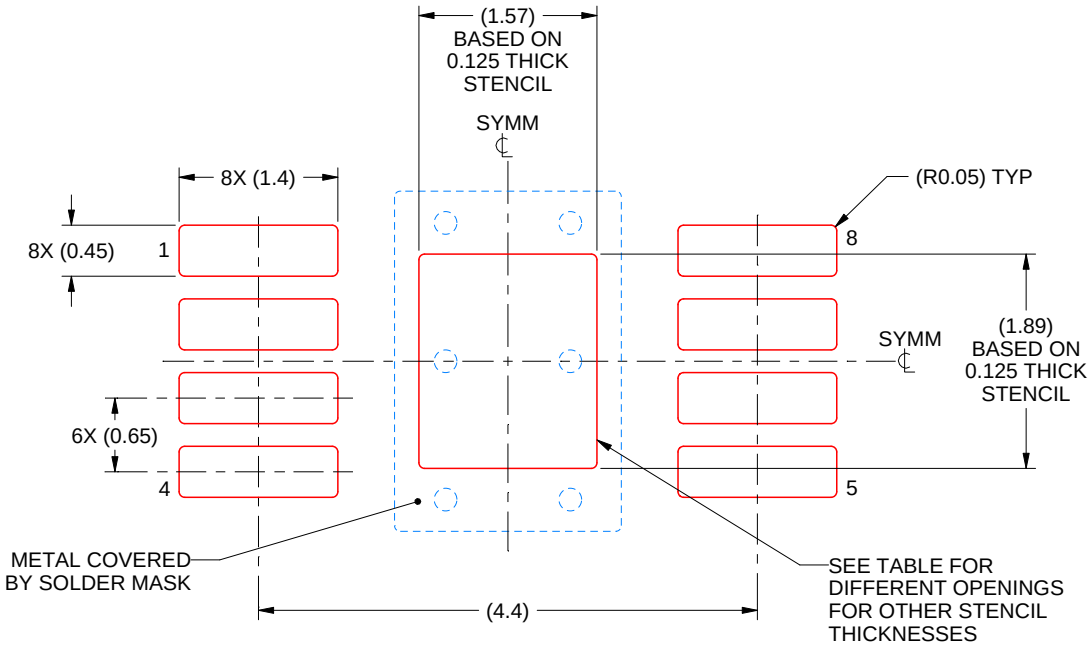


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

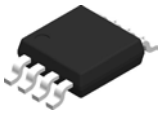
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

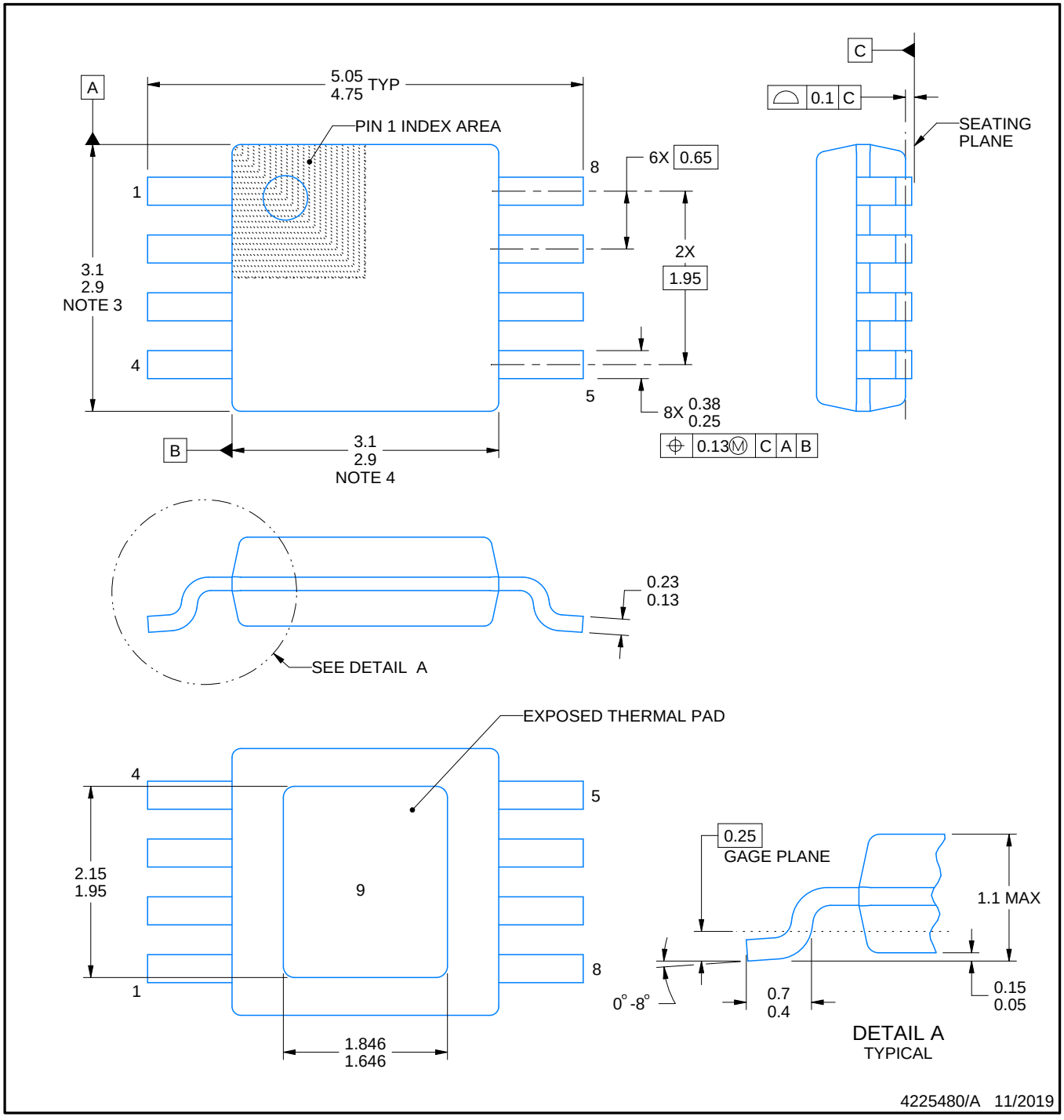
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

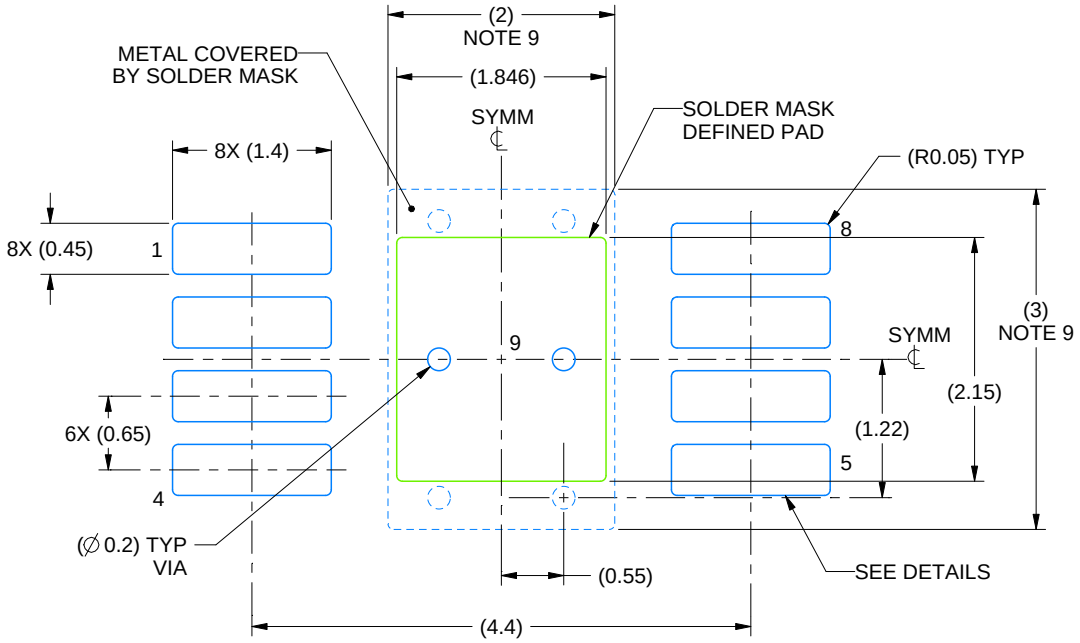
SMALL OUTLINE PACKAGE



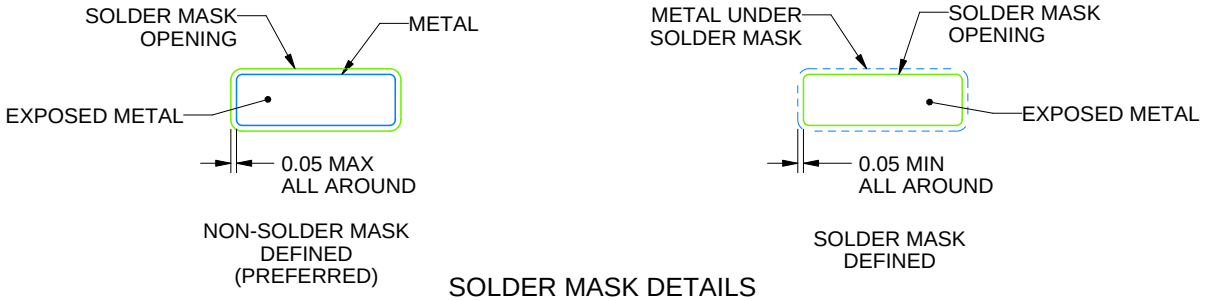
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

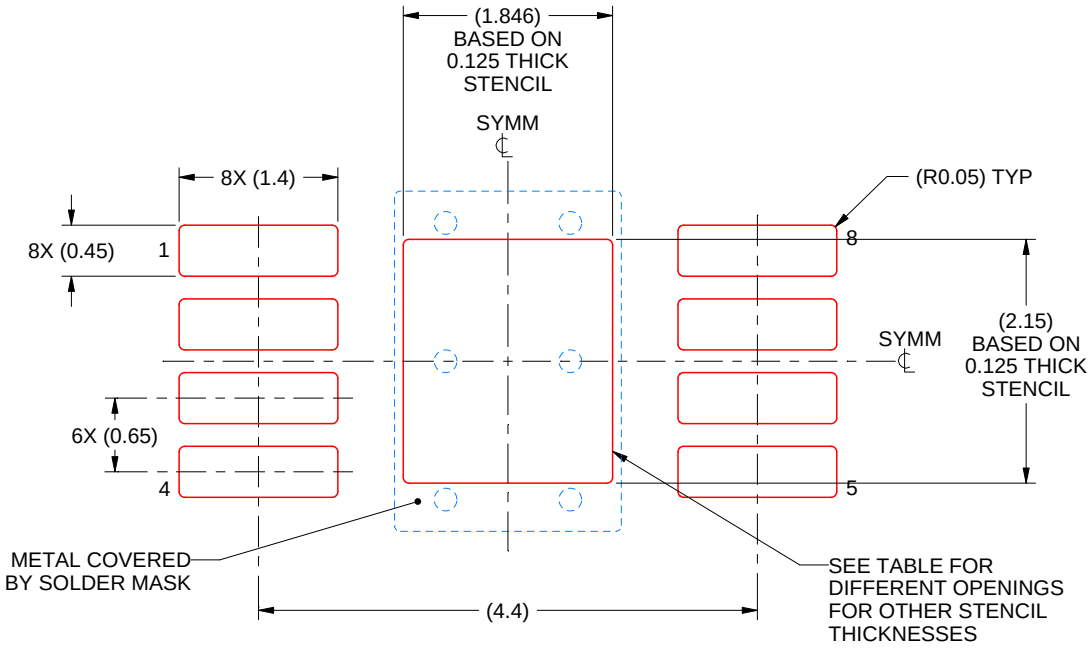


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

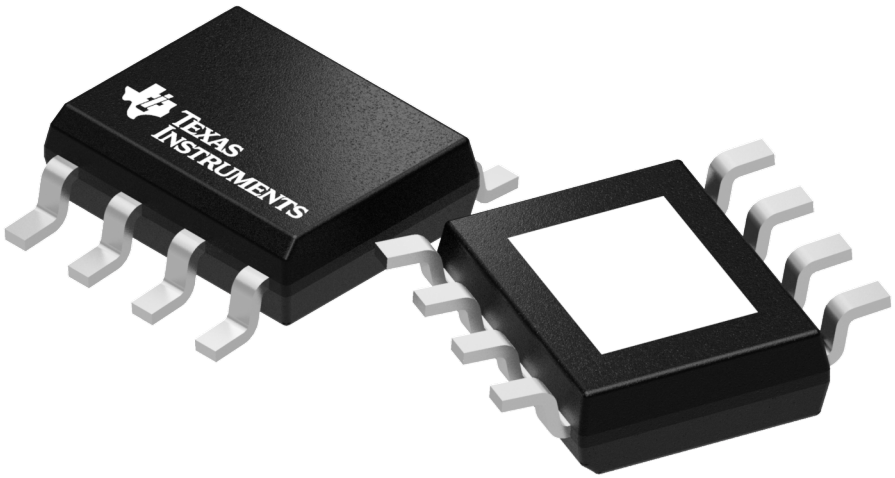
4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

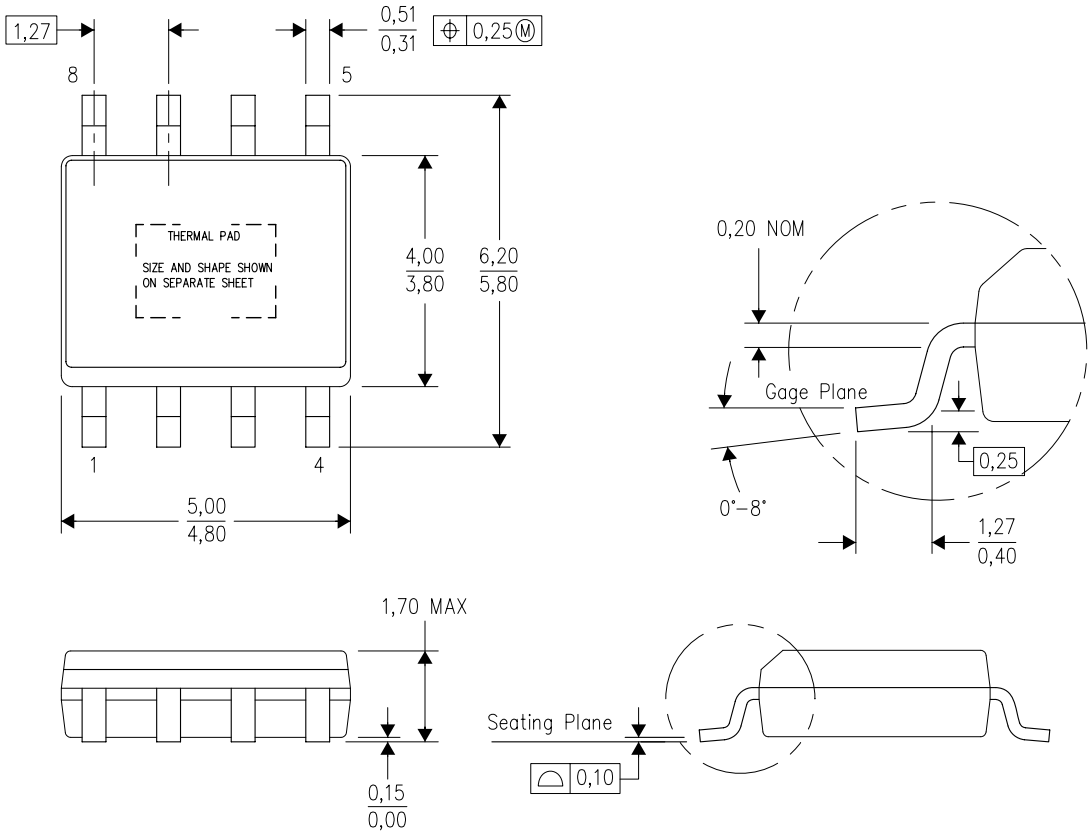
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

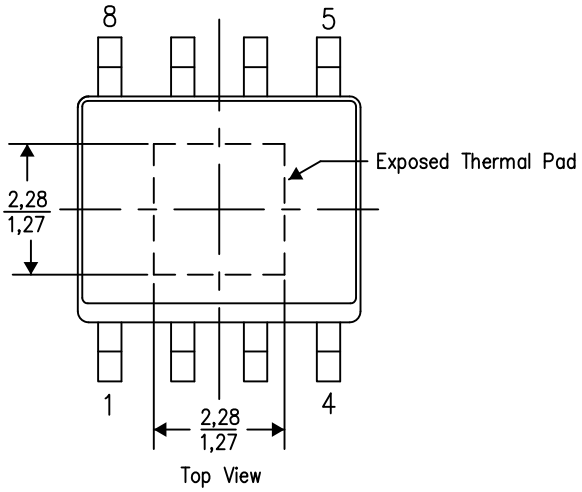
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



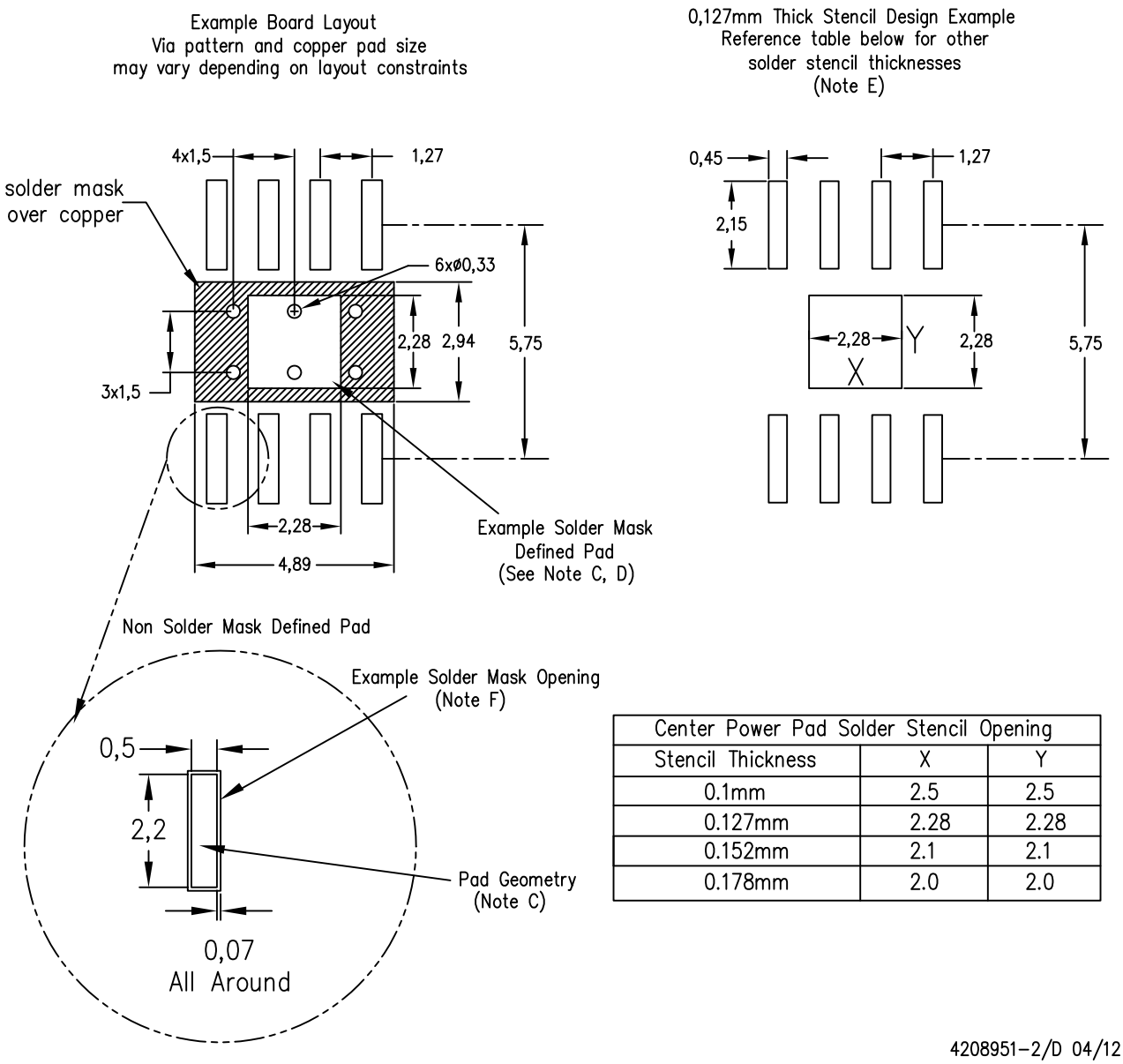
Exposed Thermal Pad Dimensions

4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

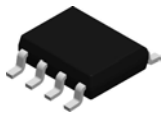
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

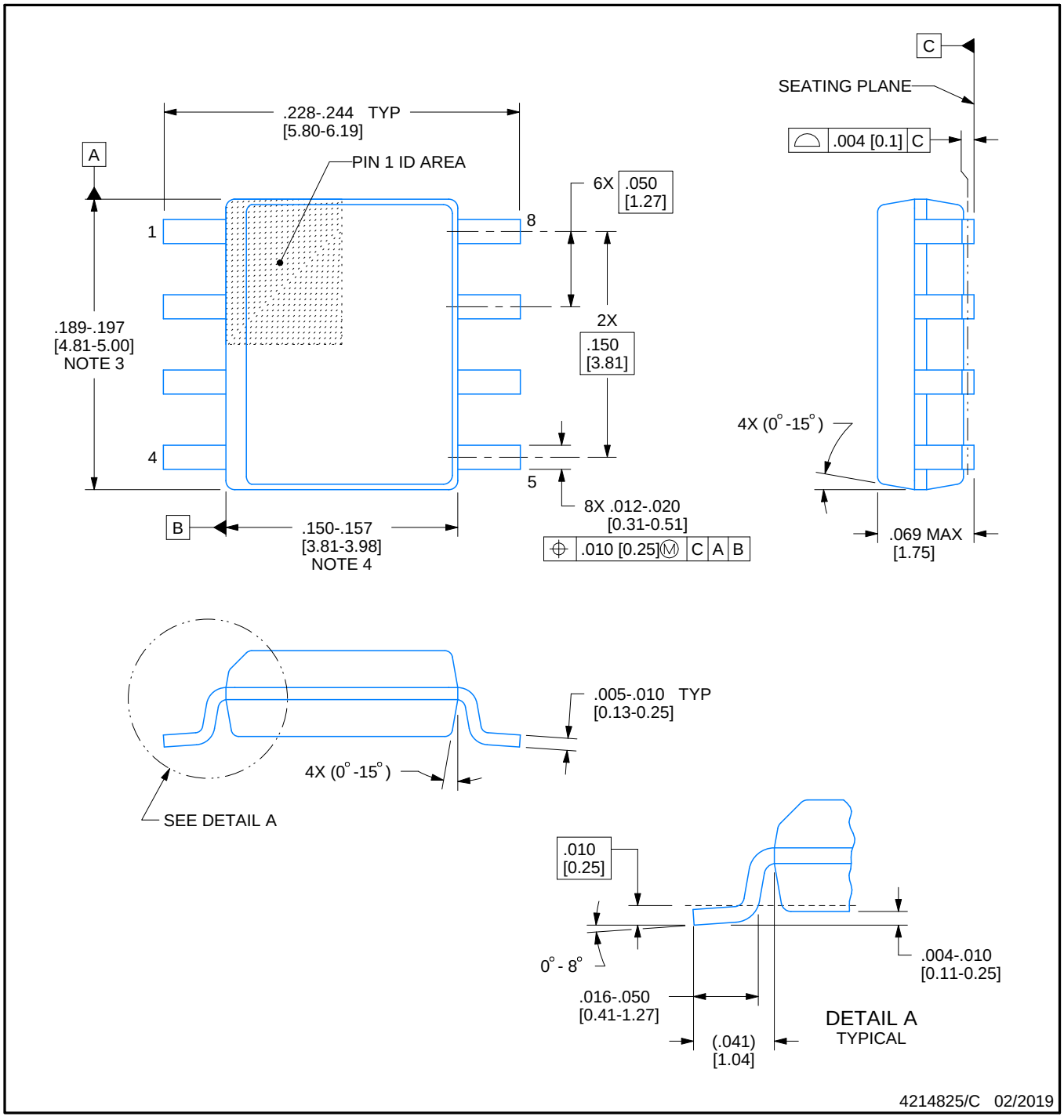


PACKAGE OUTLINE

D0008A

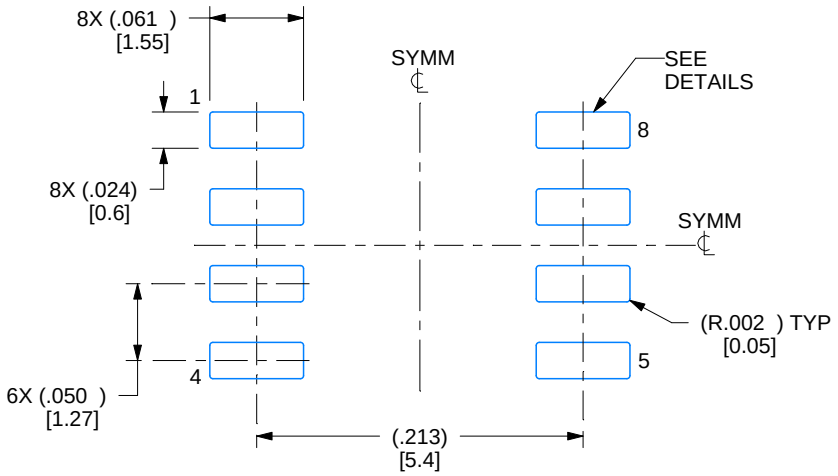
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

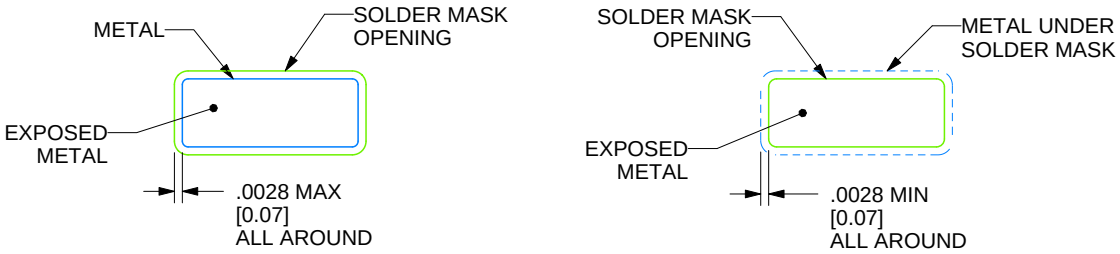


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

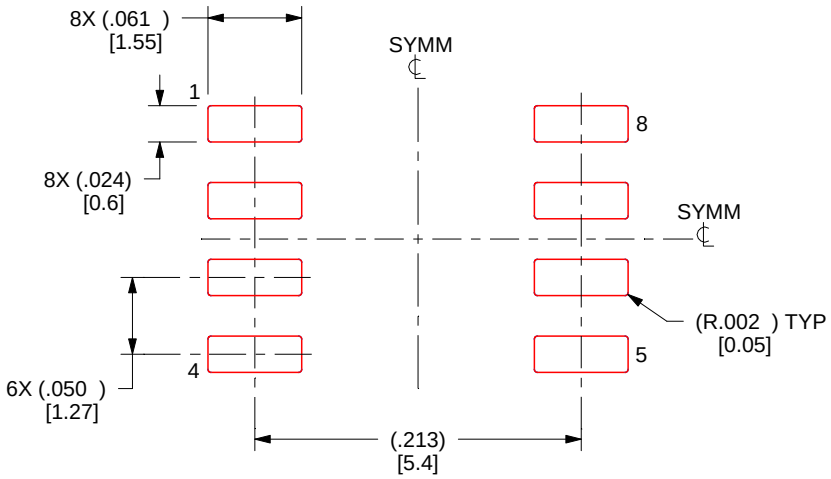
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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