4-Channel SDTV Video Amplifier with 6th-Order Filters and 5.6-V/V Gain

Check for Samples: THS7375

FEATURES

- **Four SDTV Video Amplifiers for CVBS, S-Video, Y'P'$_B$P'$_R$ 480i/576i, Y'U'V', G'B'R' (R'G'B'), or SCART**
- **Integrated Low-Pass Filters:**
  - **Sixth-Order 9.5-MHz (–3dB) Butterworth**
  - **–0.1-dB Bandwidth at 6 MHz**
  - **–1-dB Passband Bandwidth at 8 MHz**
  - **54-dB Attenuation at 27 MHz**
- **Versatile Input Biasing**
  - **DC-Coupled with 320-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp**
  - **AC-Coupled with Biasing Allowed**
- **Built-in 5.6-V/V Gain (14.95 dB)**
- **+3-V to +5-V Single-Supply Operation**
- **Rail-to-Rail Output:**
  - **Output Swings Within 100 mV from the Rails to Allow AC or DC Output Coupling**
  - **Supports Driving Two Lines per Channel**
- **Low 9.8-mA at 3.3-V Total Quiescent Current**
- **Low Differential Gain/Phase of 0.2%/0.35°**
- **Lead-Free and Green TSSOP-14 Package**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **Portable Media Player Video Buffering**
- **Security/Surveillance Systems**
- **DaVinci/OMAP/DMxxx Video Buffering**

DESCRIPTION

Fabricated using the revolutionary complementary Silicon-Germanium (SiGe) BiCom3X process, the THS7375 is a low-power, single-supply, 3 V to 5 V four-channel integrated video buffer. It incorporates a sixth-order Butterworth filter (able to be bypassed) that is useful as a digital-to-analog converter (DAC) reconstruction filter or an analog-to-digital converter (ADC) anti-aliasing filter. The 9.5-MHz filter is a perfect choice for SDTV video that includes composite (CVBS), S-video, Y'U'V', G'B'R' (R'G'B'), Y'P'$_B$P'$_R$ 480i/576i, and SCART systems.

As part of the THS7375 flexibility, the input can be configured for either ac or dc-coupled inputs. The 320-mV output level shift allows for a full sync dynamic range at the output with 0-V input. The ac-coupled modes include a transparent sync-tip clamp option for CVBS, Y', and G'B'R' signals with sync. AC-coupled biasing for C'/P'$_B$/P'$_R$ channels can easily be achieved by adding an external resistor to V_{S+}.

The THS7375 is the perfect choice for all video buffer applications. Its rail-to-rail output stage with 5.6-V/V gain allows for both ac and dc line driving. This architecture makes the THS7375 an ideal choice for DaVinci™ processors. The ability to drive two lines per channel, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 9.8-mA total quiescent current at 3.3 V and 0.1-μA disabled current makes it an excellent choice for USB-powered, portable, or other power-sensitive applications.

The THS7375 is available in a TSSOP-14 package that is lead-free and green (RoHS) compliant.

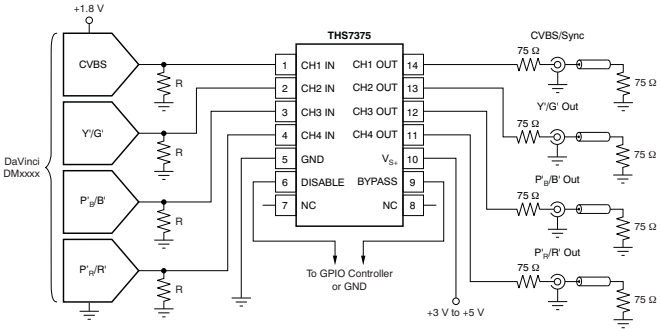


Figure 1. 3.3-V Single-Supply, DC-Input/DC-Output Coupled Video Line Driver

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
THS7375IPW	TSSOP-14	Rails, 90	Pb-Free, Green
THS7375IPWR		Tape and Reel, 2000	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material contentcan be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range unless otherwise noted.

		THS7375	UNIT
Supply voltage, V_{S+} to GND		5.5	V
Input voltage, V_I		–0.4 to V_{S+}	V
Output current, I_O		±90	mA
Continuous power dissipation		See Dissipation Ratings Table	
Maximum junction temperature, any condition(2) T_J		+150	°C
Maximum junction temperature, continuous operation, long-term reliability(3), T_J		+125	°C
Storage temperature range, T_{STG}		–65 to +150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		+300	°C
ESD ratings	Human body model (HBM)	2000	V
	Charged device model (CDM)	1000	V
	Machine model	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	AT $T_A \le +25°C$ POWER RATING(1)	AT $T_A = +85°C$ POWER RATING(1)
TSSOP-14 (PW)	35	115(2)	870 mW	348 mW

(1) Power rating is determined with a junction temperature of +125°C. This is the point where performance starts to degrade and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and reliability.
(2) These data were taken with the JEDEC High-K test printed circuit board (PCB). For the JEDEC low-K test PCB, the θ_{JA} is +185°C.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	3		5	V
Ambient temperature, T_A	–40		+85	°C

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ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V

R_L = 150 Ω to GND, dc-coupled input and output, Filter Mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7375					
		TYP	OVER TEMPERATURE			MIN/ TYP/ MAX	UNITS
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
AC PERFORMANCE							
Small-signal bandwidth (–3 dB)	V_O = 0.2 V_{PP} (1)	9.5	7.6/11.4	7.4/11.6	7.3/11.7	Min/ Max	MHz
Large-signal bandwidth (–3 dB)	V_O = 2 V_{PP} (1)	9.5	7.6/11.4	7.4/11.6	7.3/11.7	Min/ Max	MHz
–1 dB passband bandwidth		8				Typ	MHz
Bypass mode bandwidth (–3 dB)	V_O = 0.2 V_{PP}	70				Typ	MHz
Slew rate	Bypass mode	150				Typ	V/µs
Attenuation with respect to 500 kHz	f = 6.75 MHz (2)	0.3	–0.9/1.1	–1/1.4	–1.1/1.6	Min/ Max	dB
	f = 27 MHz (2)	54	42	40	39	Min	dB
Group delay	f = 100 kHz	75				Typ	ns
Group delay variation with respect to 100 kHz	f = 5.1 MHz	10				Typ	ns
Channel-to-channel delay		0.3				Typ	ns
Differential gain	NTSC/PAL	0.2/0.3				TYP	%
Differential phase	NTSC/PAL	0.35/0.5				Typ	°
Total harmonic distortion	f = 1 MHz, V_O = 2 V_{PP}	–65				Typ	dB
Signal-to-noise ratio	100 kHz to 6 MHz: non-weighted / unified weighting	61 / 70				Typ	dB
Channel-to-channel crosstalk	f = 1 MHz, worst case	–55				Typ	dB
AC gain—all channels		14.95	14.7/15.3	14.6/15.4	14.6/15.4	Min/ Max	dB
Output impedance	f = 5 MHz, Filter Mode	1.4				Typ	Ω
DC PERFORMANCE							
Biased output voltage	V_{IN} = 0 V	320	170/430	160/440	150/450	Min/ Max	mV
Input voltage range	DC input, limited by output	–0.1/0.52				Typ	V
Sync tip clamp charge current	V_{IN} = –0.1 V	200	140	130	120	Min	µA
Input resistance		800				Typ	kΩ
Input capacitance		2				Typ	pF
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to +1.65 V	3.15				Typ	V
	R_L = 150 Ω to GND	3.1	2.85	2.75	2.75	Min	V
	R_L = 75 Ω to +1.65 V	3.1				Typ	V
	R_L = 75 Ω to GND	3				Typ	V
Low output voltage swing	R_L = 150 Ω to +1.65 V (V_{IN} = –0.2 V)	0.05				Typ	V
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)	0.02	0.12	0.16	0.17	Max	V
	R_L = 75 Ω to +1.65 V (V_{IN} = –0.2 V)	0.1				Typ	V
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)	0.05				Typ	V
Output current (sourcing)	R_L = 10 Ω to +1.65 V	80				Typ	mA
Output current (sinking)	R_L = 10 Ω to +1.65 V	70				Typ	mA

(1) The min/max values listed for this specification are ensured by design and characterization only.
(2) 3.3-V supply filter specifications are ensured by 100% testing at 5-V supply along with design and characterization only.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

R_L = 150 Ω to GND, dc-coupled input and output, Filter Mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7375					
		TYP	OVER TEMPERATURE			MIN/ TYP/ MAX	UNITS
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
POWER SUPPLY							
Maximum operating voltage	V_{S+} to GND	3.3	5.5	5.5	5.5	Max	V
Minimum operating voltage	V_{S+} to GND(3)	3.3	2.85	2.85	2.85	Min	V
Maximum quiescent current	V_{IN} = 0 V; V_{S+} = 3.3 V	9.8	12	13	14	Max	mA
Minimum quiescent current	V_{IN} = 0 V; V_{S+} = 3.3 V	9.8	8	7	6.5	Min	mA
Power-supply rejection (+PSRR)		53				Typ	dB
LOGIC CHARACTERISTICS(4)							
V_{IH}	Disabled or bypass engaged	1.8	2	2	2	Min	V
V_{IL}	Enabled or bypass disengaged	0.7	0.65	0.6	0.6	Max	V
I_{IH}		0.2				Typ	µA
I_{IL}		0.2				Typ	µA
Disable time		100				Typ	ns
Enable time		100				Typ	ns
Bypass/filter switch time		5				Typ	ns
Disabled quiescent current	Disable pin = 2 V	0.1	10	10	10	Max	µA
Disabled output impedance	Disable pin = 2 V	20 ‖ 3				Typ	kΩ ‖ pF

(3) The min/max values listed for this specification are ensured by design and characterization only.
(4) The logic input pins should not be left floating. They must be connected to logic low (or GND) or logic high (or V_{S+}).

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V

R_L = 150 Ω to GND, dc-coupled input and output, Filter Mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7375					
		TYP	OVER TEMPERATURE			MIN/ TYP/ MAX	UNITS
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
AC PERFORMANCE							
Small-signal bandwidth (–3 dB)	V_O = 0.2 V_{PP} (1)	9.5	7.6/11.4	7.4/11.6	7.3/11.7	Min/ Max	MHz
Large-signal bandwidth (–3 dB)	V_O = 2 V_{PP} (1)	9.5	7.6/11.4	7.4/11.6	7.3/11.7	Min/ Max	MHz
–1 dB passband bandwidth		8				Typ	MHz
Bypass mode bandwidth (–3 dB)	V_O = 0.2 V_{PP}	70				Typ	MHz
Slew rate	Bypass mode	150				Typ	V/µs
Attenuation with respect to 500 kHz	f = 6.75 MHz	0.3	–0.9/1.1	–1/1.4	–1.1/1.6	Min/ Max	dB
	f = 27 MHz	54	42	40	39	Min	dB
Group delay	f = 100 kHz	75				Typ	ns
Group delay variation with respect to 100 kHz	f = 5.1 MHz	10				Typ	ns
Channel-to-channel delay		0.3				Typ	ns
Differential gain	NTSC/PAL	0.2/0.3				Typ	%
Differential phase	NTSC/PAL	0.35/0.5				Typ	°
Total harmonic distortion	f = 1 MHz, V_O = 2 V_{PP}	–70				Typ	dB
Signal-to-noise ratio	100 kHz to 6 MHz: non-weighted / unified weighting	61/70				Typ	dB
Channel-to-channel crosstalk	f = 1 MHz, worst case	–55				Typ	dB
AC gain—all channels		14.95	14.7/15.3	14.6/15.4	14.6/15.4	Min/ Max	dB
Output impedance	f = 5 MHz; filter mode	1.4				Typ	Ω
DC PERFORMANCE							
Biased output voltage/level shift	V_{IN} = 0 V	320	170/430	160/440	150/450	Min/ Max	mV
Input voltage range	Limited by output	–0.1/0.8				Typ	V
Sync tip clamp charge current	V_{IN} = –0.1 V	200	140	130	120	Min	µA
Input resistance		800				Typ	kΩ
Input capacitance		2				Typ	pF
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to +2.5V	4.85				Typ	V
	R_L = 150 Ω to GND	4.75	4.4	4.3	4.3	Min	V
	R_L = 75 Ω to +2.5V	4.7				Typ	V
	R_L = 75 Ω to GND	4.5				Typ	V
Low output voltage swing	R_L = 150 Ω to +2.5V (V_{IN} = –0.2 V)	0.05				Typ	V
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)	0.02	0.12	0.16	0.17	Max	V
	R_L = 75 Ω to +2.5 V (V_{IN} = –0.2 V)	0.1				Typ	V
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)	0.05				Typ	V
Output current (sourcing)	R_L = 10 Ω to +2.5 V	90				Typ	mA
Output current (sinking)	R_L = 10 Ω to +2.5 V	85				Typ	mA

(1) The min/max values listed for this specification are ensured by design and characterization only.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

R_L = 150 Ω to GND, dc-coupled input and output, Filter Mode, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7375					
		TYP	OVER TEMPERATURE			MIN/ TYP/ MAX	UNITS
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
POWER SUPPLY							
Maximum operating voltage	V_{S+} to GND	5	5.5	5.5	5.5	Max	V
Minimum operating voltage	V_{S+} to GND(2)	5	2.85	2.85	2.85	Min	V
Maximum quiescent current	V_{IN} = 0 V, V_{S+} = 5 V	10.3	12.5	13.5	14.5	Max	mA
Minimum quiescent current	V_{IN} = 0 V, V_{S+} = 5 V	10.3	8	7.5	7	Min	mA
Power-supply rejection (+PSRR)		53				Typ	dB
DISABLE CHARACTERISTICS(3)							
V_{IH}	Disabled/bypass engaged(4)	2.1	2.2	2.2	2.2	Min	V
V_{IL}	Enabled/bypass disengaged	0.8	0.8	0.8	0.8	Max	V
I_{IH}		0.2				Typ	μA
I_{IL}		0.2				Typ	μA
Disable time		80				Typ	ns
Enable time		80				Typ	ns
Bypass/filter switch time		5				Typ	ns
Disabled quiescent current	Disable pin = 3 V	1	10	10	10	Max	μA
Disabled output impedance	Disable pin = 3 V	20 ‖ 3				Typ	kΩ ‖ pF

(2) The min/max values listed for this specification are ensured by design and characterization only.
(3) The logic input pins should not be left floating. They must be connected to logic low (or GND) or logic high (or V_{S+}).
(4) Defined as applied logic voltage to achieve total quiescent current of less than 100 μA.

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PIN CONFIGURATION

PW PACKAGE
TSSOP-14
TOP VIEW

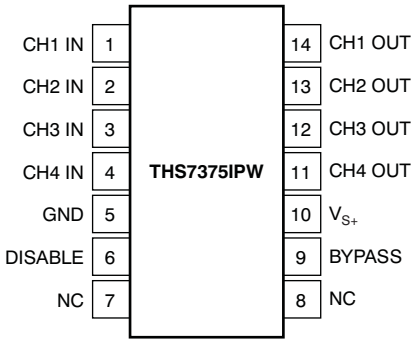
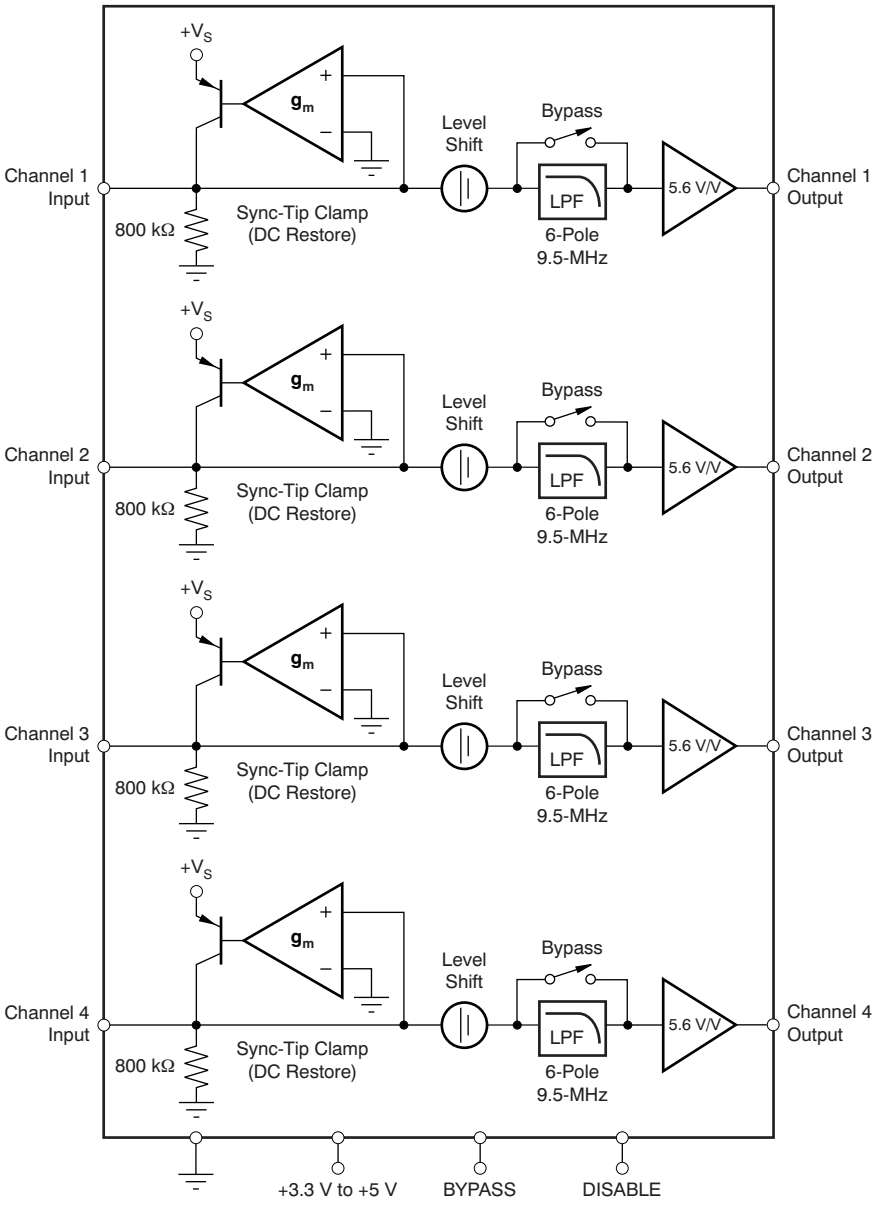


Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CH1 IN	1	I	Video input; channel 1
CH2 IN	2	I	Video input; channel 2
CH3 IN	3	I	Video input; channel 3
CH4 IN	4	I	Video input; channel 4
GND	5	I	Ground pin for all internal circuitry
DISABLE	6	I	Disable pin. Logic high disables the part; logic low enables the part. This pin must not be left floating. It must be connected to a defined logic state (or GND or V_{S+})
NC	7, 8	—	No internal connection
BYPASS	9	I	Internal filter bypass. Logic high bypasses the internal low-pass filter; logic low uses the internal filters.This pin must not be left floating. It must be connected to a defined logic state (or GND or V_{S+})
V_{S+}	10	I	Positive power-supply pin; connect to +3 V to +5 V
CH4 OUT	11	O	Video output; channel 4
CH3 OUT	12	O	Video output; channel 3
CH2 OUT	13	O	Video output; channel 2
CH1 OUT	14	O	Video output; channel 1

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FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

TOTAL QUIESCENT CURRENT vs TEMPERATURE

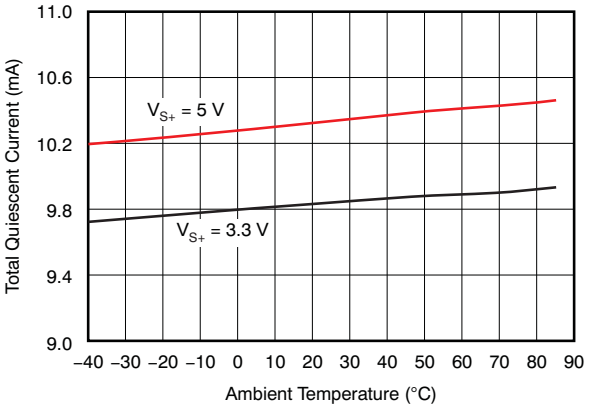


Figure 2.

OUTPUT OFFSET VOLTAGE vs TEMPERATURE

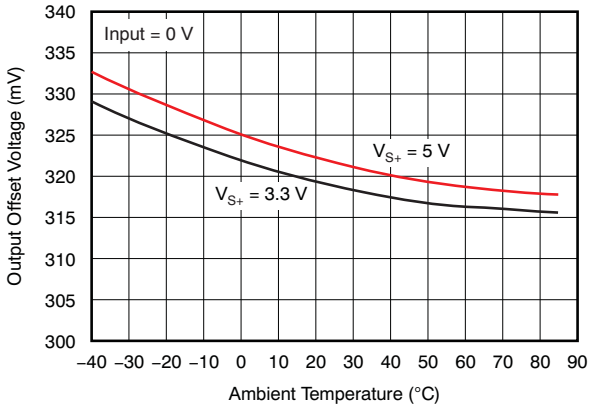


Figure 3.

INPUT RESISTANCE vs TEMPERATURE

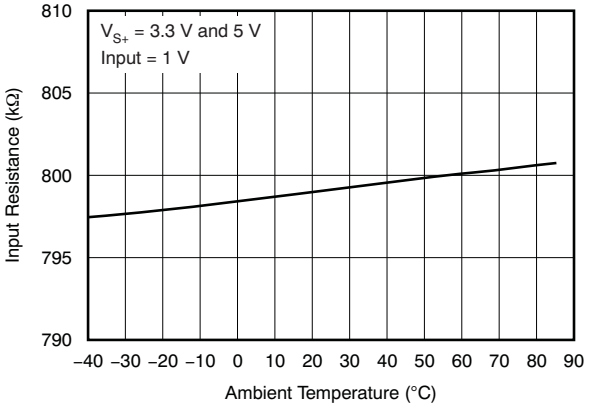


Figure 4.

MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

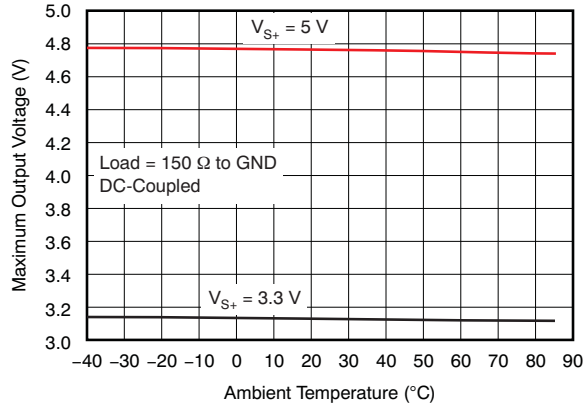


Figure 5.

MINIMUM OUTPUT VOLTAGE vs TEMPERATURE

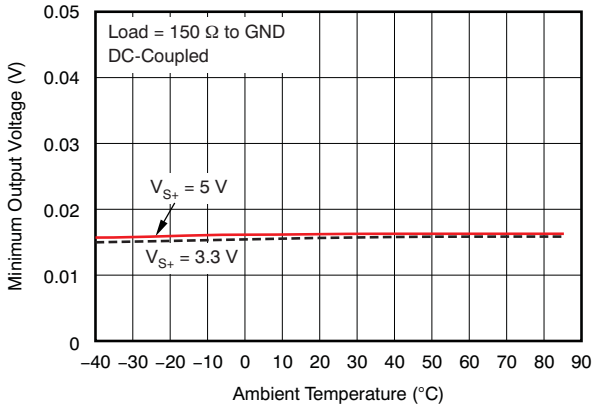


Figure 6.

ATTENUATION AT 6.75 MHz vs TEMPERATURE

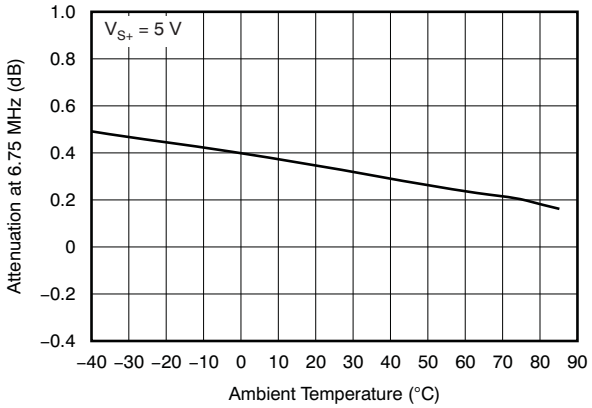


Figure 7.

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TYPICAL CHARACTERISTICS (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

ATTENUATION AT 27 MHz vs TEMPERATURE

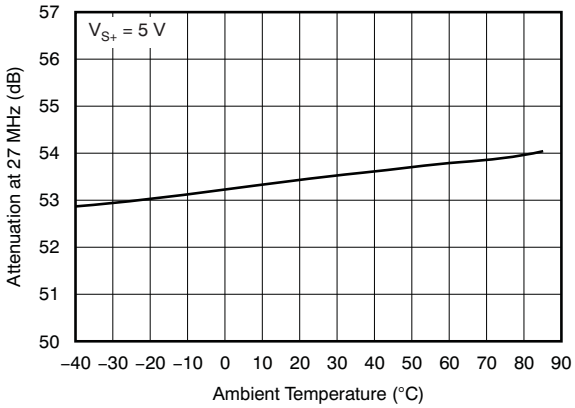


Figure 8.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL-SIGNAL GAIN vs FREQUENCY

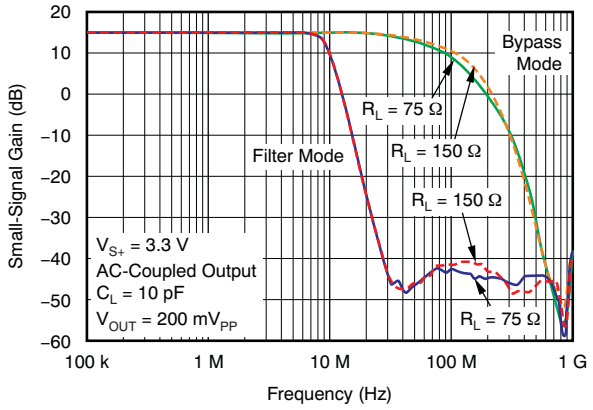


Figure 9.

SMALL-SIGNAL GAIN vs FREQUENCY

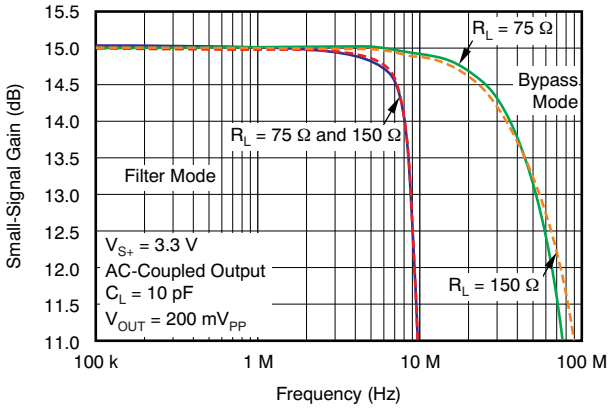


Figure 10.

PHASE vs FREQUENCY

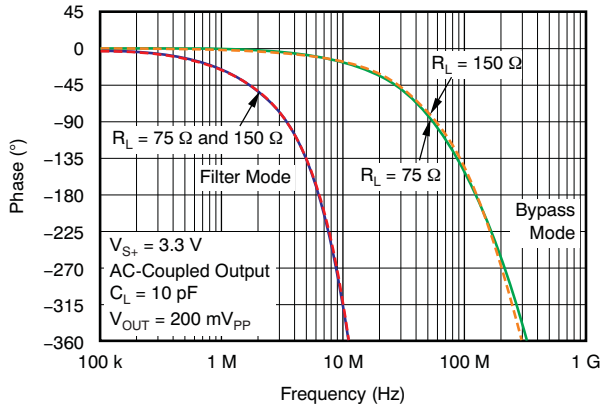


Figure 11.

GROUP DELAY vs FREQUENCY

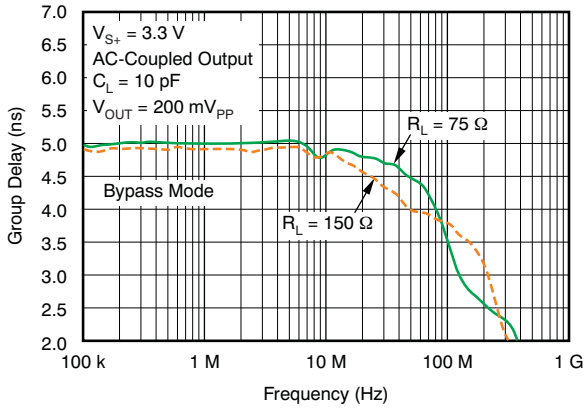


Figure 12.

GROUP DELAY vs FREQUENCY

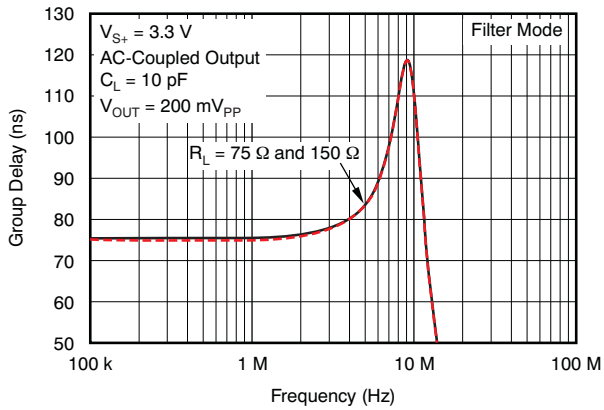


Figure 13.

LARGE-SIGNAL GAIN vs FREQUENCY

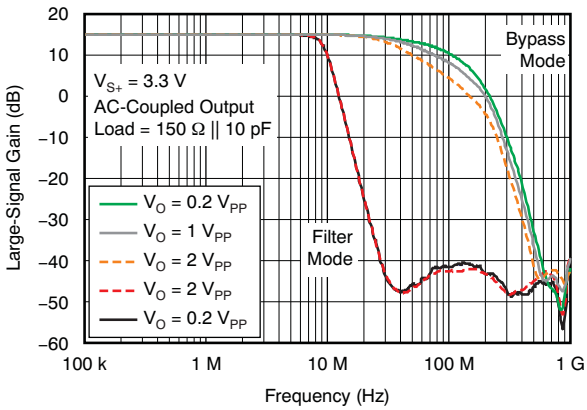


Figure 14.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

LARGE-SIGNAL GAIN vs FREQUENCY

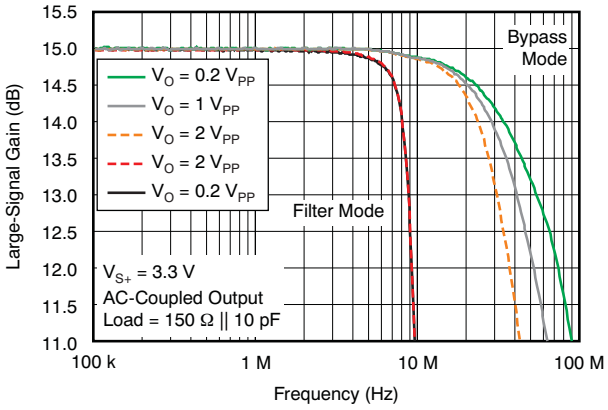


Figure 15.

SMALL-SIGNAL GAIN vs FREQUENCY

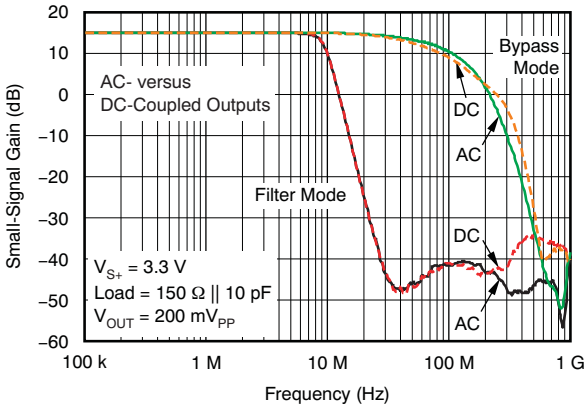


Figure 16.

SMALL-SIGNAL GAIN vs FREQUENCY

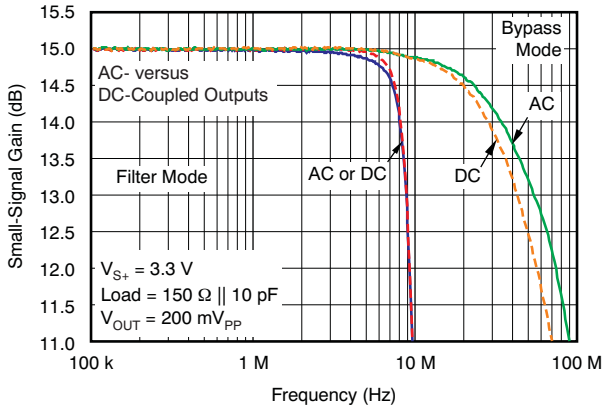


Figure 17.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

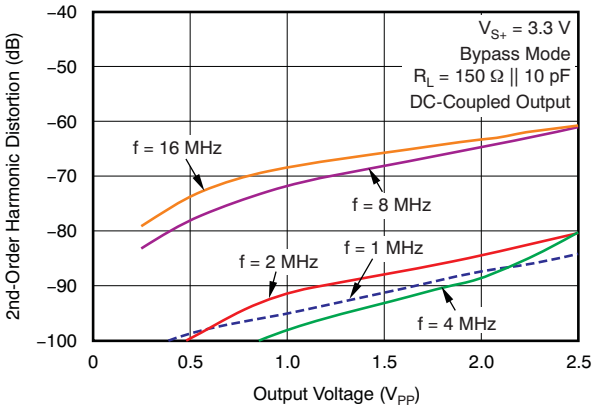


Figure 18.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

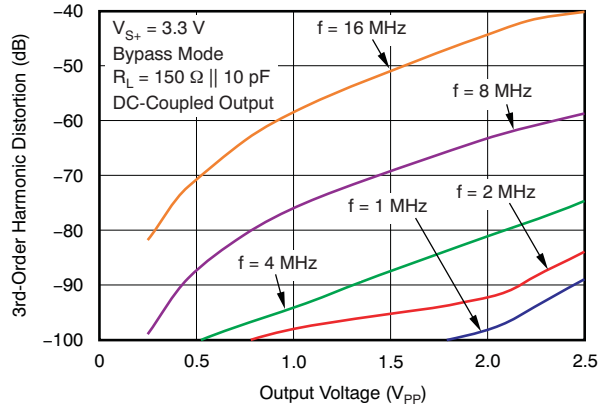


Figure 19.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

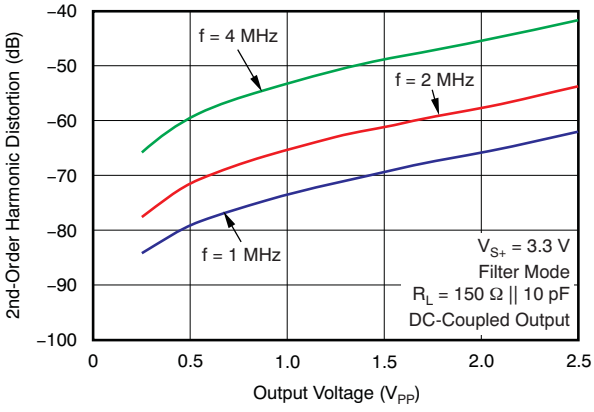


Figure 20.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

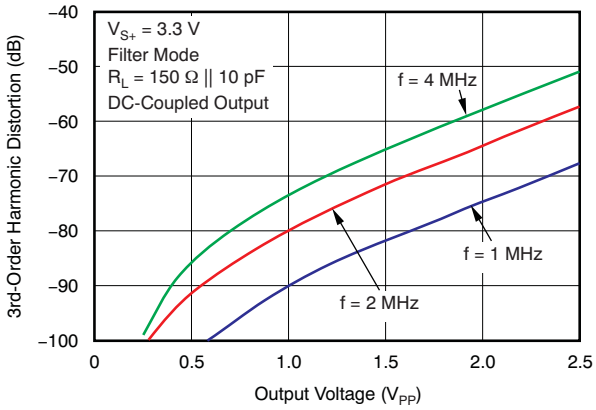


Figure 21.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

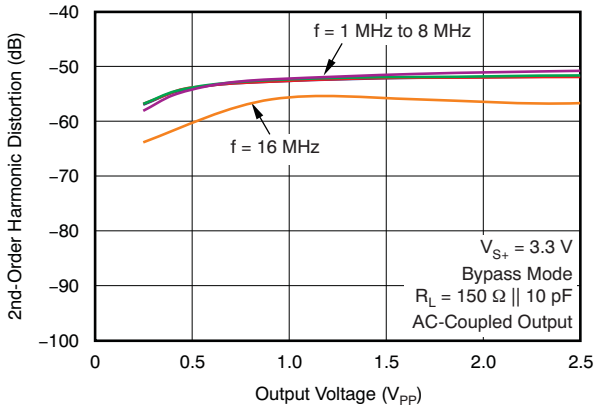


Figure 22.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

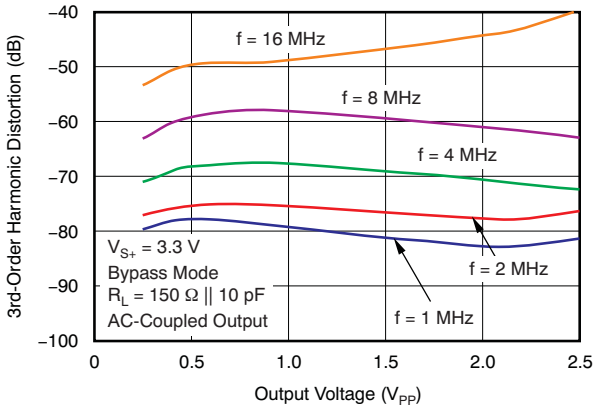


Figure 23.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

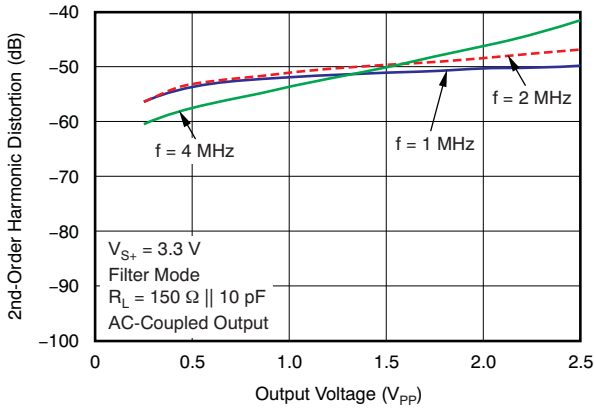


Figure 24.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

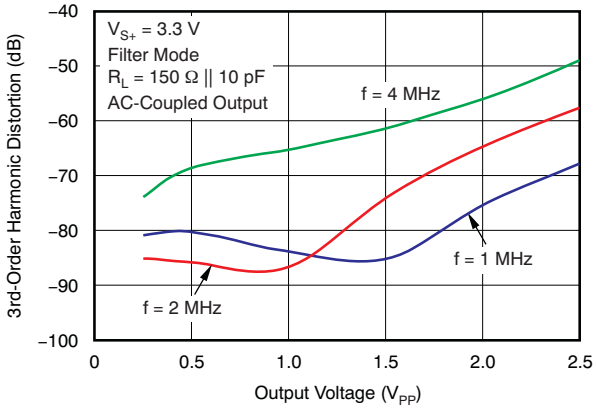


Figure 25.

OUTPUT IMPEDANCE vs FREQUENCY

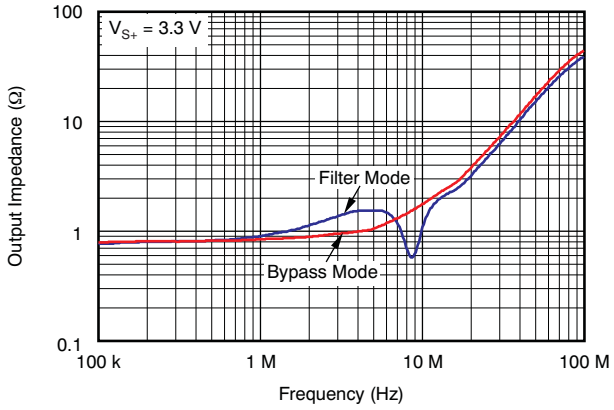


Figure 26.

TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

RETURN LOSS vs FREQUENCY

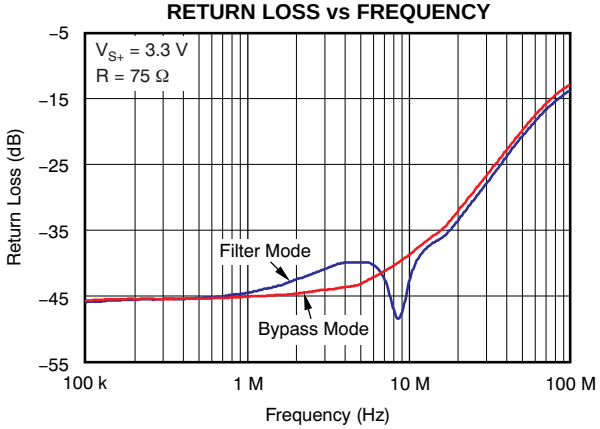


Figure 27.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL-SIGNAL GAIN vs FREQUENCY

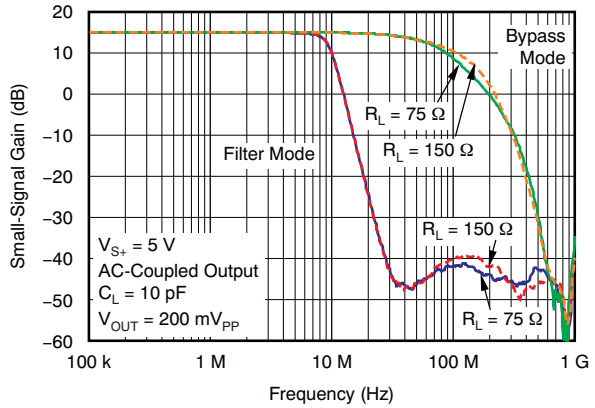


Figure 28.

SMALL-SIGNAL GAIN vs FREQUENCY

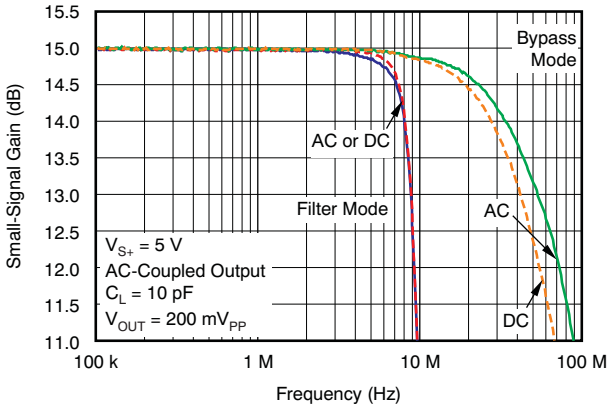


Figure 29.

PHASE vs FREQUENCY

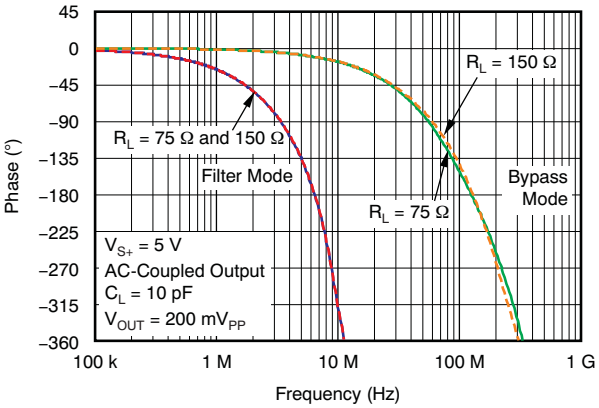


Figure 30.

GROUP DELAY vs FREQUENCY

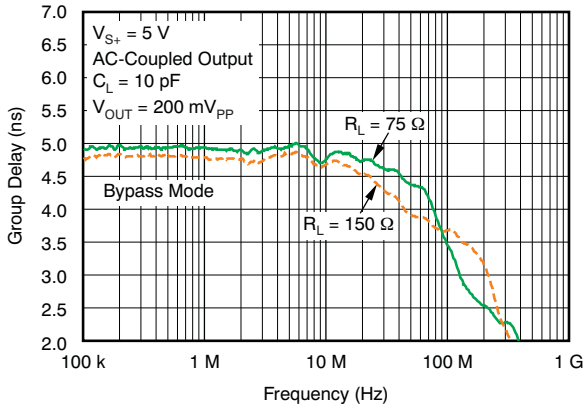


Figure 31.

GROUP DELAY vs FREQUENCY

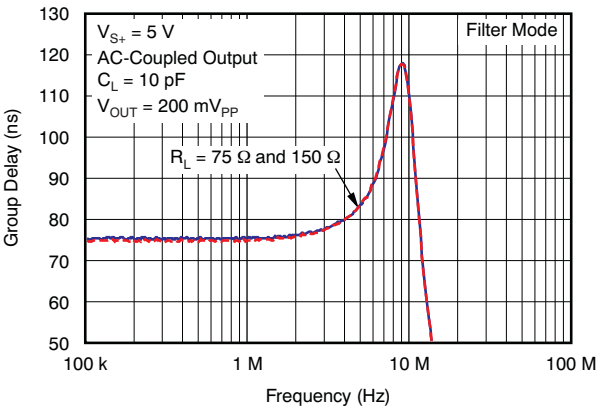


Figure 32.

LARGE-SIGNAL GAIN vs FREQUENCY

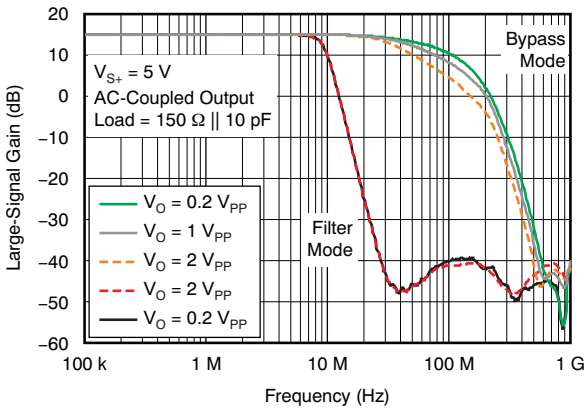


Figure 33.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

LARGE-SIGNAL GAIN vs FREQUENCY

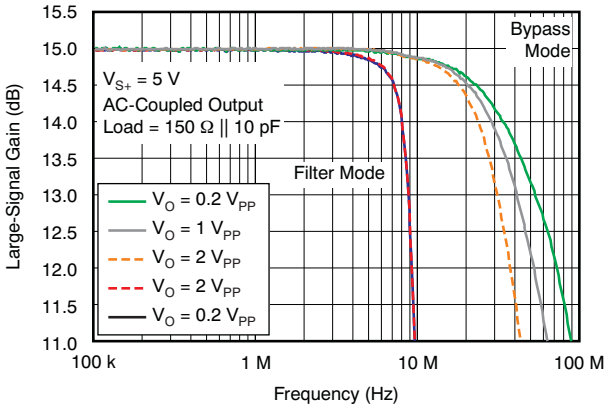


Figure 34.

SMALL-SIGNAL GAIN vs FREQUENCY

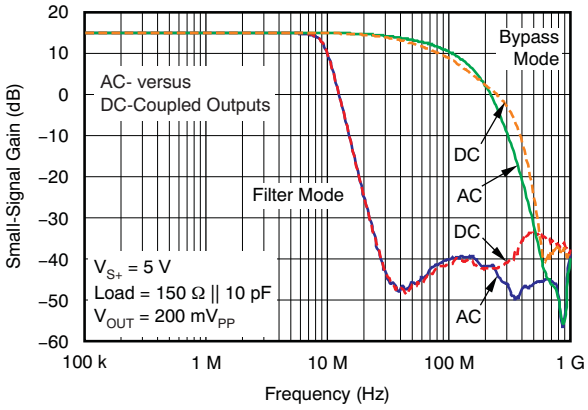


Figure 35.

SMALL-SIGNAL GAIN vs FREQUENCY

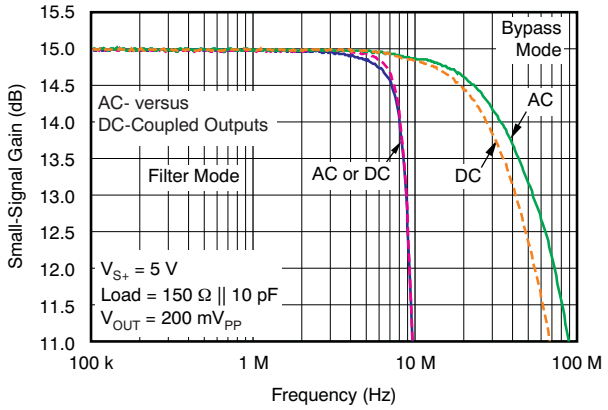


Figure 36.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

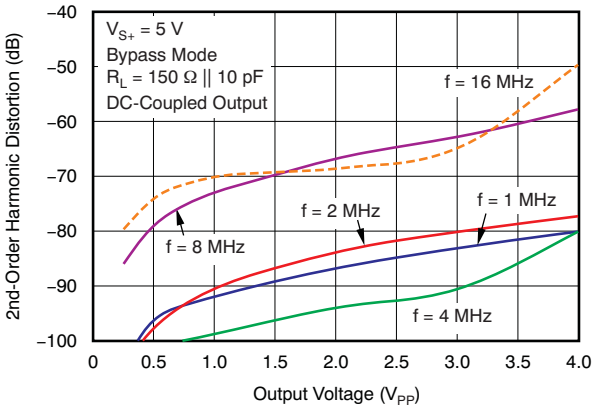


Figure 37.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

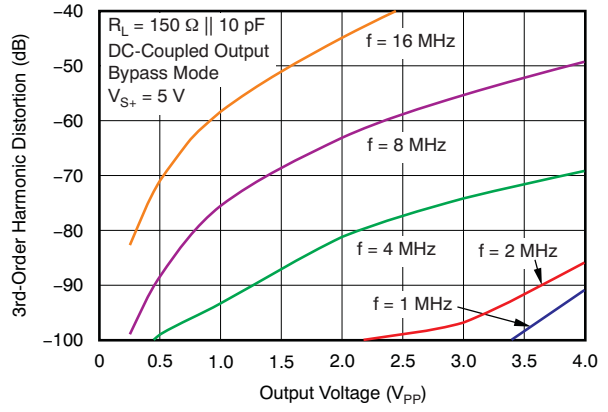


Figure 38.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

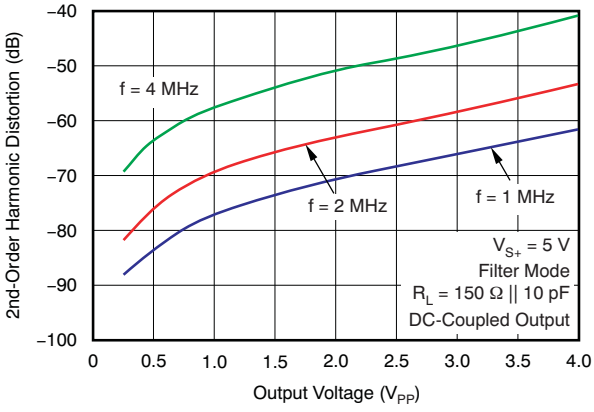


Figure 39.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

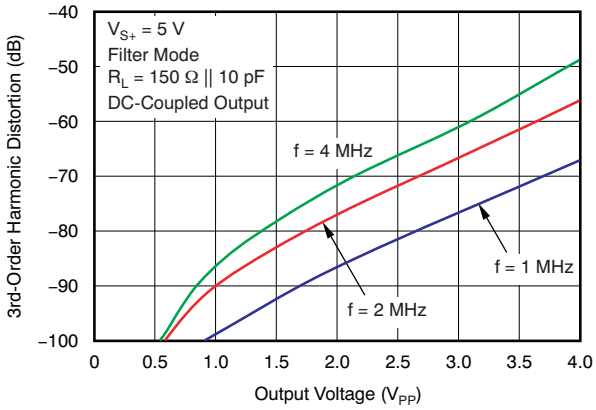


Figure 40.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

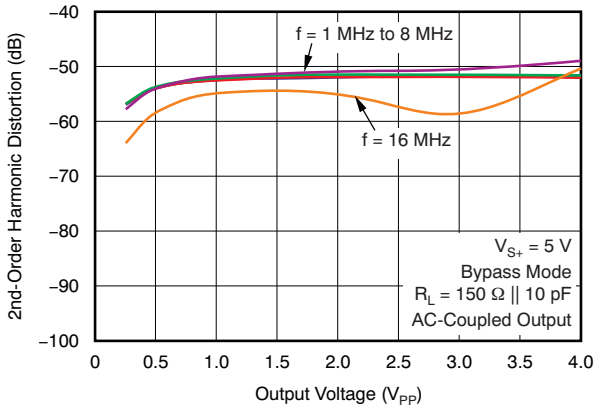


Figure 41.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

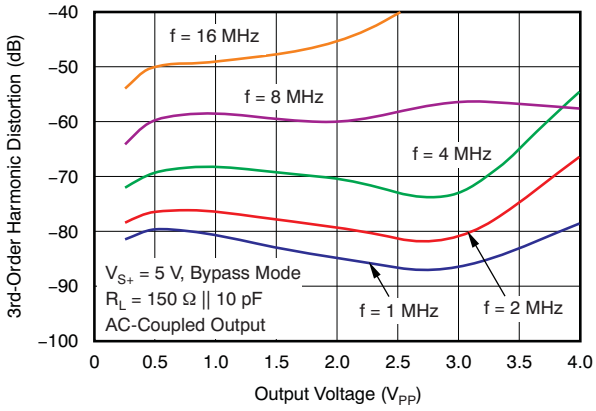


Figure 42.

2ND-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

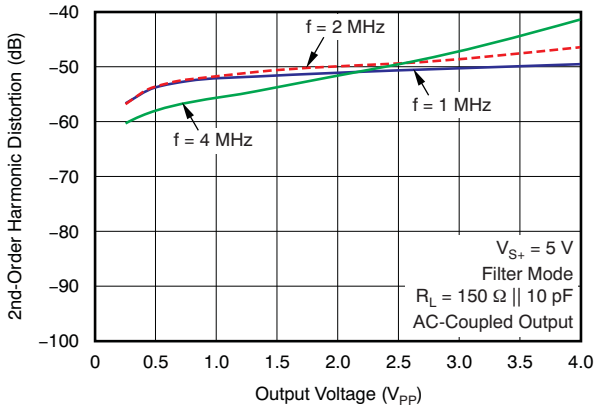


Figure 43.

3RD-ORDER HARMONIC DISTORTION vs OUTPUT VOLTAGE

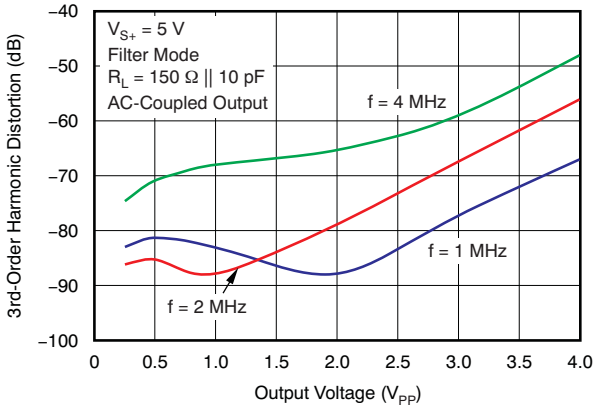


Figure 44.

OUTPUT IMPEDANCE vs FREQUENCY

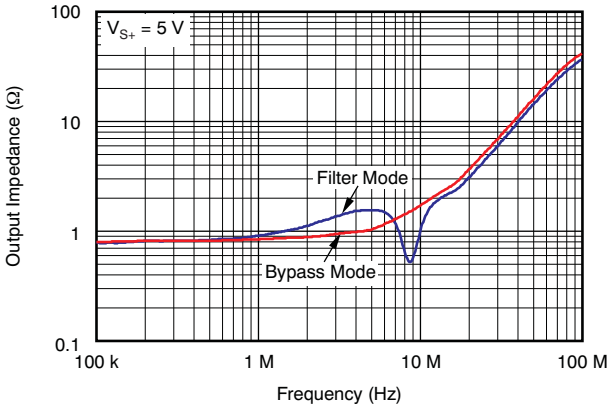


Figure 45.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

RETURN LOSS vs FREQUENCY

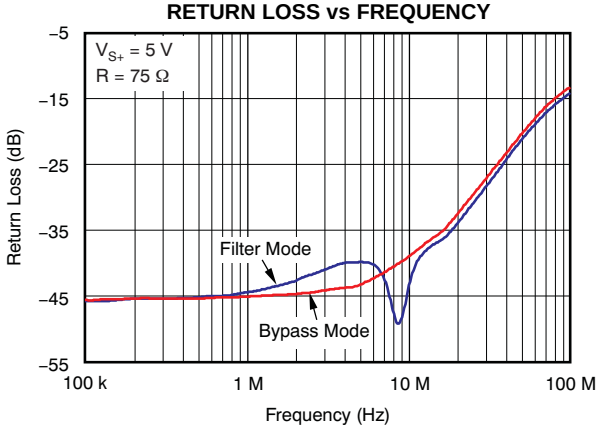


Figure 46.

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APPLICATION INFORMATION

The THS7375 is targeted for standard definition video output buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7375. Built on the revolutionary complementary Silicon Germanium (SiGe) BiCom3X process, the THS7375 incorporates many features not typically found in integrated video parts while consuming very low power. The THS7375 has the following features:

- Single-supply 3-V to 5-V operation with low total quiescent current of 9.8 mA at 3.3 V and 10.3 mA at 5 V.
- Disable mode allows for shutting down the THS7375 to save system power in power-sensitive applications.
- Input configuration accepts dc + level shift, ac sync-tip clamp, or ac-bias.
- AC-biasing is allowed with the use of a single external pull-up resistor to the positive power supply.
- Sixth-order low-pass filter for DAC reconstruction or ADC image rejection:
  - 9.5 MHz for NTSC, PAL, SECAM, composite (CVBS), S-Video Y'C', 480i/576i $Y'P'_BP'_R$, G'B'R' (R'G'B'), and SCART signals.
- Bypass mode bypasses the low-pass filter with a 70-MHz bandwidth and 150-V/μs slew rate amplifier
- Internal fixed gain of 5.6 V/V (+14.95 dB) buffer that can drive two video lines per channel with dc-coupling or traditional ac-coupling. This feature is ideal for DaVinci, DM2xx, DM3xx, DM64xx, and OMAP processors.
- Signal flow-through configuration in a TSSOP-14 package that complies with the latest lead-free (RoHS-compatible) and green manufacturing requirements.

OPERATING VOLTAGE

The THS7375 is designed to operate from 3-V to 5-V over a –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high quality, low temperature coefficient capacitors. The design of the THS7375 allows operation down to 2.85 V, but it is recommended to use at least a 3-V supply to ensure that there are no issues with headroom or clipping.

Place a 0.1-μF to 0.01-μF capacitor as close as possible to the power-supply pins. Failure to do so may result in ringing or oscillating at the THS7375 outputs. Additionally, a large capacitor (22 μF to 100 μF) should be placed on the power-supply line to minimize interference with 50-Hz/60-Hz line frequencies.

INPUT VOLTAGE

The THS7375 input range allows for an input signal range from –0.2 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 5.6 V/V (+14.95 dB) and the internal level shift that causes a 320-mV level shift, the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.2 V to 3.5 V. As a result of the gain and level shift, the linear output range limits the allowable linear input range to be from about –0.1 V to 0.8 V.

INPUT OVERVOLTAGE PROTECTION

The THS7375 is built using a very high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 47.

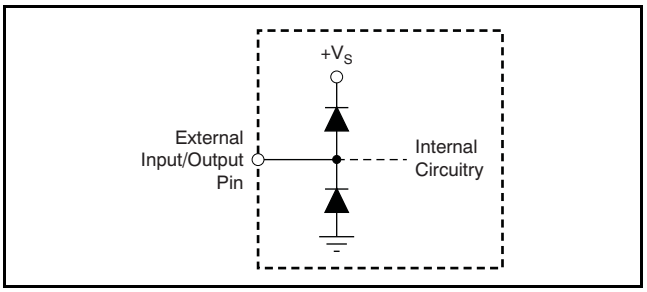


Figure 47. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

TYPICAL CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit that uses the THS7375 as a video buffer is shown in Figure 48. It shows a DAC or encoder driving the input channels of the THS7375. One channel is a composite video (CVBS) channel of a standard definition (SD) video system. The other channels are the component video $Y'P'_BP'_R$ (sometimes labeled Y'U'V' or incorrectly labeled $Y'C'_BC'_R$) signals of a 480i or 576i system. These channels could easily be the S-Video Y'/C' channels or the R'G'B' channels of a SCART system.

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (Y) term. The reason for this usage is to account for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

This rationale is also used for the chroma (C') term. Chroma is derived from the nonlinear R'G'B' terms and thus it is also nonlinear. Chominance (C) is derived from linear RGB, giving the difference between chroma (C') and chrominance (C). The color difference signals (P'_B/P'_R/U'/V') are also referenced in this way to denote the nonlinear (gamma corrected) signals.

R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This configuration is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Furthermore, because the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

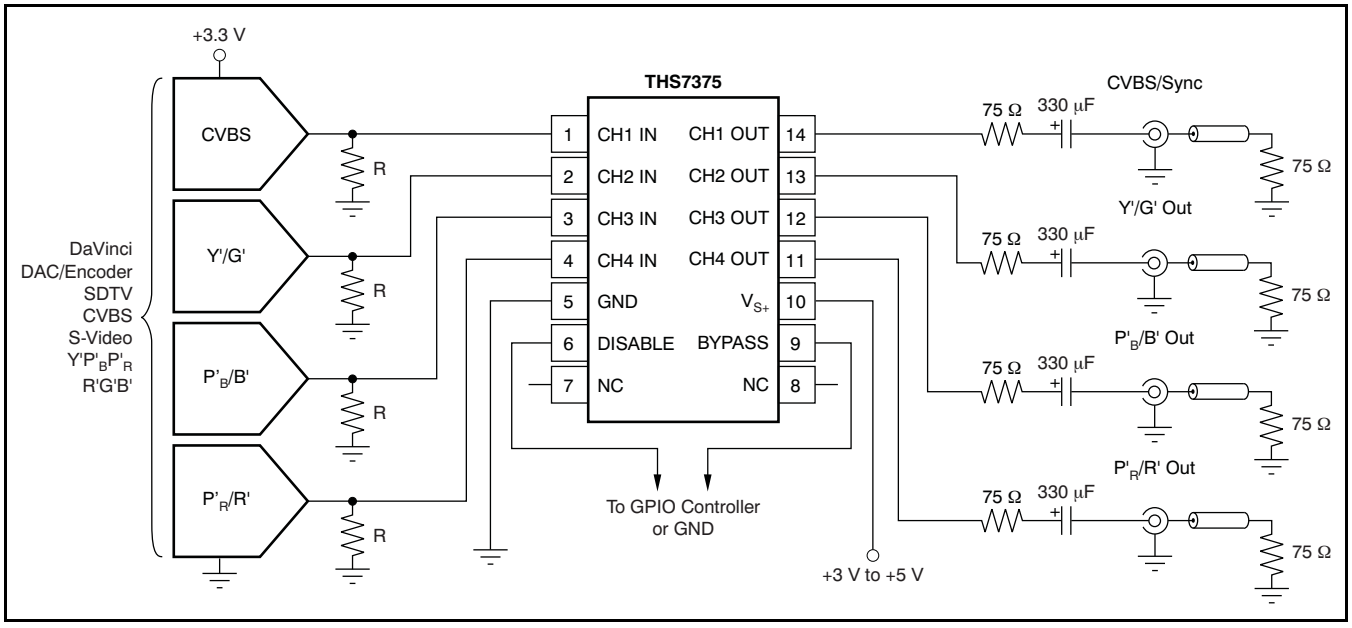


Figure 48. Typical SDTV CVBS/$Y'P'_BP'_R$ Inputs from DC-Coupled Encoder/DAC with AC-Coupled Line Driving

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INPUT MODE OF OPERATION: DC

The THS7375 allows for both ac-coupled and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7375. One of the drawbacks to dc coupling, however, is when 0 V is applied to the input. Although the input of the THS7375 allows for a 0-V input signal with no issues, the output swing of a traditional amplifier cannot yield a 0-V signal, resulting in possible clipping. This condition is true for any single-supply amplifier as a result of output transistor limitations. Both CMOS and bipolar transistors cannot go to 0 V while sinking current. This characterization of a transistor is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the receiver of this video signal uses an AGC loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This overcorrection may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control, and a reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation/clipping problems, the THS7375 has a 320-mV output level shift feature. This feature takes the input voltage and adds an internal shift to the signal. The THS7375 rail-to-rail output stage can create this output level while connected to a typical video load. This feature ensures that no saturation/clipping of the sync signals occur. This shift is constant, regardless of the input signal. For example, if a 0.4-V input is applied, the output is at (0.4 V × 5.6 V/V) + 0.32 V = 2.56 V.

Because the internal gain is fixed at 5.6 V/V (+14.95 dB), the gain dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3.3 V, the maximum output is approximately 3.15 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is [(3.2 V – 0.32 V) / 5.6 V/V] = 0.51 V. This calculation is true for up to the maximum recommended 5-V power supply that allows approximately a [(4.9 V – 0.32 V) / 5.6 V/V] = 0.818 V input range while avoiding clipping on the output.

The input impedance of the THS7375 in this mode of operation is dictated by the internal 800-kΩ pull-down resistor, as shown in Figure 49. Note that the internal voltage shift does not appear at the input pin, but only the output pin.

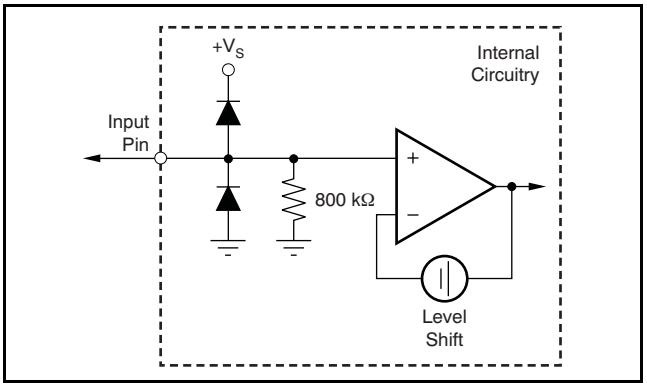


Figure 49. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION: AC SYNC-TIP CLAMP

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. The resulting video signals are generally at too high of a voltage for a dc-coupled video buffer to function properly. To account for this scenario, the THS7375 incorporates a sync-tip clamp (STC) circuit. This function requires a capacitor (nominally 0.1 μF) to be in series with the input. Note that while the term *sync-tip clamp* is used throughout this document, it should be noted that the THS7375 would probably be better termed to be a *dc restoration circuit* based on how this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7375 has an internal control loop that sets the lowest input applied voltage to clamp at ground (0 V). By setting the reference at 0 V, the THS7375 allows a dc-coupled input to also function. Therefore, the STC is considered transparent because it does not operate unless the input signal goes below ground. The signal then goes through the same level shifter, resulting in an output voltage low level of 320 mV. If the input signal tries to go below 0 V, the internal control loop of the THS7375 sources up to 3 mA of current to increase the input voltage level on the THS7375 input side of the coupling capacitor. As soon as the voltage goes above the 0-V level, the loop stops sourcing current and becomes very high impedance.

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One of the concerns about the sync tip clamp level is how the clamp reacts to a sync edge that has overshoot—common in VCR signals or reflections found in poor printed circuit board (PCB) layouts. Ideally, the STC should not react to the overshoot voltage of the input signal. Otherwise, this issue could result in clipping on the remainder of the video signal because it may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7375 has an internal low-pass filter as shown in Figure 50. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but in general it is close to an 800-ns delay. This filter slows down the response of the control loop so as not to clamp on the input overshoot voltage, but rather the flat portion of the sync signal.

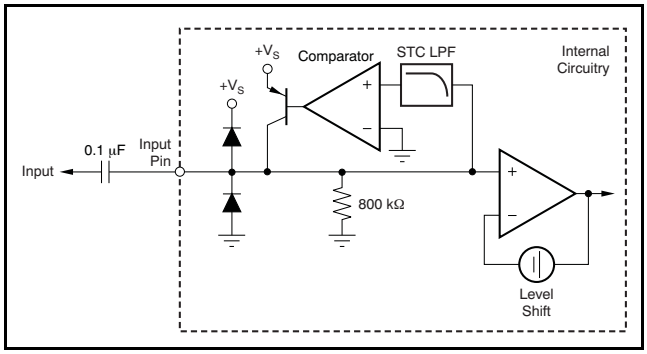


Figure 50. Equivalent AC Sync-Tip Clamp Input Circuit

As a result of this delay, the sync may have an apparent voltage shift. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because the sync is primarily for timing purposes, with synchronization occurring on the edge of the sync signal, this shift is transparent in most systems.

While this feature may not fully eliminate overshoot issues on the input signal in case of severe overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (such as 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage that appears at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This feature helps ensure a very robust STC system.

When the ac STC operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 0-V clamp level, the internal loop of the THS7375 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0-V reference level increases, the amount of source current increases proportionally—supplying up to 3 mA of current. Thus, the time period to re-establish the proper STC voltage can be very short. If the difference is very small, then the source current is also very small to account for minor voltage droop.

However, if the input signal goes above the 0-V input level, a problem arises. The problem is that the video signal is always above this level and must not be altered in any way. But if the sync level of the input signal is above this 0-V level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 0-V level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This issue is often seen by looking at the tilt (droop) of a constant luma signal being applied and observing the resulting output level. The associated change in luma level from the beginning of the video line to the end of the video line is the amount of line tilt (droop).

If the discharge current is very small, then the amount of tilt is very low, which is a generally a good thing. However, the amount of time for the system to capture the sync signal could be too long. This effect is also called *hum rejection*. Hum arises from the ac line voltage frequency of 50-Hz or 60-Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

To allow for both dc-coupling and ac-coupling in the same part, the THS7375 incorporates an 800-kΩ resistor to ground. Although a true constant-current sink is preferred over a resistor, there are significant issues when the voltage is near ground. This condition can cause the current sink transistor to saturate and cause potential problems with the signal. Also, this resistor is large enough to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is applied. If the video signal is 1 V, then there is 1 V/800 kΩ = 1.25 µA of discharge current. If more hum rejection is desired or there is a loss of sync occurring, simply decrease the 0.1-µF input coupling capacitor. A decrease from 0.1 µF to 0.047 µF increases the hum rejection by a factor of 2:1. Alternatively, an external pull-down resistor to ground may be added that decreases the overall resistance and ultimately increases the discharge current.

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To ensure proper stability of the ac STC control loop, the source impedance must be less than 1 kΩ with the input capacitor in place. Otherwise, there is a possibility for the control loop to ring; this ringing may appear on the THS7375 output. Because most DACs or encoders use resistors to establish the voltage, which are typically less than 500 Ω, meeting the less than 1-kΩ requirement is easily done. However, if the source impedance looking from the THS7375 input perspective is very high, simply adding a 1-kΩ resistor to GND ensures proper operation of the THS7375.

INPUT MODE OF OPERATION: AC BIAS

Sync-tip clamps are ideal for signals that have horizontal and/or vertical syncs associated with them. However, some video signals do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then a dc bias is required to properly set the dc operating point within the THS7375. This function is easily accomplished with the THS7375 by simply adding an external pull-up resistor to the positive power supply, as shown in Figure 51.

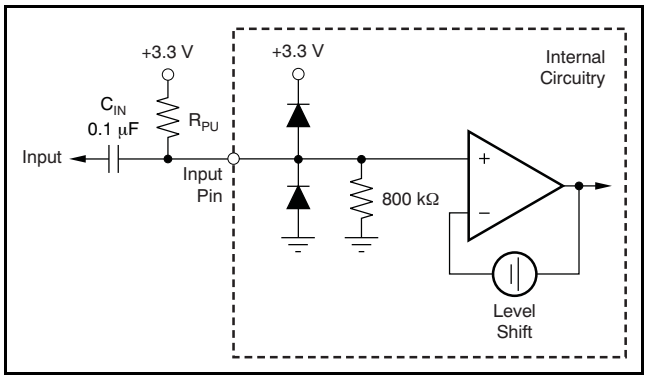


Figure 51. AC-Bias Input Mode Circuit Configuration

The dc voltage that appears at the input pin is equal to Equation 1:

$$V_{DC} = V_S \left(\frac{800\ k\Omega}{800\ k\Omega + R_{PU}} \right) \quad (1)$$

The THS7375 allowable input range is approximately (V_{S+} – 1.5 V), which allows for a very wide input voltage range but is limited by the allowable output voltage range and the internal gain. As such, the input dc bias point is very flexible; the output dc bias point is the primary factor. For example, if the output dc bias point is desired to be 1.6 V on a 3.3-V supply, then the input dc bias point is recommended to be (1.6 V – 320 mV)/5.6 = 0.228 V. Thus, the pull-up resistor calculates to approximately 10.8 MΩ. If the output dc-bias point is desired to be 1.6 V with a 5-V power supply, then the value calculates to be approximately 16.7 MΩ.

Keep in mind that the internal 800-kΩ resistor has a ±20% variance. As such, the calculations should take this variance into account. For the 0.228-V input bias voltage example above using an ideal 10.8-MΩ resistor, the input dc bias voltage is about 0.228 V (±0.045 V) which translates to an output bias voltage of about 1.6 V (±0.25 V).

If desired, an external resistor can be placed in parallel with the internal 800-kΩ resistor. This external resistor may be required if the pull-up resistor calculates to a value higher than desired. There are no consequences of this configuration other than decreasing the effective input impedance of the THS7375 system.

The value of the output bias voltage is very flexible and is left to each individual design. It is important to ensure that the signal does not clip or saturate the video signal. Thus, it is recommended to ensure the output bias voltage is between 0.9 V and (V_{S+} – 1 V). For 100% color saturated CVBS or signals with Macrovision, the CVBS signal can reach up to 1.23 V_{PP} at the input, or 2.46 V_{PP} at the output of the THS7375. In contrast, other signals are typically 1 V_{PP} or 0.7 V_{PP} at the input which translate to an output voltage of 2 V_{PP} or 1.4 V_{PP}, respectively. The output bias voltage must account for a worst-case situation depending on the signals involved.

One other issue that must be taken into account is the dc-bias point as a function of the power supply. As such, there is an impact on the system PSRR. To help reduce this impact, the input capacitor combines with the pull-up resistance to function as a low-pass filter. Additionally, the time to charge the capacitor to the final dc bias point is also a function of the pull-up resistor and the input capacitor. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. In general, it is good to have this high-pass filter at approximately 3-Hz to minimize any potential droop on a P'_B, P'_R, or non-sync B' or R' signal. A 0.1-µF input capacitor with a 10.8-MΩ pull-up resistor equates to a 2.1-Hz high-pass corner frequency.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', V', and non-sync R'G'B' signals. This method can also be used with signals with sync, if desired. The benefit of using the STC function is that it maintains a constant back-porch voltage as opposed to a back-porch voltage that

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fluctuates depending on the video content. Because the corner frequency of the input is a very low 2.5 Hz, the corner frequency of the input is also a very low 2.5 Hz, which is respectable performance relative to a STC configuration.

OUTPUT MODE OF OPERATION: DC-COUPLED

The THS7375 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac coupling capacitors, as shown in Figure 52. This approach offers the best line tilt and field tilt (or droop) performance because no ac coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt because of the input ac coupling is seen on the output regardless of the output coupling. The 80-mA output current drive capability of the THS7375 was designed to drive two video lines simultaneously (essentially, a 75-Ω load) while maintaining as wide an output dynamic range as possible.

One concern of dc coupling, however, arises if the line is terminated to ground. If the ac-bias input configuration is used, the output of the THS7375 has a dc bias on the output. With two lines terminated to ground, this configuration creates a dc current path that results in a slightly decreased high output voltage swing and an increase in power dissipation of the THS7375. While the THS7375 was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level; otherwise, long-term reliability could suffer. Although this configuration only adds less than 10 mW of power dissipation per channel, the overall low-power dissipation of the THS7375 design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures.

Note that the THS7375 can drive the line with dc coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output—typically 75-Ω. This termination helps isolate capacitive loading effects from the THS7375 output. Failure to isolate capacitive loads may result in instabilities with the output buffer, potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the THS7375 output pins should be kept below 22-pF. The best way to ensure this limit is maintained is to place the 75-Ω series output resistor as close as possible to the output pin. If an output capacitor is used, as discussed in the next section, then it should be placed after the resistor.

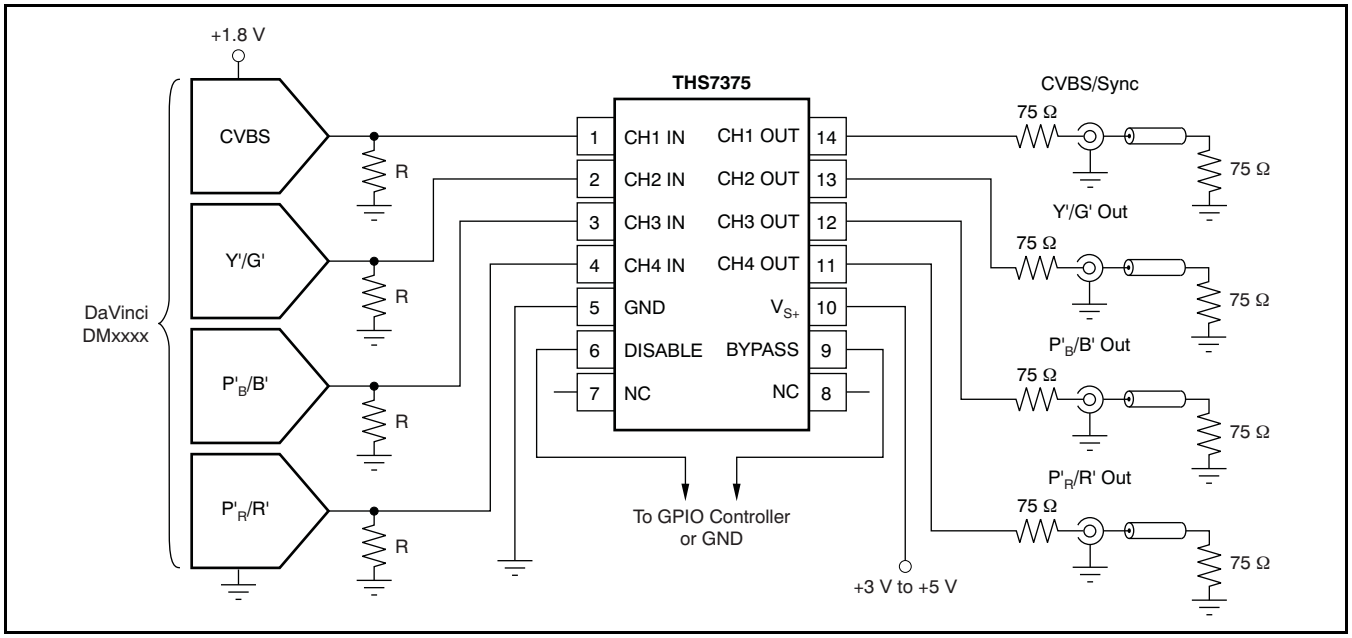


Figure 52. Typical SDTV System with DC-Coupled Line Driving

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OUTPUT MODE OF OPERATION: AC-COUPLED

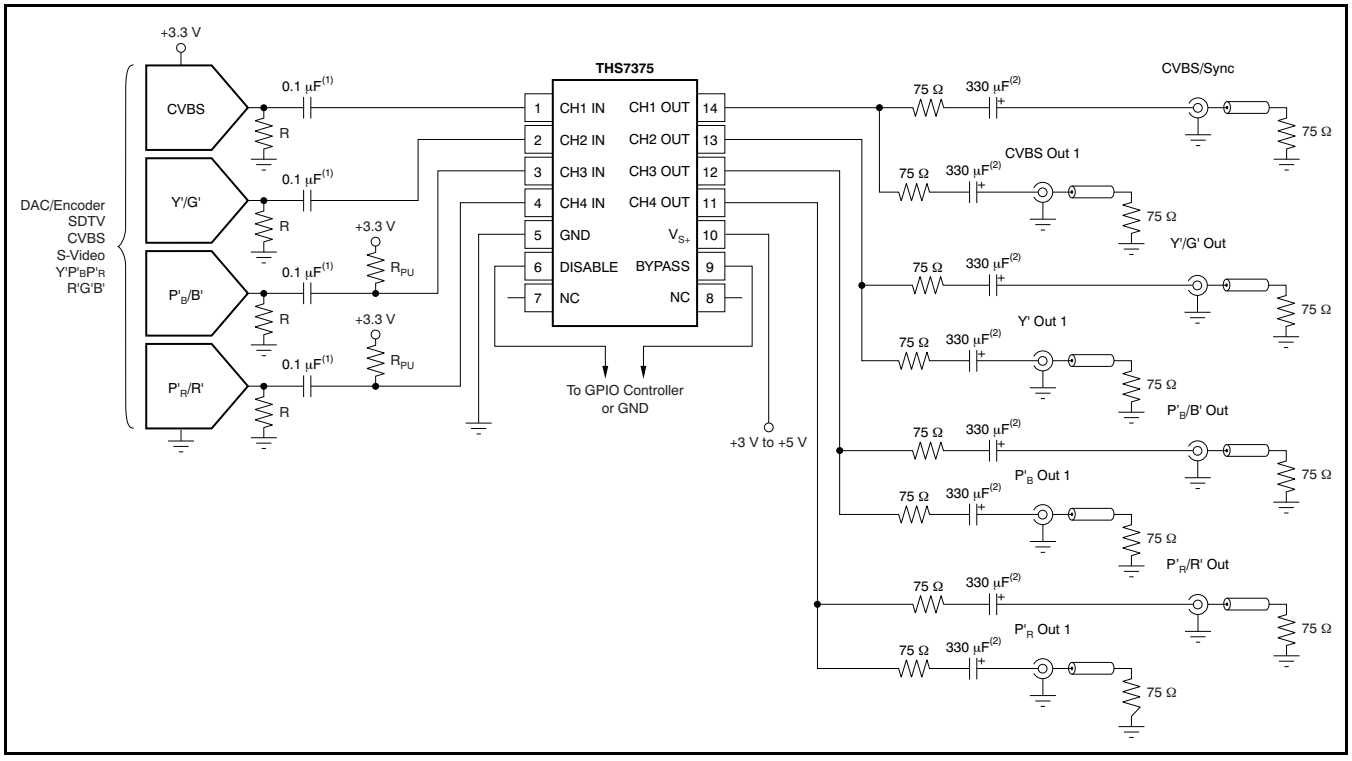
A very common method of coupling the video signal to the line is the use of a large capacitor. This capacitor is typically between 220 μF and 1000 μF, although 470 μF is very common. The value of this capacitor must be large enough to minimize the line tilt (droop) and/or field tilt associated with ac coupling as described previously in this document. AC coupling is done for several reasons, but most often to ensure full interoperability with the receiving video system. AC coupling also ensures adherence to video standard specifications. It ensures that regardless of the reference dc voltage used on the transmit side, the receive side re-establishes the dc reference voltage to its own requirements.

As with the dc output mode of operation discussed previously, each line should have a 75-Ω source termination resistor in series with the ac coupling capacitor. If two lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components, as shown in Figure 53.

This configuration helps ensure line-to-line dc isolation and avoids the potential problems discussed above. Using a single 1000-μF capacitor for two lines can be done, but there is a chance for interference to be created between the two receivers.

Lastly, because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-μF to 0.01-μF capacitor in parallel with the large 220-μF to 1000-μF capacitor. These large-value capacitors are generally aluminum electrolytic. It is well-known that these capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large because of the associated inductances involved with the leads and construction. The small 0.1-μF to 0.01-μF capacitors help pass these high-frequency (> 1-MHz) signals with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system are not required to go as low (or as high of a frequency) as the luma channels. Thus, the capacitor values of the chroma line(s) can be smaller, such as 0.1 μF.



(1) An ac-coupled input is shown in this example. DC coupling is also allowed as long as the DAC output voltage is within the allowable linear input and output voltage range of the THS7375. To dc-couple, remove the 0.1-μF input capacitors and R_{PU}.

(2) An ac-coupled output is shown in this example. DC coupling is also allowed by simply removing these capacitors.

Figure 53. Typical SDTV AC-Input System Driving Two AC-Coupled Video Lines

LOW-PASS FILTER

Each channel of the THS7375 incorporates a sixth-order low-pass filter. These video reconstruction filters minimize the passing of DAC images to the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems as a result of ADC aliasing. Another benefit of the filter is to smooth out aberrations in the signal that some DACs can have if the internal device filtering is not very good. This technique helps with picture quality and helps ensure that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat, with a relatively steep initial attenuation at the corner frequency. The problem with this characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of the very large group delay variations near the corner frequency that results in significant overshoot and ringing. While these elliptic or chebyshev filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. When considering these filter types, keep in mind that video can go from a white pixel to a black pixel over and over again, and ringing can easily occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too slow for acceptable image rejection. Thus, the Butterworth filter is a respectable compromise for both attenuation and group delay.

The THS7375 filters have a nominal corner (–3 dB) frequency at 9.5 MHz and a –1-dB passband typically at 8 MHz. This 9.5-MHz filter is ideal for standard definition (SD) NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for s-video signals (Y'C'), 480i/576i $Y'P'_BP'_R$, Y'U'V', broadcast G'B'R' (R'G'B') signals, and computer video signals. The 9.5-MHz, –3-dB corner frequency was designed to achieve 54 dB of attenuation at 27 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as the result of aliasing effects of an ADC found in a receiver.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 27 MHz for traditional SD DACs); they continue around the sampling frequencies of 2X f_S, 3X f_S, 4X f_S, etc. (54 MHz, 81 MHz, 108 MHz). Because of these multiple images that an ADC can fold down into the baseband signal, the low-pass filter must also eliminate these higher order images. The THS7375 filters are Butterworth filters and as such, do not *bounce* at higher frequencies and maintain good attenuation performance.

The 9.5-MHz filter frequency was chosen to account for process variations in the THS7375. To ensure that the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering is adequate to meet the system demands. Thus, the filter frequencies were not arbitrarily selected and are a good compromise that should meet the demands of most systems.

Benefits Over Passive Filtering

Two key benefits of using an integrated filter system such as the THS7375 over a passive system are PCB area and filter variations. The small TSSOP-14 package for four video channels is much smaller over a passive RLC network, especially a six-pole passive network. Additionally, consider that inductors have at best ±10% tolerances (normally ±15% to ±20% are common) and capacitors typically have ±10% tolerances. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay have wide variations. This approach can lead to potential performance and quality issues in mass-production environments. The THS7375 solves most of these problems with the corner frequency being essentially the only variable.

Another concern about passive filters is the use of inductors. Inductors are magnetic components and are therefore susceptible to electromagnetic coupling/interference (EMC/EMI). Some common coupling can occur because of other nearby video channels that use inductors for filtering, or it can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation that can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature change. To minimize temperature effects, the THS7375 uses low temperature coefficient resistors and high-quality/low-temperature coefficient capacitors found in the BiCom3X process.

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These filters have been specified by design to account for process and temperature variations to maintain proper filter characteristics. This architecture maintains a low channel-to-channel time delay, which is required for proper video signal performance.

Another benefit of the THS7375 over a passive RLC filter is the input and output impedance. The input impedance presented to the DAC may vary significantly with a passive network and may cause voltage variations over frequency. The THS7375 input impedance is 800 kΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impacts the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7375.

On the output side of the filter, a passive filter also has a large impedance variation over frequency. The EIA770 specifications requires the return loss be at least 25 dB over the video frequency range of usage. For a video system, this condition implies the source impedance—which includes the source and the series resistor and the filter—must be better than 75 +9/–8 Ω. The THS7375 is an operational amplifier that approximates an ideal voltage source. A voltage source is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss, this output resistance must maintain a 75-Ω impedance. A passive filter impedance variation cannot ensure this consistent performance while the THS7375 has about 1.4-Ω of output impedance at 5-MHz. Thus, the system is much better matched with a THS7375 as compared to a passive filter.

One final advantage of the THS7375 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load—the receiver 75-Ω resistor and the 75-Ω source impedance matching resistor next to the DAC to maintain the source impedance requirement. This approach forces the DAC to drive at least 1.25 V_P (100% saturation CVBS)/37.5 Ω = 33.3 mA. A DAC is a current steering element and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when four channels are being driven. With a high input impedance and the capability to drive up to two video lines, utilizing the THS7375 can reduce the DAC power dissipation significantly. This reduction occurs because the resistance the DAC is driving can be substantially increased. It is common to set this driving resistance in a DAC by a current-setting resistor on the device. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving a substantial amount of power. For example, a 3.3-V four-channel DAC dissipates 440 mW for the steering current capability alone (four channels × 33.3 mA × 3.3 V) if it must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 55 mW (four channels × 4.16 mA × 3.3 V).

Reducing System Gain

The THS7375 has a built-in gain of 5.6 V/V, or 14.95 dB. While this gain matches the needs of many of Texas Instruments' video processors, including the DaVinci family of products, the gain can be easily reduced to meet other needs. The easiest and most effective method of adjusting the gain lower is to simply use a resistor divider on the input to the THS7375, as shown in Figure 54. This solution uses resistors R1 and R2 to accomplish two requirements:

1. Terminate the video DAC with the proper resistance, and
2. Form a resistor divider in before the THS7375 input.

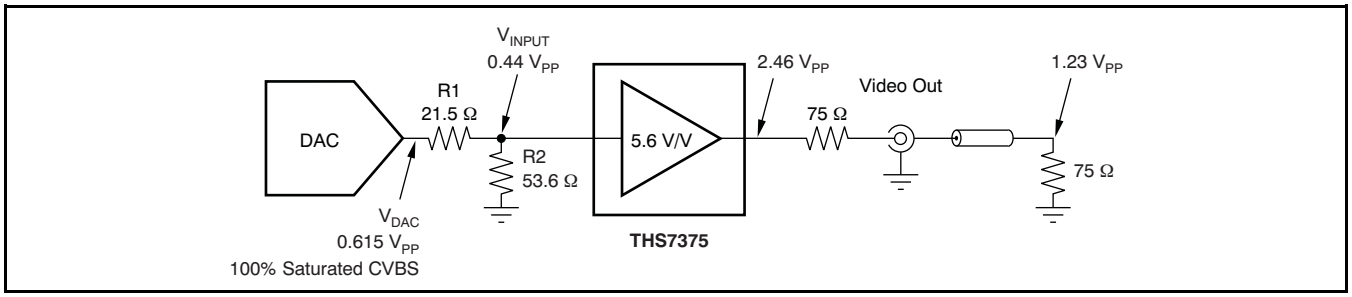


Figure 54. Configuring the THS7375 with 4-V/V (12dB) Gain

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The DAC must have a defined termination resistance to properly set the output voltage. R1 and R2 sum together to accomplish this requirement such that R1 + R2 = DAC termination resistance.

The voltage divider, formed by R1 and R2, also creates a voltage divider that reduces the signal voltage appearing at the THS7375 input terminal. The voltage appearing at the THS7375 input is equal to V_{DAC} R2/(R1 + R2).

Solving for both of these requirements and simplifying results leads to the general equations:

- DAC termination = R_{TERM} = R1 + R2
- $V_{INPUT} = V_{DAC}$ R2/(R1 + R2)
- Ratio = V_{INPUT}/V_{DAC}
- R2 = R_{TERM} × Ratio
- R1 = R_{TERM} – R2

As an example, the DAC outputs 0.615 V_{PP} and requires an amplifier gain of 4 V/V (12dB) to achieve 100% saturated color CVBS signal requirements. Additionally, the DAC requires a termination resistance of 75 Ω. Plugging these requirements into the above equations result in standard resistor values of R2 = 53.6 Ω and R1 = 21.5 Ω.

EVALUATION MODULE

To evaluate the THS7375, a product evaluation module (EVM) is available. The EVM allows for testing the THS7375 in many different cnfiguration. Inputs and outputs include BNC connectors commonly found in video systems along with 75-Ω input termination resistors, 75-Ω series source termination resistors, and 75-Ω characteristic impedance traces. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user. This EVM is designed to be used with a single-supply from 2.85 V up to 5 V.

The EVM default input configuration sets all channels for dc input coupling. The input signal must be within 0 V to about 0.52 V for proper operation with 3.3 V supply and up to 0.8 V for 5V supply. Failure to be within this range saturates and/or clips the output signal. If the input range is beyond this range, or if the signal voltage is unknown, or coming from a current sink DAC, then ac input configuration is desireable. This option is easily accomplished with the EVM by simply replacing Z1, Z2, Z3, and Z4 0-Ω resistors with 0.1-μF capacitors.

For ac-coupled input and sync-tip clamp (STC) functionality commonly used for CVBS, s-video Y', component Y' signals, and R'G'B' signals with embedded sync, then no other changes are needed. However, if a bias voltage is needed after the input capacitor which is commonly needed for s-video C', component P'_B and P'_R, and non-sync embedded R'G'B' signals, then a pull-up resistor should be added to the signal on the EVM. This adjustment is easily done by simply adding a resistor to any of the following resistor pads; RX1, RX3, RX5, or RX7. A common value to use is 10.8 MΩ. Note that even signals with embedded sync can also use bias mode if desired.

The EVM default output configuration sets all channels for ac output coupling. The 470-μF and 0.1-μF capacitors work well for most ac-coupled systems. However, if dc-coupled output is desired, then replacing the 0.1-μF capacitors—C12, C14, C16, and C17—with 0-Ω resistors works well. Removing the 470-μF capacitors is optional, but removing them from the EVM eliminates a few picofarads of stray capacitance on each signal path which may be desirable.

The THS7375EVM incorporates an easy method to configure the bypass mode and the disable mode. The use of JP1 controls the disable feature while JP4 controls the bypass feature. While there is a space on the EVM board for JP2 and JP3, these are not utilized for the THS7375. Connection of JP1 to GND applies 0 V to the disable pin and the THS7375 operates normally. Moving JP1 to $+V_S$ causes the THS7375 to be in disable mode. Connection of JP4 to GND places the THS7375 in filter mode while moving JP4 to $+V_S$ places the THS7375 in bypass mode.

Figure 55 shows the THS7375EVM schematic. Figure 56 and Figure 57 illustrate the two layers of the EVM PCB, incorporating standard high-speed layout practices. Table 2 lists the bill of materials as supplied from Texas Instruments.

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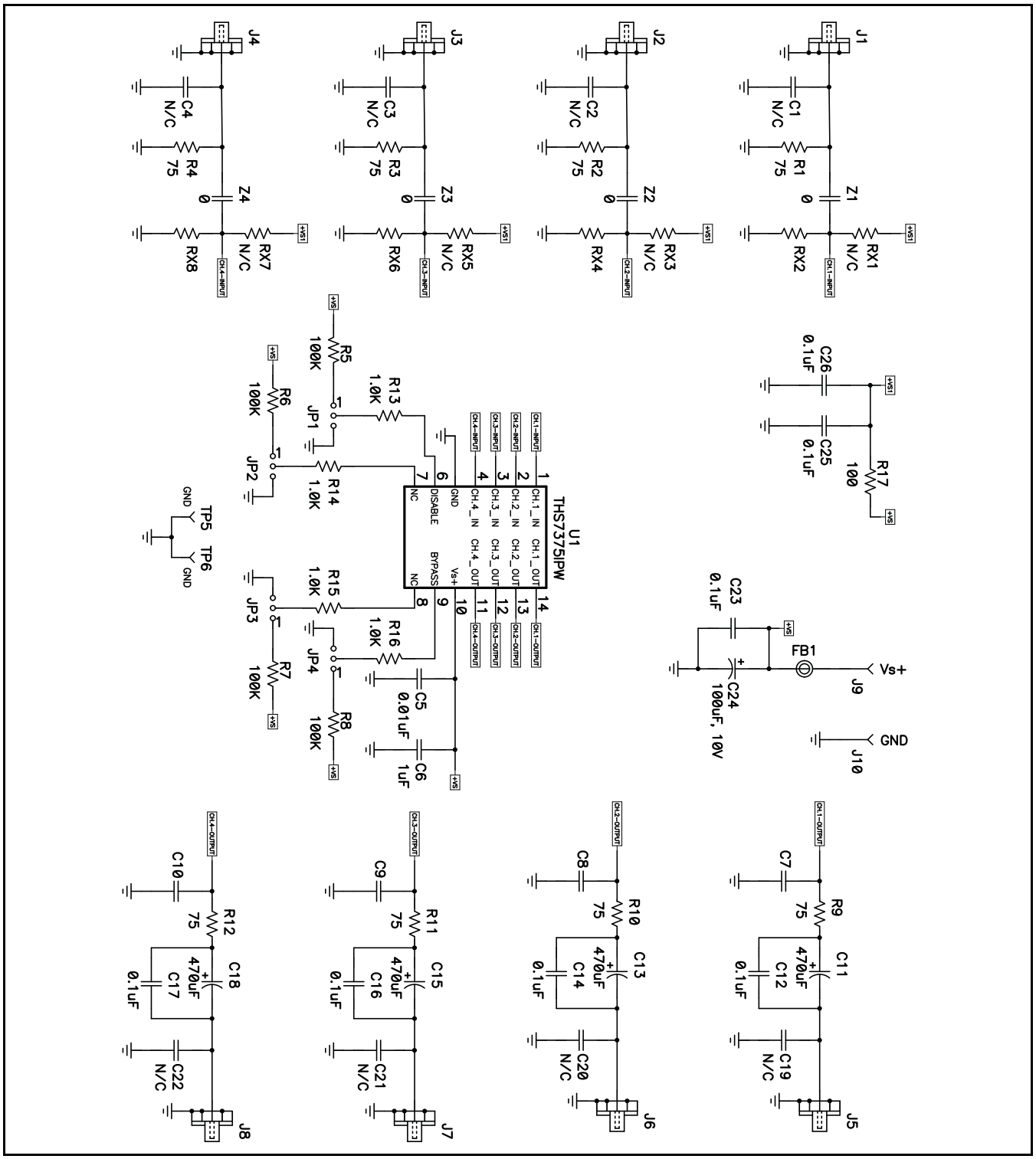


Figure 55. THS7375 EVM Schematic

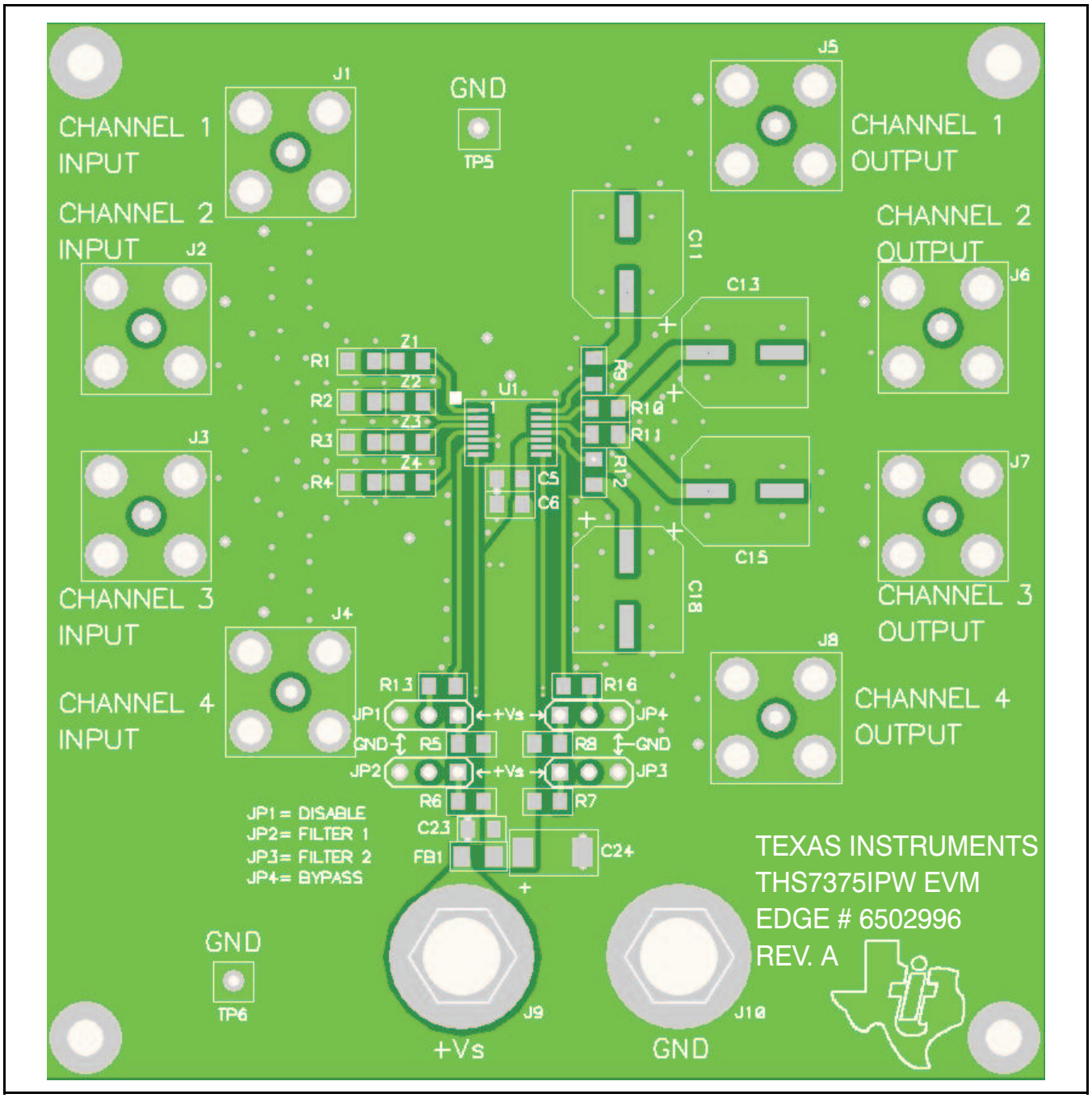


Figure 56. THS7375 EVM PCB Top Layer

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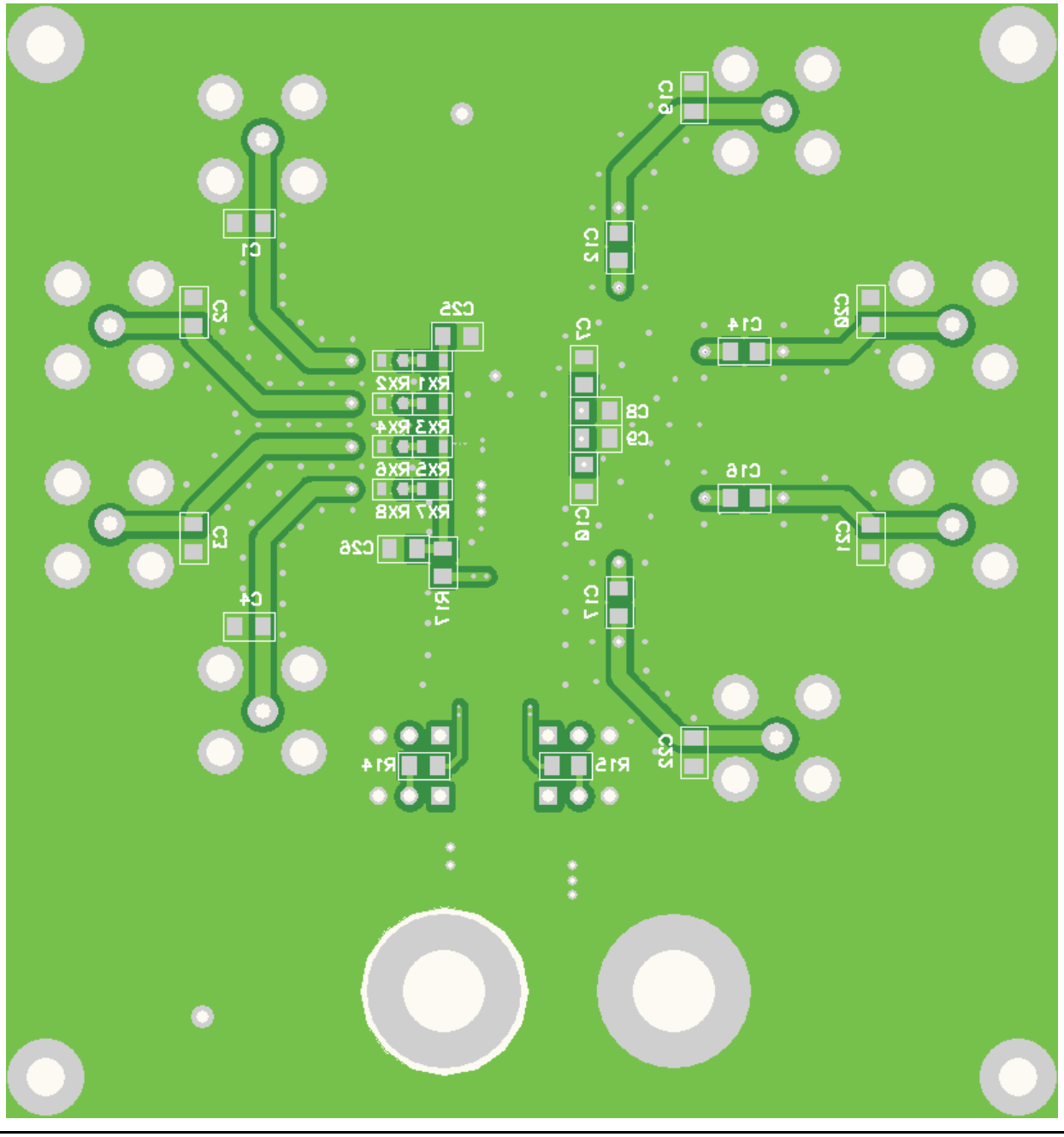


Figure 57. THS7375 EVM PCB Bottom Layer

THS7375EVM Bill of Materials

Table 2. THS7375 EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1	1	Bead, Ferrite, 2.5 A, 330 Ω	0805	(TDK) MPZ2012S331A	(Digi-Key) 445-1569-1-ND
2	C24	1	Capacitor, 100 μF, Tantalum, 10 V, 10%, Low-ESR	C	(AVX) TPSC107K010R0100	(Digi-Key) 478-1765-1-ND
3	C1–C4, C7–C10, C19, C20–C22	12	Open	0805		
4	C5	1	Capacitor, 0.01 μF, Ceramic, 100 V, X7R	0805	(AVX) 08051C103KAT2A	(Digi-Key) 478-1358-1-ND
5	C12, C14, C16, C17, C23, C25, C26	7	Capacitor, 0.1 μF, Ceramic, 50 V, X7R	0805	(AVX) 08055C104KAT2A	(Digi-Key) 478-1395-1-ND
6	C6	1	Capacitor, 1 μF, Ceramic, 16 V, X7R	0805	(TDK) C2012X7R1C105K	(Digi-Key) 445-1358-1-ND
7	C11, C13, C15, C18	4	Capacitor, Aluminum, 470 μF, 10 V, 20%	F	(Cornell) AFK477M10F24B-F	(Newark) 66K0965
8	RX1–RX8	8	Open	0603		
9	R6, R7, R14, R15	4	Open	0805		
10	Z1–Z4	4	Resistor, 0 Ω	0805	(ROHM) MCR10EZHJ000	(Digi-Key) RHM0.0ACT-ND
11	R1–R4, R9–R12	8	Resistor, 75 Ω, 1/8 W, 1%	0805	(ROHM) MCR10EZHF75.0	(Digi-Key) RHM75.0CCT-ND
12	R17	1	Resistor, 100 Ω, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1000	(Digi-Key) RHM100CCT-ND
13	R13, R16	2	Resistor, 1 kΩ, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1001	(Digi-Key) RHM1.00KCCT-ND
14	R5, R8	2	Resistor, 100 kΩ, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1003	(Digi-Key) RHM100KCCT-ND
15	J9, J10	2	Jack, Banana Receptance, 0.25" dia. hole		(SPC) 813	(Newark) 39N867
16	J1–J8	8	Connector, BNC, Jack, 75 Ω		(Amphenol) 31-5329-72RFX	(Newark) 93F7554
17	TP5, TP6	2	Test Point, Black		(Keystone) 5001	(Digi-Key) 5001K-ND
18	JP2, JP3	2	Open	3 possible		
19	JP1, JP4	2	Header, 0.1" CTRS, 0.025" sq. pins	3 possible	(Sullins) PBC36SAAN	(Digi-Key) S1011E-36-ND
20	JP1, JP4	2	Shunts		(Sullins) SSC02SYAN	(Digi-Key) S9002-ND
21	U1	1	IC, THS7375	PW	(TI) THS7375IPW	
22		4	Standoff, 4-40 HEX, 0.625" length		(Keystone) 1808	(Digi-Key) 1808K-ND
23		4	Screw, Phillips, 4-40, 0.250"		(BF) PMS 440 0031 PH	(Digi-Key) H343-ND
24		1	Printed Circuit Board		(TI) Edge# 6502996 Rev. A	

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2008) to Revision A	Page
• Added Figure 26	13
• Added Figure 45	17

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.85 V to 5.5 V single supply and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7375IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7375	Samples
THS7375IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7375	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

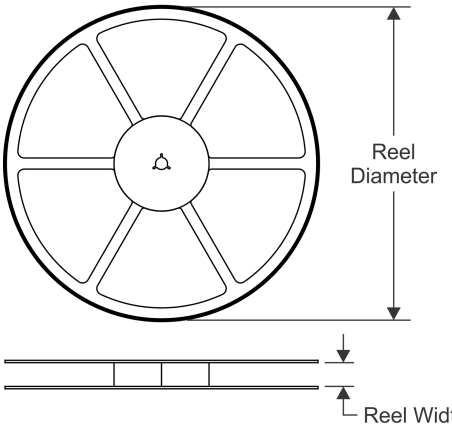
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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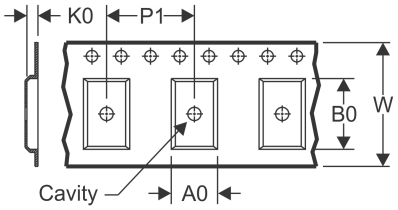
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

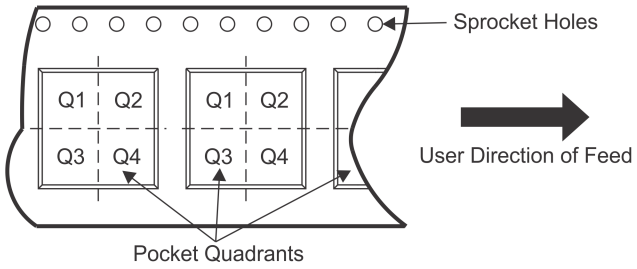


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

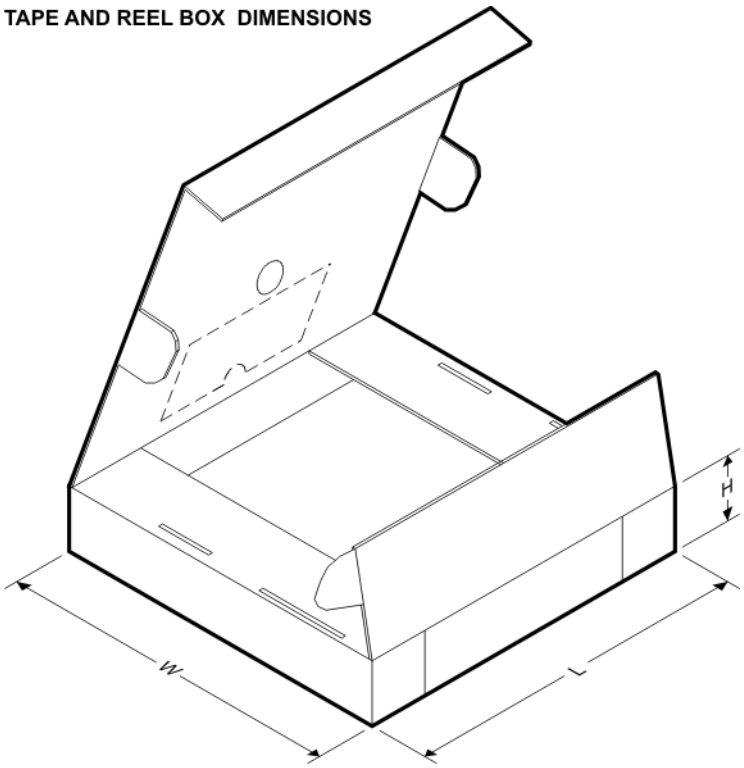
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7375IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

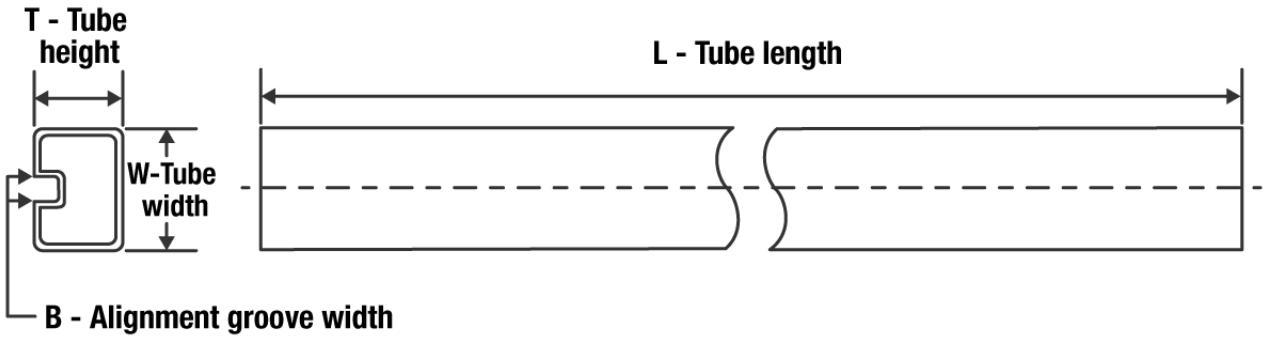
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7375IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0

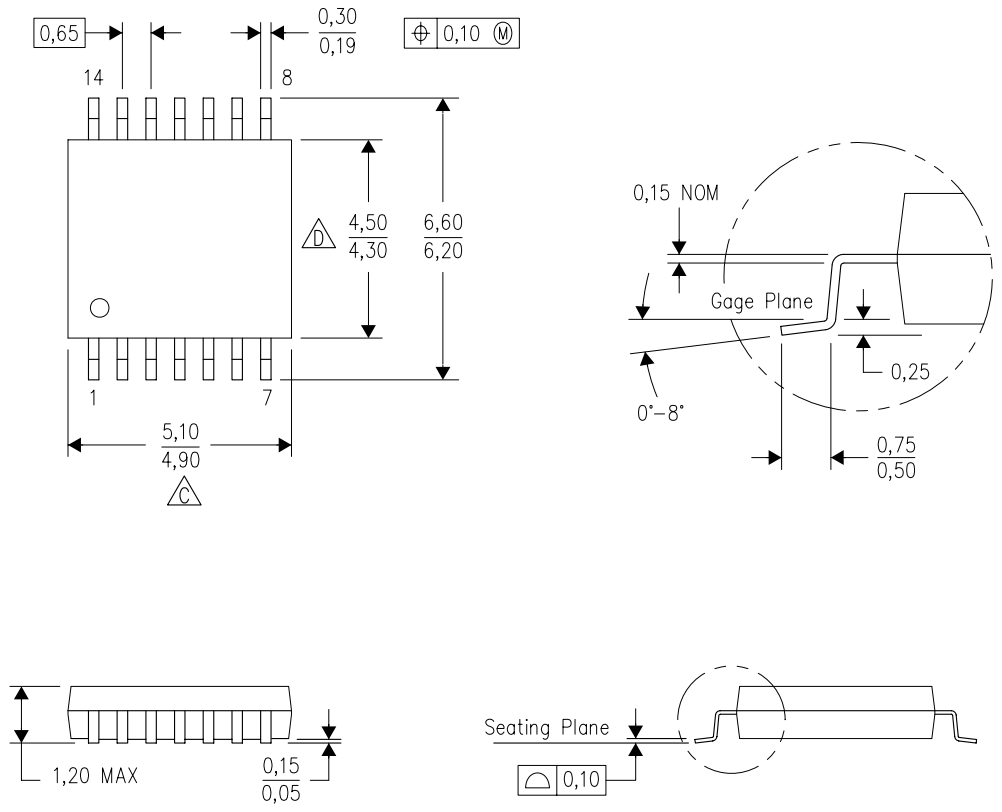
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS7375IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

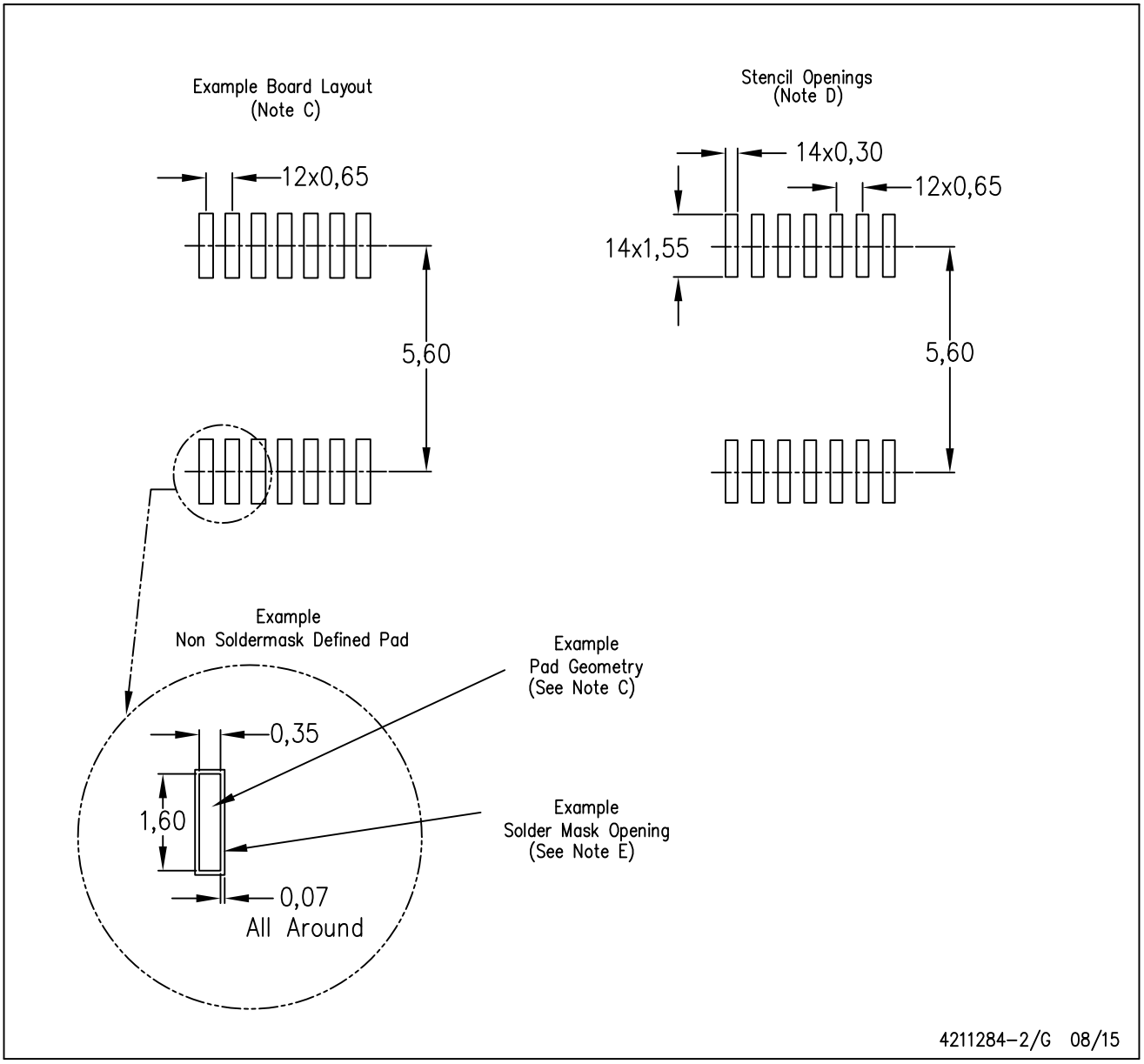
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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