具有浪涌保护功能的 THVD14x9 3.3V 至 5V RS-485 收发器

1 特性

- 满足或超过 TIA/EIA-485A 标准的要求
- 3V 至 5.5V 电源电压
- 总线 I/O 保护
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 接触放电
  - ±30kV IEC 61000-4-2 气隙放电
  - ±4kV IEC 61000-4-4 电气快速瞬变
  - ±2.5kV IEC 61000-4-5 1.2/50µs 浪涌
- 有两种速度等级
  - THVD1419：250kbps
  - THVD1429：20Mbps
- 扩展环境
  温度范围：–40°C 至 125°C
- 扩展运行
  共模范围：±12V
- 用于噪声抑制的接收器迟滞值：30mV
- 低功耗
  - 待机电源电流：< 2µA
  - 运行期间的电流：< 3mA
- 适用于热插拔功能的无干扰加电/断电
- 开路、短路和空闲总线失效防护
- 1/8 单位负载（多达 256 个总线节点）
- 采用可实现快插兼容性的行业标准 8 引脚 SOIC 封装

2 应用

- 无线基础设施
- 楼宇自动化
- HVAC 系统
- 工厂自动化和控制
- 电网基础设施
- 智能仪表
- 过程分析
- 视频监控

3 说明

THVD1419 和 THVD1429 是半双工 RS-485 收发器，集成了浪涌保护功能。电涌保护是通过在标准 8 引脚 SOIC (D) 封装中集成瞬态电压抑制器 (TVS) 二极管实现的。此功能大大提高了可靠性，可以更好地抵抗耦合到数据电缆的噪声瞬变，无需外部保护元件。

每个器件由 3.3V 或 5V 单电源供电。该系列中的器件具有很宽的共模电压范围，因此非常适合长电缆上的应用 长线缆。

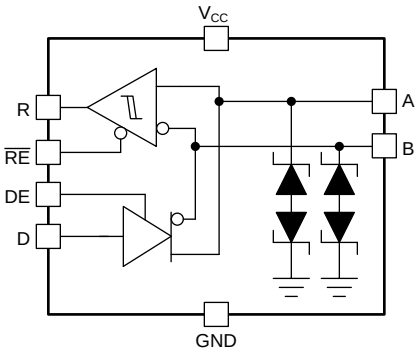
THVD1419 和 THVD1429 器件采用行业标准 SOIC 封装，无需变更 PCB 即可轻松插入。这些器件在自然通风环境下的额定温度范围为 –40°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
THVD1419 THVD1429	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可订购器件，请参阅数据表末尾的可订购产品附录。

THVD1419 和 THVD1429 方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Device Comparison Table** ... 3
6 **Pin Configuration and Functions** ... 4
7 **Specifications** ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 ESD Ratings [IEC] ... 5
7.4 Recommended Operating Conditions ... 6
7.5 Thermal Information ... 6
7.6 Power Dissipation ... 6
7.7 Electrical Characteristics ... 7
7.8 Switching Characteristics ... 8
7.9 Typical Characteristics ... 9
8 **Parameter Measurement Information** ... 11
9 **Detailed Description** ... 13
9.1 Overview ... 13
9.2 Functional Block Diagrams ... 13
9.3 Feature Description ... 13
9.4 Device Functional Modes ... 16
10 **Application and Implementation** ... 17
10.1 **Application Information** ... 17
10.2 Typical Application ... 17
11 **Power Supply Recommendations** ... 20
12 **Layout** ... 21
12.1 Layout Guidelines ... 21
12.2 Layout Example ... 21
13 器件和文档支持 ... 22
13.1 器件支持 ... 22
13.2 第三方产品免责声明 ... 22
13.3 相关链接 ... 22
13.4 接收文档更新通知 ... 22
13.5 社区资源 ... 22
13.6 商标 ... 22
13.7 静电放电警告 ... 22
13.8 术语表 ... 22
14 机械、封装和可订购信息 ... 22

4 修订历史记录

Changes from Revision B (December 2018) to Revision C **Page**

- 将 THVD1419 从：“*产品预览*” 更改为：“*生产数据*“ ... 1
- Changed power dissipation numbers of THVD1419 ... 6
- Changed THVD1419 driver switching characteristics ... 8
- Changed THVD1419 receiver switching characteristics ... 8
- Added 图 7 to 图 9 ... 9

Changes from Revision A (December 2018) to Revision B **Page**

- 将 THVD1429 从：“*预告信息*” 更改为：“*生产数据*” ... 1

Copyright © 2018–2019, Texas Instruments Incorporated

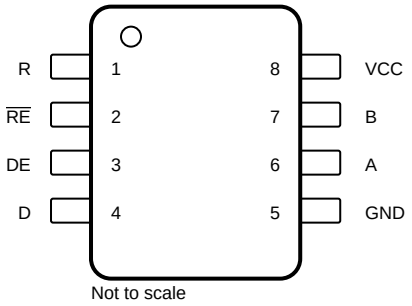
5 Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1419	Half	DE, $\overline{RE}$	up to 250 kbps	256
THVD1429			up to 20 Mbps	

Copyright © 2018–2019, Texas Instruments Incorporated

6 Pin Configuration and Functions

THVD1419, THVD1429 Devices
8-Pin D Package (SOIC)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	5	Ground	Device ground
R	1	Digital output	Receive data output
V_{CC}	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)

Copyright © 2018–2019, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	-0.5	7	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-15	15	V
Input voltage	Range at any logic pin (D, DE, or /RE)	-0.3	5.7	V
Receiver output current	I_O	-24	24	mA
Storage temperature range		-65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, 2010	Bus terminals and GND	±16	kV
			All other pins	±8	kV
		Charged device model (CDM), per JEDEC JESD22-C101E	All pins	±1.5	kV

7.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact Discharge, per IEC 61000-4-2	Bus pins and GND	±8	kV
		Air-Gap Discharge, per IEC 61000-4-2	Bus pins and GND	±30	kV
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus pins and GND	±4	kV
$V_{(surge)}$	Surge	Per IEC 61000-4-5, 1.2/50 μs	Bus pins and GND	±2.5	kV

Copyright © 2018–2019, Texas Instruments Incorporated

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode) (1)	-12		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	-12		12	V
I_O	Output current, driver	-60		60	mA
I_{OR}	Output current, receiver	-8		8	mA
R_L	Differential load resistance	54			Ω
$1/t_{UI}$	Signaling rate: THVD1419			250	kbps
$1/t_{UI}$	Signaling rate: THVD1429			20	Mbps
T_A	Operating ambient temperature	-40		125	℃
T_J	Junction temperature	-40		150	℃

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.5 Thermal Information

THERMAL METRIC(1)		THVD14x9 D (SOIC) 8-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.6 Power Dissipation

PARAMETER	Description	TEST CONDITIONS	VALUE	UNIT
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 ^{0}C, 50% duty cycle square wave at maximum signaling rate, THVD1419	Unterminated: R_L = 300 Ω, C_L = 50 pF	230	mW
		RS-422 load: R_L = 100 Ω, C_L = 50 pF	350	mW
		RS-485 load: R_L = 54 Ω, C_L = 50 pF	470	mW
	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 ^{0}C, 50% duty cycle square wave at maximum signaling rate, THVD1429	Unterminated: R_L = 300 Ω, C_L = 50 pF	350	mW
		RS-422 load: R_L = 100 Ω, C_L = 50 pF	290	mW
		RS-485 load: R_L = 54 Ω, C_L = 50 pF	300	mW

Copyright © 2018–2019, Texas Instruments Incorporated

7.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -12 V ≤ V_{test} ≤ 12 V, see 图 10		1.5	3.5		V
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -12 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, see 图 10		2.1			V
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 100 Ω, see 图 11		2	4		V
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 54 Ω, see 图 11		1.5	3.5		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω, see 图 11		-200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC} / 2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -7 V ≤ V_O ≤ 12 V		-250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		50	125	µA
			V_I = -7 V	-100	-65		µA
			V_I = -12 V	-150	-100		µA
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of ±12 V		See(1)	-100	-20	mV
V_{TH-}	Negative-going input threshold voltage			-200	-130	See(1)	mV
V_{HYS}	Input hysteresis				30		mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz			220		pF
V_{OH}	Output high voltage	I_{OH} = -8 mA		V_{CC} – 0.4	V_{CC} – 0.3		V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}		-1		1	µA
Logic							
I_{IN}	Input current (D, DE, $\overline{RE}$)	4.5 V ≤ V_{CC} ≤ 5.5 V		-6.2		6.2	µA
Device							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{CC}, No load		2.4	3	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2	2.6	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0V, No load		700	960	µA
		Driver and receiver disabled	$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	2	µA
T_{SD}	Thermal shutdown temperature				170		℃

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.

Copyright © 2018–2019, Texas Instruments Incorporated

7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: THVD1419						
t_r, t_f	Differential output rise / fall time	R_L = 54 Ω, C_L = 50 pF, see 图 12		300	500	ns
t_{PHL}, t_{PLH}	Propagation delay			200	450	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				40	ns
t_{PHZ}, t_{PLZ}	Disable time			20	50	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V, see 图 13 and 图 14		60	250	ns
		$\overline{RE}$ = V_{CC}, see 图 13 and 图 14		3	11	µs
Receiver: THVD1419						
t_r, t_f	Output rise / fall time	C_L = 15 pF, see 图 15		14	20	ns
t_{PHL}, t_{PLH}	Propagation delay			30	50	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time			35	45	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$,	Enable time	DE = V_{CC}, see 图 16		80	120	ns
		DE = 0 V, see 图 17		5	14	µs
Driver: THVD1429						
t_r, t_f	Differential output rise / fall time	R_L = 54 Ω, C_L = 50 pF, see 图 12		9	16	ns
t_{PHL}, t_{PLH}	Propagation delay			12	25	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				6	ns
t_{PHZ}, t_{PLZ}	Disable time			18	40	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V, see 图 13 and 图 14		16	40	ns
		$\overline{RE}$ = V_{CC}, see 图 13 and 图 14		2.8	11	µs
Receiver: THVD1429						
t_r, t_f	Output rise / fall time	C_L = 15 pF, see 图 15		2	6	ns
t_{PHL}, t_{PLH}	Propagation delay			12	45	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				6	ns
t_{PHZ}, t_{PLZ}	Disable time			14	28	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$,	Enable time	DE = V_{CC}, see 图 16		75	110	ns
		DE = 0 V, see 图 17		4.8	14	µs

版权 © 2018–2019, Texas Instruments Incorporated

7.9 Typical Characteristics

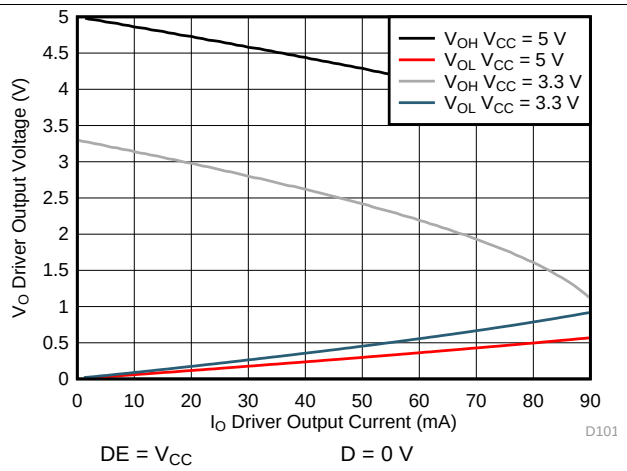


图 1. Driver Output Voltage vs Driver Output Current

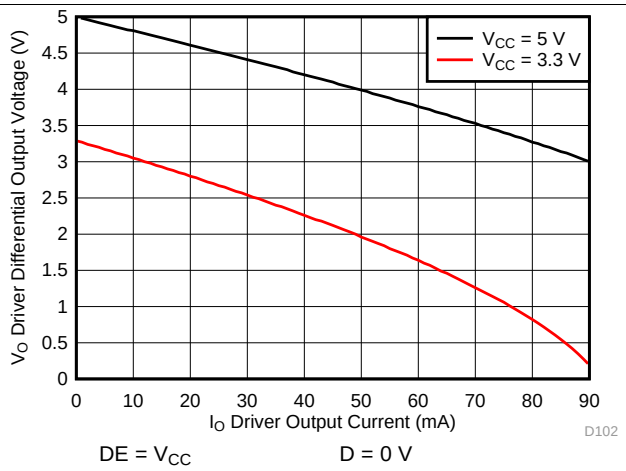


图 2. Driver Differential Output voltage vs Driver Output Current

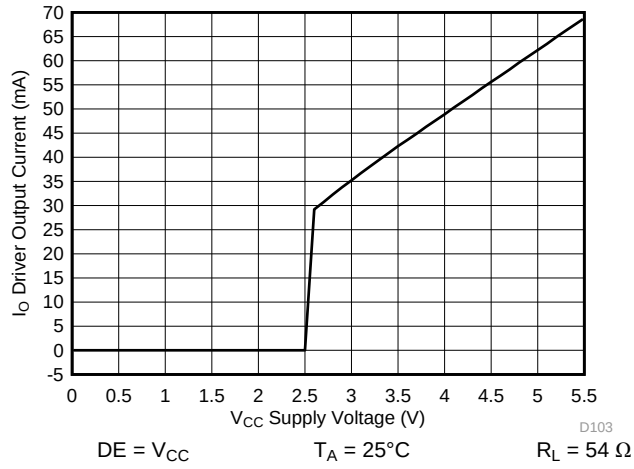


图 3. Driver Output Current vs Supply Voltage

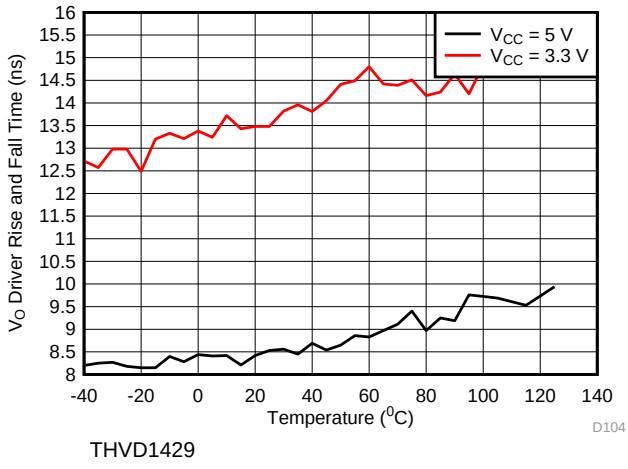


图 4. Driver Rise or Fall Time vs Temperature

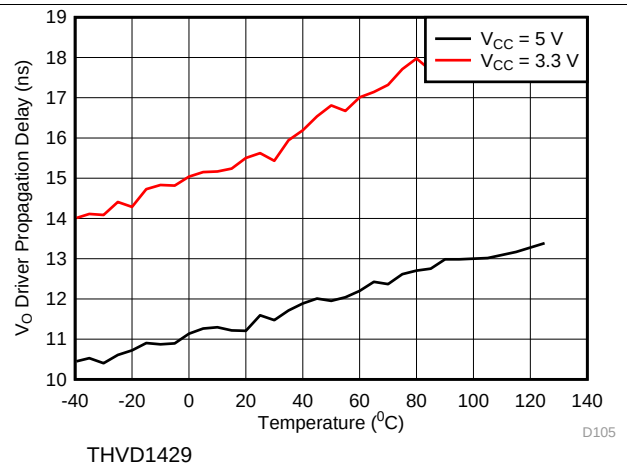


图 5. Driver Propagation Delay vs Temperature

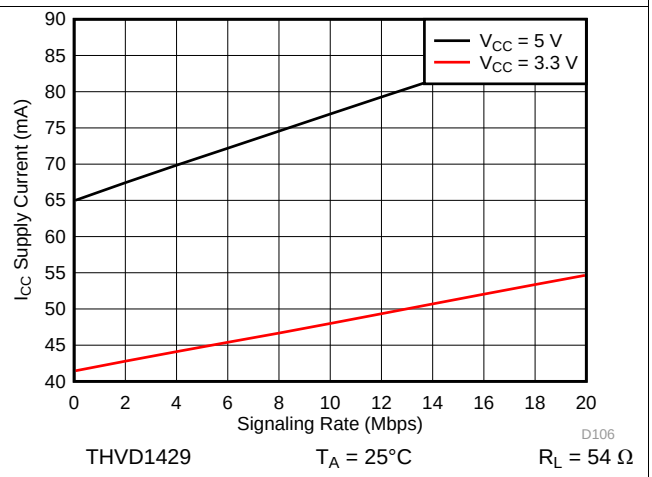


图 6. Supply Current vs Signal Rate

Typical Characteristics (接下页)

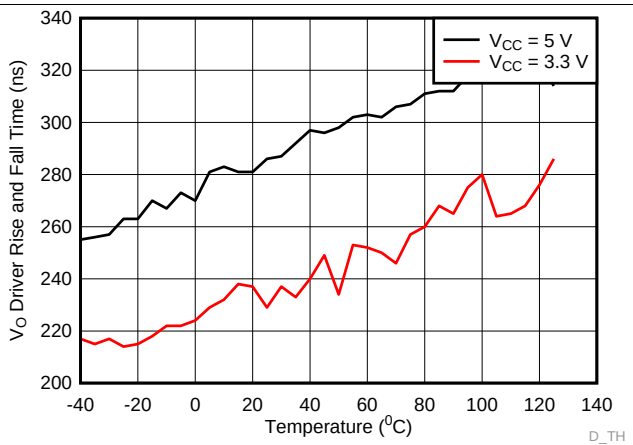


图 7. Driver Rise or Fall Time vs Temperature

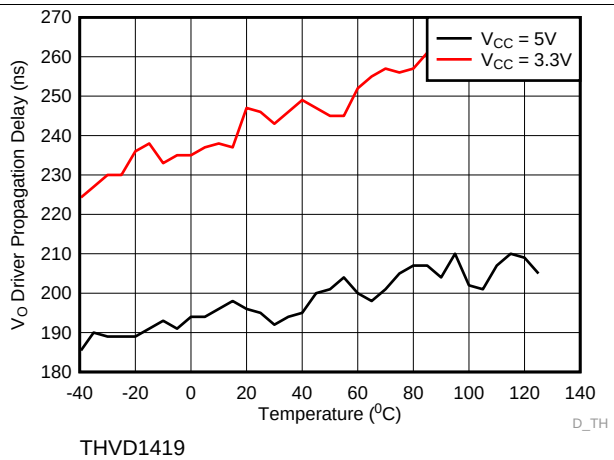


图 8. Driver Propagation Delay vs Temperature

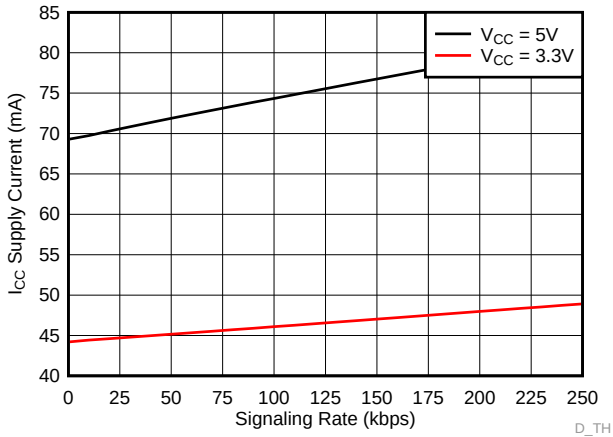


图 9. Supply Current vs Signal Rate

版权 © 2018–2019, Texas Instruments Incorporated

8 Parameter Measurement Information

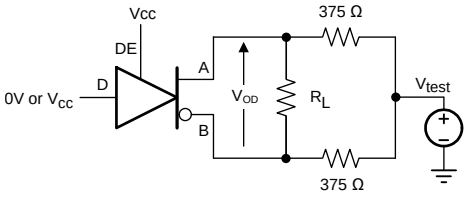


图 10. Measurement of Driver Differential Output Voltage With Common-Mode Load

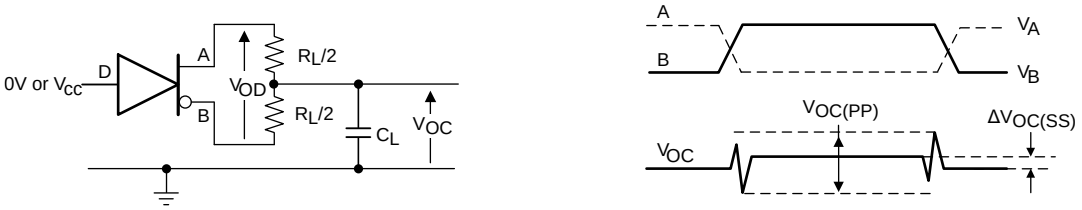


图 11. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

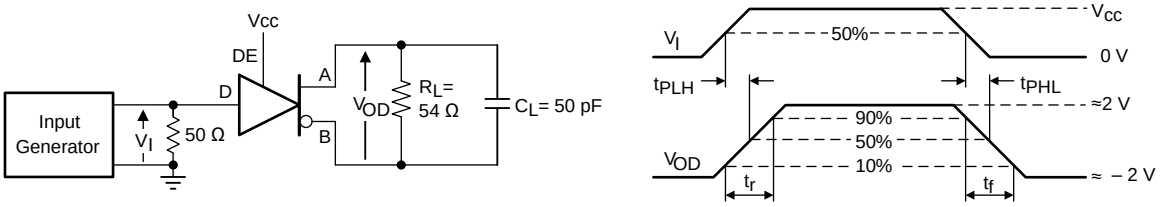


图 12. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

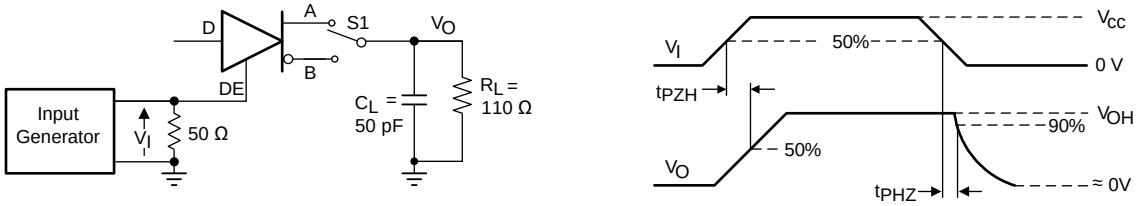


图 13. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

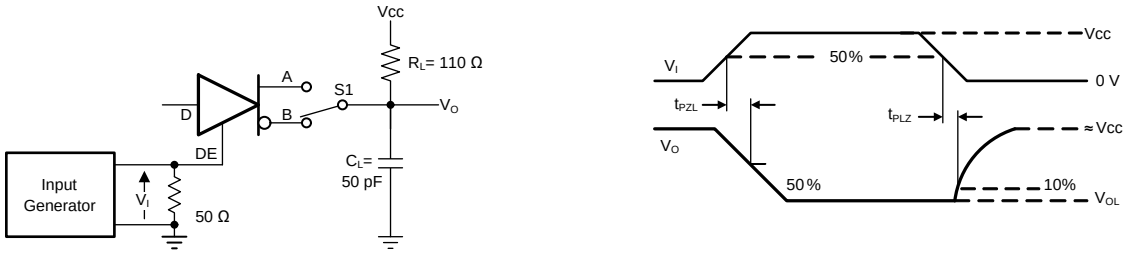


图 14. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (接下页)

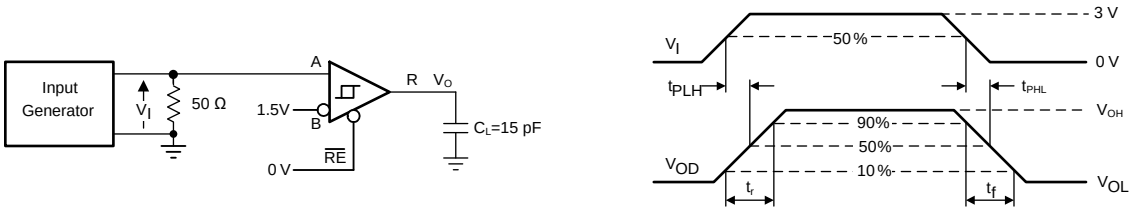


图 15. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

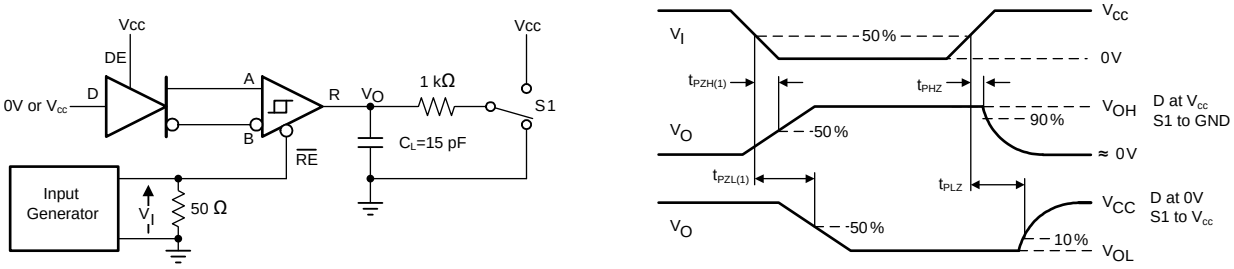


图 16. Measurement of Receiver Enable/Disable Times With Driver Enabled

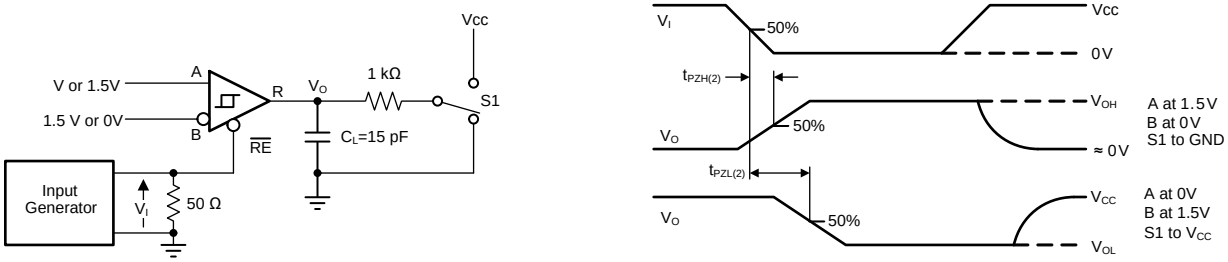


图 17. Measurement of Receiver Enable Times With Driver Disabled

版权 © 2018–2019, Texas Instruments Incorporated

9 Detailed Description

9.1 Overview

THVD1419 and THVD1429 are surge-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 250 kbps and 20 Mbps respectively. Surge protection is achieved by integrating transient voltage suppresser (TVS) diodes in the standard 8-pin SOIC (D) package.

These devices have active-high driver enables and active-low receiver enables. A standby current of less than 2 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagrams

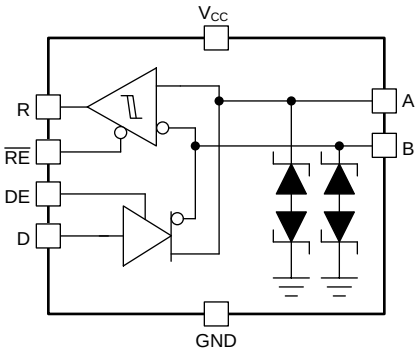


图 18. THVD1419 and THVD1429 Block Diagram

9.3 Feature Description

9.3.1 Electrostatic Discharge (ESD) Protection

The bus pins of the THVD14x9 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

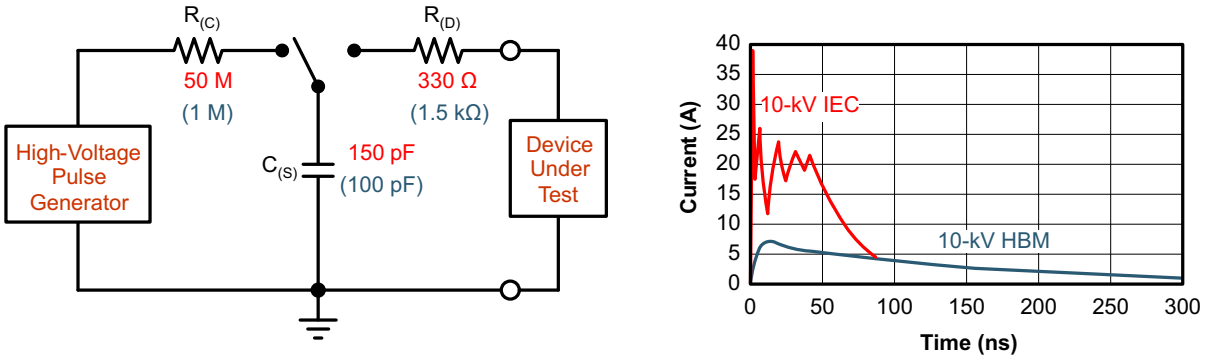


图 19. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables.

Feature Description (接下页)

9.3.2 Electrical Fast Transient (EFT) Protection

Inductive loads such as relays, switch contactors, or heavy-duty motors can create high-frequency bursts during transition. The IEC 61000-4-4 test is intended to simulate the transients created by such switching of inductive loads on AC power lines. 图 20 shows the voltage waveforms in to 50-Ω termination as defined by the IEC standard.

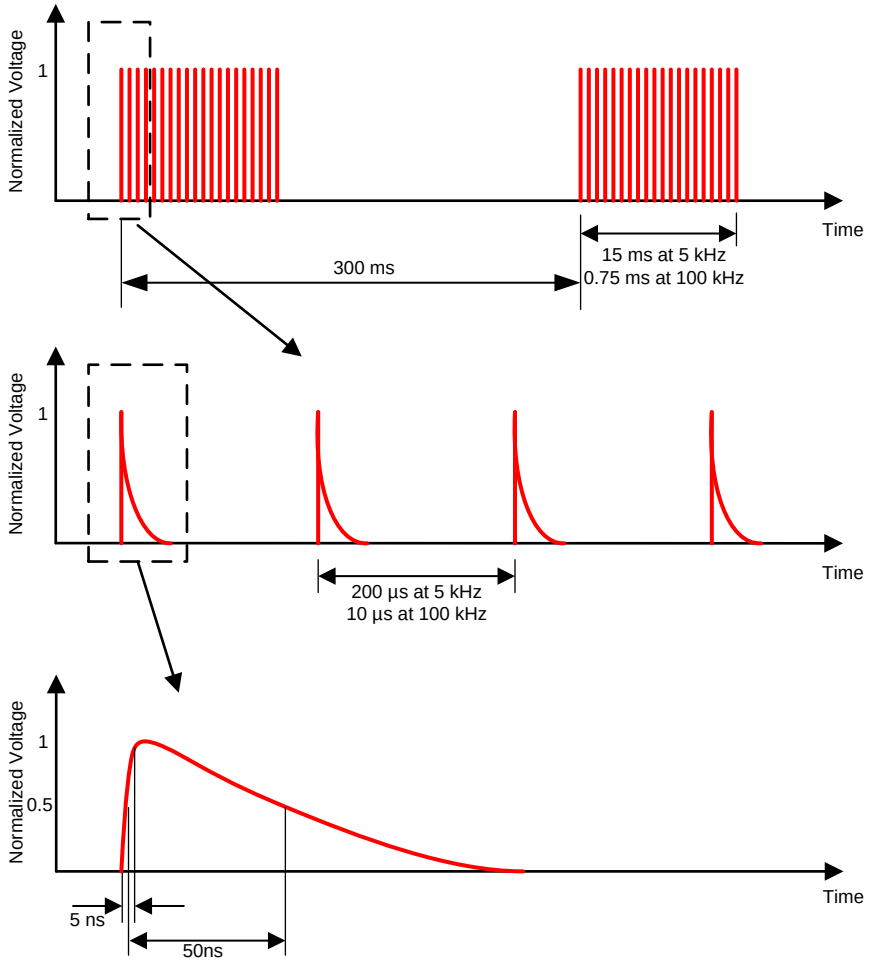


图 20. EFT Voltage Waveforms

Internal ESD protection circuits of the THVD14x9 protect the transceivers against EFT ±4 kV.

9.3.3 Surge Protection

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

图 21 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

版权 © 2018–2019, Texas Instruments Incorporated

Feature Description (接下页)

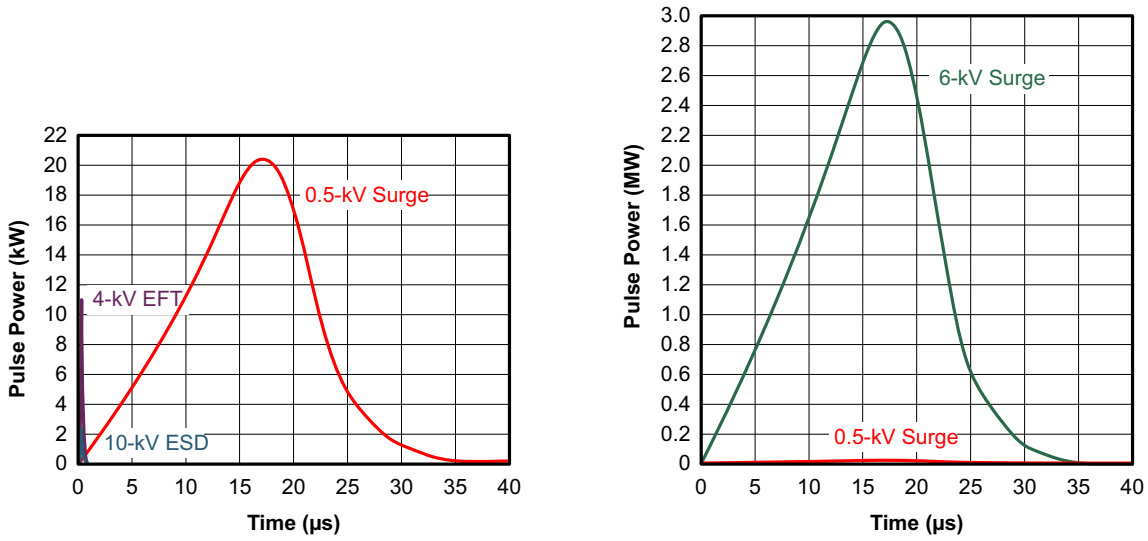


图 21. Power Comparison of ESD, EFT, and Surge Transients

图 22 shows the test setup used to validate THVD14x9 surge performance according to the IEC 61000-4-5 1.2/50-µs surge pulse.

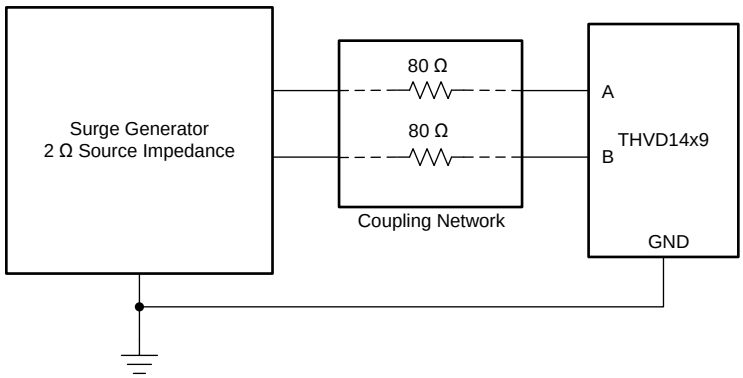


图 22. THVD14x9 Surge Test Setup

THVD14x9 product family is robust to ±2.5-kV surge transients without the need for any external components.

9.3.4 Failsafe Receiver

The differential receivers of the THVD14x9 family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

版权 © 2018–2019, Texas Instruments Incorporated

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

版权 © 2018–2019, Texas Instruments Incorporated

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

THVD14x9 are half-duplex RS-485 transceivers with integrated system-level surge protection. Standard 8-pin SOIC (D) package allows drop-in replacement into existing systems and eliminate system-level protection components.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

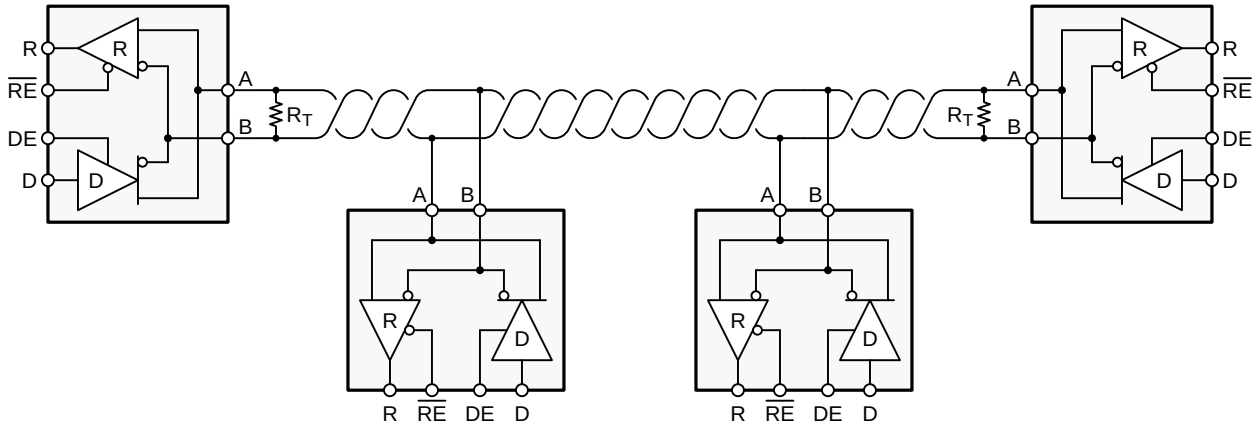


图 23. Typical RS-485 Network With Half-Duplex Transceivers

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

版权 © 2018–2019, Texas Instruments Incorporated

Typical Application (接下页)

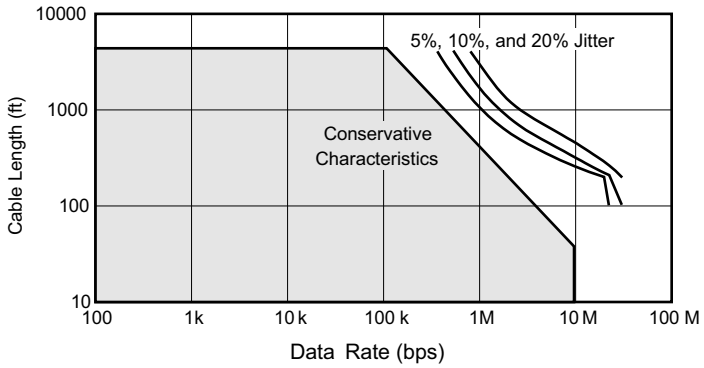


图 24. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 20 Mbps for the THVD1429) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 公式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD14x9 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

版权 © 2018–2019, Texas Instruments Incorporated

Typical Application (接下页)

10.2.2 Detailed Design Procedure

RS-485 transceivers operate in noisy industrial environments typically require surge protection at the bus pins. 图 25 compares 1-kV surge protection implementation with a regular RS-485 transceiver (such as THVD14x0) against with the THVD14x9. The internal TVS protection of the THVD14x9 achieves ±2.5 kV IEC 61000-4-5 surge protection without any additional external components, reducing system level bill of materials.

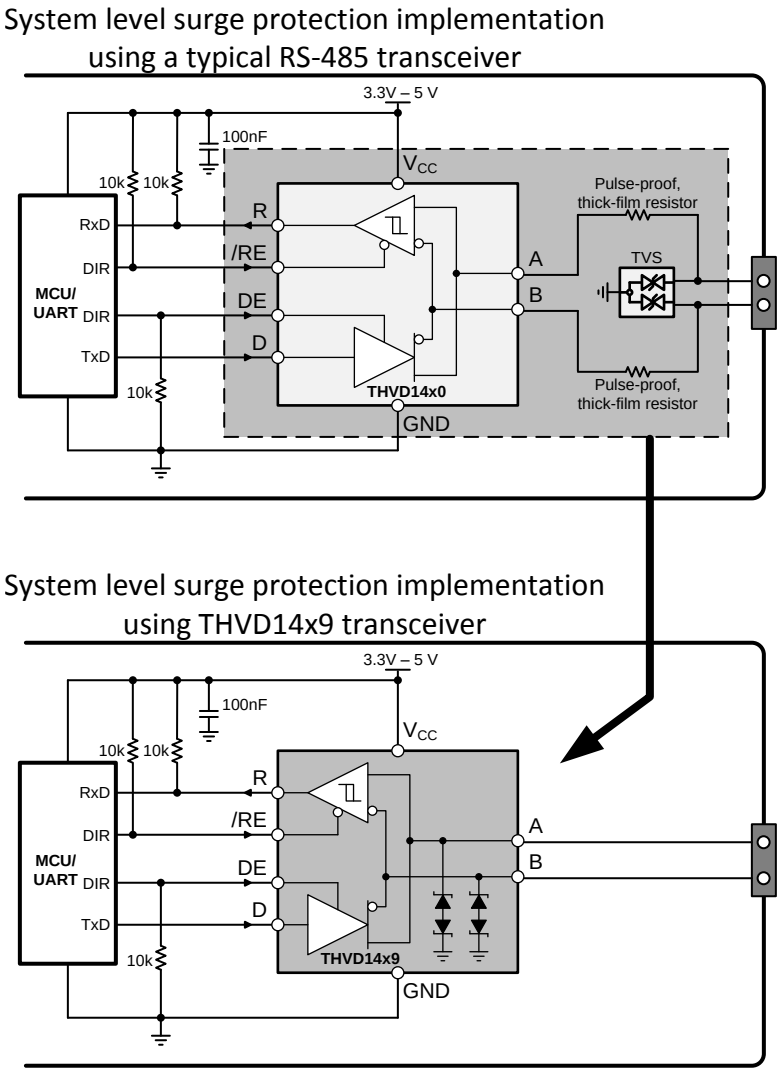
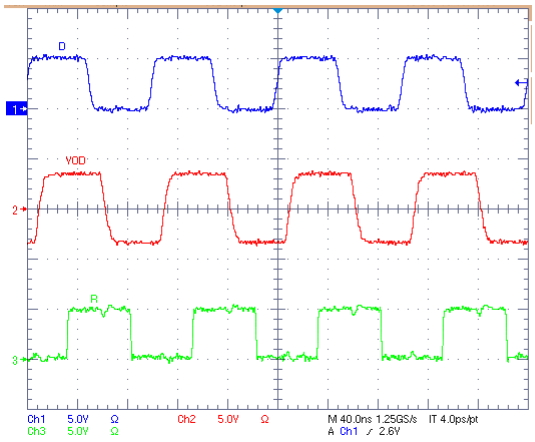


图 25. Implementation of System-Level Surge Protection Using THVD14x9

Typical Application (接下页)

10.2.3 Application Curves



V_{CC} = 5 V 54-Ω Termination T_A = 25°C

图 26. THVD1429 Waveforms at 20 Mbps

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

版权 © 2018–2019, Texas Instruments Incorporated

12 Layout

12.1 Layout Guidelines

Additional external protection components generally are not needed when using THVD14x9 transceivers.

1. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
2. Use at least two vias for V_{CC} and ground connections of decoupling capacitors to minimize effective via-inductance.
3. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.

12.2 Layout Example

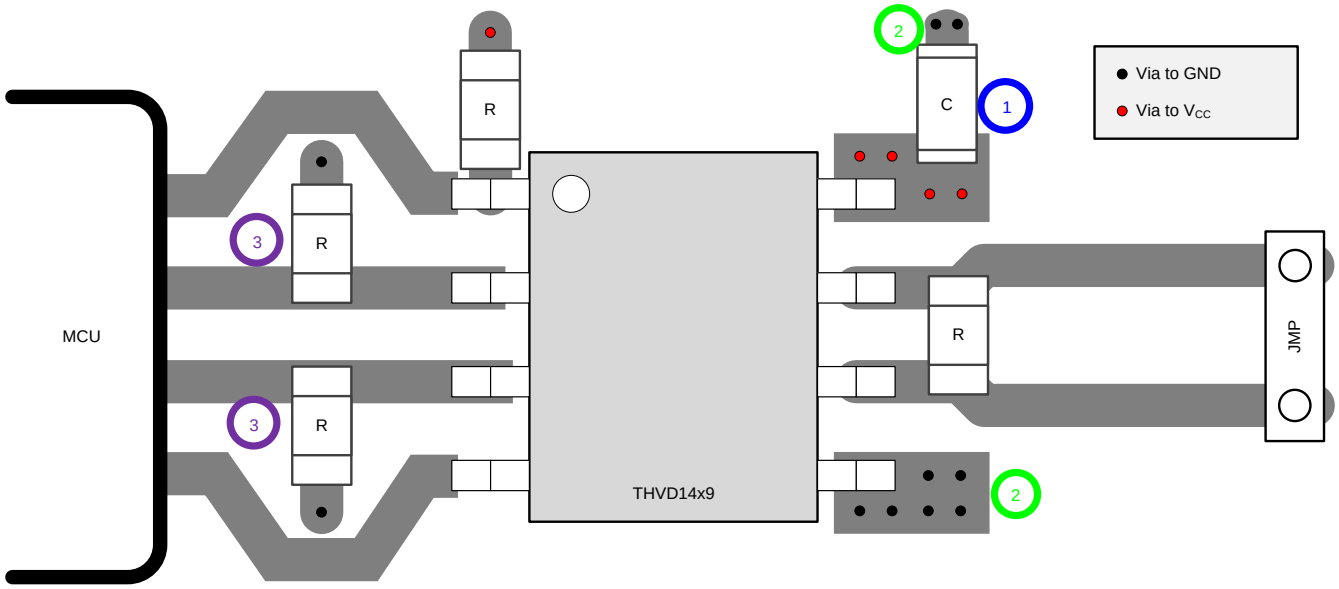


图 27. Half-Duplex Layout Example

13 器件和文档支持

13.1 器件支持

13.2 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 3. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
THVD1419	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
THVD1429	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。.

13.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 商标

E2E is a trademark of Texas Instruments.

13.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

版权 © 2018–2019, Texas Instruments Incorporated

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1419DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1419	Samples
THVD1419DT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1419	Samples
THVD1429DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1429	Samples
THVD1429DT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1429	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

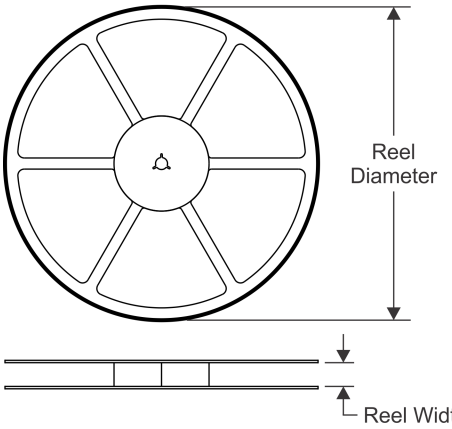
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

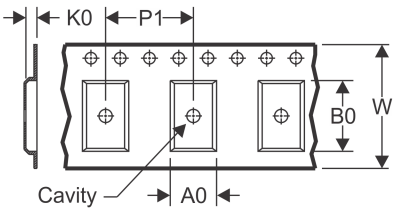
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

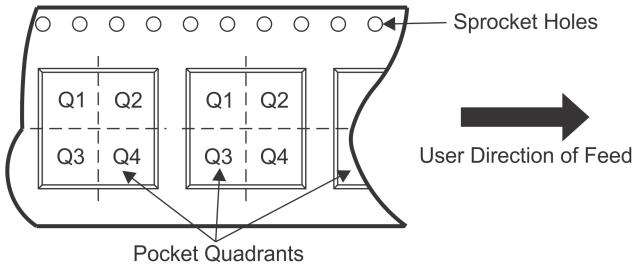


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

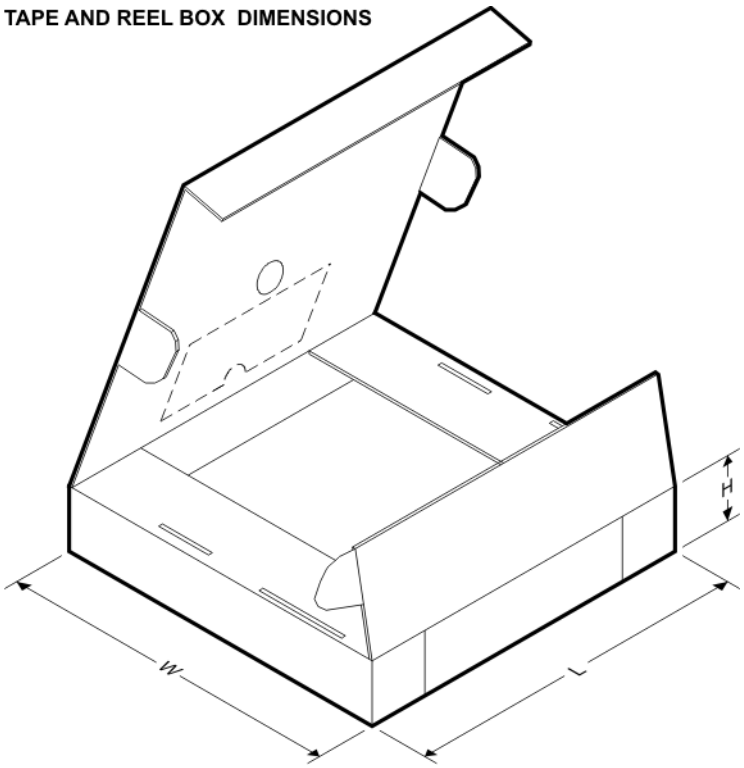
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

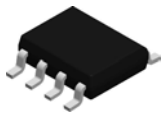
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1419DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1419DT	SOIC	D	8	250	177.8	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1429DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1429DT	SOIC	D	8	250	177.8	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1419DR	SOIC	D	8	2500	346.0	346.0	29.0
THVD1419DT	SOIC	D	8	250	213.0	191.0	35.0
THVD1429DR	SOIC	D	8	2500	346.0	346.0	29.0
THVD1429DT	SOIC	D	8	250	213.0	191.0	35.0

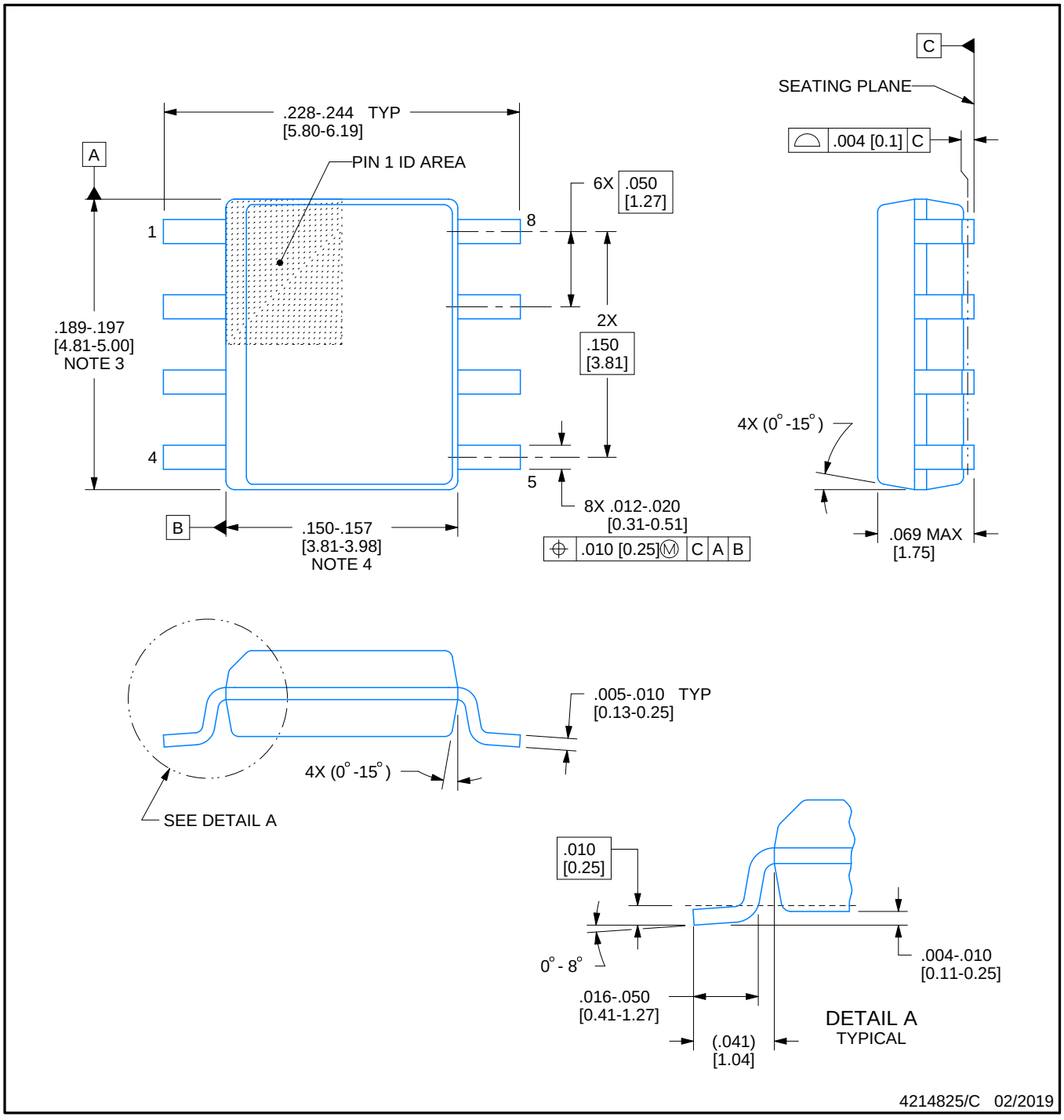


PACKAGE OUTLINE

D0008A

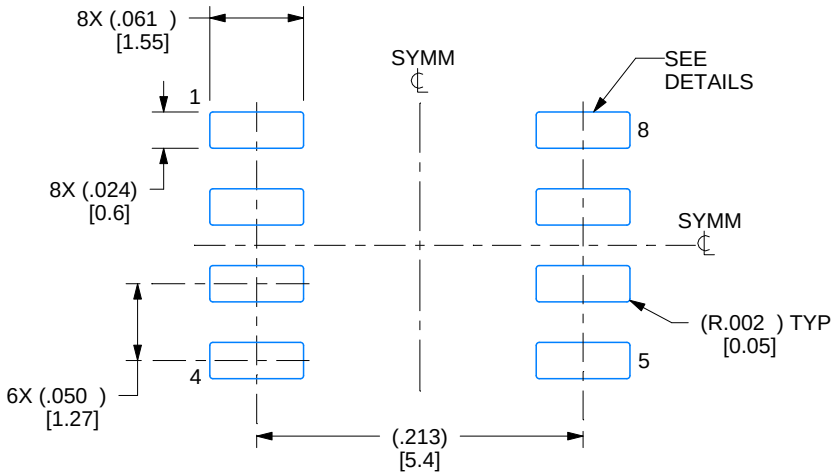
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

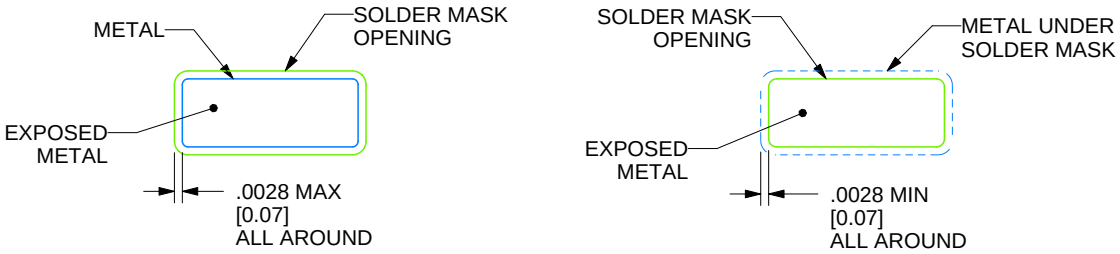


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

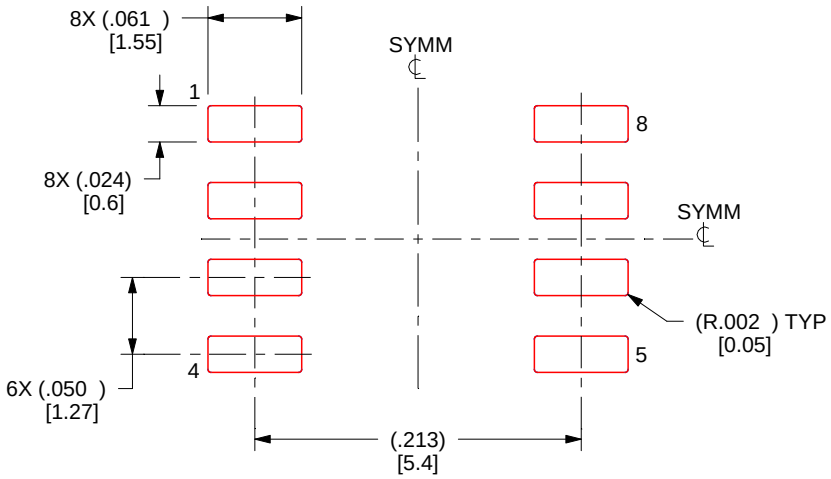
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司