

## TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: [TL082-N](#)

### FEATURES

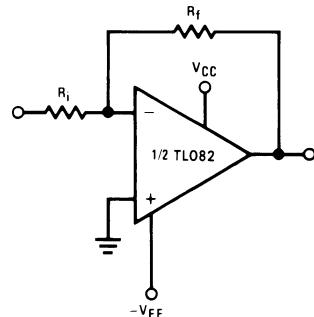
- Internally Trimmed Offset Voltage: 15 mV
- Low Input Bias Current: 50 pA
- Low Input Noise Voltage: 16nV/ $\sqrt{\text{Hz}}$
- Low Input Noise Current: 0.01 pA/ $\sqrt{\text{Hz}}$
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/ $\mu\text{s}$
- Low Supply Current: 3.6 mA
- High Input Impedance:  $10^{12}\Omega$
- Low Total Harmonic Distortion:  $\leq 0.02\%$
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2  $\mu\text{s}$

### DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage ( BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

### Typical Connection



### Connection Diagram

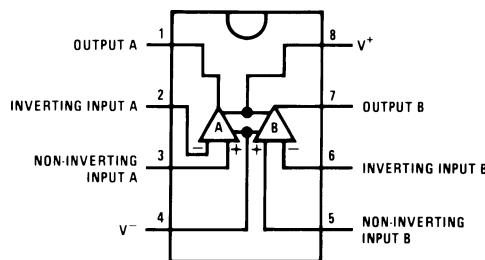


Figure 1. PDIP/SOIC Package (Top View)  
See Package Number D0008A or P0008E

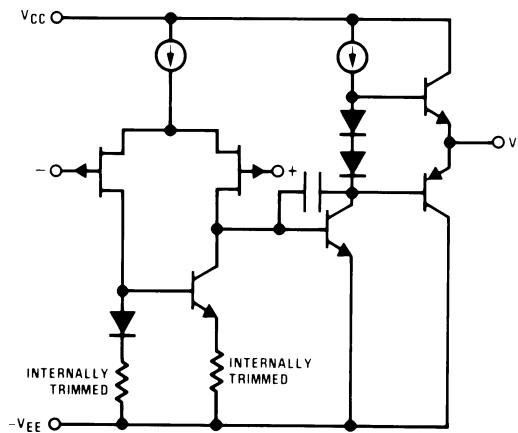


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## Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)(2)</sup>

Supply Voltage	$\pm 18V$
Power Dissipation <sup>(3)</sup>	(4)
Operating Temperature Range	0°C to +70°C
$T_j(\text{MAX})$	150°C
Differential Input Voltage	$\pm 30V$
Input Voltage Range <sup>(5)</sup>	$\pm 15V$
Output Short Circuit Duration	Continuous
Storage Temperature Range	-65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD rating to be determined.	

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The power dissipation limit, however, cannot be exceeded.
- (4) For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the P008E package.
- (5) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**DC Electrical Characteristics (1)**

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
$V_{OS}$	Input Offset Voltage	$R_S = 10 \text{ k}\Omega, T_A = 25^\circ\text{C}$ Over Temperature		5	15	$\text{mV}$
					20	$\text{mV}$
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10 \text{ k}\Omega$		10		$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current	$T_j = 25^\circ\text{C}, (1) (2)$ $T_j \leq 70^\circ\text{C}$		25	200	$\text{pA}$
					4	$\text{nA}$
$I_B$	Input Bias Current	$T_j = 25^\circ\text{C}, (1) (2)$ $T_j \leq 70^\circ\text{C}$		50	400	$\text{pA}$
					8	$\text{nA}$
$R_{IN}$	Input Resistance	$T_j = 25^\circ\text{C}$		$10^{12}$		$\Omega$
$A_{VOL}$	Large Signal Voltage Gain	$V_S = \pm 15\text{V}, T_A = 25^\circ\text{C},$ $V_O = \pm 10\text{V}, R_L = 2 \text{ k}\Omega$ Over Temperature	25	100		$\text{V/mV}$
			15			$\text{V/mV}$
$V_O$	Output Voltage Swing	$V_S = \pm 15\text{V}, R_L = 10 \text{ k}\Omega$	$\pm 12$	$\pm 13.5$		$\text{V}$
$V_{CM}$	Input Common-Mode Voltage Range	$V_S = \pm 15\text{V}$	$\pm 11$	+15 -12		$\text{V}$
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	70	100		$\text{dB}$
PSRR	Supply Voltage Rejection Ratio	(3)	70	100		$\text{dB}$
$I_S$	Supply Current			3.6	5.6	$\text{mA}$

- (1) These specifications apply for  $V_S = \pm 15\text{V}$  and  $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ .  $V_{OS}$ ,  $I_B$  and  $I_{OS}$  are measured at  $V_{CM} = 0$ .
- (2) The input bias currents are junction leakage currents which approximately double for every  $10^\circ\text{C}$  increase in the junction temperature,  $T_j$ . Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation,  $P_D$ .  $T_j = T_A + \theta_{jA} P_D$  where  $\theta_{jA}$  is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- (3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.  $V_S = \pm 6\text{V}$  to  $\pm 15\text{V}$ .

**AC Electrical Characteristics (1)**

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25^\circ\text{C}, f = 1\text{Hz-20 kHz}$ (Input Referred)		-120		$\text{dB}$
SR	Slew Rate	$V_S = \pm 15\text{V}, T_A = 25^\circ\text{C}$	8	13		$\text{V}/\mu\text{s}$
GBW	Gain Bandwidth Product	$V_S = \pm 15\text{V}, T_A = 25^\circ\text{C}$		4		$\text{MHz}$
$e_n$	Equivalent Input Noise Voltage	$T_A = 25^\circ\text{C}, R_S = 100\Omega,$ $f = 1000 \text{ Hz}$		25		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Equivalent Input Noise Current	$T_j = 25^\circ\text{C}, f = 1000 \text{ Hz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$A_V = +10, R_L = 10\text{k},$ $V_O = 20 \text{ Vp-p},$ $\text{BW} = 20 \text{ Hz-20 kHz}$		<0.02		$\%$

- (1) These specifications apply for  $V_S = \pm 15\text{V}$  and  $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ .  $V_{OS}$ ,  $I_B$  and  $I_{OS}$  are measured at  $V_{CM} = 0$ .

### Typical Performance Characteristics

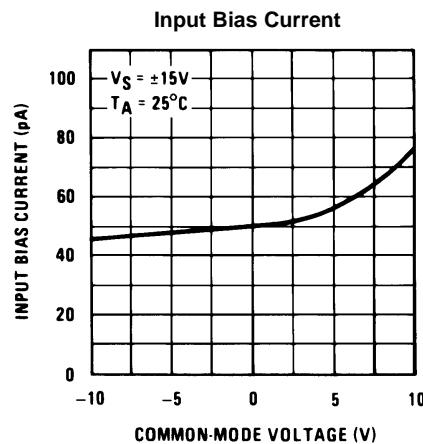


Figure 2.

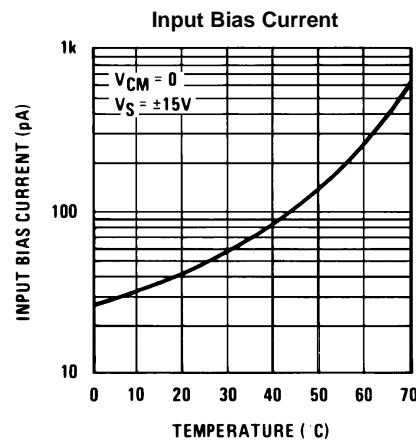


Figure 3.

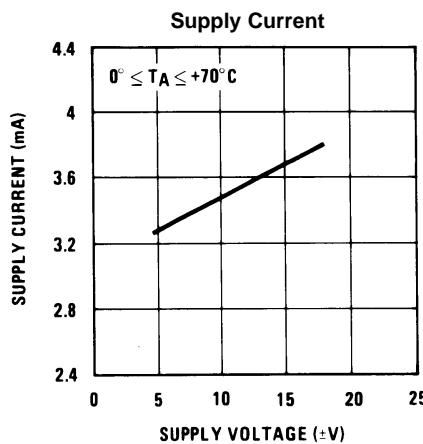


Figure 4.

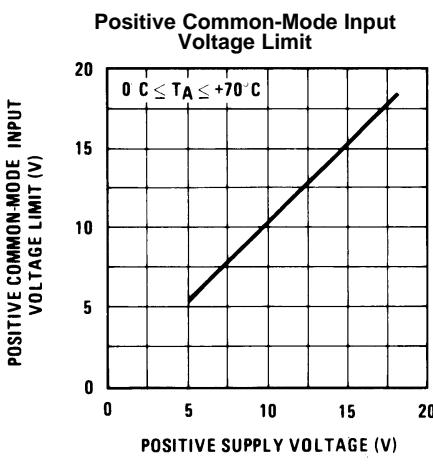


Figure 5.

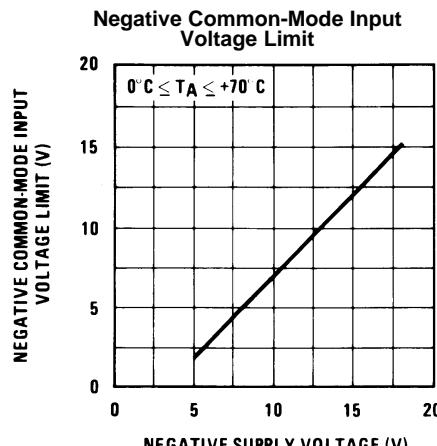


Figure 6.

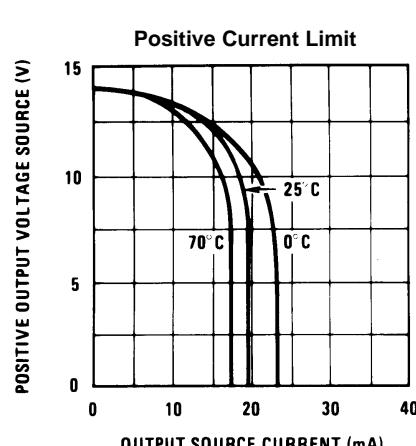


Figure 7.

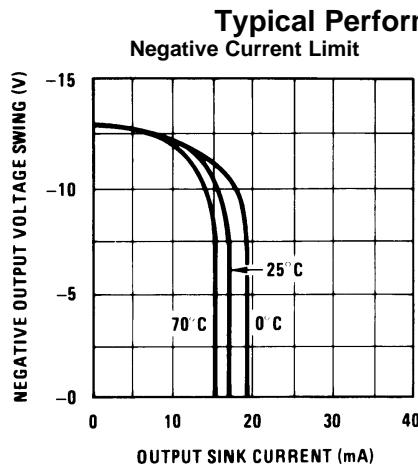


Figure 8.

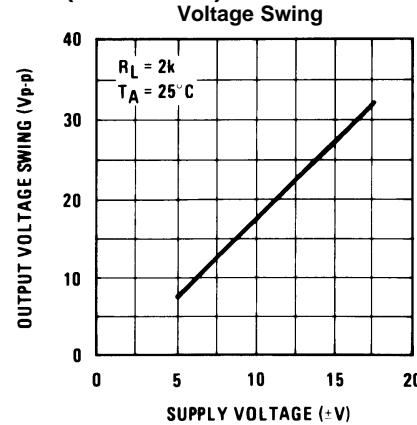


Figure 9.

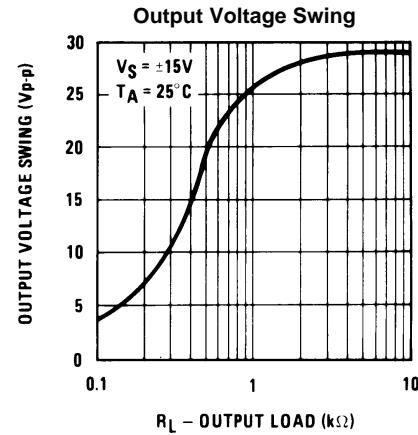


Figure 10.

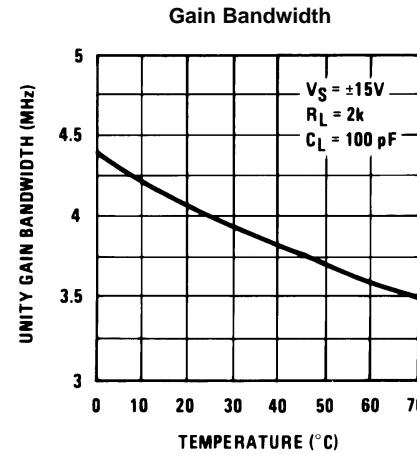


Figure 11.

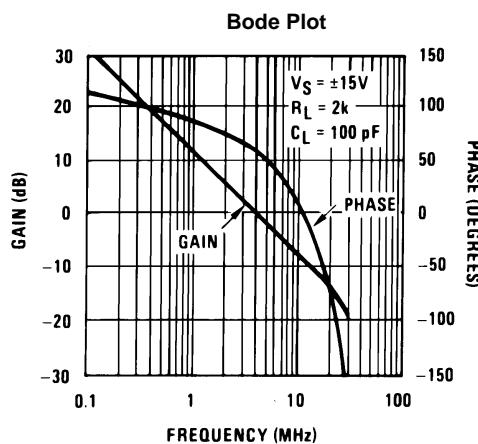


Figure 12.

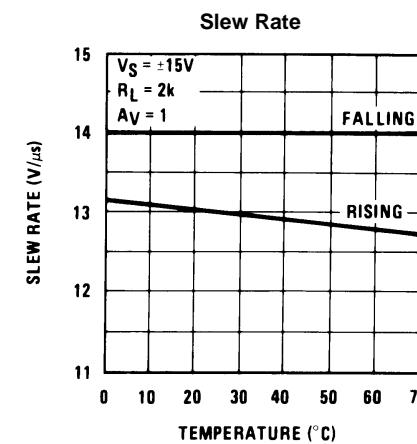


Figure 13.

### Typical Performance Characteristics (continued)

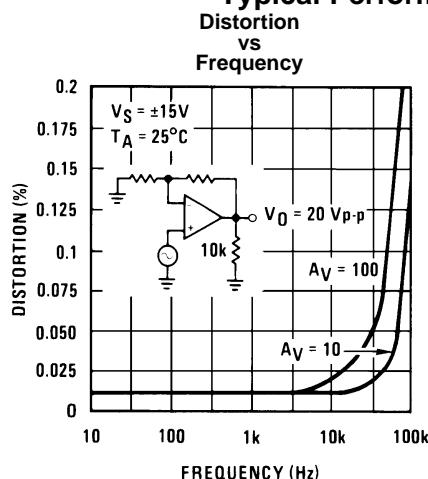


Figure 14.

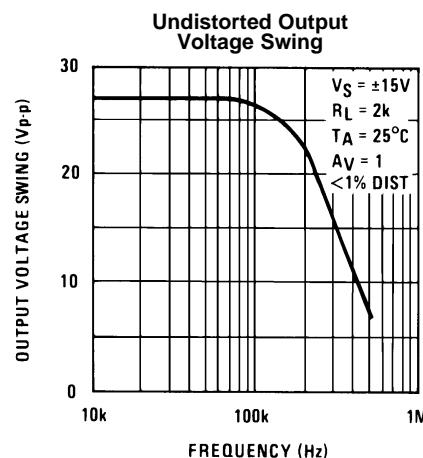


Figure 15.

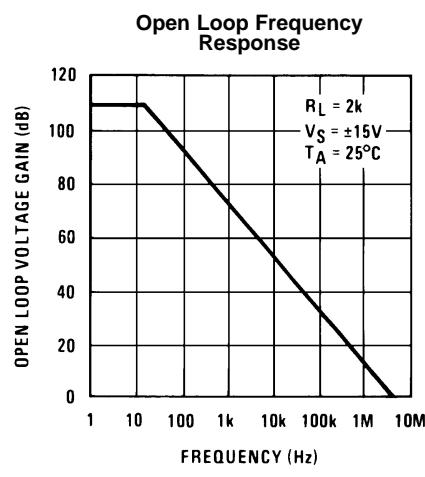


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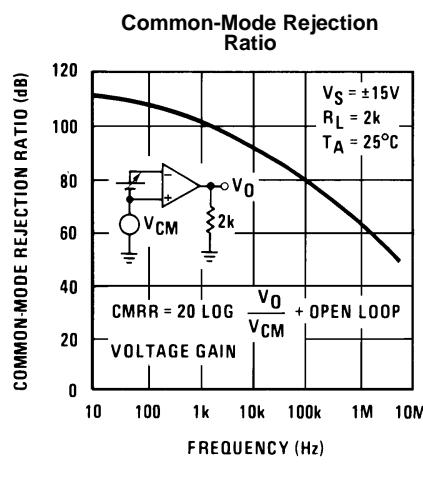


Figure 17.

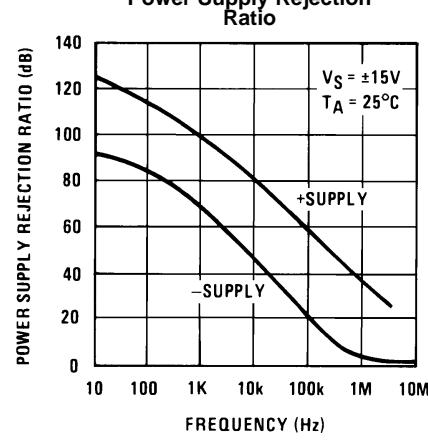


Figure 18.

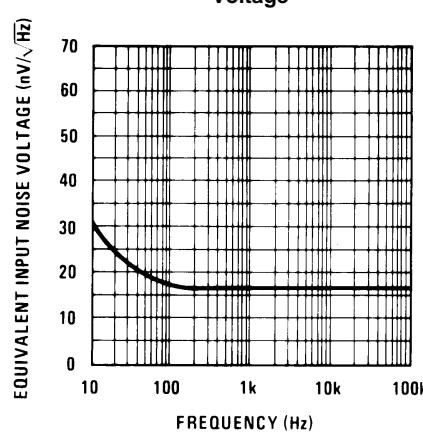
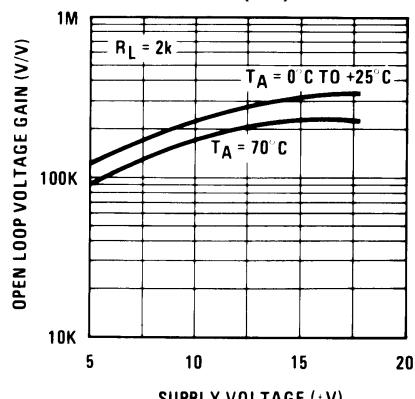


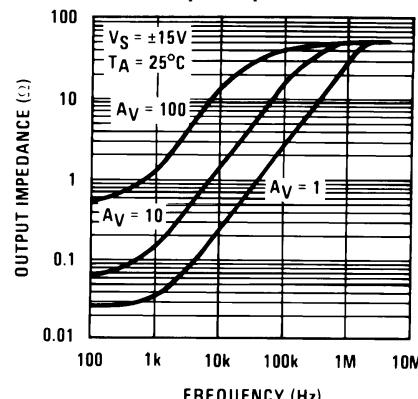
Figure 19.

### Typical Performance Characteristics (continued)

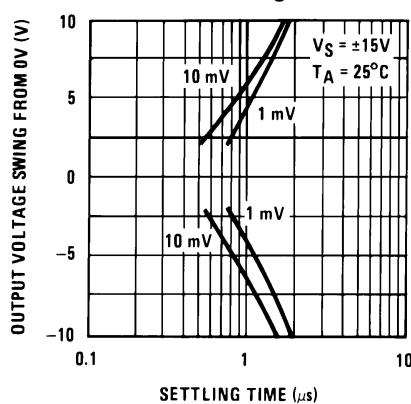
**Open Loop Voltage Gain (V/V)**


**Figure 20.**

### Output Impedance


**Figure 21.**

### Inverter Setting Time


**Figure 22.**

### Pulse Response

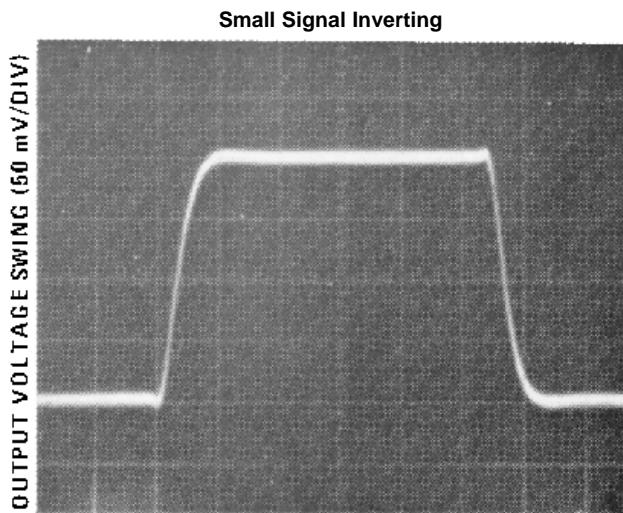


Figure 23.

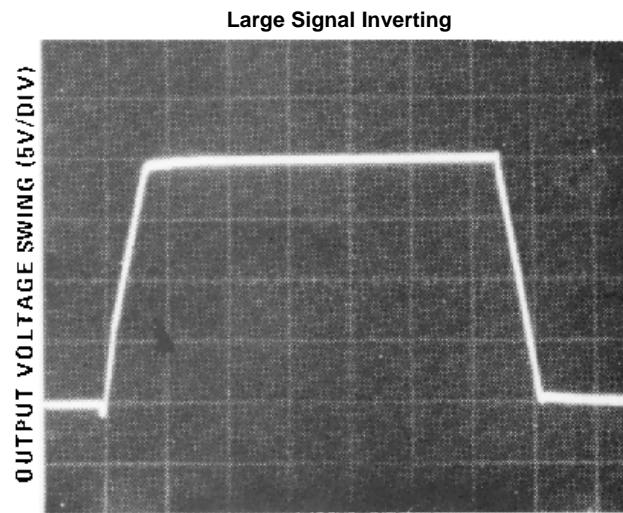


Figure 24.

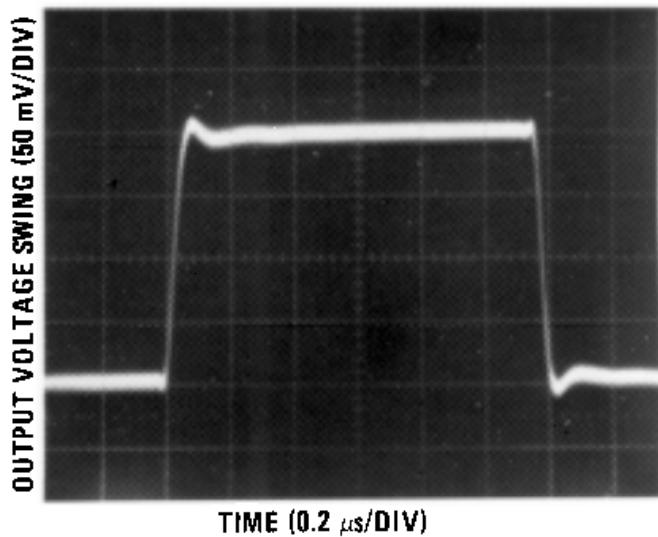


Figure 25.

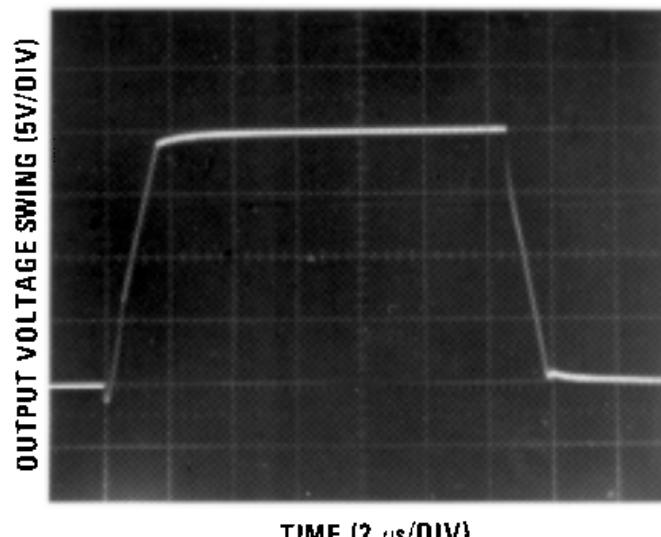


Figure 26.

**Pulse Response (continued)**

Current Limit ( $R_L = 100\Omega$ )

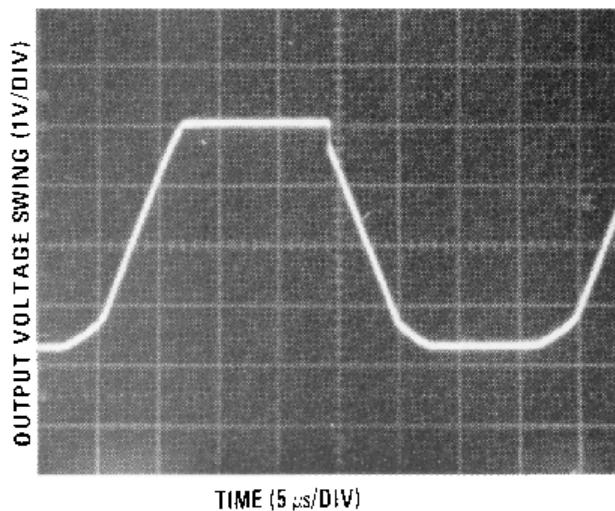


Figure 27.

## APPLICATION HINTS

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on  $\pm 6$ V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

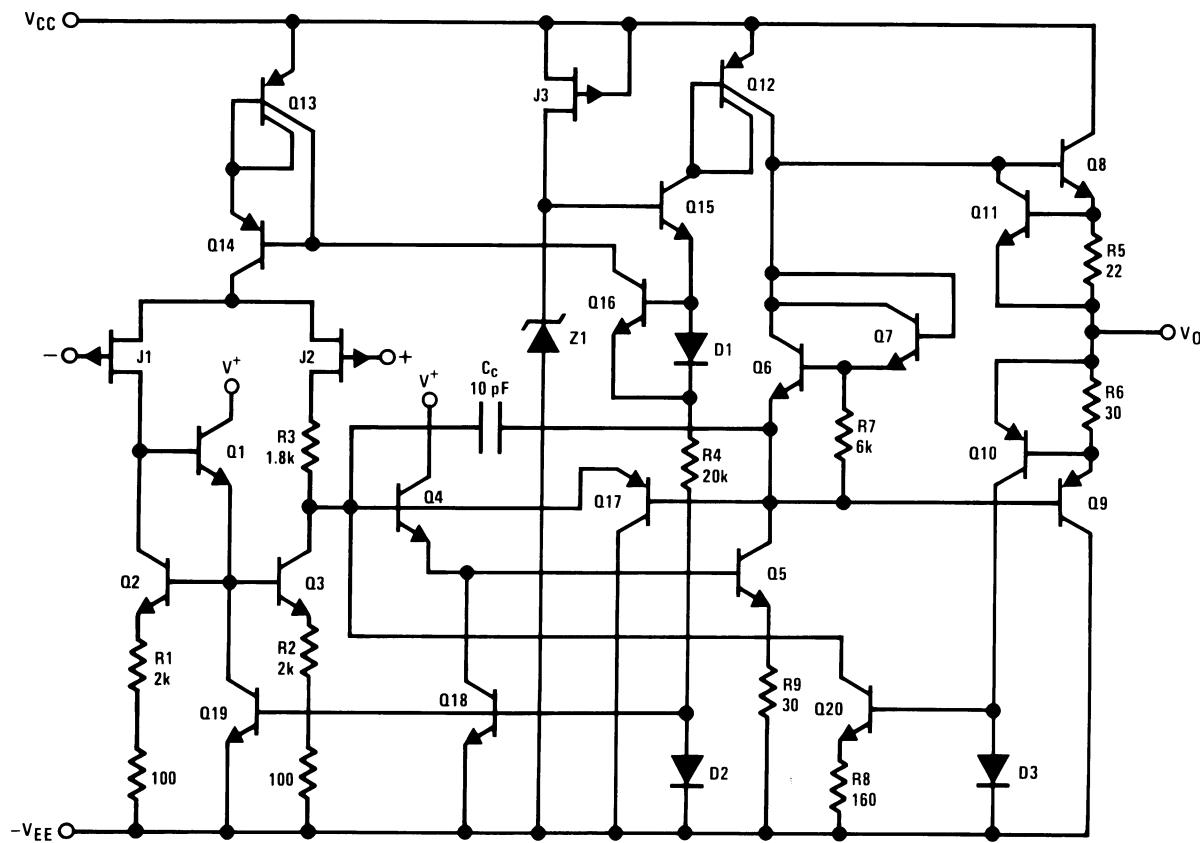
The amplifiers will drive a  $2\text{ k}\Omega$  load resistance to  $\pm 10\text{V}$  over the full temperature range of  $0^\circ\text{C}$  to  $+70^\circ\text{C}$ . If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

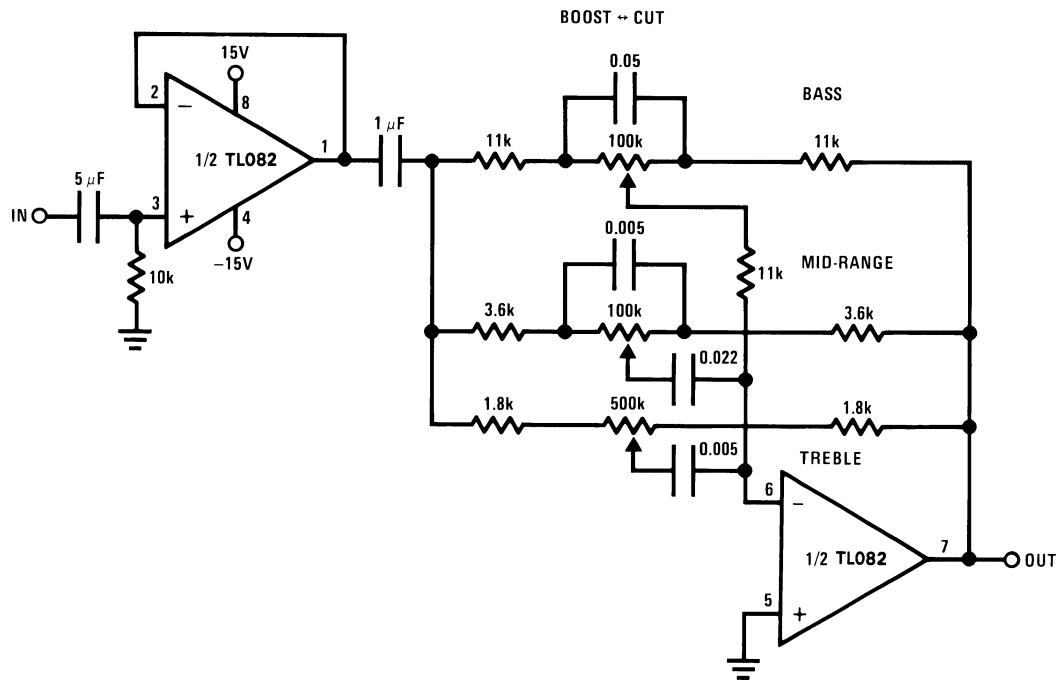
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

**Detailed Schematic**


## Typical Applications



- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

All controls flat.

Bass and treble boost, mid flat.

Bass and treble cut, mid flat.

Mid boost, bass and treble flat.

Mid cut, bass and treble flat.

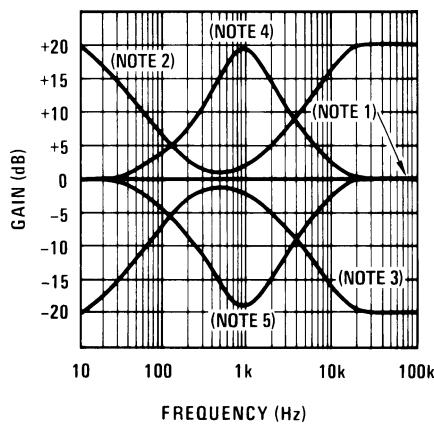
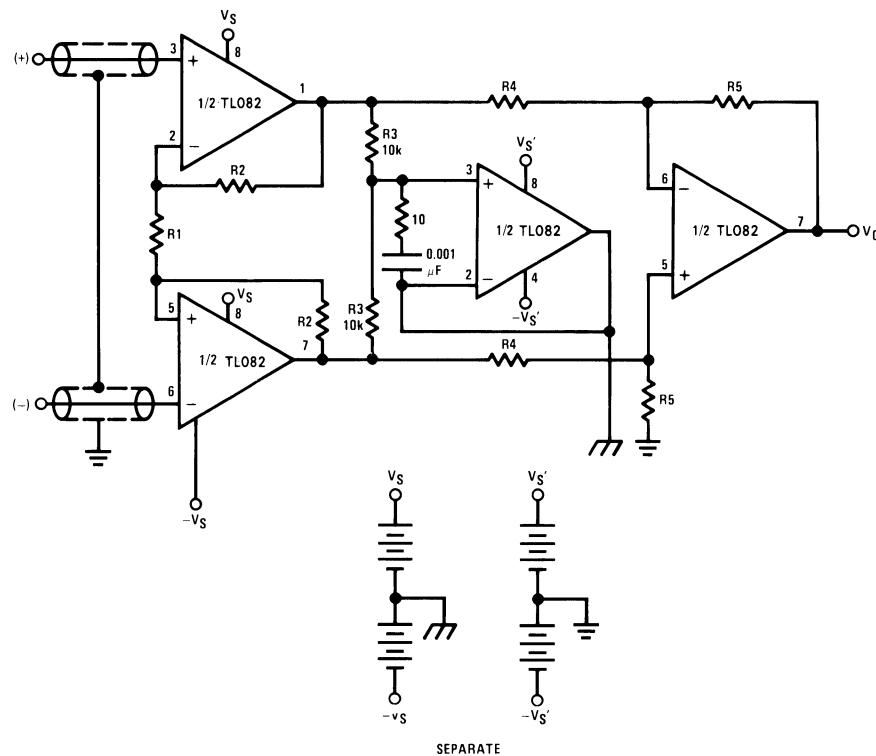


Figure 28. Three-Band Active Tone Control



$$A_V = \left( \frac{2R_2}{R_1} + 1 \right) \frac{R_5}{R_4}$$

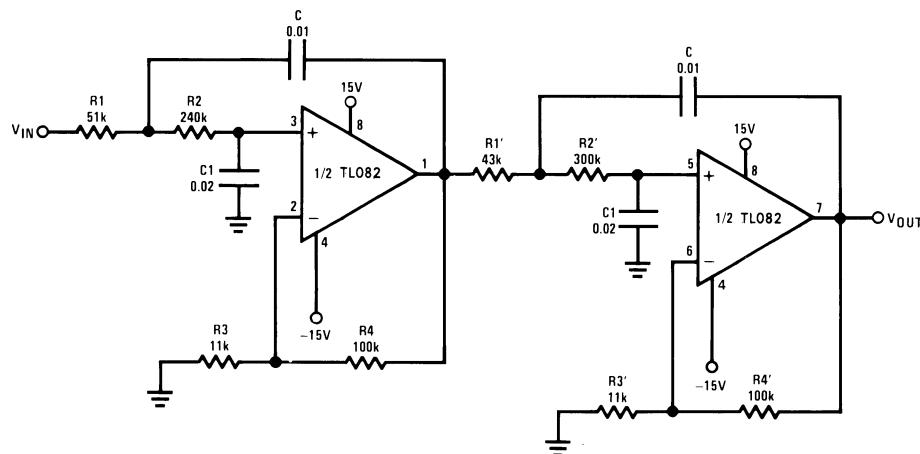
 and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With  $A_{VT} = 1400$ , resistor matching = 0.01%: CMRR = 136 dB

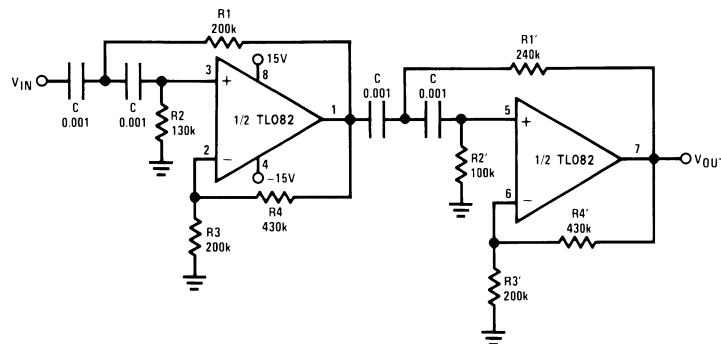
- Very high input impedance
- Super high CMRR

**Figure 29. Improved CMRR Instrumentation Amplifier**



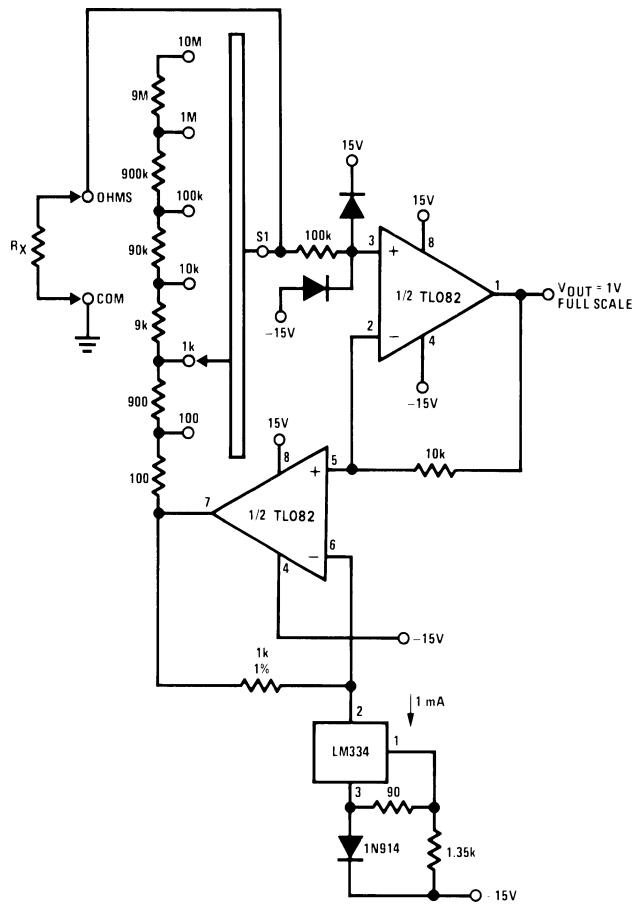
- Corner frequency ( $f_c$ ) =  $\sqrt{\frac{1}{R_1 R_2 C_1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R_1' R_2' C_1}} \cdot \frac{1}{2\pi}$
- Passband gain ( $H_0$ ) =  $(1 + R_4/R_3) (1 + R_4'/R_3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Figure 30. Fourth Order Low Pass Butterworth Filter



- Corner frequency ( $f_c$ ) =  $\sqrt{\frac{1}{R_1 R_2 C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R_1' R_2' C^2}} \cdot \frac{1}{2\pi}$
- Passband gain ( $H_0$ ) =  $(1 + R_4/R_3) (1 + R_4'/R_3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Figure 31. Fourth Order High Pass Butterworth Filter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where  $R_{LADDER}$  is the resistance from switch S1 pole to pin 7 of the TL082CP.

**Figure 32. Ohms to Volts Converter**

## REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	15

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082CM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL082CMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL082CP/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	TL082 CP	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

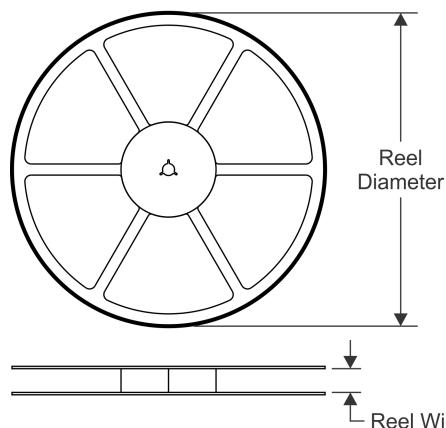
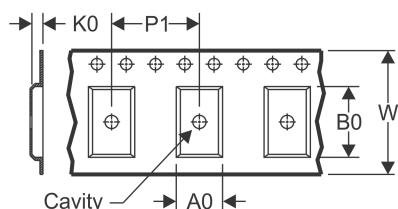
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL082-N :**

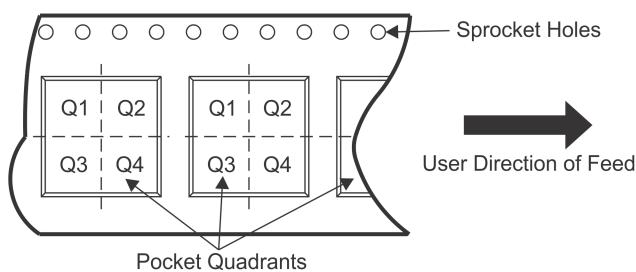
- Automotive : [TL082-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


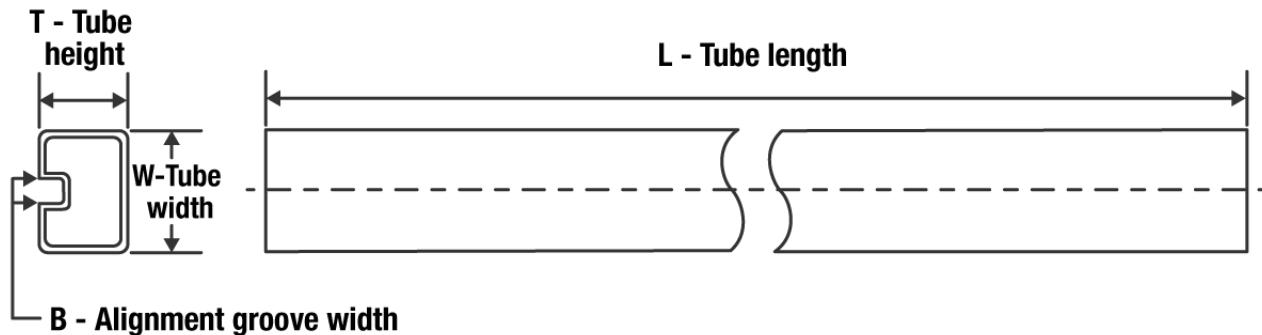
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

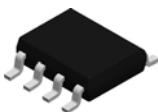
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

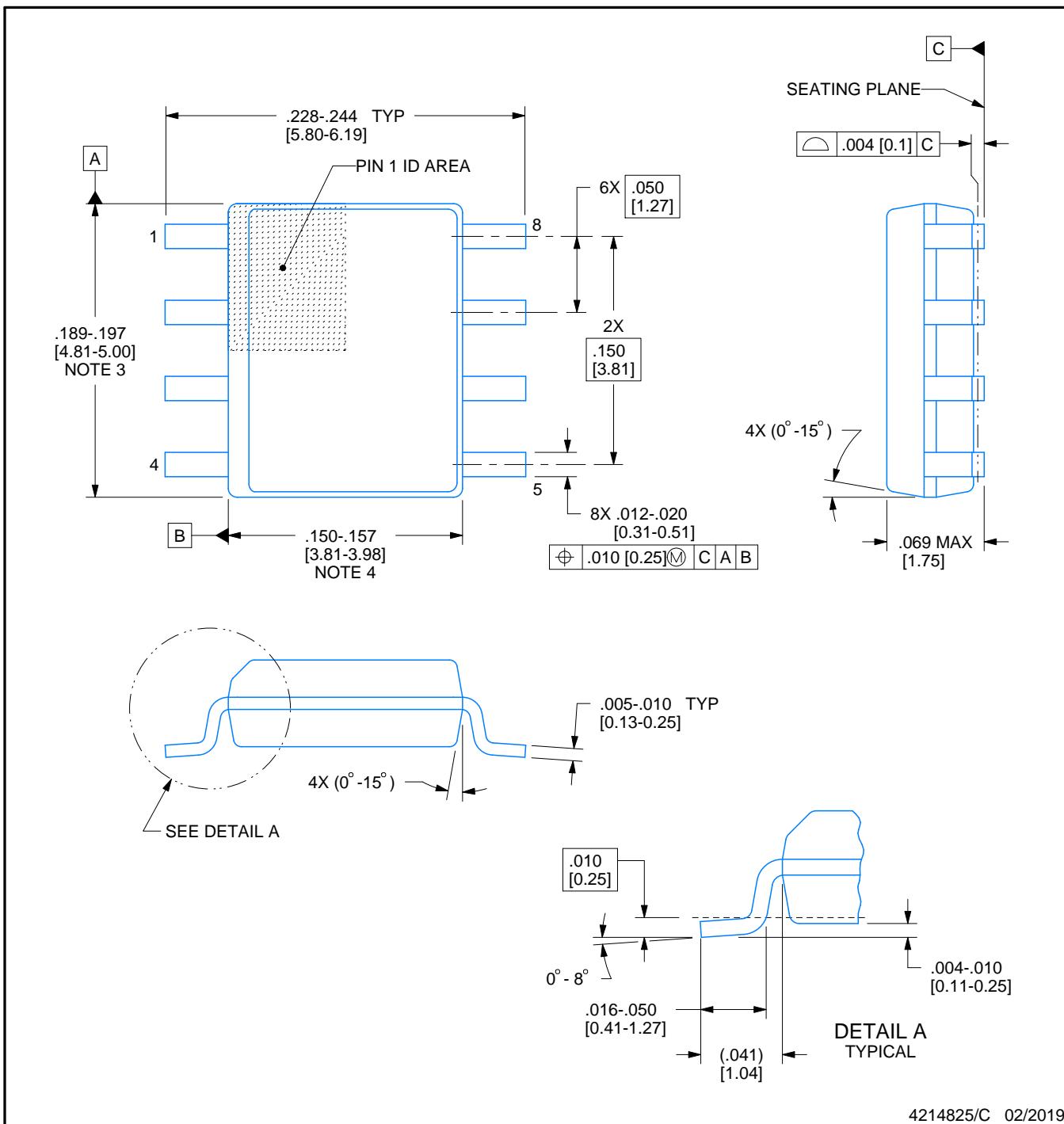
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL082CM/NOPB	D	SOIC	8	95	495	8	4064	3.05
TL082CP/NOPB	P	PDIP	8	40	502	14	11938	4.32



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

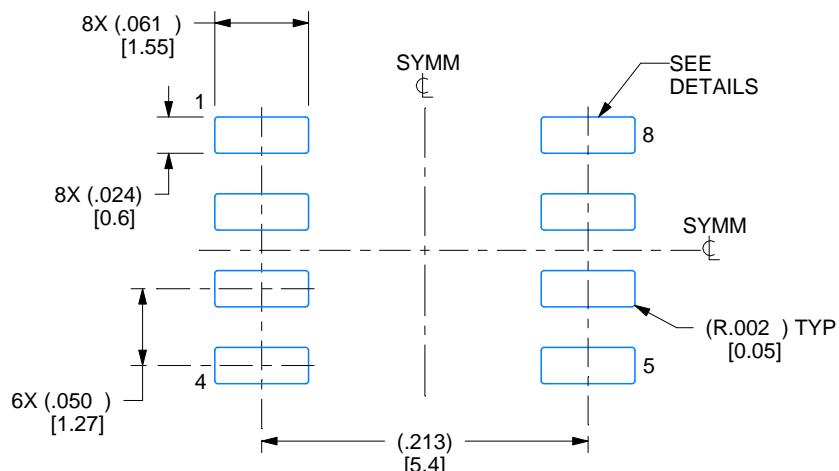
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

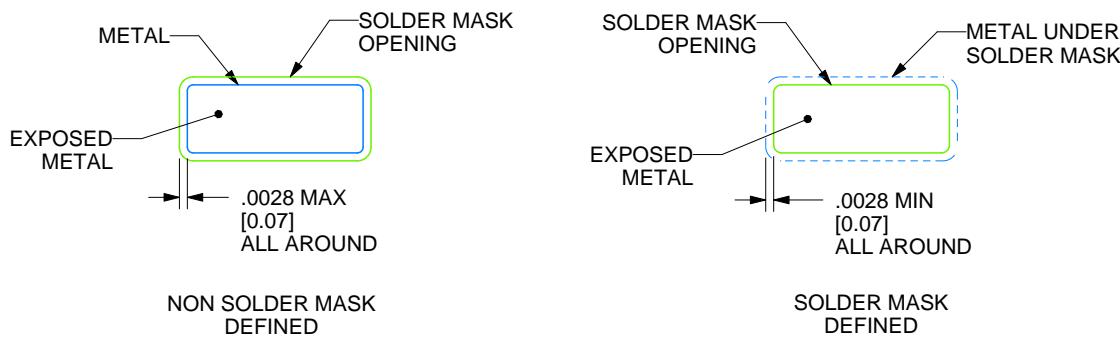
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

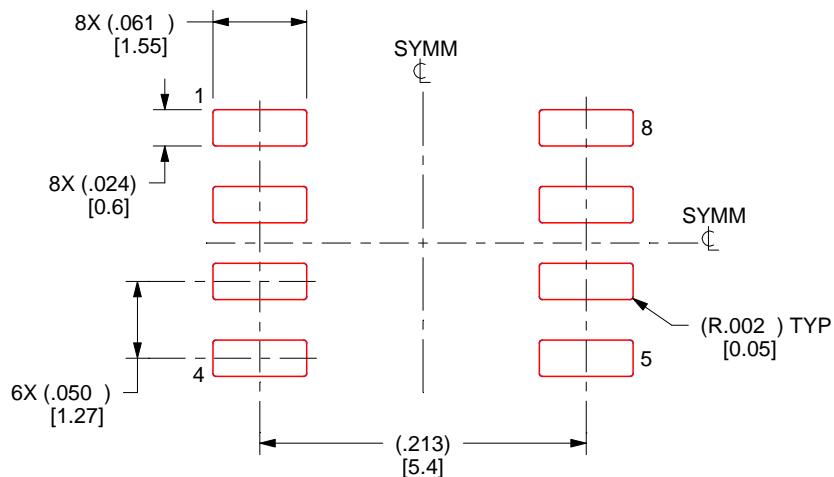
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

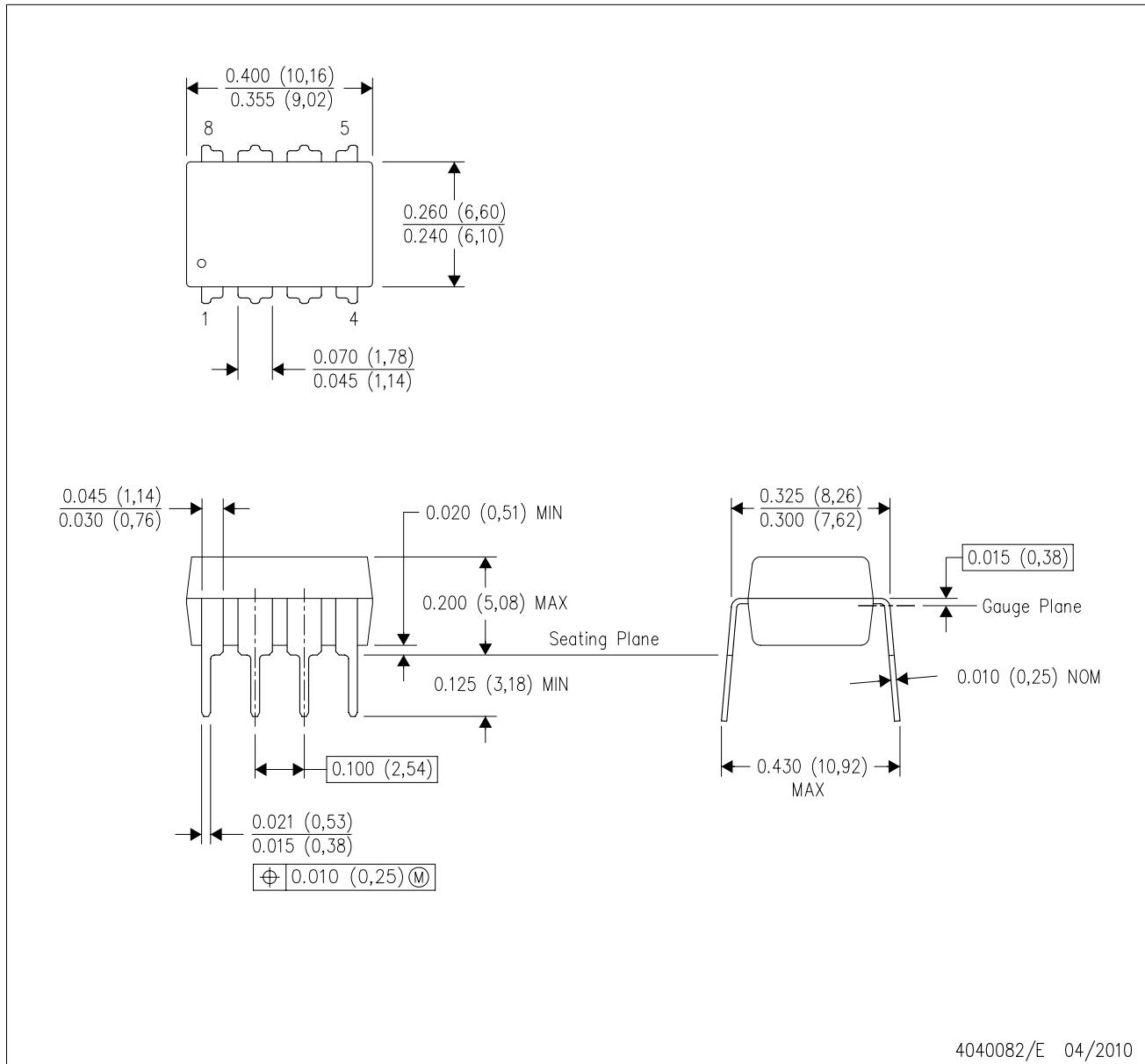
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 variation BA.

4040082/E 04/2010

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