

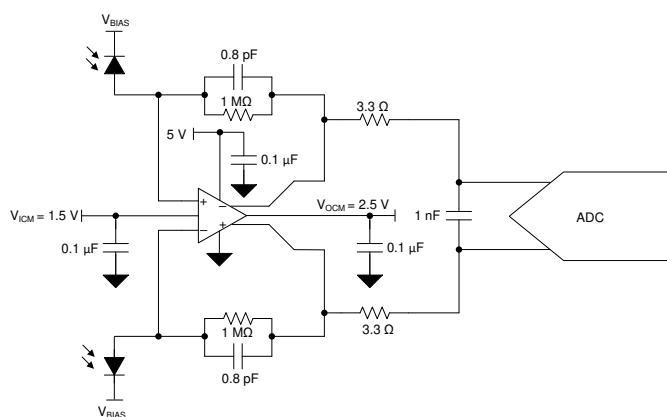
THS4567 220 MHz, High Input Impedance, Fully Differential Amplifier with Independent Input and Output Common-Mode Control

1 Features

- Gain Bandwidth Product (GBWP): 220 MHz
- Slew Rate: 500 V/ μ s
- Bandwidth: 42 MHz ($G = 10$ V/V)
- Voltage Noise: 4.2 nV/ $\sqrt{\text{Hz}}$
- Supply Current (I_Q): 2 mA
- I_Q : 28 μ A (Shutdown)
- Rail-to-Rail Output (RRO)
- High Impedance CMOS Inputs
- Independent Input and Output Common-Mode Control
- Disable Input Common-Mode Loop to Use as a Standard Fully Differential Amplifier (FDA)
- Single-Supply Range: 3.3 V to 5.5 V
- Split-Supply Range: ± 1.65 V to ± 2.75 V
- Operating Temperature Range: -40°C to 125°C

2 Applications

- [Absolute Optical Encoder](#)
- [AC Drive Position Feedback](#)
- [Linear Motor Position Sensor](#)
- [Clinical Pulse Oximeter](#)
- Optical Coherence Tomography



Single-Stage Differential-Input to Differential-Output, TIA and ADC Driver for Optical Encoders

3 Description

The THS4567 device is a novel fully-differential amplifier (FDA) that includes independent input common-mode (VICM) and output-common mode (VOCM) control. Standard FDAs only possess output common-mode control. The THS4567 is a decoupled amplifier with a minimum stable gain of 10 V/V.

The THS4567 operates as a fully differential transimpedance amplifier (TIA) and analog-to-digital converter (ADC) driver in a single integrated stage.

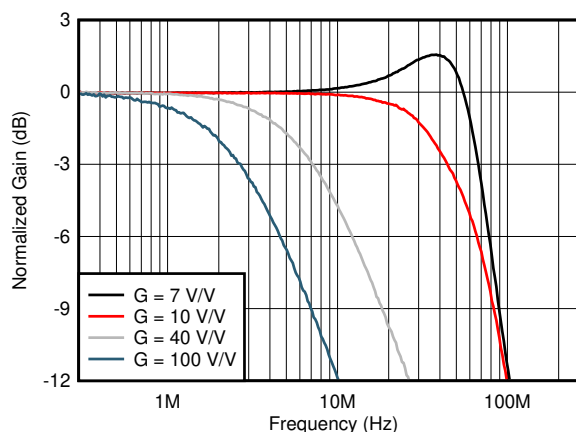
The VICM loop decouples the reverse bias across the photodiode(PD) from the amplifiers input and output swing compliance ranges thereby allowing the designer to maximize the PD reverse bias and minimize the PD capacitance. The VICM loop can be disabled which then allows the THS4567 to operate as a standard FDA.

The VOCM loop sets the differential output common-mode voltage and is typically set at the subsequent ADC stage common-mode reference voltage.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4567	WQFN (10)	2.00 mm × 2.00 mm

- (1) For all available packages, see the package option addendum at the end of the data sheet.



Small-Signal Frequency Response vs Gain

D201



Table of Contents

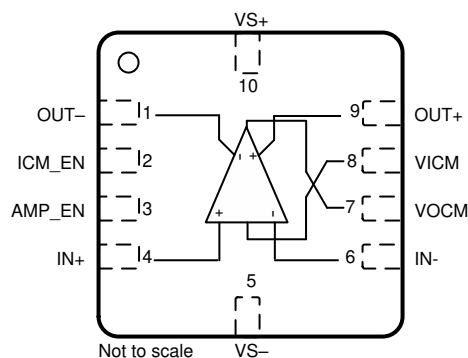
1 Features	1	7.4 Device Functional Modes.....	18
2 Applications	1	8 Application and Implementation	19
3 Description	1	8.1 Application Information.....	19
4 Revision History	2	8.2 Typical Application.....	20
5 Pin Configuration and Functions	3	8.3 Differential TIA with 0-V Biased Photodiode.....	24
6 Specifications	4	8.4 Differential AC Coupled TIA.....	25
6.1 Absolute Maximum Ratings	4	9 Power Supply Recommendations	25
6.2 ESD Ratings	4	10 Layout	26
6.3 Recommended Operating Conditions	4	10.1 Layout Guidelines.....	26
6.4 Thermal Information	4	10.2 Layout Example.....	26
6.5 Electrical Characteristics: Differential TIA Mode, ICM loop enabled	5	11 Device and Documentation Support	27
6.6 Electrical Characteristics: FDA operation, ICM loop disabled	6	11.1 Documentation Support.....	27
6.7 Typical Characteristics: $(V_{S+}) - (V_{S-}) = 5\text{ V}$	9	11.2 Receiving Notification of Documentation Updates..	27
7 Detailed Description	16	11.3 Support Resources.....	27
7.1 Overview.....	16	11.4 Trademarks.....	27
7.2 Functional Block Diagram.....	16	11.5 Electrostatic Discharge Caution.....	27
7.3 Feature Description.....	17	11.6 Glossary.....	27
		12 Mechanical, Packaging, and Orderable Information	27

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

5 Pin Configuration and Functions



**Figure 5-1. RUN Package
10-Pin WQFN
Top View**

Table 5-1. Pin Functions

NAME	PIN NO.	I/O	DESCRIPTION
AMP_EN	3	I	Amplifier enable. HIGH (Default) = normal operation; LOW = power-off mode.
ICM_EN	2	I	Input common-mode loop enable. HIGH (Default) = ICM loop enabled (TIA mode); ICM loop disabled (FDA mode).
IN+	4	I	Noninverting (positive) amplifier input (V_{IN+} = voltage measured at pin 4).
IN-	6	I	Inverting (negative) amplifier input (V_{IN-} = voltage measured at pin 6).
OUT+	9	O	Noninverting (positive) amplifier output (V_{OUT+} = voltage measured at pin 9).
OUT-	1	O	Inverting (negative) amplifier output (V_{OUT-} = voltage measured at pin 1).
VICM	8	I	Input common-mode voltage input (VICM = voltage applied at pin 8, V_{ICM} = voltage measured at pin 8).
VOCM	7	I	Output common-mode voltage input (VOCM = voltage applied at pin 7, V_{OCM} = average output voltage).
VS+	10	–	Positive power-supply input (V_{S+} = voltage applied at pin 10).
VS-	5	–	Negative power-supply input (V_{S-} = voltage applied at pin 5).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _S	Total supply voltage (V _{S+} – V _{S-})		5.75	V
	Input, output, enable and common-mode pin voltage range	(V _{S-}) – 0.5	(V _{S+}) + 0.5	V
	Differential input pin voltage		±1	V
I _{IN}	Continuous input current		±10	mA
I _{OUT}	Continuous output current ⁽²⁾		±20	mA
T _J	Junction temperature		150	°C
T _A	Operating free-air temperature	–40	125	°C
T _{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V _S	Total supply voltage	3.3	5	5.5	V
T _A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		THS4567	UNIT
		RUN (WQFN)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	118	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	70.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	57.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	3.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	57.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics: Differential TIA Mode, ICM loop enabled

$V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{OCM} = \text{Open}$, $V_{ICM} = \text{Open}$, $R_F = 1\text{ M}\Omega$, $C_F = 0.4\text{ pF}$, $C_{IN} = 10\text{ pF}$ (on each input pin), $AMP_EN = 2.5\text{ V}$, ICM loop enabled ($ICM_EN = 2.5\text{ V}$) and $T_A = 25^\circ\text{C}$. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE (ICM LOOP)						
GBWP	Differential-transimpedance gain bandwidth product	V _{OUT} = 100 mV _{PP}		220		MHz
	Input Common-Mode control loop small-signal bandwidth	V _{OUT} = 100 mV _{PP}		5		MHz
i _N	Input differential current noise	f = 100 kHz, ICM loop disabled		0.02		pA/√Hz
		f= 100 kHz, output current of ICM loop, I _{CM_CTL} ⁽³⁾ < 750 nA		0.35		
		f= 100 kHz, Output current of ICM loop, I _{CM_CTL} ⁽³⁾ < 2.8 μA		0.5		
		f= 100 kHz, Output current of ICM loop, I _{CM_CTL} ⁽³⁾ < 5.5 μA		0.65		
		f= 100 kHz, Output current of ICM loop, I _{CM_CTL} ⁽³⁾ < 17 μA		1.1		
		f= 100 kHz, Output current of ICM loop, I _{CM_CTL} ⁽³⁾ < 55 μA		1.9		
DC PERFORMANCE (ICM LOOP)						
V _{ICM} ⁽¹⁾	VICM pin default voltage above V _{S-}	VICM pin open (voltage measured at pin 8)	1.4	1.55	1.75	V
V _{ICM} ⁽¹⁾	Default input common-mode voltage above V _{S-}	VICM pin open, V _{ICM} = (V _{IN+} + V _{IN-})/2	1.4	1.55	1.75	V
ΔV _{ICM} /ΔT _A	Input common-mode voltage drift	T _A = −40°C to +125°C, VICM pin open		160		μV/°C
ΔV _{ICM} /ΔI _{CM_CTL}	Input common-mode voltage vs. I _{CM_CTL} current ^{(2) (3)}	I _{CM_CTL} variation = 5 μA to 20 μA	2	2.8	3.6	mV/μA
ΔV _{ICM} /ΔT _A	Input common-mode voltage offset drift	T _A = −40°C to +125°C, VICM pin driven to midsupply		22		μV/°C
V _{IN_OS}	Input common-mode offset error	VICM pin driven to midsupply, I _{CM_CTL} = 0 ⁽²⁾ , V _{IN_OS} = (V _{ICM} − VICM)	−25	±2.5	25	mV
	VICM pin DC input resistance	VICM pin driven to midsupply		200		kΩ
	VICM input high	≤ ±20-mV shift from midsupply offset, I _{CM_CTL} ≤ 100 μA	V _{S+} − 1.5	V _{S+} − 1.3		V
	VICM input low	≤ ±20-mV shift from midsupply offset, I _{CM_CTL} ≤ 100 μA		V _{S-} + 0.8	V _{S-} + 1	V
I _{CM_OS}	Input common-mode control current offset mismatch between inputs	I _{CM_OS} = ΔI _(CM_CTL, IN+/IN-) /Average I _{CM_CTL} , I _{CM_CTL} = 10 μA		0.5%		

- (1) V_{ICM} refers to the common-mode or average voltage at the FDA inputs ($IN+$ and $IN-$). When the input common-mode (ICM) control function is enabled ($ICM_EN = \text{HIGH}$), the device generates matched source/sink control currents to drive the input pins towards the VICM pin reference voltage. Therefore VICM represents the voltage at pin 8, while V_{ICM} represents the average input voltage.
- (2) I_{CM_CTL} refers to the magnitude of the matched source/sink control currents generated by the ICM loop at the device I_{IN+} and I_{IN-} pins.
- (3) A positive I_{CM_CTL} current is defined as a sinking (pull-down) current, generated by the ICM control loop to balance the total currents (external common-mode + feedback) that flow into the FDA input pins.

6.6 Electrical Characteristics: FDA operation, ICM loop disabled

$V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{OCM} = \text{Open}$, $V_{ICM} = \text{Open}$, $R_F = 5\text{ k}\Omega$, Gain = 10 V/V, ICM loop disabled ($ICM_EN = -2.5\text{ V}$), $R_L = 1\text{ k}\Omega$ and $T_A = 25^\circ\text{C}$. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V _{OUT} ⁽²⁾ = 100 mV _{PP}		43		MHz
LSBW	Large-signal bandwidth	V _{OUT} ⁽²⁾ = 8 V _{PP}		28		MHz
GBWP	Gain bandwidth product			220		MHz
	Slew rate	V _{OUT} = 8V Step, 20% ↔ 80%		500		V/μs
t _R , t _F	Rise and fall time	V _{OUT} = 100 mV _{PP} , 10% ↔ 90%		8		ns
	0.1% settling time	V _{OUT} = 8V Step		65		ns
	0.001% settling time			175		
HD2	Second-order harmonic distortion	f= 100 kHz, V _{OUT} = 2 V _{PP}		−115		dBc
		f= 100 kHz, V _{OUT} = 8 V _{PP}		−105		
HD3	Third-order harmonic distortion	f= 100 kHz, V _{OUT} = 2 V _{PP}		−118		dBc
		f= 100 kHz, V _{OUT} = 8 V _{PP}		−108		
e _N	Input differential voltage noise	f = 100 kHz		4.2		nV/√Hz
i _N	Input current noise, each input			10		fA/√Hz
Z _{OUT}	Closed-loop differential output impedance			0.2		Ω
DC PERFORMANCE						
A _{OL}	Open-loop gain		104	117		dB
V _{OS}	Input-referred offset voltage	V _{OS} = (V _{IN+} − V _{IN−})	−10	0.2	10	mV
ΔV _{OS} /ΔT _A	Input-referred offset voltage drift	T _A = −40°C to +125°C		1		μV/°C
I _{BN} , I _{BI}	Input bias current	Noninverting and inverting inputs		20		pA
I _{OS}	Input offset current	(I _{BN} − I _{BI})		±20		pA
INPUT						
	Differential input resistance	Effective shunt resistance between inputs		1		GΩ
	Common-mode input resistance	Effective shunt resistance to AC GND at each input		1		
	Differential input capacitance	Effective shunt capacitance between inputs		0.6		pF
	Common-mode input capacitance	Effective shunt capacitance to AC GND at each input		0.9		
CMRR	Common-mode rejection ratio	CMRR = (ΔV _{CM} /ΔV _{OS}). Inputs shifted ±500 mV around midsupply	70	80		dB
CMIR+	Common-mode input high	T _A = 25°C, A _{OL} > 90 dB	V _{S+} − 1.85	V _{S+} − 1.6		V
		T _A = −40°C to +125°C, A _{OL} > 90 dB		V _{S+} − 1.65		
CMIR−	Common-mode input low	T _A = 25°C, A _{OL} > 90 dB	V _{S−} + 0.2	V _{S−} − 0.2		V
		T _A = −40°C to +125°C, A _{OL} > 90 dB		V _{S−} − 0.1		

6.6 Electrical Characteristics: FDA operation, ICM loop disabled (continued)

$V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{OCM} = \text{Open}$, $V_{ICM} = \text{Open}$, $R_F = 5\text{ k}\Omega$, Gain = 10 V/V, ICM loop disabled (ICM_EN = -2.5 V), $R_L = 1\text{ k}\Omega$ and $T_A = 25^\circ\text{C}$. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Output voltage range to either supply	$R_L = 20\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, input driven to $\pm V_S/\text{Gain}$	$V_S - 0.125$	$V_S - 0.075$		V
	Output voltage range to either supply	$R_L = 20\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, V_{OS} shift < 150 μV from default offset	$V_S - 0.175$	$V_S - 0.125$		V
	Output voltage range to either supply	$R_L = 20\text{ k}\Omega$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, V_{OS} shift < 150 μV from default offset		$V_S - 0.175$		V
	Output voltage range to either supply	$R_L = 1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, V_{OS} shift < 150 μV from default offset	$V_S - 0.25$	$V_S - 0.2$		V
	Output voltage range to either supply	$R_L = 1\text{ k}\Omega$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, V_{OS} shift < 150 μV from default offset		$V_S - 0.25$		V
OUTPUT COMMON-MODE (VOCM) CONTROL						
	Output common-mode loop SSBW	VOCM ⁽³⁾ pin driven $\pm 0.5\text{ mV}$ around midsupply		5		MHz
	Output common-mode loop LSBW	VOCM pin driven $\pm 0.5\text{ V}$ around midsupply		4.5		MHz
$\Delta V_{OUT}/\Delta V_{OCM}$	DC output balance ⁽²⁾ ⁽³⁾	$V_{OCM} = \pm 1\text{ V}$		80		dB
$\Delta V_{OCM}/\Delta V_{OCM}$	Output common-mode gain ⁽³⁾	VOCM pin driven $\pm 1\text{ V}$ around midsupply	0.99	1	1.01	V/V
	Input DC bias current of VOCM pin	VOCM pin driven to midsupply		100		nA
	Input impedance of VOCM pin	VOCM pin driven $\pm 0.5\text{ mV}$ around midsupply		200 1		k Ω pF
	VOCM input pin voltage offset from mid-supply ⁽⁴⁾	VOCM pin open	-8	-2	4	mV
V_{OCM_OS}	Output common-mode voltage offset from midsupply	VOCM pin open	-30	± 2.5	30	mV
$\Delta V_{OCM_OS}/T_A$	Output common-mode voltage offset drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, VOCM pin open		-22		$\mu\text{V}/^\circ\text{C}$
V_{OCM_OS}	Output common-mode voltage offset from midsupply	VOCM pin driven to midsupply	-25	± 1.5	25	mV
$\Delta V_{OCM_OS}/T_A$	Output common-mode voltage offset drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, VOCM pin driven to midsupply		-18		$\mu\text{V}/^\circ\text{C}$
	VOCM input headroom to V_{S+}	$\leq \pm 10\text{ mV}$ shift from V_{OCM_OS}		0.9	1	V
	VOCM input headroom to V_{S+}	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $\leq \pm 10\text{ mV}$ shift from V_{OCM_OS}		1		V
	VOCM input headroom from V_{S-}	$\leq \pm 10\text{ mV}$ shift from V_{OCM_OS}		0.9	1	V
	VOCM input headroom from V_{S-}	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $\leq \pm 10\text{ mV}$ shift from V_{OCM_OS}		1		V
$\Delta V_{OCM_OS}/\Delta V_{S+}$	Positive power-supply rejection ratio	VOCM = 0 V (driven)		76		dB
$\Delta V_{OCM_OS}/\Delta V_{S-}$	Negative power-supply rejection ratio			80		

6.6 Electrical Characteristics: FDA operation, ICM loop disabled (continued)

$V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{OCM} = \text{Open}$, $V_{ICM} = \text{Open}$, $R_F = 5\text{ k}\Omega$, Gain = 10 V/V, ICM loop disabled ($ICM_EN = -2.5\text{ V}$), $R_L = 1\text{ k}\Omega$ and $T_A = 25^\circ\text{C}$. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SUPPLY							
I _Q	Quiescent current	T _A = 25°C	1.4	1.9	2.5	mA	
I _Q	Quiescent current	VICM loop enabled	1.5	2	2.7	mA	
I _Q	Disabled quiescent current	AMP_EN = V _{S−}	10	28	40	μA	
+PSRR	Power-supply rejection ratio to V _{S+}	VOCM is driven	70	94		dB	
−PSRR	Power-supply rejection ratio to V _{S−}	VOCM is driven	90	110		dB	
POWER DOWN							
V _{IH}	Enable voltage (Amplifier ON above this voltage)	AMP_EN and ICM_EN	V _{S+} − 0.7 V _{S+} − 0.5			V	
V _{IL}	Disable voltage threshold (Amplifier OFF below this voltage)		V _{S+} − 2 V _{S+} − 1.8				
I _{IH}	Control pin HIGH Input bias current	AMP_EN and ICM_EN driven to (V _{S+}) − 0.25 V	3.5			7	μA
	External pull-down current required to switch ON→OFF ⁽¹⁾		175				μA
I _{IL}	Control pin LOW Input bias current	AMP_EN and ICM_EN driven to V _{S−}	−5	−1.1			μA
t _{AMP_ON}	Turn-ON time delay (Main amplifier)	Time to V _{OUT} stabilized within 1% of the final value	1.5				μs
t _{AMP_OFF}	Turn-OFF time delay (Main amplifier)	Time to supply current ≤ 100 μA	0.9				μs

- (1) Leaving the AMP_EN pin floating is not recommended. When using a pull-up resistor ensure that the necessary bias current can be supplied.
- (2) V_{OUT} is the differential output voltage, $(V_{OUT-} - V_{OUT+})$.
- (3) VOCM refers to the voltage measured at pin 7. $V_{OCM} = [(V_{OUT+} + V_{OUT-})/2]$ refers to the average output voltage.
- (4) The offset between the voltage measured at the VOCM pin and the midsupply voltage.

6.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V

V_{S+} = 2.5 V, V_{S-} = –2.5 V, V_{OCM} = open, V_{ICM} = open, R_F = 5 k Ω , G = 10 V/V, ICM loop disabled, R_L = 1 k Ω , single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).

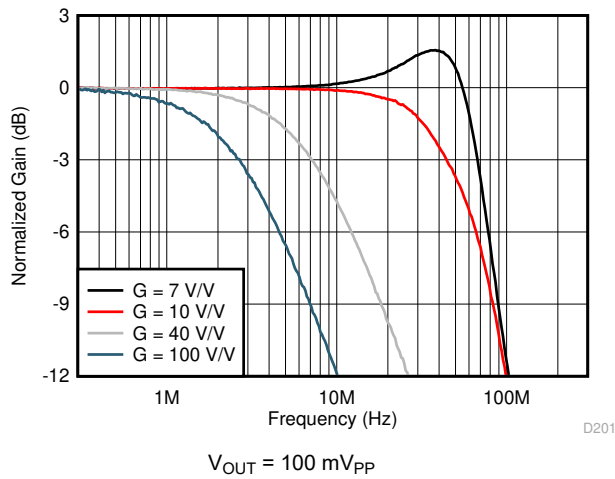


Figure 6-1. Small-Signal Frequency Response vs Gain

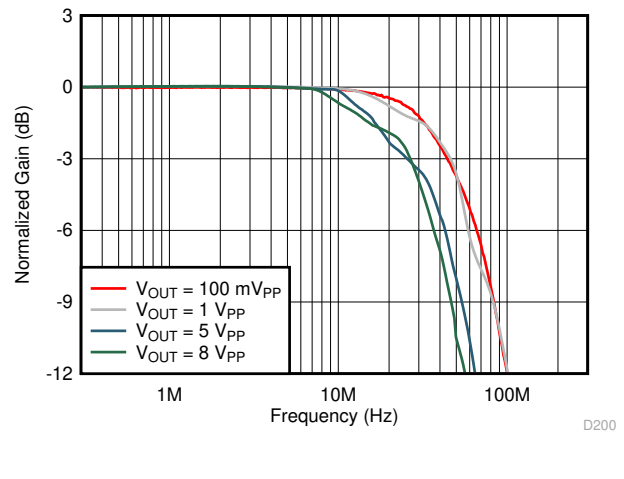


Figure 6-2. Frequency Response vs V_{OUT}

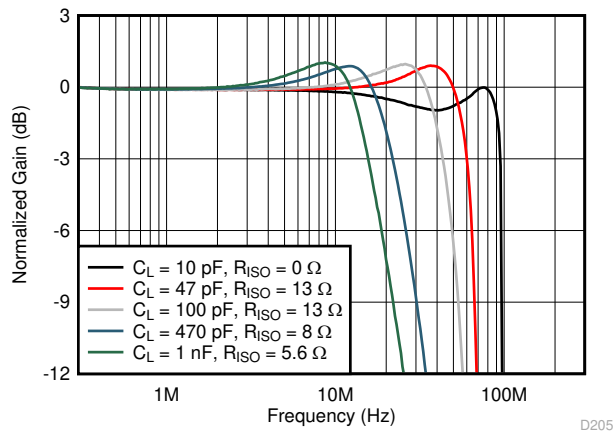


Figure 6-3. Small-Signal Frequency Response vs C_L

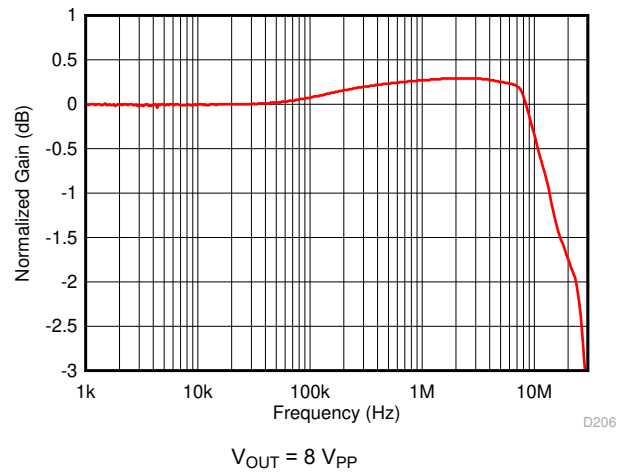


Figure 6-4. Large-Signal Frequency Response Flatness

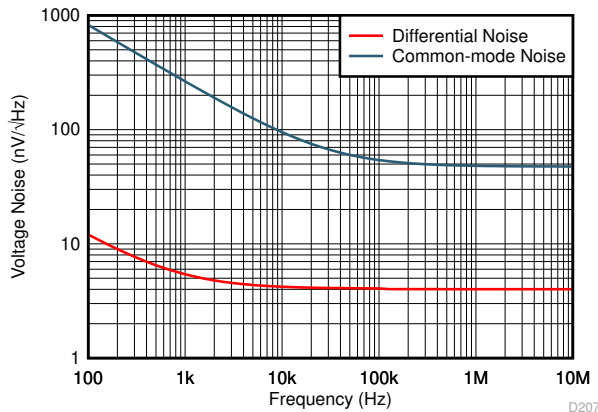


Figure 6-5. Input Referred Voltage Noise vs Frequency

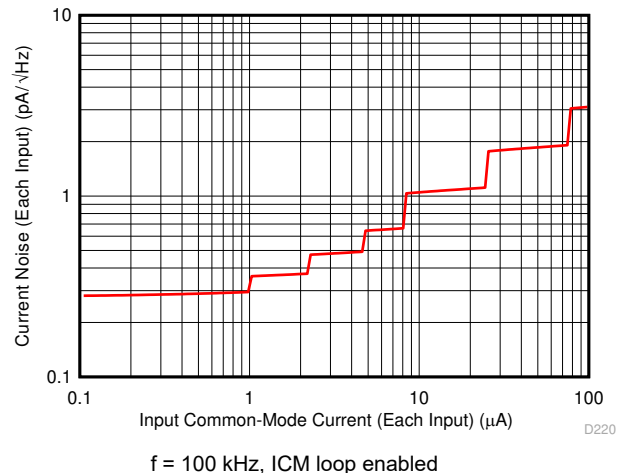


Figure 6-6. Input Referred Current Noise vs I_{CM_CTL}

6.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V (continued)

V_{S+} = 2.5 V, V_{S-} = -2.5 V, V_{OCM} = open, V_{ICM} = open, R_F = 5 k Ω , G = 10 V/V, ICM loop disabled, R_L = 1 k Ω , single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).

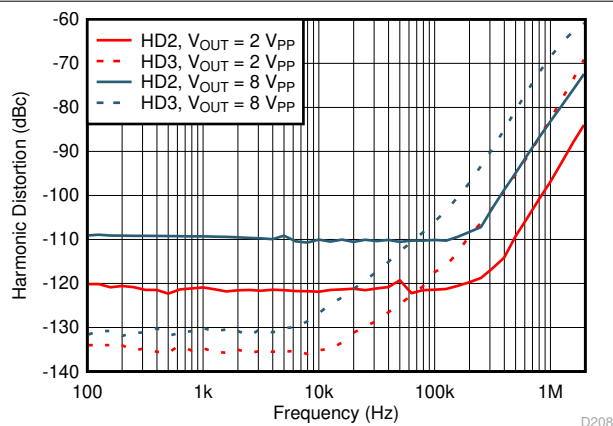


Figure 6-7. Harmonic Distortion vs Frequency

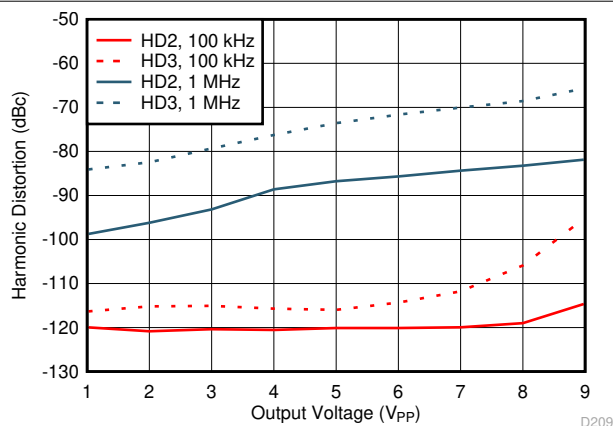


Figure 6-8. Harmonic Distortion vs V_{OUT}

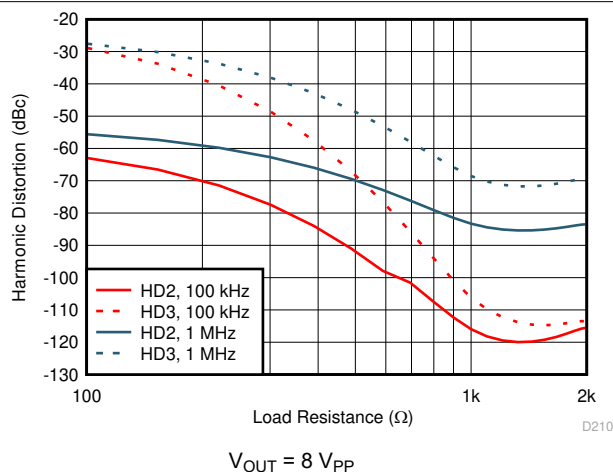


Figure 6-9. Harmonic Distortion vs R_L

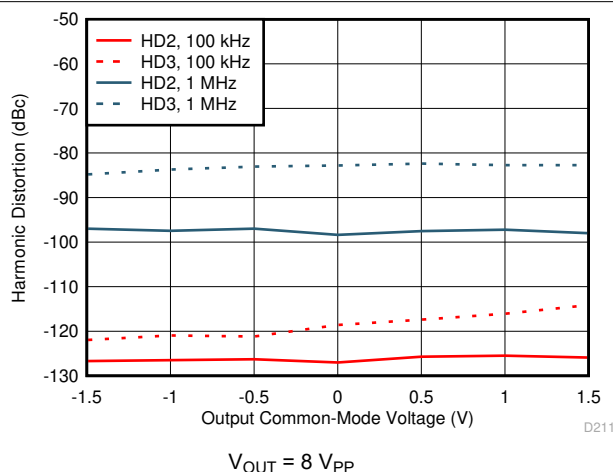


Figure 6-10. Harmonic Distortion vs V_{OCM}

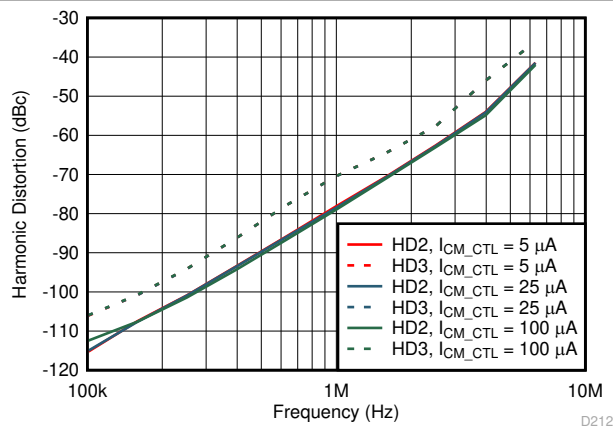


Figure 6-11. Harmonic Distortion vs I_{CM_CTL}

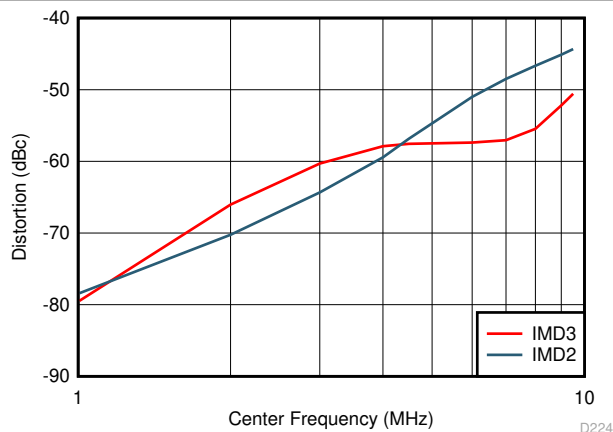
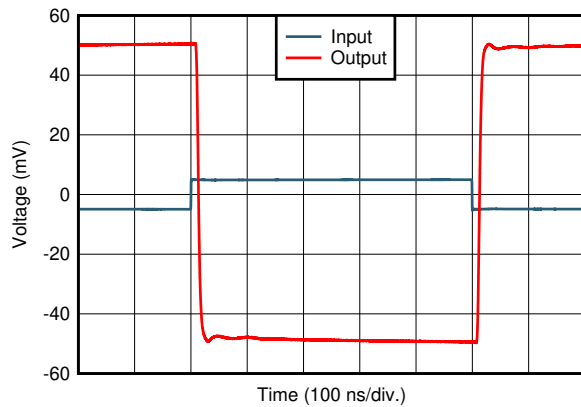


Figure 6-12. Intermodulation Distortion vs Frequency

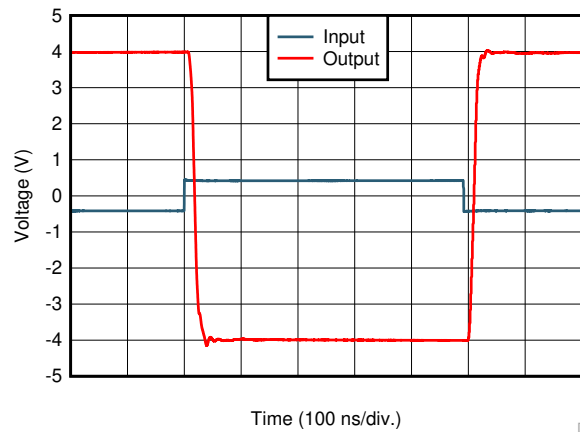
6.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V (continued)

V_{S+} = 2.5 V, V_{S-} = –2.5 V, V_{OCM} = open, V_{ICM} = open, R_F = 5 k Ω , G = 10 V/V, ICM loop disabled, R_L = 1 k Ω , single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).



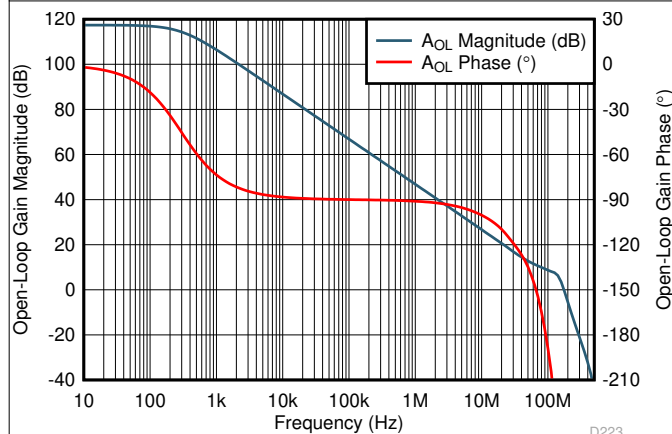
D213

Figure 6-13. Small-Signal Transient Response



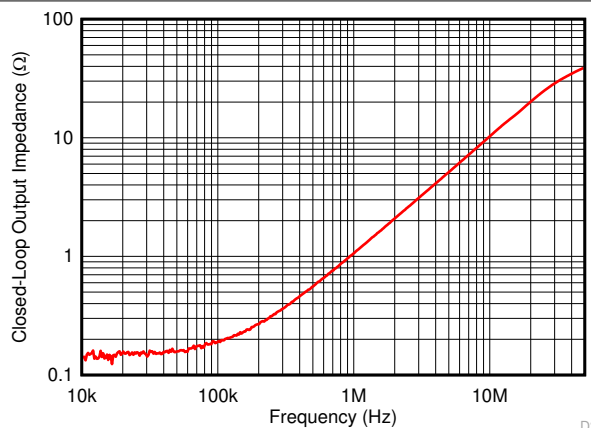
D214

Figure 6-14. Large-Signal Transient Response



D223

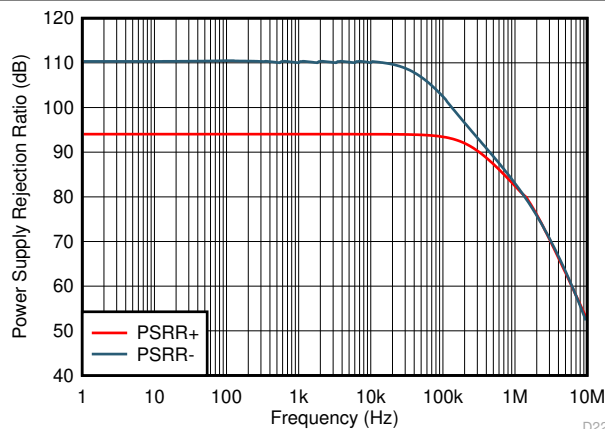
Figure 6-15. Open-Loop Gain



D215

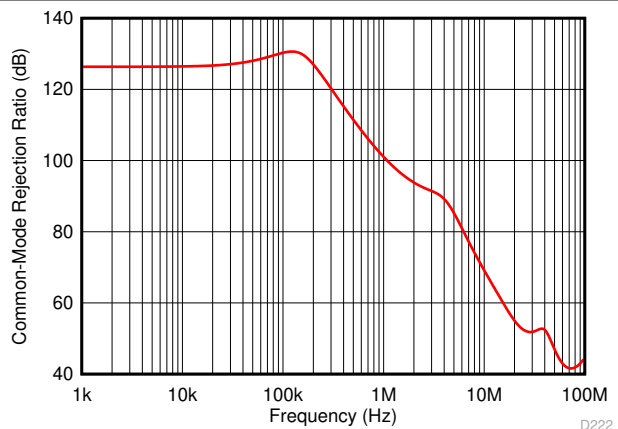
$G = 1$ V/V, $V_{OUT} = 2$ V_{PP}, with V_{OCM} adjusted

Figure 6-16. Closed-Loop Output Impedance vs Frequency



D221

Figure 6-17. Power-Supply Rejection Ratio vs Frequency

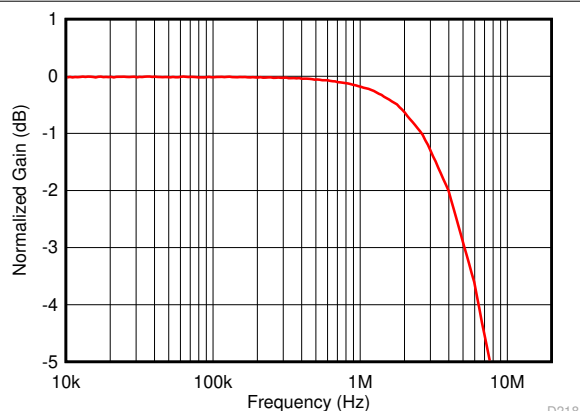


D222

Figure 6-18. Common-Mode Rejection Ratio vs Frequency

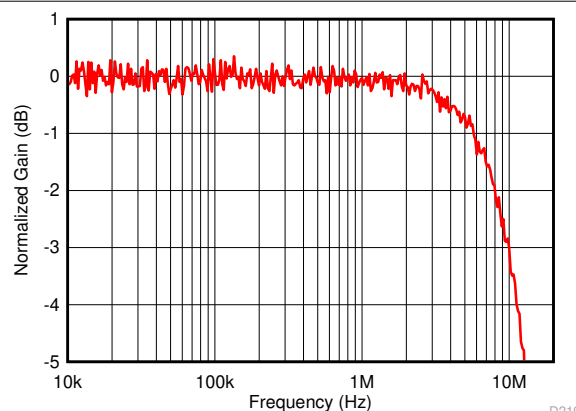
6.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V (continued)

V_{S+} = 2.5 V, V_{S-} = -2.5 V, V_{OCM} = open, V_{ICM} = open, R_F = 5 k Ω , G = 10 V/V, ICM loop disabled, R_L = 1 k Ω , single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).



VOCM pin driven with 100 mV_{PP} signal. Average output voltage measured.

Figure 6-19. VOCM Loop Small-Signal Frequency Response



VICM pin driven with 100 mV_{PP} signal. Average input voltage measured.

Figure 6-20. VICM Loop Small-Signal Frequency Response

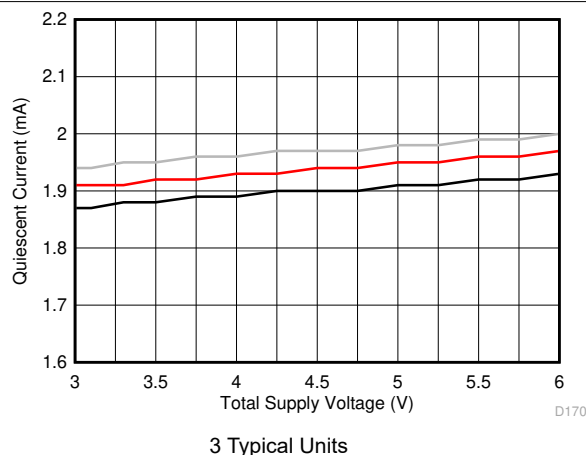


Figure 6-21. Quiescent Current vs Total Supply Voltage

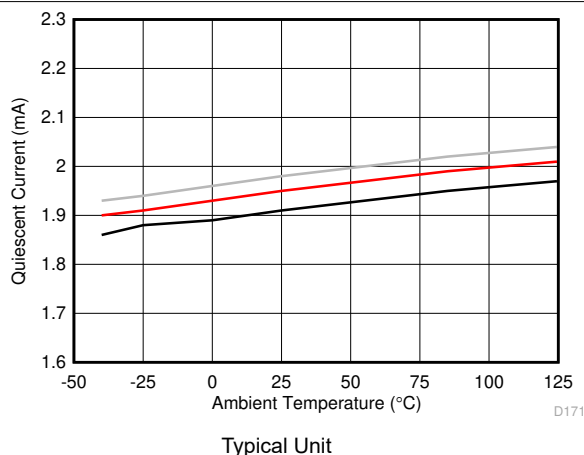


Figure 6-22. Quiescent Current vs Ambient Temperature

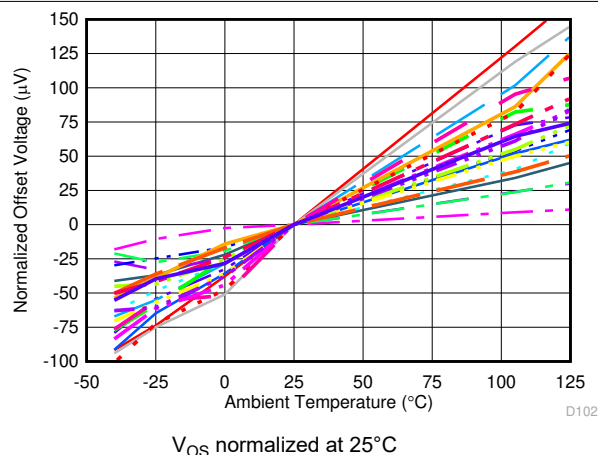


Figure 6-23. Offset Voltage vs Ambient Temperature

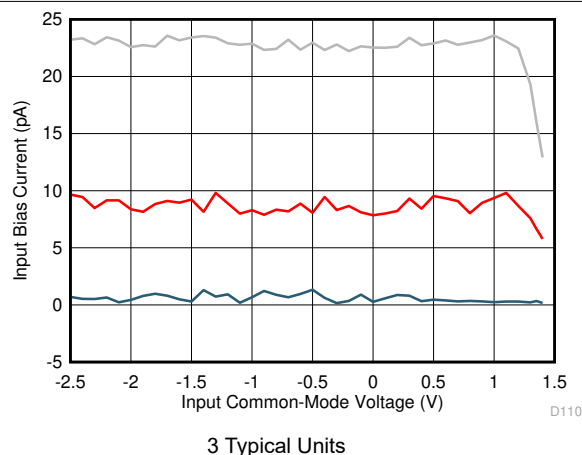


Figure 6-24. Input Bias Current vs Input Common-Mode Voltage

6.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V (continued)

V_{S+} = 2.5 V, V_{S-} = -2.5 V, V_{OCM} = open, V_{ICM} = open, R_F = 5 k Ω , G = 10 V/V, ICM loop disabled, R_L = 1 k Ω , single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).

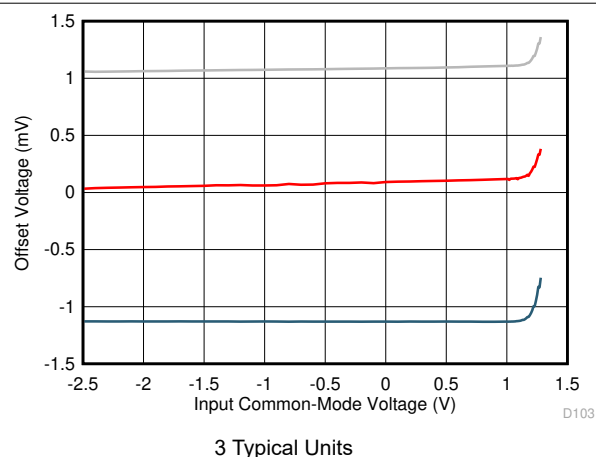


Figure 6-25. Offset Voltage vs Input Common-Mode Voltage

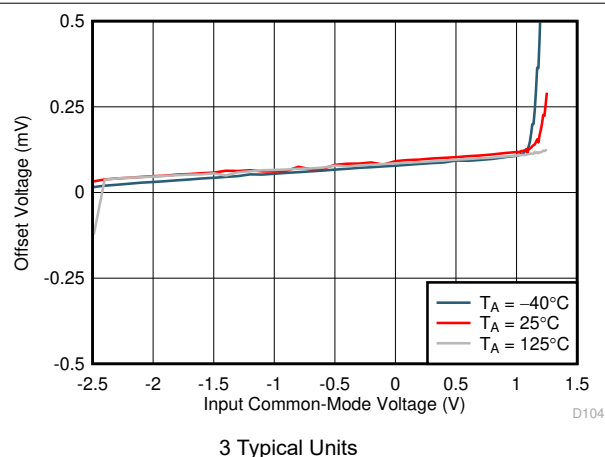


Figure 6-26. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature

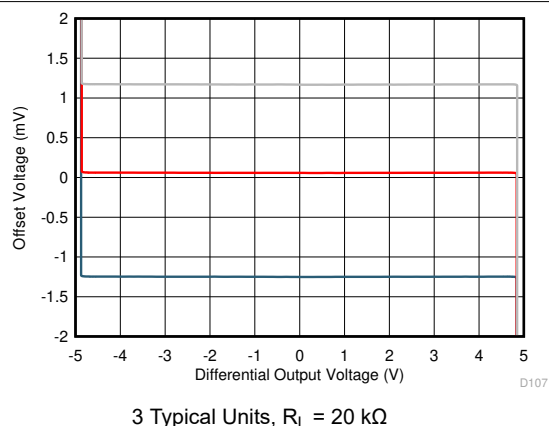


Figure 6-27. Offset Voltage vs Differential Output Voltage

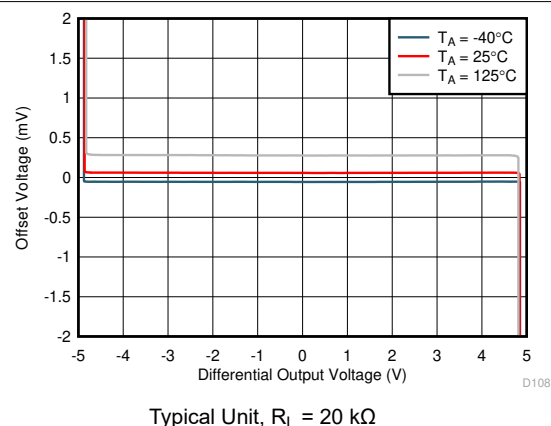


Figure 6-28. Offset Voltage vs Differential Output Voltage vs Ambient Temperature

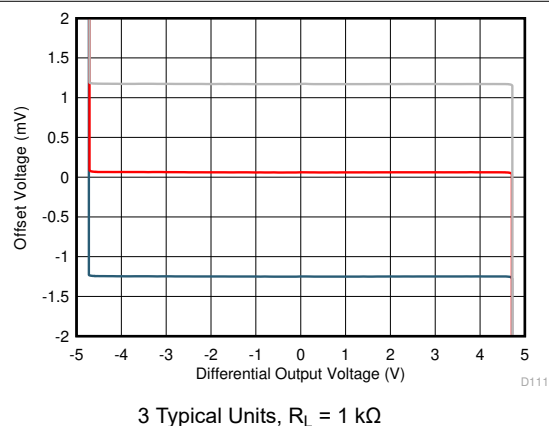


Figure 6-29. Offset Voltage vs Differential Output Voltage

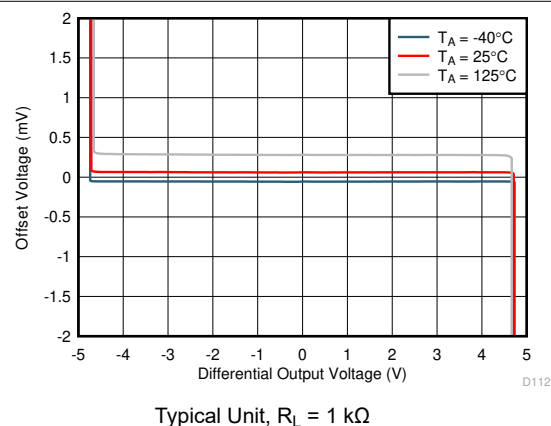


Figure 6-30. Offset Voltage vs Differential Output Voltage vs Ambient Temperature

6.7 Typical Characteristics: $(V_{S+}) - (V_{S-}) = 5\text{ V}$ (continued)

$V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{OCM} = \text{open}$, $V_{ICM} = \text{open}$, $R_F = 5\text{ k}\Omega$, $G = 10\text{ V/V}$, ICM loop disabled, $R_L = 1\text{ k}\Omega$, single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).

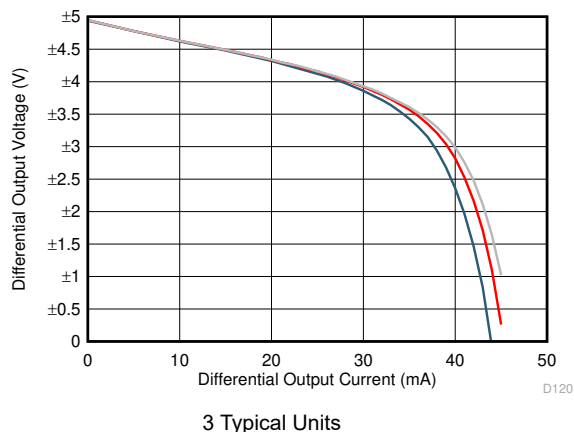


Figure 6-31. Differential Output Voltage vs Load Current

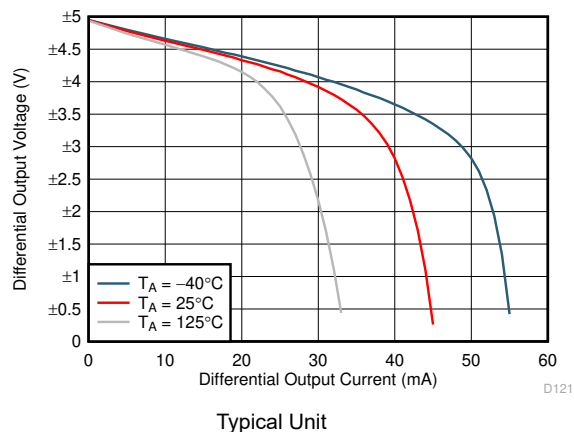


Figure 6-32. Differential Output Voltage vs Load Current vs Ambient Temperature

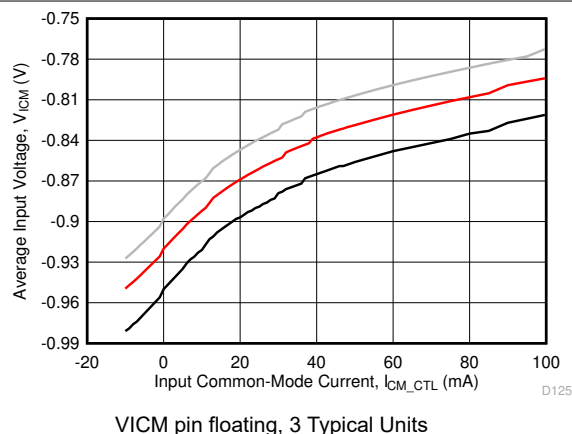


Figure 6-33. Average Input Voltage vs Input Common-Mode Current

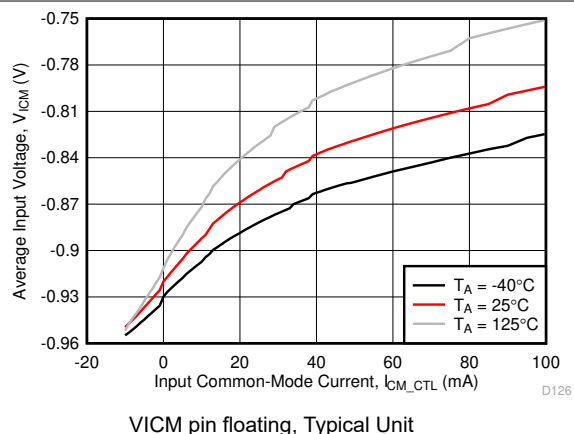


Figure 6-34. Average Input Voltage vs Input Common-Mode Current vs Ambient Temperature

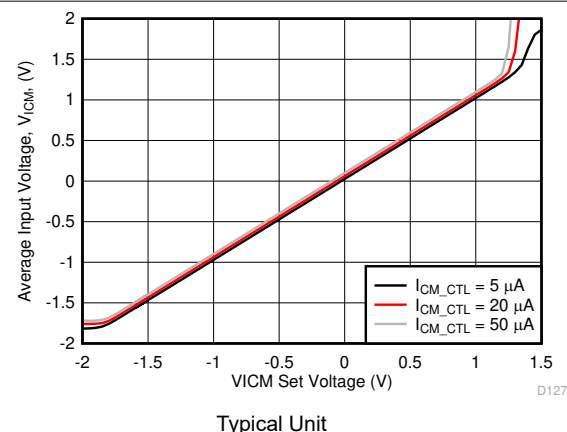


Figure 6-35. Average Input Voltage vs VICM Set Voltage

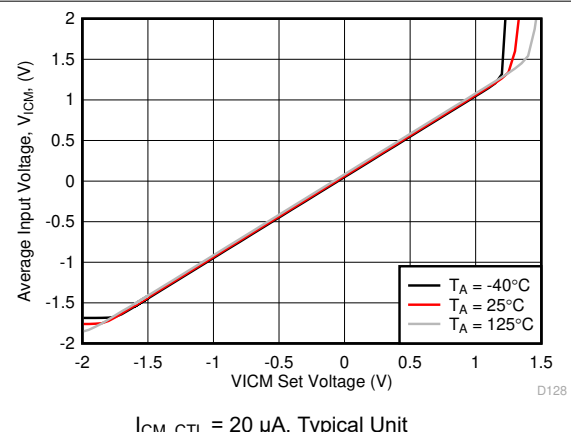
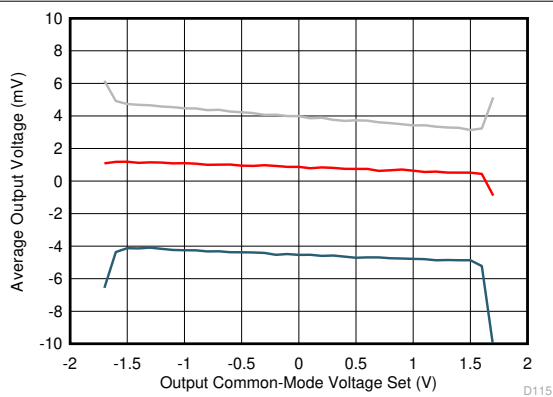


Figure 6-36. Average Input Voltage vs VICM Set Voltage vs Ambient Temperature

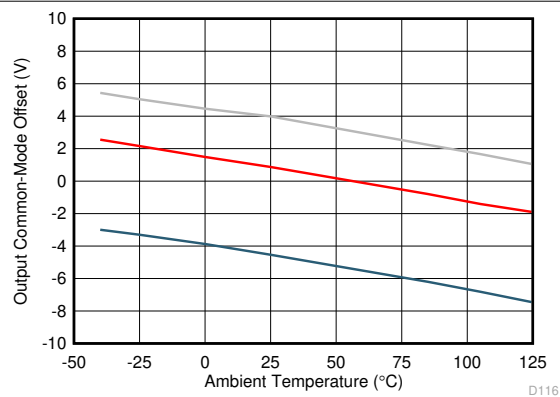
6.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V (continued)

V_{S+} = 2.5 V, V_{S-} = –2.5 V, V_{OCM} = open, V_{ICM} = open, R_F = 5 k Ω , G = 10 V/V, ICM loop disabled, R_L = 1 k Ω , single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25^\circ\text{C}$, 1 (unless otherwise noted).



V_{OCM} offset = (V_{OCM} - V_{OCM}), 3 Typical Units

Figure 6-37. Output Common-Mode Offset Voltage vs Output Common-Mode Set Voltage



V_{OCM} = 0 V, 3 Typical Units

Figure 6-38. Output Common-Mode Offset Voltage vs Ambient Temperature

7 Detailed Description

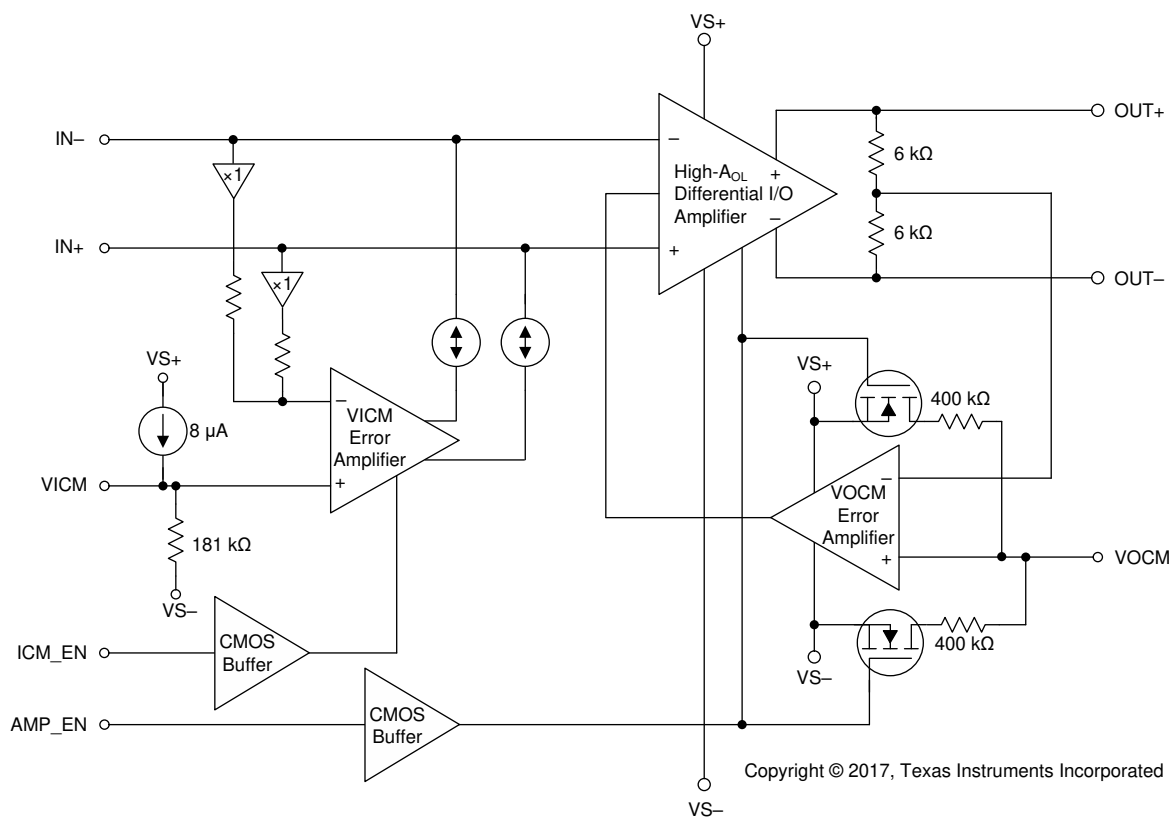
7.1 Overview

The THS4567 device is a unique fully differential amplifier that features an input common-mode control loop in addition to the output common-mode control loop typically found in all fully differential amplifiers. The THS4567 device has a high impedance CMOS input stage with a very low input bias current. The independent input and output common-mode control along with the high impedance CMOS inputs make the THS4567 device an ideal high-gain, low-noise, fully-differential transimpedance amplifier.

The input common-mode loop of the THS4567 device may be disabled by setting the ICM_EN pin below its turnoff threshold voltage, turning it into a standard fully differential amplifier with output common-mode control only. The THS4567 device operates over a wide power supply voltage range from 3.3 V to 5.5 V, which makes this device an excellent choice for driving differential ADCs and buffering DAC outputs.

This device features a low-power mode with a unique active pullup resistor that improves EMI reliability of the shutdown pin when left floating. The AMP_EN and ICM_EN pins draw very little bias current when the logic voltage is outside the switching threshold region. Within the switching threshold region, the bias current increases, especially close to the transition region. The increased bias current prevents the logic from inadvertently switching in the presence of EMI.

7.2 Functional Block Diagram



7.3 Feature Description

The THS4567 architecture features three main building blocks:

1. A high open loop gain differential I/O main amplifier.
2. An output common-mode control error amplifier that sets the common-mode of the differential outputs of the main amplifier.
3. An input common-mode control error amplifier that sets the common-mode of the differential inputs of the main amplifier, independent of the output common-mode.

7.3.1 Main Amplifier

The main differential I/O amplifier has a wide gain bandwidth product of 220 MHz and is stable in gain configurations > 10 V/V. [Figure 6-15](#) shows the open-loop response of the main amplifier. The main amplifier has a high-impedance CMOS input stage with very low input bias currents, which makes it ideal for use in high-gain transimpedance systems or as a voltage amplifier with large feedback and gain resistors.

7.3.2 Output Common-Mode Control

The output common-mode loop works by sensing the average voltage between the two outputs of the main amplifier through the two 6-k Ω internal resistors in [Section 7.2](#) and comparing it against the voltage at the V_{OCM} pin. The V_{OCM} error amplifier then adjusts the internal bias of the main amplifier to minimize the error voltage between its input pins. The voltage at the V_{OCM} node defaults to midsupply through the two 400-k Ω internal bias string resistors between V_{S+} and V_{S-}. When using the V_{OCM} at its default voltage, connect an external capacitor to the V_{OCM} pin to bypass the noise from the internal 400-k Ω resistors. When the amplifier is disabled, the default midsupply bias string is disabled to save power. The THS4567 device output common-mode can also be set by driving the V_{OCM} pin externally through a low output impedance source. Ensure that the source is capable of driving the input impedance of the V_{OCM} pin.

7.3.3 Input Common-Mode Control

The THS4567 device features a unique input common-mode control error amplifier that sets the input common-mode voltage independent of the output common-mode voltage. The V_{ICM} error amplifier works by sensing the average voltage at the main amplifiers inputs and then sourcing or sinking an equal amount of current into both the input nodes of the main amplifier to maintain the input common-mode voltage equal to voltage at the V_{ICM} pin. If the V_{ICM} pin is left floating, its input voltage defaults to 1.5-V above V_{S-}. This voltage is set by the combination of the 8- μ A current source and the 181-k Ω resistor shown in [Section 7.2](#). When using the V_{ICM} at its default voltage, connect an external capacitor to the V_{ICM} pin to bypass the noise from the internal 181-k Ω resistor. The V_{ICM} voltage can be set to an arbitrary value by driving the V_{ICM} pin externally through a low output impedance source. The input common-mode control loop can be disabled by setting I_{CM_EN} pin low. With the input common-mode loop disabled the THS4567 device behaves like a standard fully-differential amplifier (FDA).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

For proper shutdown mode operation, the amplifier enable (AMP_EN) pin must be asserted to the desired voltage. An internal pullup resistor is provided on the AMP_EN pin so that if the pin is floated, then the device defaults to an ON state. For applications that require the device to be constantly powered on when the supplies are present, tie the AMP_EN pin to the positive supply voltage (VS+).

The disable operation is referenced from the positive supply. For an OFF state condition, the disable control pin must be 2 V below the positive supply.

7.4.2 Differential Transimpedance Amplifier Mode

The primary use case of the input common-mode control loop is in differential transimpedance amplifier applications where two photodiodes are excited by a differential input. Any ambient light that is incident on both photodiodes will produce a DC offset current which is subsequently rejected by the input common-mode loop. The input common-mode loop enables the use of very high feedback resistors to amplify the differential photodiode current while simultaneously rejecting common-mode currents. Disabling the input common-mode loop allows the common-mode current to flow through the feedback resistors thereby reducing the effective output swing for the differential signal component. The THS4567 device can reject sourcing or sinking photodiode currents.

The high impedance CMOS inputs of the THS4567 device minimizes the amplifiers input current noise enabling the use of very high transimpedance gains ($>100\text{ k}\Omega$), while the low input voltage noise maximizes the system signal-to-noise ratio (SNR). The high gain bandwidth product of the THS4567 device allows it be used as a single-stage differential transimpedance amplifier while driving a high performance ADC driver.

7.4.3 Fully Differential Amplifier (FDA) Mode

With the input common-mode loop disabled, the THS4567 device behaves like a standard FDA. It can convert a single-ended input signal to a differential output or a differential input to a differential output with independent output common-mode control. For a detailed understanding of FDA operation check out the [training video](#).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Noise Analysis

To simplify the noise calculation of an FDA configured as a TIA, split the circuit into two identical halves and treat each half as an independent op amp circuit. The noise of an op amp configured as a TIA is shown in [Transimpedance Considerations for High-Speed Amplifiers](#) and is repeated in [Equation 1](#). The equivalent noise circuit is shown in [Figure 8-1](#). The amplifiers voltage noise e_{NOP} in [Figure 8-1](#) is the specified input-referred voltage noise of the THS4567 (e_N) divided by 1.414. This method enables us to analyze the FDA as two identical and uncorrelated halves. The total noise of the FDA is the total noise of each half multiplied by 1.414.

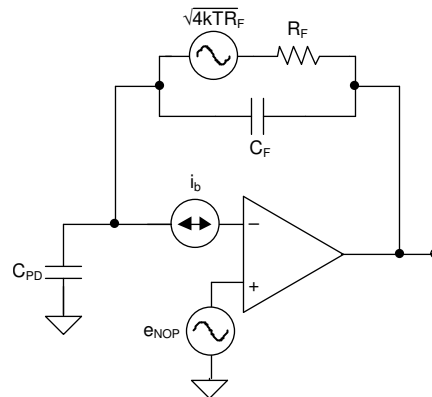


Figure 8-1. Transimpedance Amplifier Noise Analysis Circuit

To minimize the total noise of a TIA the circuit designer should:

1. Minimize the current noise of the op amp (i_b). Since the THS4567 device has CMOS inputs its current noise contribution can be ignored.
2. Maximize the transimpedance gain (R_F).
3. Minimize the amplifiers voltage noise (e_N). The THS4567 possesses a class leading 4.2 nV/ $\sqrt{\text{Hz}}$ of broadband voltage noise while consuming less than 2.5 mA of quiescent current.
4. Minimize the photodiode capacitance (C_{PD}).

The capacitance of a photodiode can be minimized by increasing its reverse bias. The THS4567 input and output common-mode can be independently controlled. The independent control feature allows the circuit designer to set photodiode's anode close to the negative supply voltage while tying its cathode close to the positive supply voltage to maximize the reverse bias across the photodiode. The output common-mode is then set to match the next stage ADCs input common-mode range. In a standard op amp TIA, the input common-mode is biased close to the positive supply to maximize the output swing of the amplifier. This bias configuration limits the reverse bias across the photodiode thereby increasing its input capacitance. The THS4567 device is optimized to reduce total system noise by optimizing the noise source from each contributing source in [Equation 1](#).

$$i_{EQ} = \sqrt{i_b^2 + \frac{4kT}{R_F} + \left[\left(\frac{e_n}{R_F} \right)^2 + \frac{(e_n \cdot 2\pi \cdot F \cdot C_s)^2}{3} \right]} / 2 \quad (1)$$

where

- i_b = current noise of the THS4567 device
- $4kT = 16 \times 10^{-21} \text{J}$ at 290 degrees Kelvin
- R_F = feedback resistor
- e_n = voltage noise of the THS4567 device
- C_s = total input capacitance from the THS4567, photodiode and any PCB parasitics
- F = noise integration frequency limit

8.2 Typical Application

The primary use case for the THS4567 input common-mode loop is in differential transimpedance applications that have a large common-mode offset due to ambient light. In this section we compare the performance of the THS4567 device with the input common-mode loop enabled (TIA mode) as shown in [Figure 8-2](#) versus a differential TIA implementation built using two discrete op amp channels (OPA mode) as shown in [Figure 8-3](#).

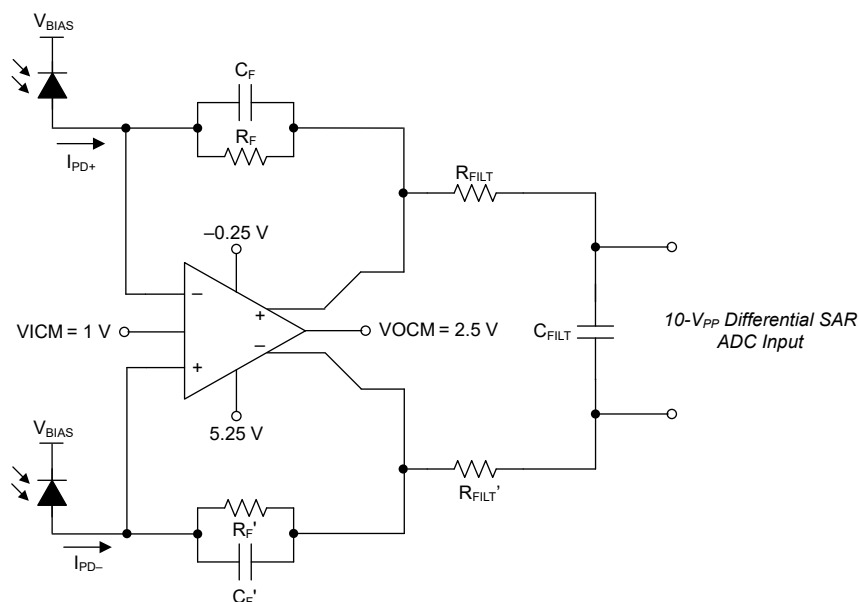


Figure 8-2. THS4567 with Integrated Differential TIA + ADC Driver

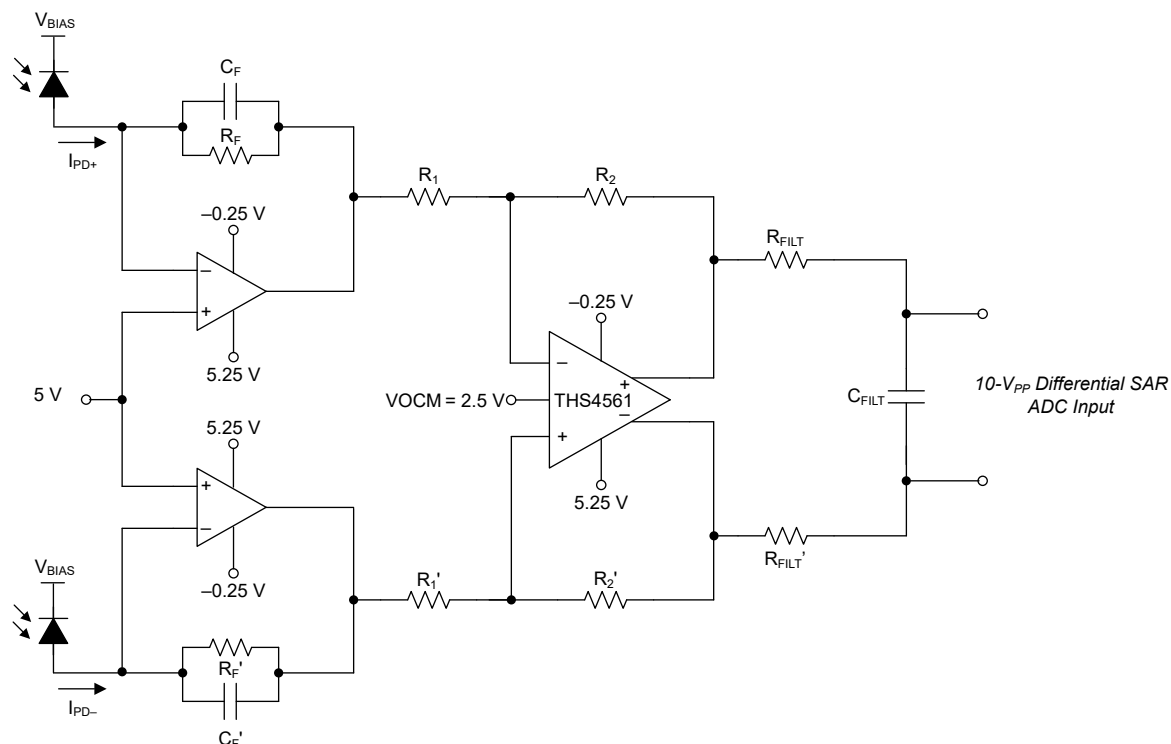


Figure 8-3. Discrete Differential Op Amp TIA + 2nd Stage ADC Driver

8.2.1 Design Requirements

The requirements for this application are:

- Supply voltage: 5.5 V
- ADC full-scale range: 10 V_{PP} differential
- ADC input common-mode voltage: 2.5 V
- Ambient light current offset (DC): 10 μA
- Single-sided signal current: 5 μA_{PP} (each photodiode). Differential signal current = 10 μA_{PP}
- Input signal frequency: 100 kHz

8.2.2 Detailed Design Procedure (THS4567 in TIA Mode)

The output current from each photodiode is shown in [Figure 8-4](#). A detailed procedure on how to set the various bias voltages and select the optimal value of transimpedance gain follows.

- Set $V_{S+} = 5.25\text{ V}$ and $V_{S-} = -0.25\text{ V}$ to allow the THS4567 to swing 10 V_{PP} (differential) without introducing distortion due to limited headroom.
- Set ICM_EN = logic high to enable the THS4567 TIA mode of operation.
- Set V_{OCM} to 2.5 V to match the ADC input common-mode range.
- With the photodiodes (PDs) configured with a cathode bias as shown in [Figure 8-2](#) both PDs will source current when light is incident on them. To maximize the reverse bias across the PD, V_{BIAS} is typically set to the amplifiers positive supply voltage or the highest available positive supply voltage.
- The maximum output current from the PD is the sum of the ambient light current and the maximum signal current.

$$I_{TOTAL} = I_{AMBIENT} + I_{SIGNAL} = 10\text{ }\mu\text{A} + 5\text{ }\mu\text{A} = 15\text{ }\mu\text{A} \quad (2)$$

- In the TIA mode, V_{ICM} is set to its minimum input common-mode compliance limit (1.25 V) to maximize the reverse bias across the PDs thereby reducing the PD capacitance.

$$\text{Reverse bias across the photodiodes} = (5.25\text{ V} - 1.25\text{ V}) = 4\text{ V} \quad (3)$$

- In the TIA mode, the ICM loop cancels the common-mode input current due to ambient light ($10\text{ }\mu\text{A}$) at the amplifier's input pin and only the differential signal current flows through the feedback resistors R_F and R_F' . The maximum TIA gain is therefore the ratio of the maximum differential output swing and the maximum differential signal current as shown in [Equation 4](#).

$$\text{Maximum TIA gain} = (10\text{ V}_{PP} / 10\text{ }\mu\text{A}) = 1\text{ M}\Omega \quad (4)$$

- Once the feedback resistor value is set, select the value of feedback capacitance as described in [Transimpedance Considerations for High-Speed Amplifiers](#).

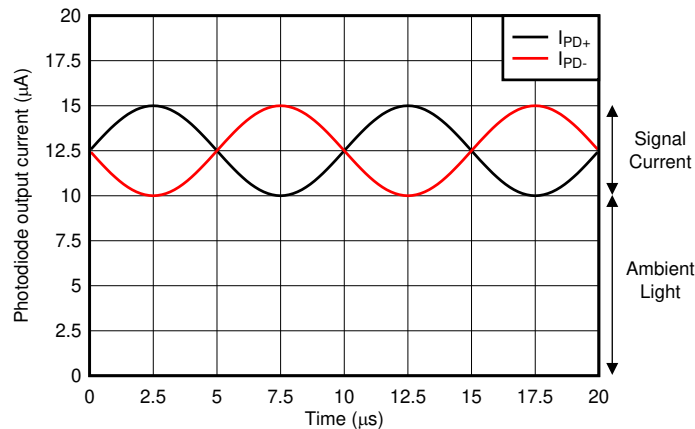


Figure 8-4. Photodiode Differential Output Current

8.2.2.1 OPA Mode Configuration

The OPA mode configuration is shown in [Figure 8-3](#). This configuration results in a reverse bias of $(5.25\text{ V} - 5\text{ V}) = 0.25\text{ V}$ across the PD thereby greatly increasing the PD capacitance compared to the TIA mode.

In the OPA mode there is no input common-mode current cancellation so the maximum value of feedback resistance (R_F , R_F') is the ratio of the maximum single-ended output swing and the maximum single-ended input current as shown in [Equation 5](#).

$$\text{Maximum TIA gain} = (5\text{ V}/15\text{ }\mu\text{A}) = 333.33\text{ k}\Omega \quad (5)$$

The total differential swing is $333.33\text{ k}\Omega \times 10\text{ }\mu\text{A}_{PP} = 3.33\text{ V}$. To maximize the ADC gain range a subsequent amplifier gain stage is needed. The second gain stage which is typically implemented with a standard FDA like the [THS4561](#) will also adjust the output common-mode to match the ADCs input common-mode compliance range.

As the level of ambient light increases relative to the differential signal from the PD, the maximum gain configuration in the OPA mode will decrease while it stays constant for the THS4567 TIA mode.

8.2.3 Application Curves

[Figure 8-5](#) shows the output of the THS4567 device in TIA mode. The output common-mode is centered on $V_{OCM} = 2.5\text{ V}$ and the differential output of 10 V_{PP} maximizes the subsequent ADCs entire common-mode range.

[Figure 8-6](#) shows the output of the first stage transimpedance amplifier setup shown in [Figure 8-3](#). The output common-mode is centered on 0.83 V . The offset in the common-mode is caused by the offset due to the ambient light. More importantly the differential output swing is only 3.33 V . To maximize the ADC dynamic range the subsequent THS4561 differential amplifier stage is configured in a signal gain of 3 V/V . The THS4561 device will also perform a level shift to center the output common-mode to 2.5 V .

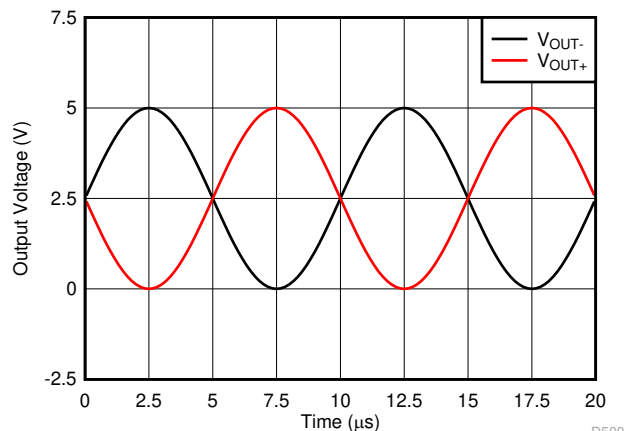


Figure 8-5. Output of THS4567 (TIA Mode)

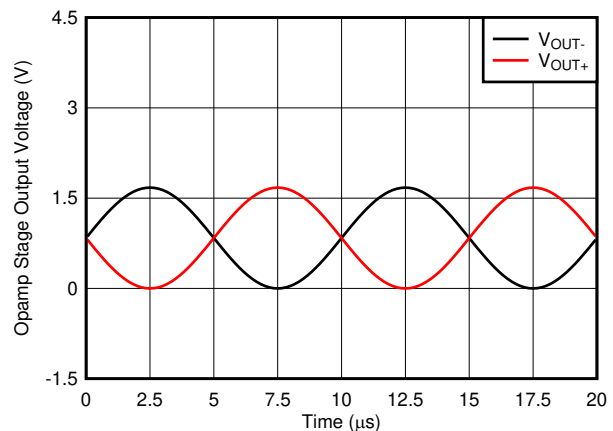


Figure 8-6. Output of the 1st Stage Discrete Op Amp Transimpedance Amplifier (OPA Mode)

The noise performance of the THS4567 device (half-circuit) is then compared against the noise of the [OPA607](#) and the [OPA365](#) in OPA mode. Using [Equation 1](#) we can estimate the total input referred spot noise for the THS4567 device. [Transimpedance Considerations for High-Speed Amplifiers](#) is used to estimate the noise of the OPA607 and OPA365 transimpedance amplifier stage in OPA mode.

A PD capacitance of 5 pF is assumed. In a real world system the PD capacitance will be higher in OPA mode because of the lower reverse bias across the PD. The calculated noise results are shown in [Table 8-1](#) where the benefit of the THS4567 device can clearly be seen. The spot noise has been normalized to the closed loop bandwidth. The OPA mode architecture would require a second gain stage to maximize the ADCs input full scale range. The second stage would increase the power consumption and degrade the noise.

Table 8-1. Noise Comparison

Amplifier Specification	THS4567	OPA607	OPA365
Photodiode Capacitance (pF)	5	5	5
Amplifier Input Capacitance (pF)	1	17	8
Amplifier Voltage Noise (nV/ $\sqrt{\text{Hz}}$)	4.2	3.8	4.5
TIA Gain (k Ω)	1000	333.33	333.33
Closed Loop Bandwidth (MHz)	2.4	1	1.4
Input-Referred Spot Noise (pA/ $\sqrt{\text{Hz}}$)	0.2	0.39	0.36

8.3 Differential TIA with 0-V Biased Photodiode

The circuit in [Figure 8-7](#) can be used for a differential TIA with 0-V reverse bias across the photodiode. The VICM loop should be disabled in this configuration since the loop can only source or sink DC current. Any DC current generated by the photodiode in the configuration shown will be differential in nature.

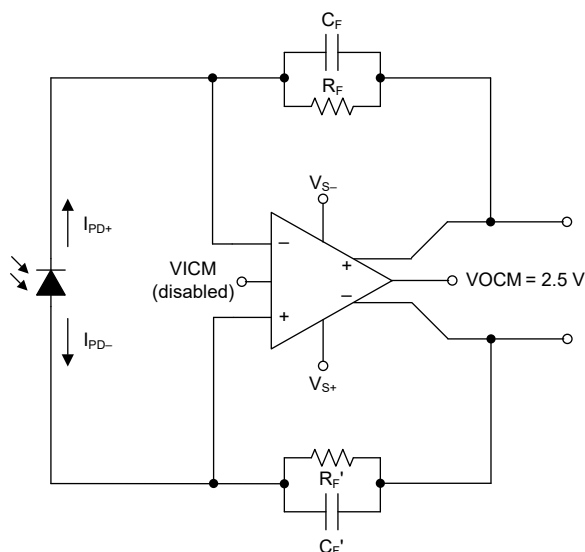


Figure 8-7. Differential TIA with 0-V Biased Photodiode

8.4 Differential AC Coupled TIA

The circuit in Figure 8-8 can be used as a differential AC-coupled TIA with variable reverse bias across the photodiode. Since no DC current flows in the feedback network due to the AC coupling the VICM loop can be disabled.

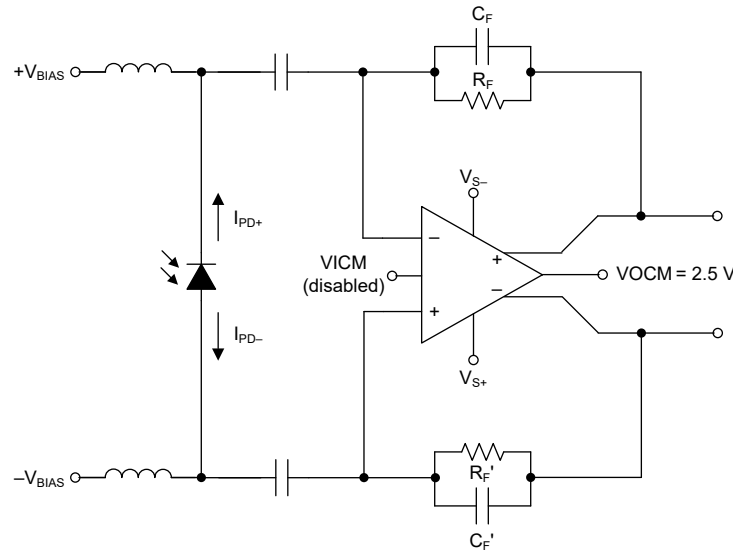


Figure 8-8. Differential AC Coupled TIA

9 Power Supply Recommendations

The THS4567 device is principally intended to operate with a nominal single-supply voltage of 3.3 V to 5.5 V. Split (or bipolar) supplies can be used with the THS4567 device, as long as the total value across the device remains less than 5.5 V. A low power-supply source impedance must be maintained across frequency so use multiple bypass capacitors in parallel. Place the bypass capacitors as close to the supply pins as possible. Place the smallest capacitor ($< 10\text{ nF}$) on the same side of the PCB as the THS4567 device. Larger capacitors ($> 1\text{ }\mu\text{F}$) can be placed further away and shared among different devices in the system.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.01 μF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 μF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- The THS4567 outputs are sensitive to capacitive loading. Isolate the output of the THS4567 from any capacitive load by placing series isolation resistors close to the amplifiers output pins.

10.2 Layout Example

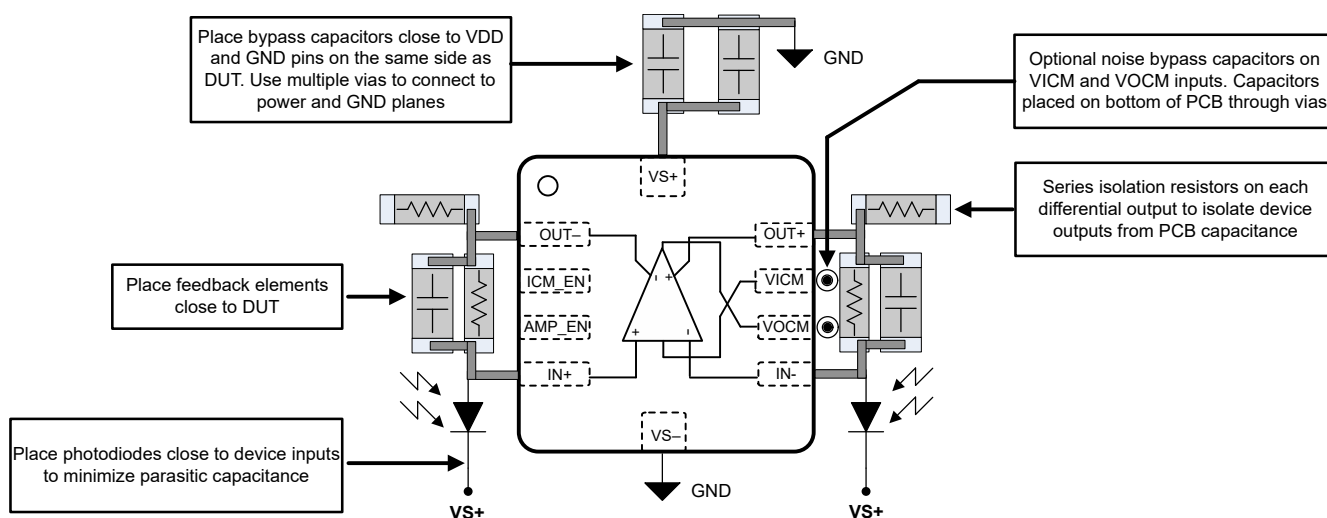


Figure 10-1. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [RUN_FDA_4567 EVM user's guide](#)
- Texas Instruments, [Fully-Differential Amplifiers application note](#)
- Texas Instruments, [Fully Differential Amplifiers TI Precision Labs](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4567IRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SN67	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

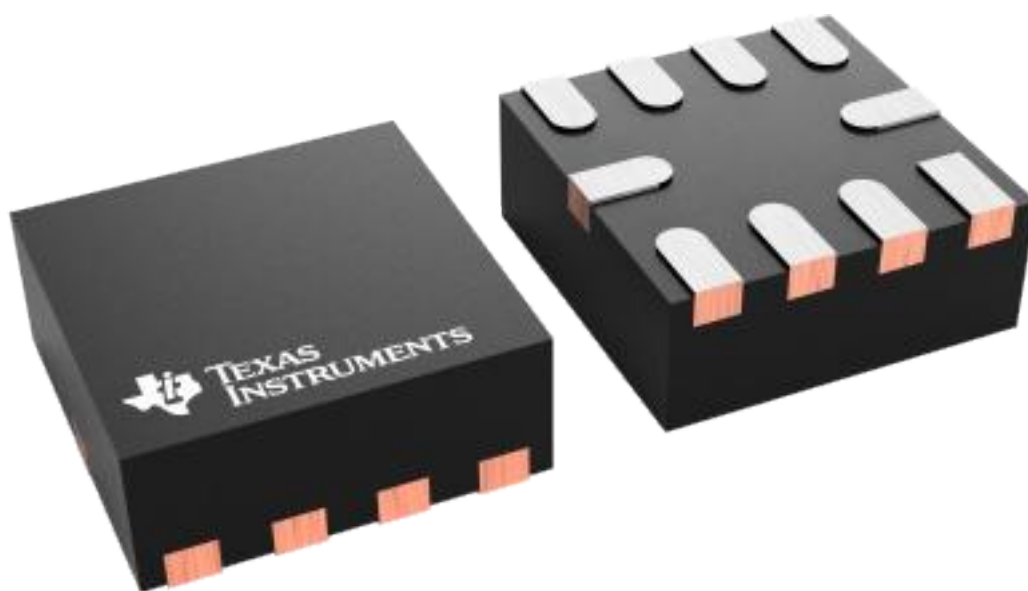
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228249/A



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

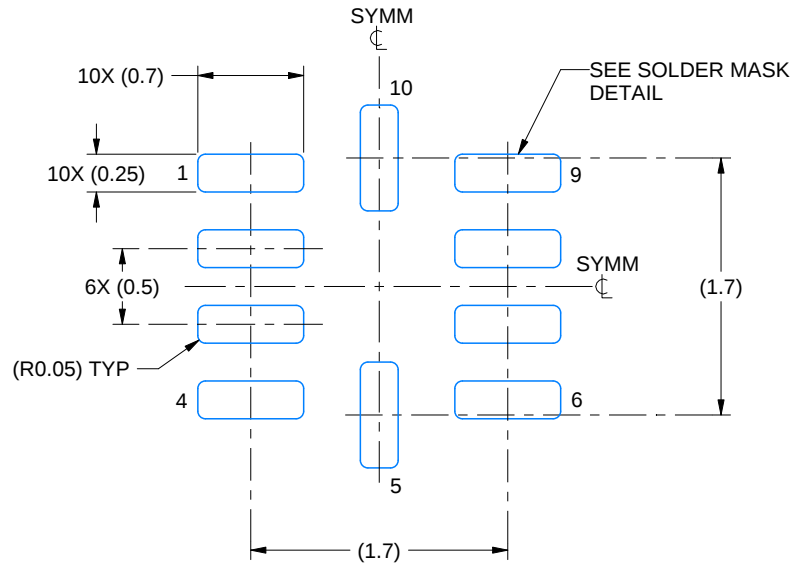
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

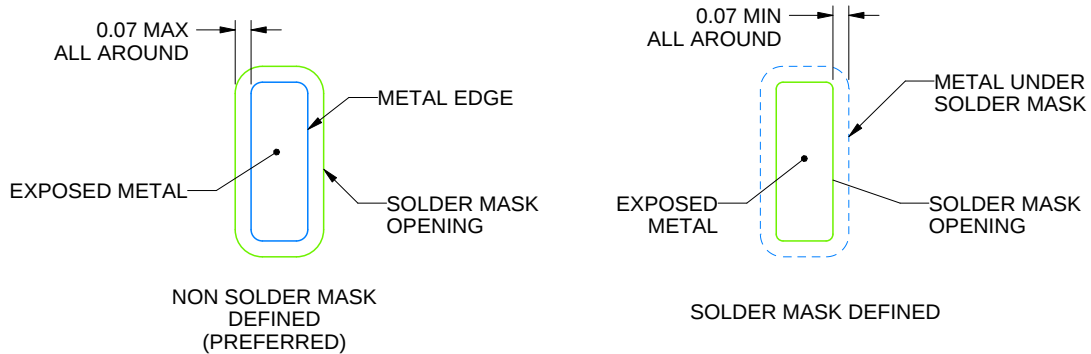
RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

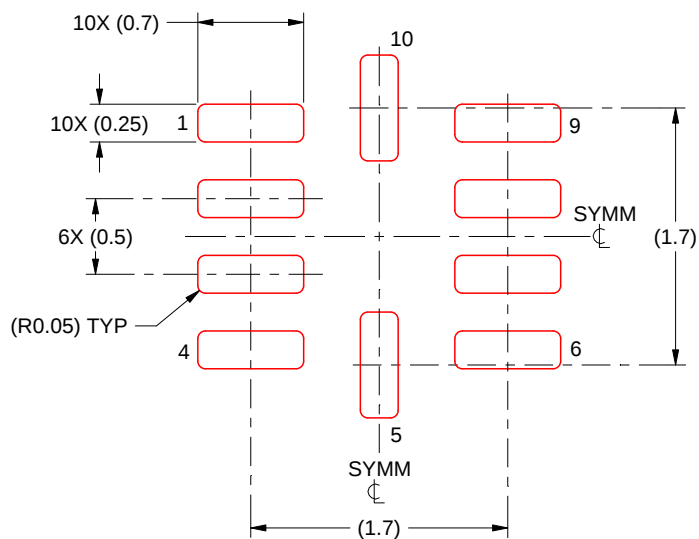
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated