TEXAS INSTRUMENTS

TL071, TL071A, TL071B
TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL072M, TL074M
ZHCSHV5N – SEPTEMBER 1978 – REVISED JULY 2017

TL07xx 低噪声 JFET 输入运算放大器

1 特性

- 低功耗
- 宽共模和差分电压范围
- 低输入偏置和失调电流
- 输出短路保护
- 低总谐波失真：0.003%（典型值）
- 低噪声
  V_n = 18nV/√Hz（典型值，f = 1kHz）
- 高输入阻抗：JFET 输入级
- 内部频率补偿
- 无锁存运行
- 高压摆率：13V/μs（典型值）
- 共模输入电压范围
  包括 V_{CC+}

2 应用

- 电机集成系统：UPS
- 驱动器和控制解决方案：交流逆变器和变频驱动器
- 可再生能源：光伏逆变器
- 专业音频混合器
- DLP 正投影系统
- 示波器

3 说明

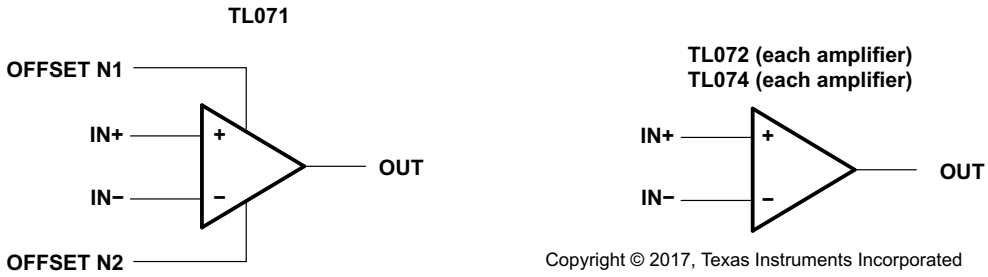
TL07xx JFET 输入运算放大器在单片集成电路中集成了匹配良好的高压 JFET 和双极晶体管。这些器件具有高压摆率、低输入偏置和失调电流以及低失调电压温度系数。TL07x 系列的低谐波失真和低噪声等特性使其非常适合用于高保真和音频前置放大器 应用。TL071 器件具有失调引脚以支持外部输入失调校正。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TL07xxD	SOIC (14)	8.65mm x 3.91mm
	SOIC (8)	4.90mm x 3.90mm
TL07xxJG	CDIP (8)	9.59mm x 6.67mm
TL074xJ	CDIP (14)	19.56mm × 6.92mm
TL07xxP	PDIP (8)	9.59mm x 6.35mm
TL07xxPS	SO (8)	6.20mm x 5.30mm
TL074xN	PDIP (14)	19.3mm × 6.35mm
TL074xNS	SO (14)	10.30mm × 5.30mm
TL07xxPW	TSSOP (8)	4.40mm x 3.00mm
TL074xPW	TSSOP (14)	5.00 mm × 4.40 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑符号



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision M (February 2014) to Revision N **Page**

- 根据最新文档和翻译标准更新了数据表文本 ... 1
- 已添加 在数据表中添加 TL072M 和 TL074M 器件 ... 1
- 重写以下部分的文本：*说明*部分 ... 1
- 已更改 将*器件信息* 表中的 TL07x 8 引脚 PDIP 封装更改为 8 引脚 CDIP 封装 ... 1
- 已删除 *器件信息* 表中的 20 引脚 LCCC 封装 ... 1
- 已添加 在首页原理图中添加 2017 年版权声明 ... 1
- Deleted *引脚配置和功能* 部分的 TL071x FK (LCCC) 引脚图和引脚表 ... 4
- 更新了*引脚配置和功能* 部分的引脚图和引脚表 ... 5
- Deleted *绝对最大额定值* 表中的不同输入电压参数 ... 10
- Deleted *绝对最大额定值* 表的表注 ... 10
- Added 为*绝对最大额定值* 表添加新的表注 ... 10
- Changed 将*绝对最大额定值* 表中的最小电源电压值从 –18V 更改为 –0.3V ... 10
- Changed 将*绝对最大额定值* 表中的最大电源电压从 18V 更改为 36V ... 10
- Changed 将最小输入电压值从 –15V 更改为 $V_{CC–}$ – 0.3V（*绝对最大额定值* 表） ... 10
- Changed 将最大输入电压从 15V 更改为 $V_{CC–}$ + 36V（*绝对最大额定值* 表） ... 10
- Added 在*绝对最大额定值* 表中添加输入钳位电流参数 ... 10
- Changed 将共模电压最大值从 V_{CC+} – 4V 更改为 V_{CC+}（*建议运行条件* 表） ... 10
- Changed 将*建议运行条件* 表中的器件从 TL07xA 和 TL07xB 更改为 TL07xAC 和 TL07xBC ... 10
- Added 在*建议运行条件* 表中添加 TL07xI 自然通风工作温度最小值 –40°C ... 10
- Added 将 U (CFP) 封装热指标值添加到*热性能信息：TL072x（续）* 表 ... 11

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修订历史记录 (接下页)

- Added 将 W (CFP) 封装热指标值添加到*热性能信息：TL074x（续）* 表 12
- 已添加 图 20 至 表 1 20
- 已添加 图 20 至*典型特性* 部分 23
- 已添加 *典型应用* 部分的第二条应用曲线 29
- 调整*布局指南* 部分的文档参考的格式 32
- 更新*相关文档* 部分的文档参考的格式 34

Changes from Revision L (February 2014) to Revision M — Page

- 添加了*器件信息* 表、*引脚配置和功能* 部分、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分 1
- 将*典型特性* 移入*规格* 部分。 20

Changes from Revision K (January 2014) to Revision L — Page

- 将 T_{stg} 移到*处理额定值* 表 10
- 添加了*器件和文档支持* 部分 34
- 添加了*机械、封装和可订购信息* 部分 34

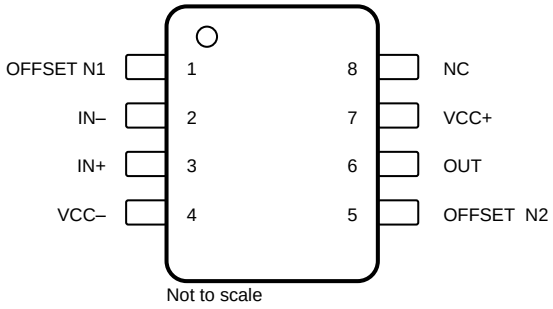
Changes from Revision J (March 2005) to Revision K — Page

- 根据新的 TI 数据表格式更新文档 - 无规格变化。 1
- 添加了 ESD 警告 34

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5 引脚配置和功能

TL071x D、P 和 PS 封装
8 引脚 SOIC、PDIP、SO
俯视图



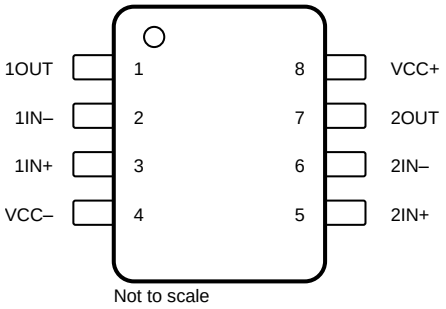
NC = 无内部连接

引脚功能：TL071x

引脚		I/O	说明
名称	编号		
IN–	2	I	反相输入
IN+	3	I	同相输入
NC	8	—	不连接
OFFSET N1	1	—	输入失调电压调节
OFFSET N2	5	—	输入失调电压调节
OUT	6	O	Output
VCC–	4	—	电源
VCC+	7	—	电源

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TL072x D、JG、P、PS 和 PW 封装
8 引脚 SOIC、CDIP、PDIP、SO
俯视图



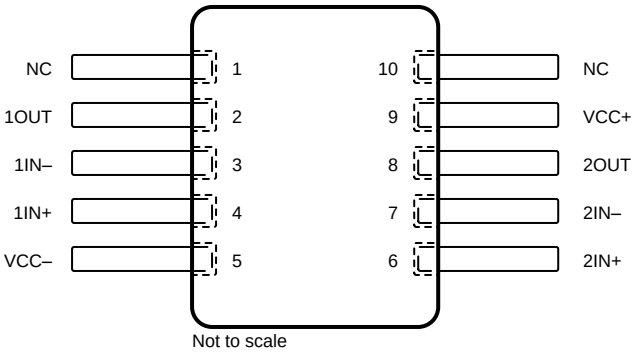
Not to scale

SOT-23 的: TL072x

引脚		I/O	说明
名称	编号		
1IN–	2	I	反相输入
1IN+	3	I	同相输入
1OUT	1	O	Output
2IN–	6	I	反相输入
2IN+	5	I	同相输入
2OUT	7	O	Output
VCC–	4	—	电源
VCC+	8	—	电源

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TL072x U 封装
10 引脚 CFP
俯视图



Not to scale

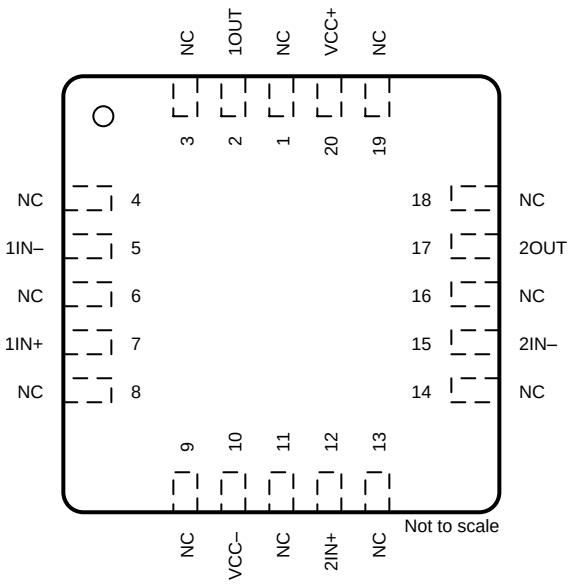
NC = 无内部连接

引脚功能：TL072x

引脚		I/O	说明
名称	编号		
1IN–	3	I	反相输入
1IN+	4	I	同相输入
1OUT	2	O	Output
2IN–	7	I	反相输入
2IN+	6	I	同相输入
2OUT	8	O	Output
NC	1, 10	—	不连接
VCC–	5	—	电源
VCC+	9	—	电源

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TL072 FK 封装
20 引脚 LCCC
俯视图



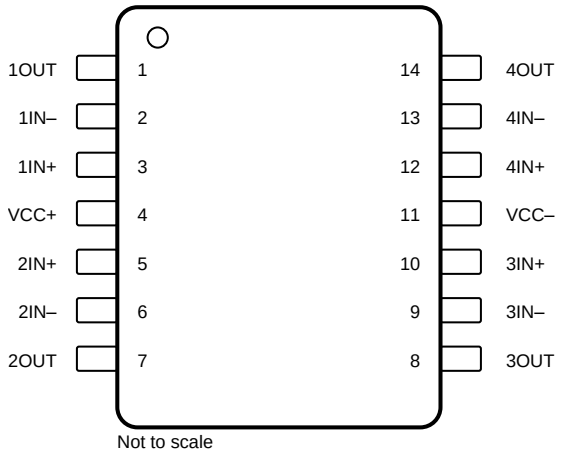
NC = 无内部连接

引脚功能：TL072x

引脚		I/O	说明
名称	编号		
1IN–	5	I	反相输入
1IN+	7	I	同相输入
1OUT	2	O	Output
2IN–	15	I	反相输入
2IN+	12	I	同相输入
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	不连接
VCC–	10	—	电源
VCC+	20	—	电源

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TL074 D、N、NS、PW、J 和 W 封装
14 引脚 SOIC、PDIP、SO、TSSOP、CDIP 和 CFP
俯视图



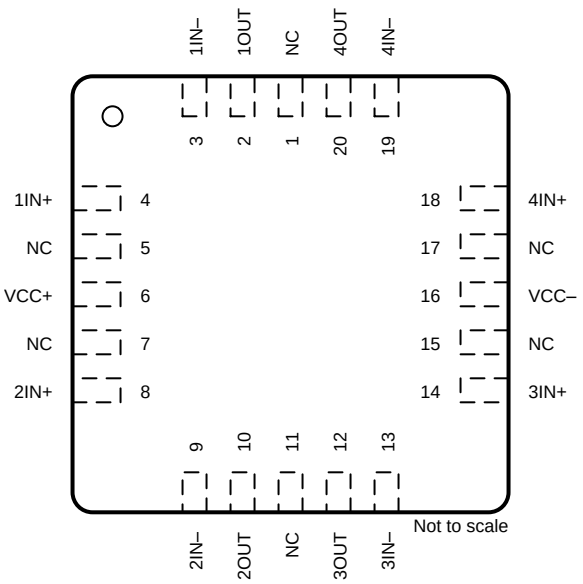
Not to scale

SOT-23 的: TL074x

引脚		I/O	说明
名称	编号		
1IN–	2	I	反相输入
1IN+	3	I	同相输入
1OUT	1	O	Output
2IN–	6	I	反相输入
2IN+	5	I	同相输入
2OUT	7	O	Output
3IN–	9	I	反相输入
3IN+	10	I	同相输入
3OUT	8	O	Output
4IN–	13	I	反相输入
4IN+	12	I	同相输入
4OUT	14	O	Output
$V_{CC–}$	11	—	电源
V_{CC+}	4	—	电源

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TL074 FK 封装
20 引脚 LCCC
俯视图



NC = 无内部连接

引脚功能：TL074x

引脚		I/O	说明
名称	编号		
1IN–	3	I	反相输入
1IN+	4	I	同相输入
1OUT	2	O	Output
2IN–	9	I	反相输入
2IN+	8	I	同相输入
2OUT	10	O	Output
3IN–	13	I	反相输入
3IN+	14	I	同相输入
3OUT	12	O	Output
4IN–	19	I	反相输入
4IN+	18	I	同相输入
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	不连接
VCC–	16	—	电源
VCC+	6	—	电源

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6 规格

6.1 绝对最大额定值

在自然通风温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
V_{CC+} - $V_{CC–}$	电源电压	–0.3	36	V
V_I	输入电压(2)	$V_{CC–}$ – 0.3	$V_{CC–}$ + 36	V
I_{IK}	输入钳位电流		-50	mA
	输出短路持续时间(3)	无限		
T_J	工作等效结温温度		150	°C
	60 秒内的外壳温度 - FK 封装		260	°C
	10 秒内距离外壳 1.8mm（1/16 英寸）的引线温度		300	°C
T_{stg}	贮存温度	-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些仅为在应力额定值下的工作情况，对于额定值下的器件的功能性操作以及在超出*推荐的操作条件*下的任何其它操作，在此并未说明。长时间处于最大绝对额定情况下会影响设备的可靠性。
(2) 差分电压仅受输入电压限制。
(3) 输出端可能短路至接地端或任一电源。必须限制温度和电源电压以确保不超过额定功耗。

6.2 ESD 额定值

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文档 JEP155 规定：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在自然通风温度范围内测得（除非另有说明）

			最小值	最大值	单位
V_{CC+}	电源电压 (1)		5	15	V
$V_{CC–}$	电源电压 (1)		–5	-15	V
V_{CM}	共模电压		$V_{CC–}$ + 4	V_{CC+}	V
T_A	自然通风工作温度范围	TL07xM	–55	125	°C
		TL08xQ	-40	125	
		TL07xI	-40	85	
		TL07xAC、TL07xBC、TL07xC	0	70	

(1) V_{CC+} 和 $V_{CC–}$ 不要求具有相同的幅度，只要总 V_{CC} (V_{CC+} – $V_{CC–}$) 介于 10V 与 30V 之间即可。

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6.4 热性能信息：TL071x

热指标(1)		TL071x			单位
		D (SOIC)	P (PDIP)	PS (SO)	
		8 引脚	8 引脚	8 引脚	
$R_{\theta JA}$	结至环境热阻	97	85	95	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	—	—	—	°C/W

(1) 有关传统和最新热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

6.5 热性能信息：TL072x

热指标(1)		TL072x				单位
		D (SOIC)	JG (CDIP)	P (PDIP)	PS (SO)	
		8 引脚	8 引脚	8 引脚	8 引脚	
$R_{\theta JA}$	结至环境热阻	97	—	85	95	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	—	15.05	—	—	°C/W

(1) 有关传统和最新热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

6.6 热性能信息：TL072x（续）

热指标(1)		TL072x			单位
		PW (TSSOP)	U (CFP)	FK (LCCC)	
		8 引脚	10 引脚	20 引脚	
$R_{\theta JA}$	结至环境热阻	150	169.8	—	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	—	62.1	5.61	°C/W
$R_{\theta JB}$	结至电路板热阻	—	176.2	—	°C/W
ψ_{JT}	结至顶部特征参数	—	48.4	—	°C/W
ψ_{JB}	结至电路板特征参数	—	144.1	—	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	—	5.4	—	°C/W

(1) 有关传统和最新热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

6.7 热性能信息：TL074x

热指标(1)		TL074x			单位
		D (SOIC)	N (PDIP)	NS (SO)	
		14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	86	80	76	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	—	—	—	°C/W

(1) 有关传统和最新热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

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6.8 热性能信息：TL074x（续）

热指标(1)		TL074x			单位
		J (CDIP)	PW (TSSOP)	W (CFP)	
		14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	—	113	128.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	14.5	—	56.1	°C/W
$R_{\theta JB}$	结至电路板热阻	—	—	127.6	°C/W
ψ_{JT}	结至顶部特征参数	—	—	29	°C/W
ψ_{JB}	结至电路板特征参数	—	—	106.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	—	—	0.5	°C/W

(1) 有关传统和最新热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

6.9 热性能信息：TL074x（续）

热指标(1)		TL074x	单位
		FK (LCCC)	
		20 引脚	
$R_{\theta JA}$	结至环境热阻	—	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	5.61	°C/W

(1) 有关传统和最新热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

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6.10 电气特性：TL071C、TL072C、TL074C

$V_{CC±}$ = ±15V（除非另有说明）

参数		测试条件 (1) (2)		最小值	典型值	最大值	单位
V_{IO}	输入失调电压	V_O = 0 R_S = 50Ω	T_A = 25°C		3	10	mV
			T_A = 完整范围			13	
α	输入失调电压的温度系数	V_O = 0 R_S = 50Ω	T_A = 完整范围		18		μV/°C
I_{IO}	输入失调电流	V_O = 0	T_A = 25°C		5	100	pA
			T_A = 完整范围			10	nA
I_{IB}	输入偏置电流 (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = 完整范围			7	nA
V_{ICR}	共模输入电压范围	T_A = 25°C		±11	–12 至 15		V
V_{OM}	最大峰值输出电压摆幅	R_L = 10kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10kΩ	T_A = 完整范围	±12			
		R_L ≥ 2kΩ		±10			
A_{VD}	大信号差分电压放大	V_O = ±10V R_L ≥ 2kΩ	T_A = 25°C	25	200		V/mV
			T_A = 完整范围	15			
B_1	单位增益带宽	T_A = 25°C			3		MHz
r_I	输入电阻	T_A = 25°C			10^{12}		Ω
CMRR	共模抑制比	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50Ω	T_A = 25°C	70	100		dB
k_{SVR}	电源电压抑制比 ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9V 至 ±15V V_O = 0 R_S = 50Ω	T_A = 25°C	70	100		dB
I_{CC}	电源电流（每个放大器）	V_O = 0；空载	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	串扰衰减	A_{VD} = 100	T_A = 25°C		120		dB

(1) 除非另有说明，所有特性均在开环条件下以零共模电压测定。
(2) 完整范围为 T_A = 0°C 至 70°C。
(3) FET 输入运算放大器的输入偏置电流是正常的结反向电流，此电流对温度敏感，如图 1 所示。必须使用脉冲技术来保持结温尽可能接近环境温度。

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6.11 电气特性：TL071AC、TL072AC、TL074AC

$V_{CC\pm}$ = ±15V（除非另有说明）

参数		测试条件 (1) (2)		最小值	典型值	最大值	单位
V_{IO}	输入失调电压	V_O = 0 R_S = 50Ω	T_A = 25°C		3	6	mV
			T_A = 完整范围			7.5	
α	输入失调电压的温度系数	V_O = 0 R_S = 50Ω	T_A = 完整范围		18		μV/°C
I_{IO}	输入失调电流	V_O = 0	T_A = 25°C		5	100	pA
			T_A = 完整范围			2	nA
I_{IB}	输入偏置电流 (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = 完整范围			7	nA
V_{ICR}	共模输入电压范围	T_A = 25°C		±11	–12 至 15		V
V_{OM}	最大峰值输出电压摆幅	R_L = 10kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10kΩ	T_A = 完整范围	±12			
		R_L ≥ 2kΩ		±10			
A_{VD}	大信号差分电压放大	V_O = ±10V R_L ≥ 2kΩ	T_A = 25°C	50	200		V/mV
			T_A = 完整范围	25			
B_1	单位增益带宽	T_A = 25°C			3		MHz
r_I	输入电阻	T_A = 25°C			10^{12}		Ω
CMRR	共模抑制比	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50Ω	T_A = 25°C	75	100		dB
k_{SVR}	电源电压抑制比 ($\Delta V_{CC\pm}$ / ΔV_{IO})	V_{CC} = ±9V 至 ±15V V_O = 0 R_S = 50Ω	T_A = 25°C	80	100		dB
I_{CC}	电源电流（每个放大器）	V_O = 0；空载	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	串扰衰减	A_{VD} = 100	T_A = 25°C		120		dB

(1) 除非另有说明，所有特性均在开环条件下以零共模电压测定。
(2) 完整范围为 T_A = 0°C 至 70°C。
(3) FET 输入运算放大器的输入偏置电流是正常的结反向电流，此电流对温度敏感，如图 1 所示。必须使用脉冲技术来保持结温尽可能接近环境温度。

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6.12 电气特性：TL071BC、TL072BC、TL074BC

$V_{CC\pm}$ = ±15V（除非另有说明）

参数		测试条件 (1) (2)		最小值	典型值	最大值	单位
V_{IO}	输入失调电压	V_O = 0 R_S = 50Ω	T_A = 25°C		2	3	mV
			T_A = 完整范围			5	
α	输入失调电压的温度系数	V_O = 0 R_S = 50Ω	T_A = 完整范围		18		μV/°C
I_{IO}	输入失调电流	V_O = 0	T_A = 25°C		5	100	pA
			T_A = 完整范围			2	nA
I_{IB}	输入偏置电流 (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = 完整范围			7	nA
V_{ICR}	共模输入电压范围	T_A = 25°C		±11	–12 至 15		V
V_{OM}	最大峰值输出电压摆幅	R_L = 10kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10kΩ	T_A = 完整范围	±12			
		R_L ≥ 2kΩ		±10			
A_{VD}	大信号差分电压放大	V_O = ±10V R_L ≥ 2kΩ	T_A = 25°C	50	200		V/mV
			T_A = 完整范围	25			
B_1	单位增益带宽	T_A = 25°C			3		MHz
r_I	输入电阻	T_A = 25°C			10^{12}		Ω
CMRR	共模抑制比	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50Ω	T_A = 25°C	75	100		dB
k_{SVR}	电源电压抑制比 ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9V 至 ±15V V_O = 0 R_S = 50Ω	T_A = 25°C	80	100		dB
I_{CC}	电源电流（每个放大器）	V_O = 0；空载	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	串扰衰减	A_{VD} = 100	T_A = 25°C		120		dB

(1) 除非另有说明，所有特性均在开环条件下以零共模电压测定。
(2) 完整范围为 T_A = 0°C 至 70°C。
(3) FET 输入运算放大器的输入偏置电流是正常的结反向电流，此电流对温度敏感，如图 1 所示。必须使用脉冲技术来保持结温尽可能接近环境温度。

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6.13 电气特性：TL071I、TL072I、TL074I

$V_{CC±}$ = ±15V（除非另有说明）

参数		测试条件 (1) (2)		最小值	典型值	最大值	单位
V_{IO}	输入失调电压	V_O = 0 R_S = 50Ω	T_A = 25°C		3	6	mV
			T_A = 完整范围			8	
α	输入失调电压的温度系数	V_O = 0 R_S = 50Ω	T_A = 完整范围		18		μV/°C
I_{IO}	输入失调电流	V_O = 0	T_A = 25°C		5	100	pA
			T_A = 完整范围			2	nA
I_{IB}	输入偏置电流 (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = 完整范围			7	nA
V_{ICR}	共模输入电压范围	T_A = 25°C		±11	–12 至 15		V
V_{OM}	最大峰值输出电压摆幅	R_L = 10kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10kΩ	T_A = 完整范围	±12			
		R_L ≥ 2kΩ		±10			
A_{VD}	大信号差分电压放大	V_O = ±10V R_L ≥ 2kΩ	T_A = 25°C	50	200		V/mV
			T_A = 完整范围	25			
B_1	单位增益带宽	T_A = 25°C			3		MHz
r_I	输入电阻	T_A = 25°C			10^{12}		Ω
CMRR	共模抑制比	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50Ω	T_A = 25°C	75	100		dB
k_{SVR}	电源电压抑制比 ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9V 至 ±15V V_O = 0 R_S = 50Ω	T_A = 25°C	80	100		dB
I_{CC}	电源电流（每个放大器）	V_O = 0；空载	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	串扰衰减	A_{VD} = 100	T_A = 25°C		120		dB

(1) 除非另有说明，所有特性均在开环条件下以零共模电压测定。
(2) T_A = –40°C 至 85°C.
(3) FET 输入运算放大器的输入偏置电流是正常的结反向电流，此电流对温度敏感，如图 1 所示。必须使用脉冲技术来保持结温尽可能接近环境温度。

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6.14 电气特性：TL071M、TL072M

$V_{CC\pm}$ = ±15V（除非另有说明）

参数		测试条件 (1) (2)		最小值	典型值	最大值	单位
V_{IO}	输入失调电压	V_O = 0 R_S = 50Ω	T_A=25°C		3	6	mV
			T_A = 完整范围			9	
α_{VIO}	输入失调电压的温度系数	V_O = 0 R_S = 50Ω	T_A = 完整范围		18		μV/°C
I_{IO}	输入失调电流	V_O = 0	T_A=25°C		5	100	pA
			T_A = 完整范围			20	nA
I_{IB}	输入偏置电流	V_O = 0	T_A=25°C		65	200	pA
			T_A = 完整范围			50	nA
V_{ICR}	共模输入电压范围	T_A=25°C		±11	–12 至 15		V
V_{OM}	最大峰值输出电压摆幅	R_L = 10kΩ	T_A=25°C	±12	±13.5		V
		R_L ≥ 10kΩ	T_A = 完整范围	±12			
		R_L ≥ 2kΩ		±10			
A_{VD}	大信号差分电压放大	V_O = ±10V R_L ≥ 2kΩ	T_A=25°C	35	200		V/mV
			T_A = 完整范围	15			
B_1	单位增益带宽				3		MHz
r_i	输入电阻				10^{12}		Ω
CMRR	共模抑制比	V_{IC} = $V_{ICR(min)}$， V_O = 0 R_S = 50Ω	T_A=25°C	80	86		dB
k_{SVR}	电源电压抑制比 ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9V 至 ±15V V_O = 0 R_S = 50Ω	T_A=25°C	80	86		dB
I_{CC}	电源电流 （每个放大器）	V_O = 0；空载	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	串扰衰减	A_{VD} = 100	T_A = 25°C		120		dB

(1) FET 输入运算放大器的输入偏置电流是正常的结反向电流，此电流对温度敏感，如图 1 所示。必须使用脉冲技术来保持结温尽可能接近环境温度。
(2) 除非另有说明，所有特性均在开环条件下以零共模电压测定。完整范围为 T_A = –55°C 至 +125°C。

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6.15 电气特性：TL074M

$V_{CC±}$ = ±15V（除非另有说明）

参数		测试条件 (1) (2)		最小值	典型值	最大值	单位
V_{IO}	输入失调电压	V_O = 0 R_S = 50Ω	T_A=25°C		3	9	mV
			T_A = 完整范围			15	
α_{VIO}	输入失调电压的温度系数	V_O = 0，R_S = 50Ω	T_A = 完整范围		18		µV/°C
I_{IO}	输入失调电流	V_O = 0	T_A=25°C		5	100	pA
			T_A = 完整范围			20	nA
I_{IB}	输入偏置电流	V_O = 0	T_A=25°C		65	200	pA
			T_A = 完整范围			20	nA
V_{ICR}	共模输入电压范围	T_A=25°C		±11	–12 至 15		V
V_{OM}	最大峰值输出电压摆幅	R_L = 10kΩ	T_A=25°C	±12	±13.5		V
		R_L ≥ 10kΩ	T_A = 完整范围	±12			
		R_L ≥ 2kΩ		±10			
A_{VD}	大信号差分电压放大	V_O = ±10V R_L ≥ 2kΩ	T_A=25°C	35	200		V/mV
			T_A = 完整范围	15			
B_1	单位增益带宽				3		MHz
r_i	输入电阻				10^{12}		Ω
CMRR	共模抑制比	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50Ω	T_A=25°C	80	86		dB
k_{SVR}	电源电压抑制比 ($\Delta V_{CC±}/\Delta V_{IO}$)	V_{CC} = ±9V 至 ±15V V_O = 0 R_S = 50Ω	T_A=25°C	80	86		dB
I_{CC}	电源电流 （每个放大器）	V_O = 0；空载	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	串扰衰减	A_{VD} = 100	T_A = 25°C		120		dB

(1) FET 输入运算放大器的输入偏置电流是正常的结反向电流，此电流对温度敏感，如图 1 所示。必须使用脉冲技术来保持结温尽可能接近环境温度。
(2) 除非另有说明，所有特性均在开环条件下以零共模电压测定。完整范围为 T_A = –55°C 至 +125°C。

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6.16 开关特性：TL07xM

$V_{CC±}$ = ±15V，T_A = 25°C

参数		测试条件		最小值	典型值	最大值	单位
SR	单位增益下的压摆率	V_I = 10V C_L = 100pF	R_L = 2kΩ 请参阅图 21	5	13		V/μs
t_r	上升时间过冲因素	V_I = 20V C_L = 100pF	R_L = 2kΩ 请参阅图 21		0.1		μs
					20%		
V_n	等效输入噪声电压	R_S = 20Ω	f = 1kHz		18		nV/√Hz
			f = 10Hz 至 10kHz		4		μV
I_n	等效输入噪声电流	R_S = 20Ω	f = 1kHz		0.01		pA/√Hz
THD	总谐波失真	$V_I$rms = 6V R_L ≥ 2kΩ f = 1kHz	A_{VD} = 1 RS ≤ 1kΩ		0.003%		

6.17 开关特性：TL07xC、TL07xAC、TL07xBC、TL07xI

$V_{CC±}$ = ±15V，T_A = 25°C

参数		测试条件		最小值	典型值	最大值	单位
SR	单位增益下的压摆率	V_I = 10V C_L = 100pF	R_L = 2kΩ 请参阅图 21	8	13		V/μs
t_r	上升时间过冲因素	V_I = 20V C_L = 100pF	R_L = 2kΩ 请参阅图 21		0.1		μs
					20%		
V_n	等效输入噪声电压	R_S = 20Ω	f = 1kHz		18		nV/√Hz
			f = 10Hz 至 10kHz		4		μV
I_n	等效输入噪声电流	R_S = 20Ω	f = 1kHz		0.01		pA/√Hz
THD	总谐波失真	$V_I$rms = 6V R_L ≥ 2kΩ f = 1kHz	A_{VD} = 1 RS ≤ 1kΩ		0.003%		

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6.18 典型特性

高温和低温下的数据仅适用于各种器件在自然通风条件下的额定工作温度范围内。

表 1. 典型特性：图形列表

			图表
I_{IB}	输入偏置电流	与自然通风温度间的关系	图 1
V_{OM}	最大峰值输出电压	与频率间的关系	图 2
			图 3
			图 4
		与自然通风温度间的关系	图 5
		与负载电阻间的关系	图 6
		与电源电压间的关系	图 7
A_{VD}	大信号差分电压放大	与自然通风温度间的关系	图 8
		与负载电阻间的关系	图 9
	相移	与频率间的关系	图 9
	标称单位增益带宽	与自然通风温度间的关系	图 10
	标称相移	与自然通风温度间的关系	图 10
CMRR	共模抑制比	与自然通风温度间的关系	图 11
	输入失调电压变化	与共模电压间的关系	图 20
I_{CC}	电源电流	与自然通风温度间的关系	图 13
		与电源电压间的关系	图 12
P_D	总功率损耗	与自然通风温度间的关系	图 14
	标称压摆率	与自然通风温度间的关系	图 15
V_n	等效输入噪声电压	与频率间的关系	图 16
THD	总谐波失真	与频率间的关系	图 17
	大信号脉冲响应	与时间间的关系	图 18
V_O	输出电压	与经历时间间的关系	图 19

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6.18.1 典型特性

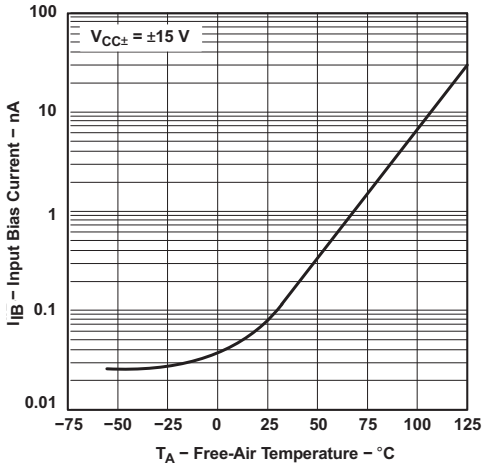


图 1. 输入偏置电流与自然通风温度间的关系

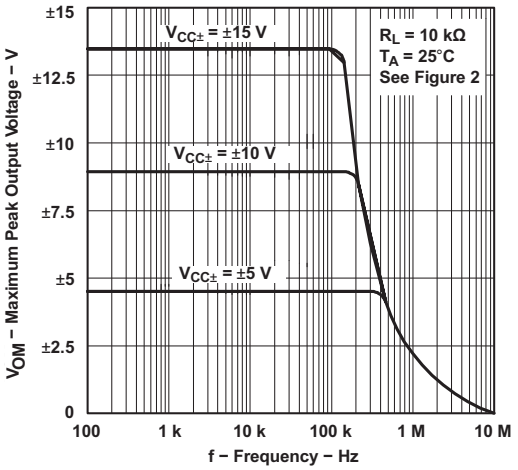


图 2. 最大峰值输出电压与频率间的关系

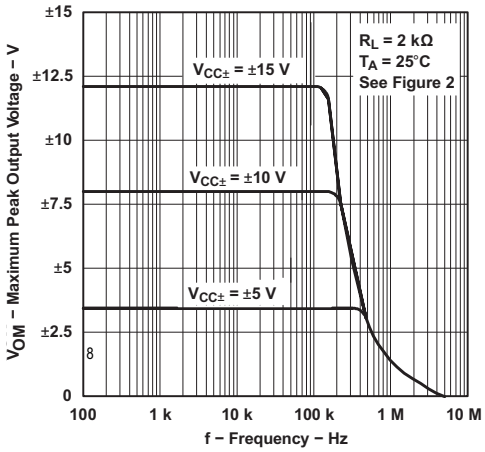


图 3. 最大峰值输出电压与频率间的关系

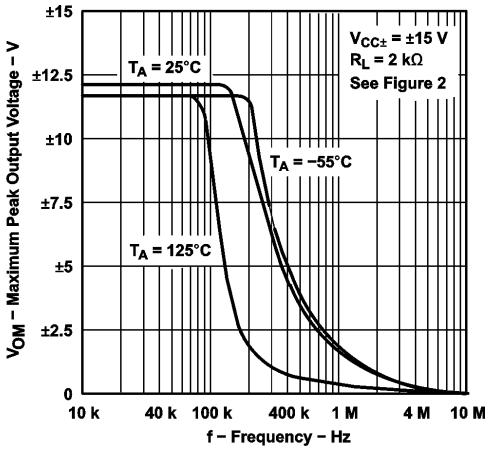


图 4. 最大峰值输出电压与频率间的关系

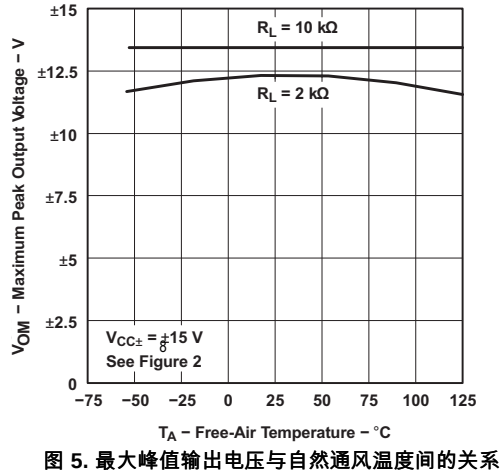


图 5. 最大峰值输出电压与自然通风温度间的关系

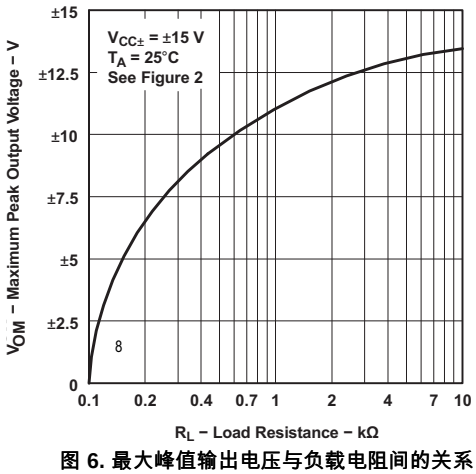


图 6. 最大峰值输出电压与负载电阻间的关系

典型特性 (接下页)

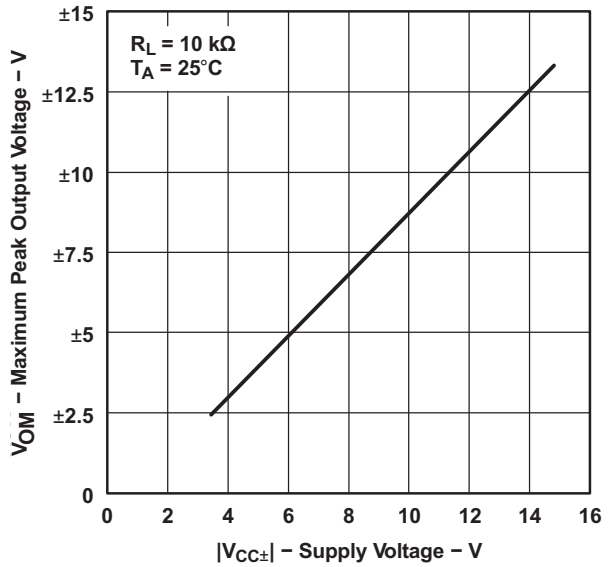


图 7. 最大峰值输出电压与电源电压间的关系

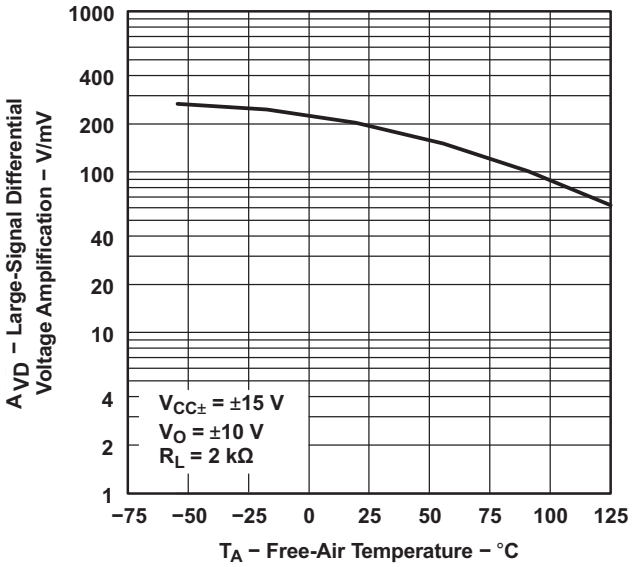


图 8. 大信号差分电压放大与自然通风温度间的关系

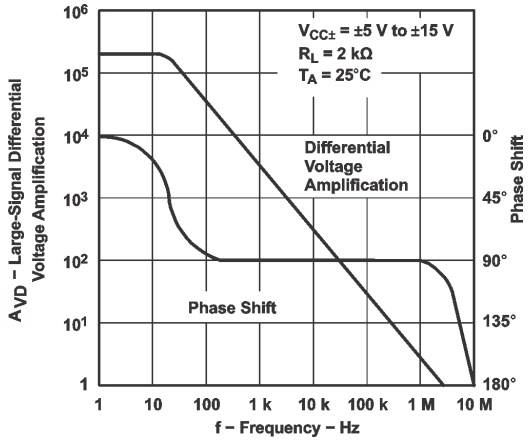


图 9. 大信号差分电压放大和相移与频率间的关系

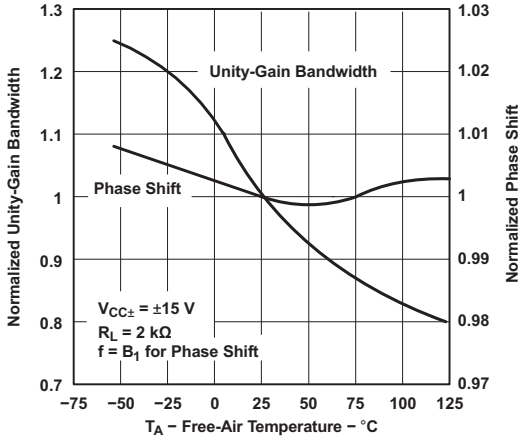


图 10. 标称单位增益带宽和相移与自然通风温度间的关系

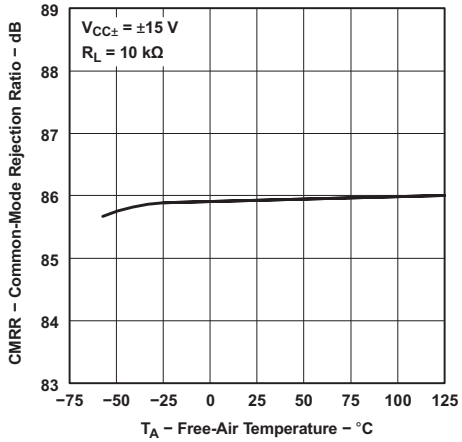


图 11. 共模抑制比与自然通风温度间的关系

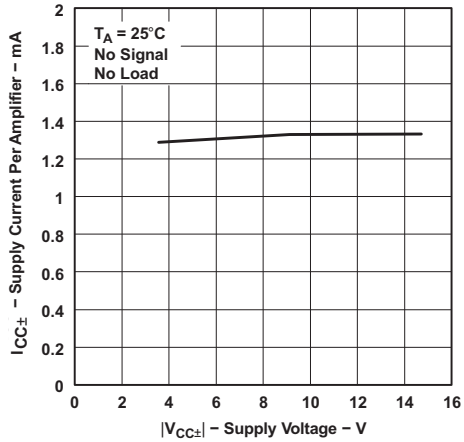


图 12. 每个放大器的电源电流与电源电压间的关系

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典型特性 (接下页)

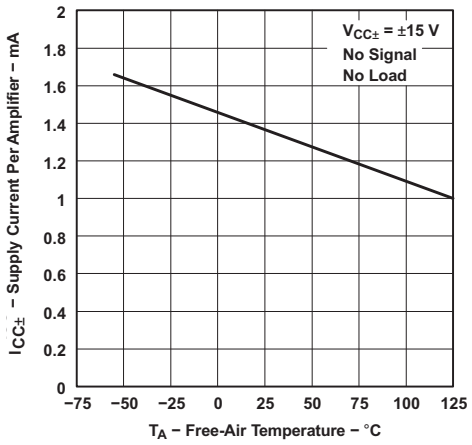


图 13. 每个放大器的电源电流与自然通风温度间的关系

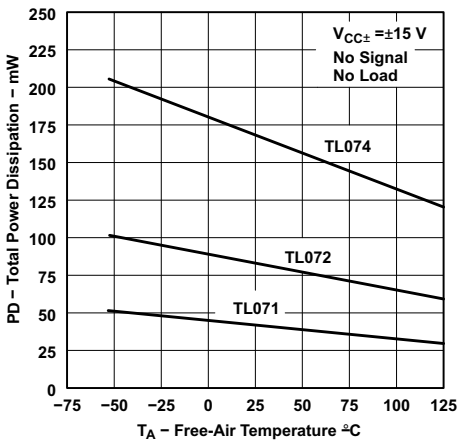


图 14. 总功率损耗与自然通风温度间的关系

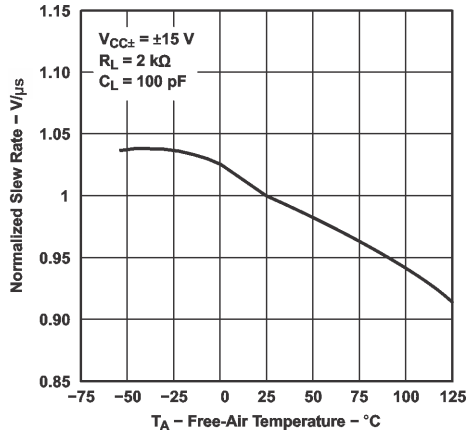


图 15. 标称压摆率与自然通风温度间的关系

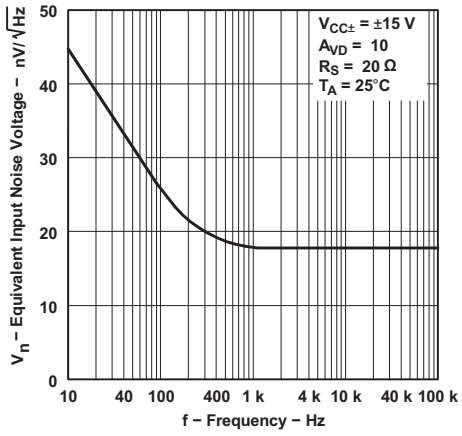


图 16. 等效输入噪声电压与频率间的关系

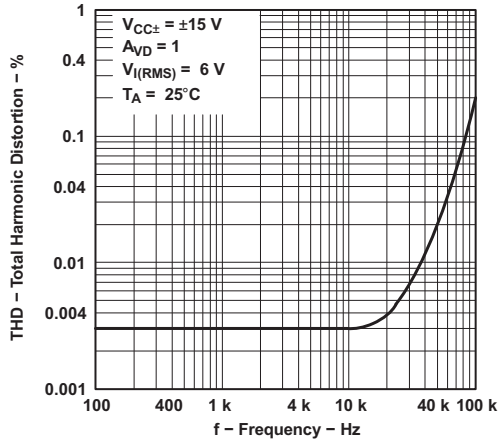


图 17. 总谐波失真与频率间的关系

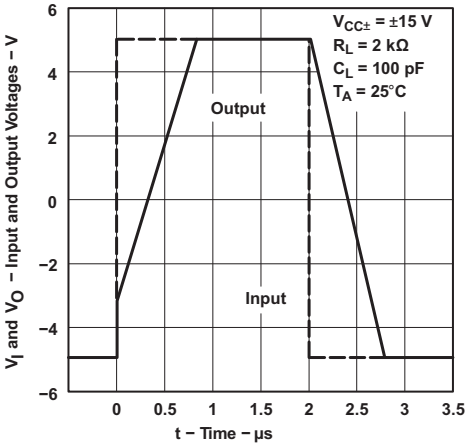


图 18. 电压跟随器大信号脉冲响应

典型特性 (接下页)

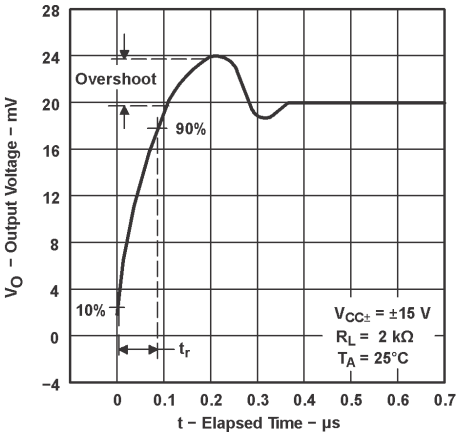


图 19. 输出电压与经历时间间的关系

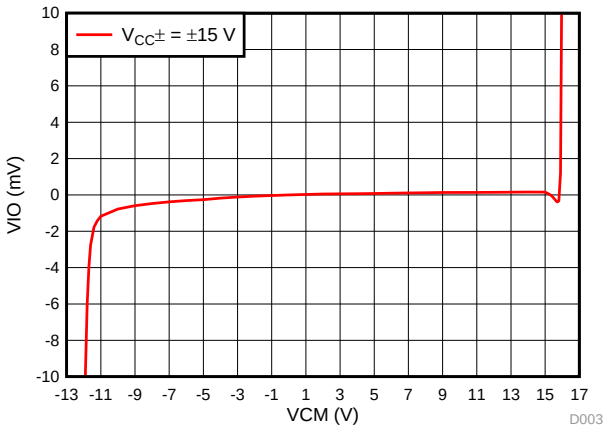


图 20. V_{IO} 与 V_{CM} 间的关系

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6.1 参数测量信息

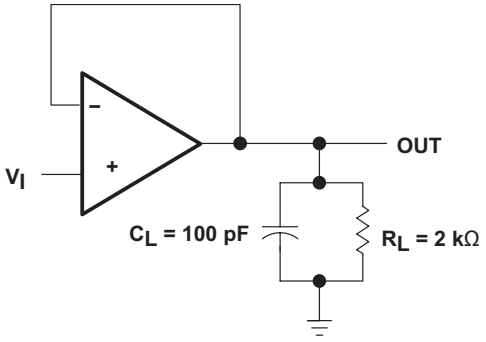


图 21. 单位增益放大器

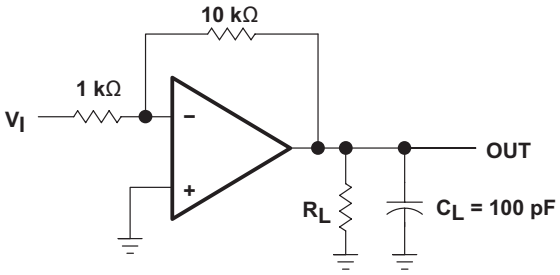


图 22. 增益为 10 的反相放大器

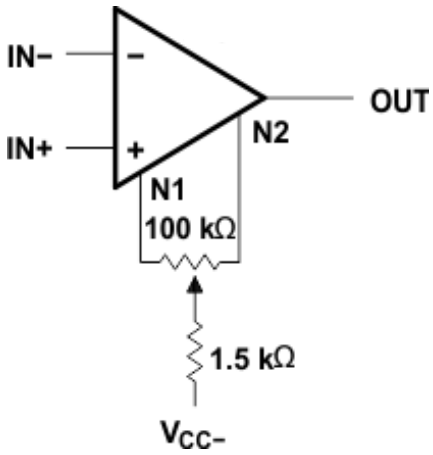


图 23. 输入失调电压零点电路

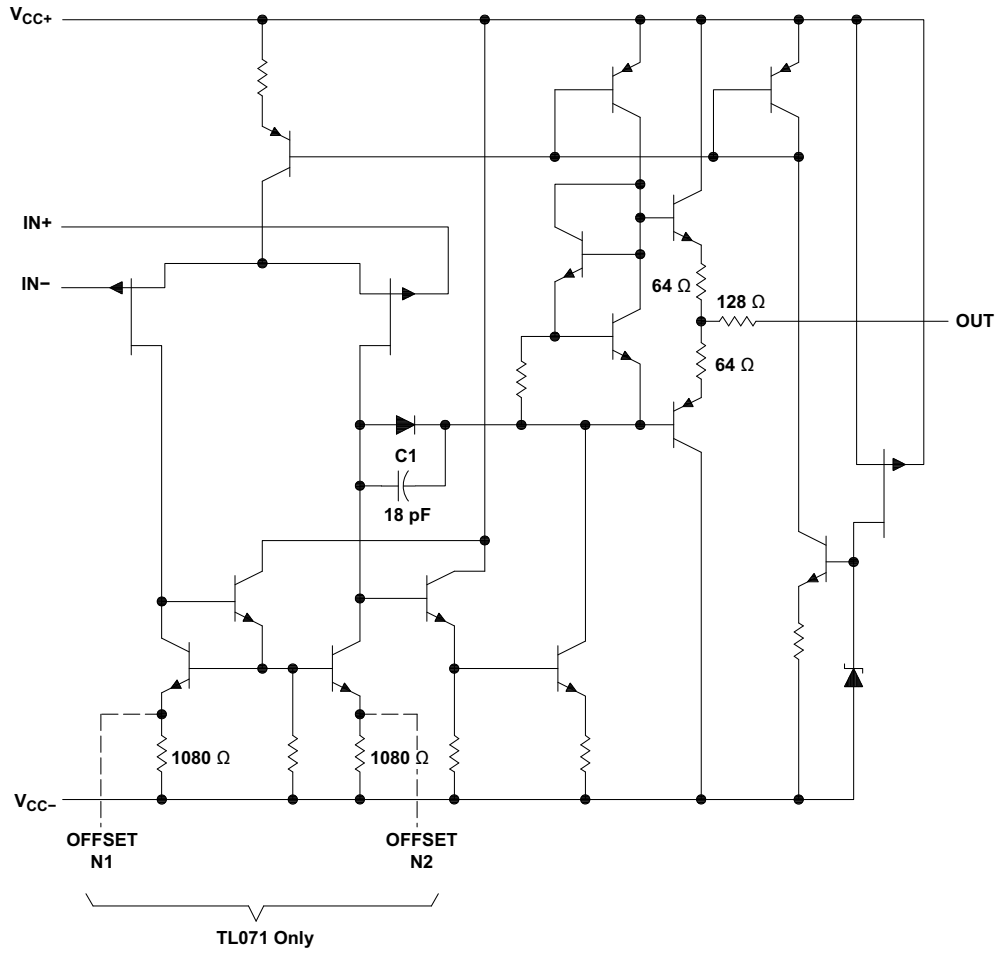
7 详细 说明

7.1 概述

JFET 输入运算放大器（TL07xx 系列器件）与 TL08x 系列器件类似，具有低输入偏置和失调电流以及高压摆率。TL07xx 系列的低谐波失真和低噪声等特性使其非常适合用于高保真和音频前置放大器 应用。每个放大器 特性 JFET 输入（用于高输入阻抗），这些输入与集成在一个单片芯片上的双极输出级耦合在一起。

后缀为 C 的器件的额定工作温度范围是 0°C 至 70°C。后缀为 I 的器件的额定工作温度范围是 −40°C 至 +85°C。后缀为 M 的器件在 –55°C 至 +125°C 的完整军用温度范围内运行。

7.2 功能框图



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

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7.3 特性 说明

7.3.1 总谐波失真

音频信号的谐波失真由电路中的电子组件产生。总谐波失真 (THD) 用于衡量音频系统中的信号所累积的谐波失真。这些器件具有 0.003% 的极低 THD，这意味着 TL07x 器件用在音频信号应用中时几乎不增加谐波失真 应用。

7.3.2 压摆率

压摆率是运算放大器在输入发生变化时可以改变输出的速率。这些器件具有 13V/μs 的压摆率。

7.4 器件功能模式

这些器件会在连接电源时上电。这些器件可根据应用情况作为单电源运算放大器或双电源放大器使用。

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8 应用和实现

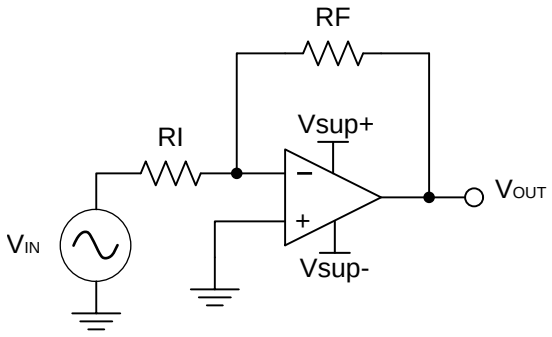
注

以下 应用 部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。TI 的客户应负责确定组件是否适用于其应用。客户应验证并测试其设计是否能够实现，以确保系统功能。

8.1 应用信息

运算放大器的典型应用是反相放大器。该放大器在输入端接受正电压，然后使电压变为负电压。该放大器以相同的方式使负输入电压变为正电压。

8.2 典型应用



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图 24. 反相放大器

8.2.1 设计要求

所选用的电源电压必须大于输入电压范围和输出范围。例如，此应用将 ±0.5V 的信号扩展到了 ±1.8V。将电源设置在 ±12V 就足以满足此应用的要求。

8.2.2 详细设计流程

确定反相放大器所需的增益：

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

确定所需增益后，请选择 RI 或 RF 的值。由于放大器电路使用毫安级的电流，因此通常需要选择千欧姆级的值。这样可以确保该器件不会消耗过多电流。此示例使用的 RI 为 10kΩ，这意味着对 RF 使用的值为 36kΩ。这是由公式 3 算出的。

$$A_V = -\frac{RF}{RI} \quad (3)$$

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典型应用 (接下页)

8.2.3 应用曲线

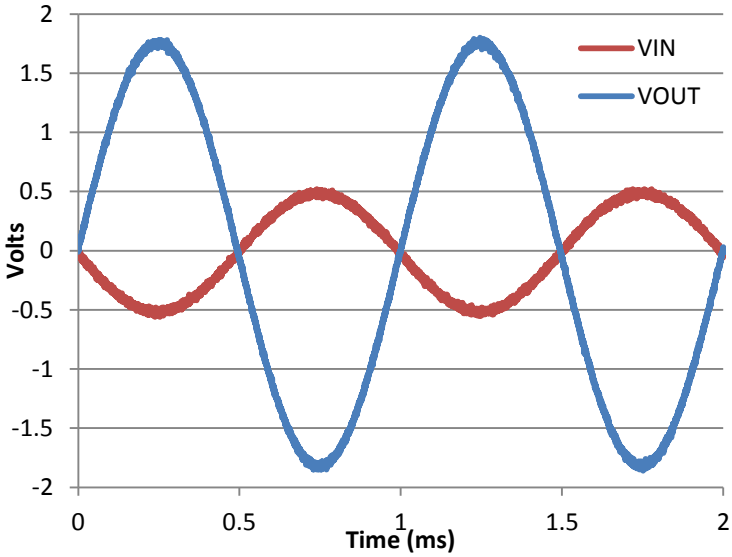


图 25. 反相放大器的输入和输出电压

8.3 单位增益缓冲器

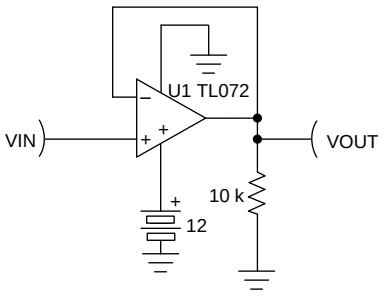


图 26. 单电源单位增益放大器

8.3.1 设计要求

- V_{CC} 必须位于*建议运行条件* 规定的有效范围内。此示例使用的 V_{CC} 值为 12V。
- 输入电压必须位于建议的共模范围内（如*建议运行条件* 中所示）。有效的共模范围为 4V 至 12V（$V_{CC–}$ + 4V 至 V_{CC+}）。
- 输出受制于输出范围，通常为 1.5V 至 10.5V，即 $V_{CC–}$ + 1.5V 至 V_{CC+} – 1.5V。

8.3.2 详细设计流程

- 避免输入电压值低于 1V，从而防止输出变高时出现相位反转。
- 避免输入值低于 4V，从而防止降级的 V_{IO} 导致视在增益大于 1。这种情况可能会导致一些二阶滤波器设计出现不稳定。

单位增益缓冲器 (接下页)

8.3.3 应用曲线

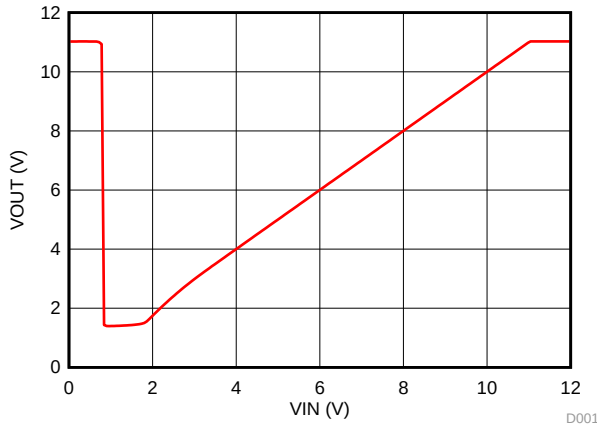


图 27. 静态电流与输入电压间的关系

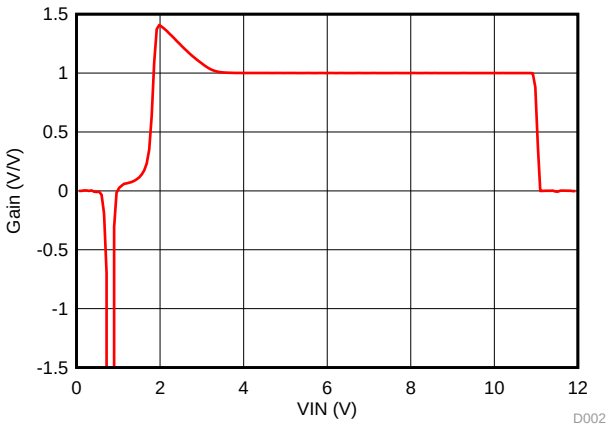


图 28. 增益与输入电压间的关系

8.4 系统示例

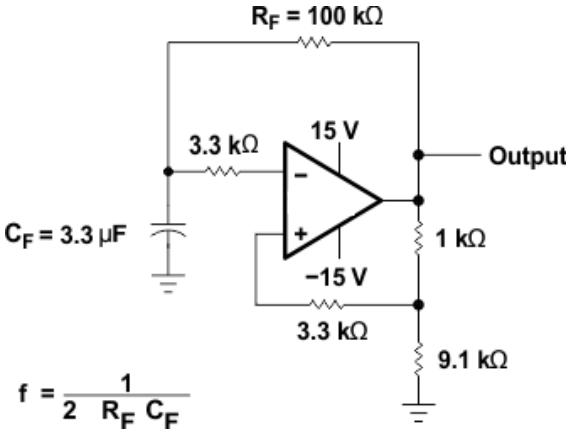


图 29. 0.5Hz 方波振荡器

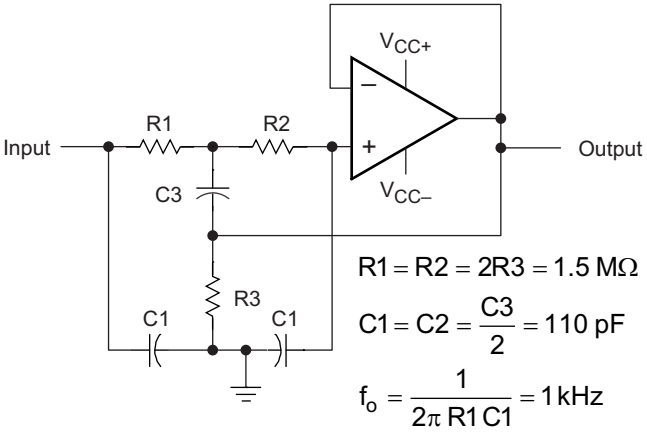


图 30. 高 Q 值陷波滤波器

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系统示例 (接下页)

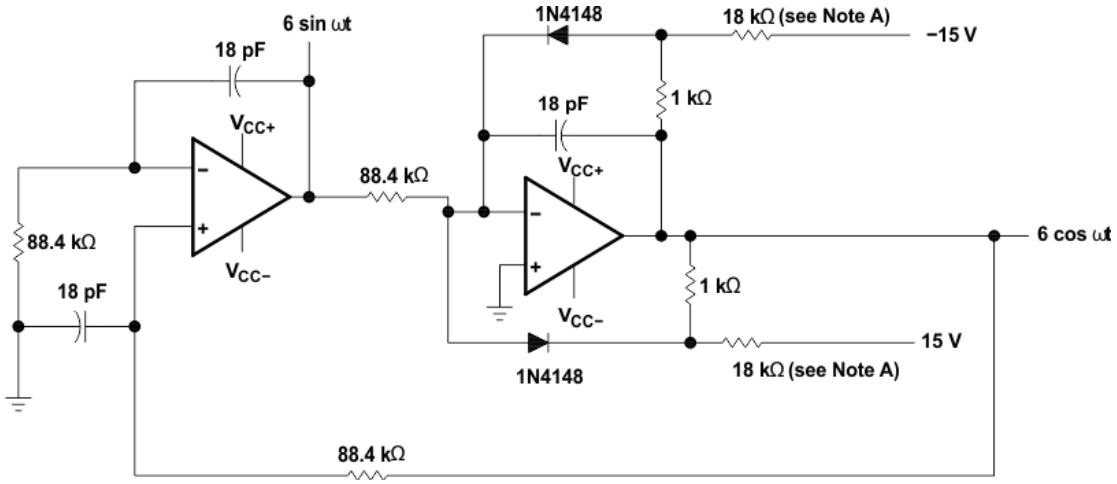


图 31. 100kHz 正交振荡器

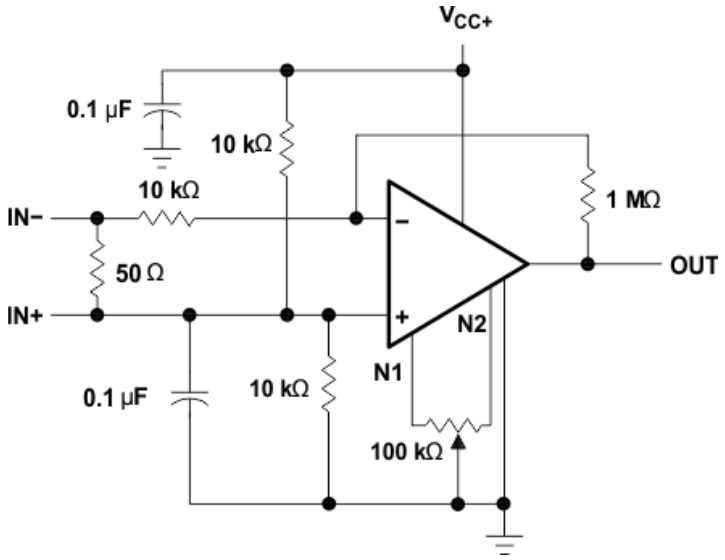


图 32. 交流放大器

9 电源建议

CAUTION

单电源的电源电压超过 36V 或双电源的电源电压范围超出 ±18V 可能会对器件造成永久损坏（请参阅*绝对最大额定值*）。

将 0.1μF 旁路电容器置于电源引脚附近，可减少从高噪声电源或高阻抗电源中耦合进来的误差。有关旁路电容器放置的更多详细信息，请参阅*布局*。

10 布局

10.1 布局准则

为了实现器件的最佳运行性能，应使用良好的 PCB 布局规范，包括：

- 噪声可通过全部电路电源引脚以及运算放大器自身传入模拟电路。旁路电容器通过提供位于模拟电路本地的低阻抗电源来降低耦合噪声。
  - 在每个电源引脚和接地端之间连接低 ESR 0.1μF 陶瓷旁路电容器，放置位置尽量靠近器件。从 V+ 到接地端的单个旁路电容器适用于单通道电源 应用。
- 将电路的模拟和数字部分单独接地是最简单和最有效的噪声抑制方法之一。多层 PCB 中通常将一层或多层专门作为接地层。接地平面有助于散热和降低 EMI 噪声拾取。请小心地对数字接地和模拟接地进行物理隔离，同时应注意接地电流。有关更多详细信息，请参阅*《电路板布局技巧》*。
- 为了减少寄生耦合，请让输入走线尽可能远离电源或输出走线。如果这些走线不能保持分离状态，最好让敏感走线与有噪声的走线垂直相交，而不是平行相交。
- 外部组件的位置应尽量靠近器件。如*布局示例* 中所示，使 RF 和 RG 接近反相输入可最大限度地减小寄生电容。
- 尽可能缩短输入走线。切记：输入走线是电路中最敏感的部分。
- 考虑在关键走线周围设定驱动型低阻抗保护环。这样可显著减少附近走线在不同电势下产生的泄漏电流。

10.2 布局示例

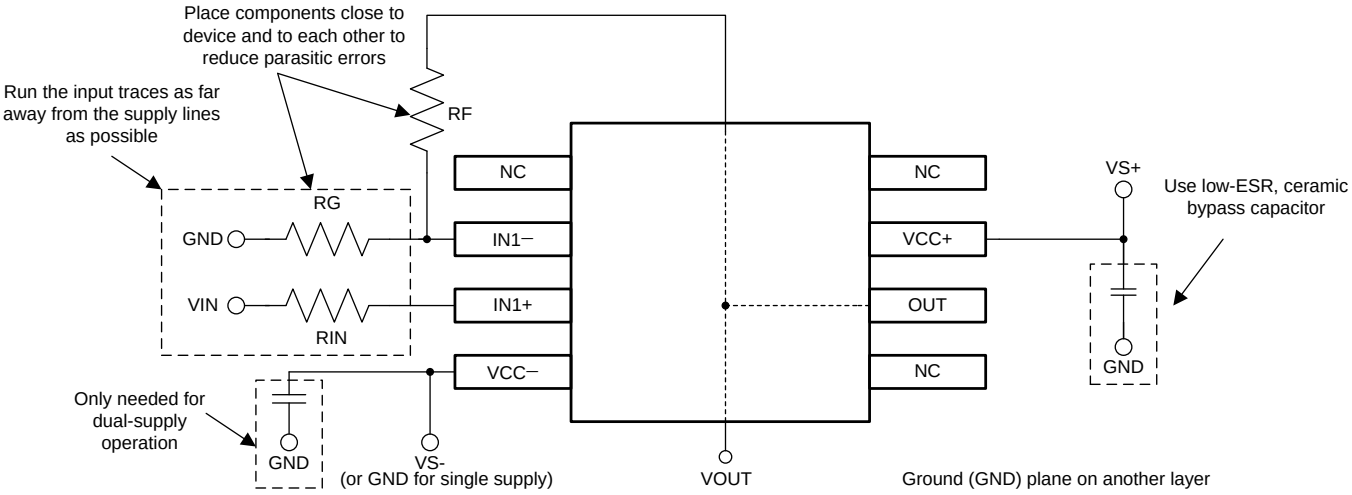


图 33. 同相配置的运算放大器电路板布局

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布局示例 **(**接下页**)**

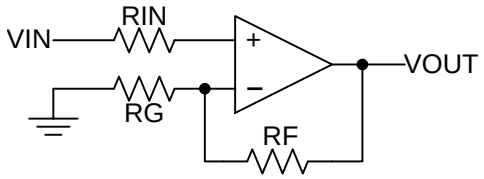


图 34. 同相配置的运算放大器原理图

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

如需相关文档，请参阅：

《电路板布局布线技巧》（文献编号：SLOA089）

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 **2.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TL071	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL071A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL071B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL072	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL072A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL072B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL072M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL074	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL074A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL074B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TL074M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023052A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
8102305HA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
8102305PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
81023062A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
8102306CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
8102306DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
TL071ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples
TL071BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples
TL071ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL072ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072BCPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRE4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
TL072MJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL072MJG	Samples
TL072MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
TL072MUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
TL074ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074BCNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CNSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074MFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MFK	Samples
TL074MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
TL074MJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MJ	Samples
TL074MJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
TL074MWB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

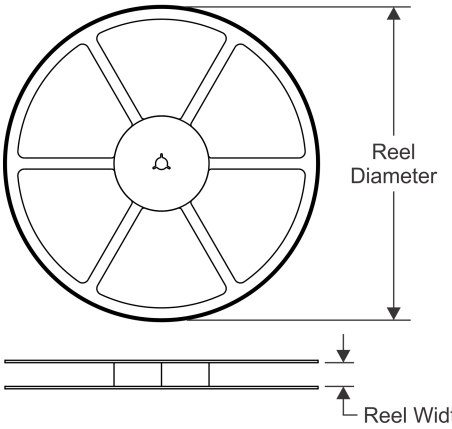
- Catalog : TL072, TL074
- Enhanced Product : TL072-EP, TL072-EP, TL074-EP, TL074-EP
- Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

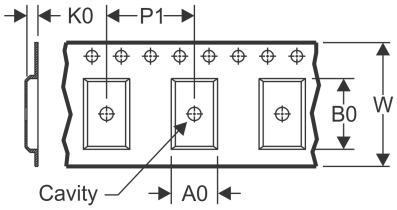
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

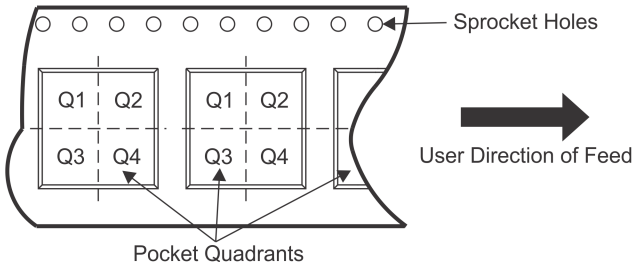


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

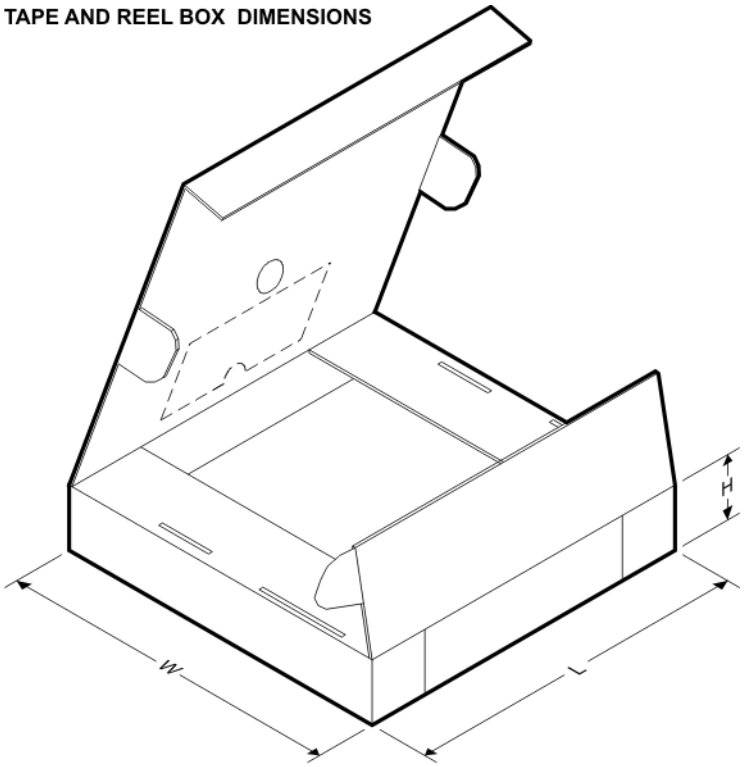


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

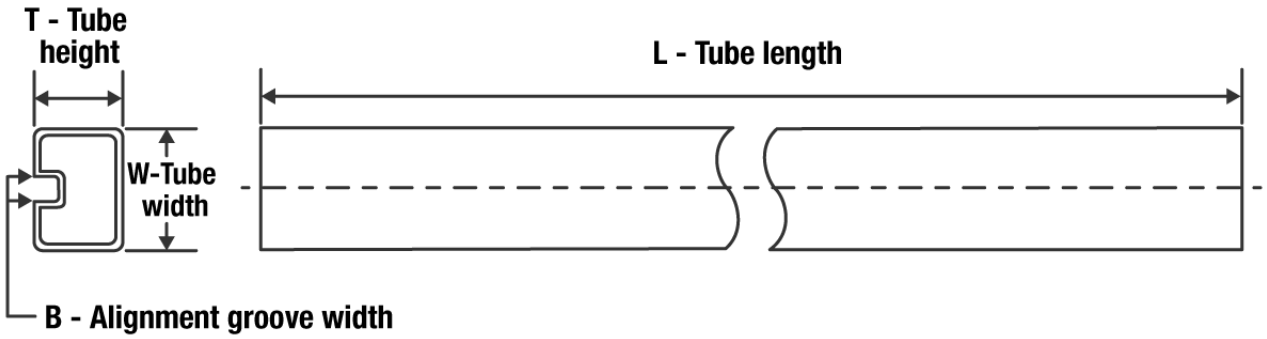


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071CDR	SOIC	D	8	2500	853.0	449.0	35.0
TL071CPSR	SO	PS	8	2000	853.0	449.0	35.0
TL071IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072CDR	SOIC	D	8	2500	853.0	449.0	35.0
TL072CPSR	SO	PS	8	2000	853.0	449.0	35.0
TL072CPWR	TSSOP	PW	8	2000	853.0	449.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072IDR	SOIC	D	8	2500	853.0	449.0	35.0
TL074ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074ACNSR	SO	NS	14	2000	853.0	449.0	35.0
TL074BCDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074CDBR	SSOP	DB	14	2000	853.0	449.0	35.0
TL074CDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074CDRG4	SOIC	D	14	2500	340.5	336.1	32.0
TL074CNSR	SO	NS	14	2000	853.0	449.0	35.0
TL074CPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TL074IDR	SOIC	D	14	2500	340.5	336.1	32.0

TUBE

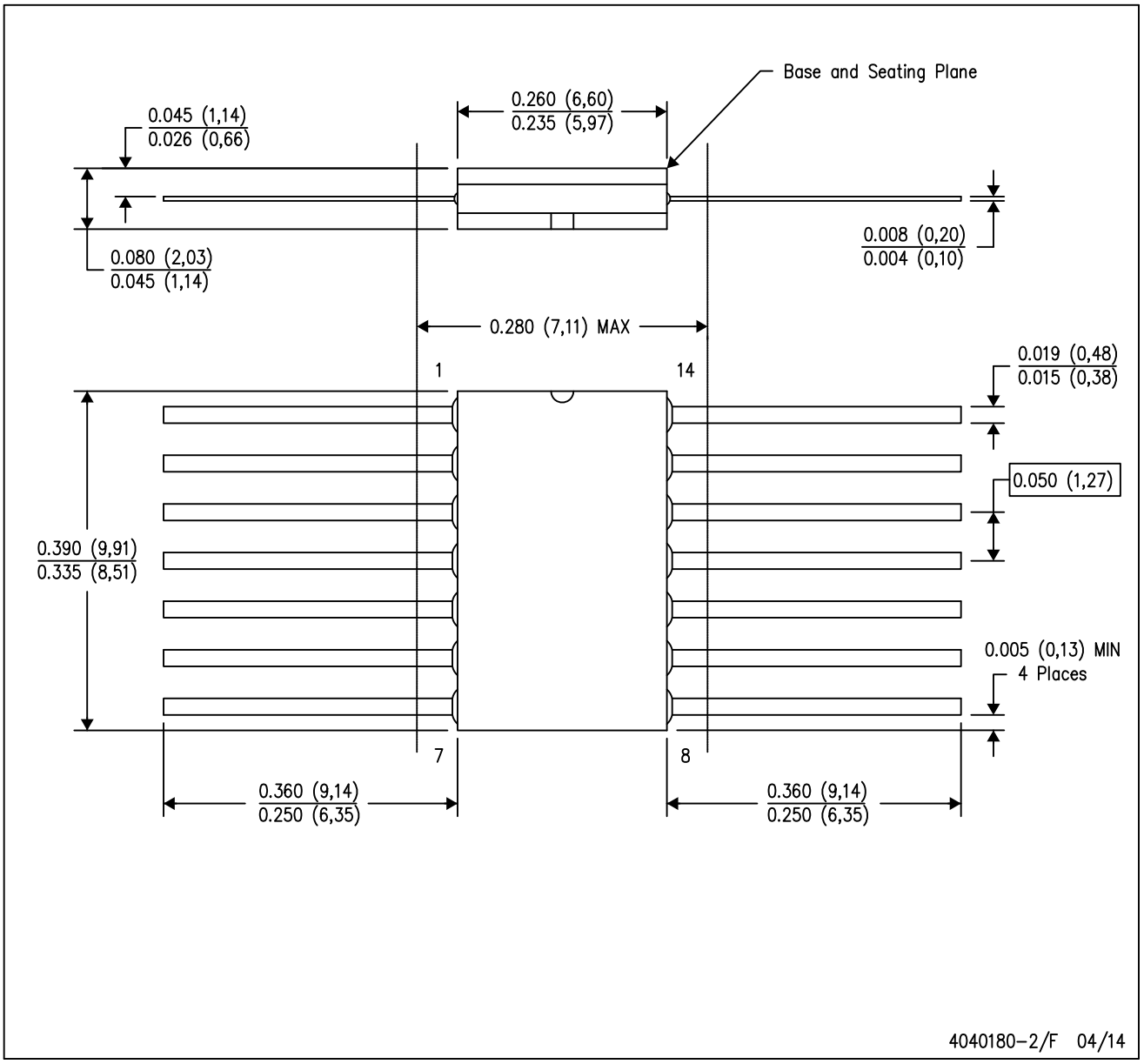


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023052A	FK	LCCC	20	1	506.98	12.06	2030	NA
81023062A	FK	LCCC	20	1	506.98	12.06	2030	NA
TL071ACD	D	SOIC	8	75	507	8	3940	4.32
TL071ACDG4	D	SOIC	8	75	507	8	3940	4.32
TL071ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCD	D	SOIC	8	75	507	8	3940	4.32
TL071BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CD	D	SOIC	8	75	506.6	8	3940	4.32
TL071CD	D	SOIC	8	75	507	8	3940	4.32
TL071CP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL071ID	D	SOIC	8	75	507	8	3940	4.32
TL071IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACD	D	SOIC	8	75	507	8	3940	4.32
TL072ACDE4	D	SOIC	8	75	507	8	3940	4.32
TL072ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072BCD	D	SOIC	8	75	507	8	3940	4.32
TL072BCDE4	D	SOIC	8	75	507	8	3940	4.32
TL072BCDG4	D	SOIC	8	75	507	8	3940	4.32
TL072BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL072BCPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072CD	D	SOIC	8	75	506.6	8	3940	4.32
TL072CD	D	SOIC	8	75	507	8	3940	4.32
TL072CDE4	D	SOIC	8	75	507	8	3940	4.32
TL072CDE4	D	SOIC	8	75	506.6	8	3940	4.32
TL072CDG4	D	SOIC	8	75	507	8	3940	4.32
TL072CDG4	D	SOIC	8	75	506.6	8	3940	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL072CP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072ID	D	SOIC	8	75	506.6	8	3940	4.32
TL072ID	D	SOIC	8	75	507	8	3940	4.32
TL072IDE4	D	SOIC	8	75	506.6	8	3940	4.32
TL072IDE4	D	SOIC	8	75	507	8	3940	4.32
TL072IDG4	D	SOIC	8	75	506.6	8	3940	4.32
TL072IDG4	D	SOIC	8	75	507	8	3940	4.32
TL072IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL074ACD	D	SOIC	14	50	507	8	3940	4.32
TL074ACDE4	D	SOIC	14	50	507	8	3940	4.32
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCD	D	SOIC	14	50	507	8	3940	4.32
TL074BCDE4	D	SOIC	14	50	507	8	3940	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CD	D	SOIC	14	50	507	8	3940	4.32
TL074CDG4	D	SOIC	14	50	507	8	3940	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL074ID	D	SOIC	14	50	507	8	3940	4.32
TL074IDE4	D	SOIC	14	50	507	8	3940	4.32
TL074IDG4	D	SOIC	14	50	507	8	3940	4.32
TL074IN	N	PDIP	14	25	506	13.97	11230	4.32
TL074MFK	FK	LCCC	20	1	506.98	12.06	2030	NA
TL074MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

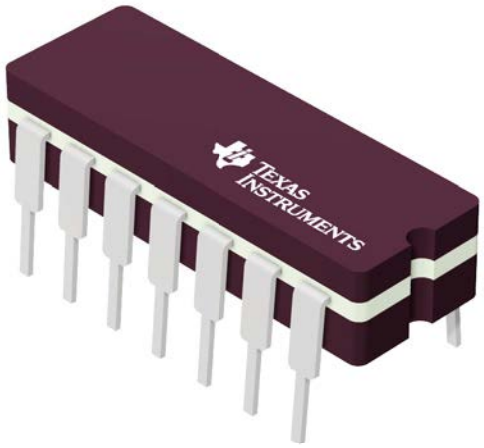


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

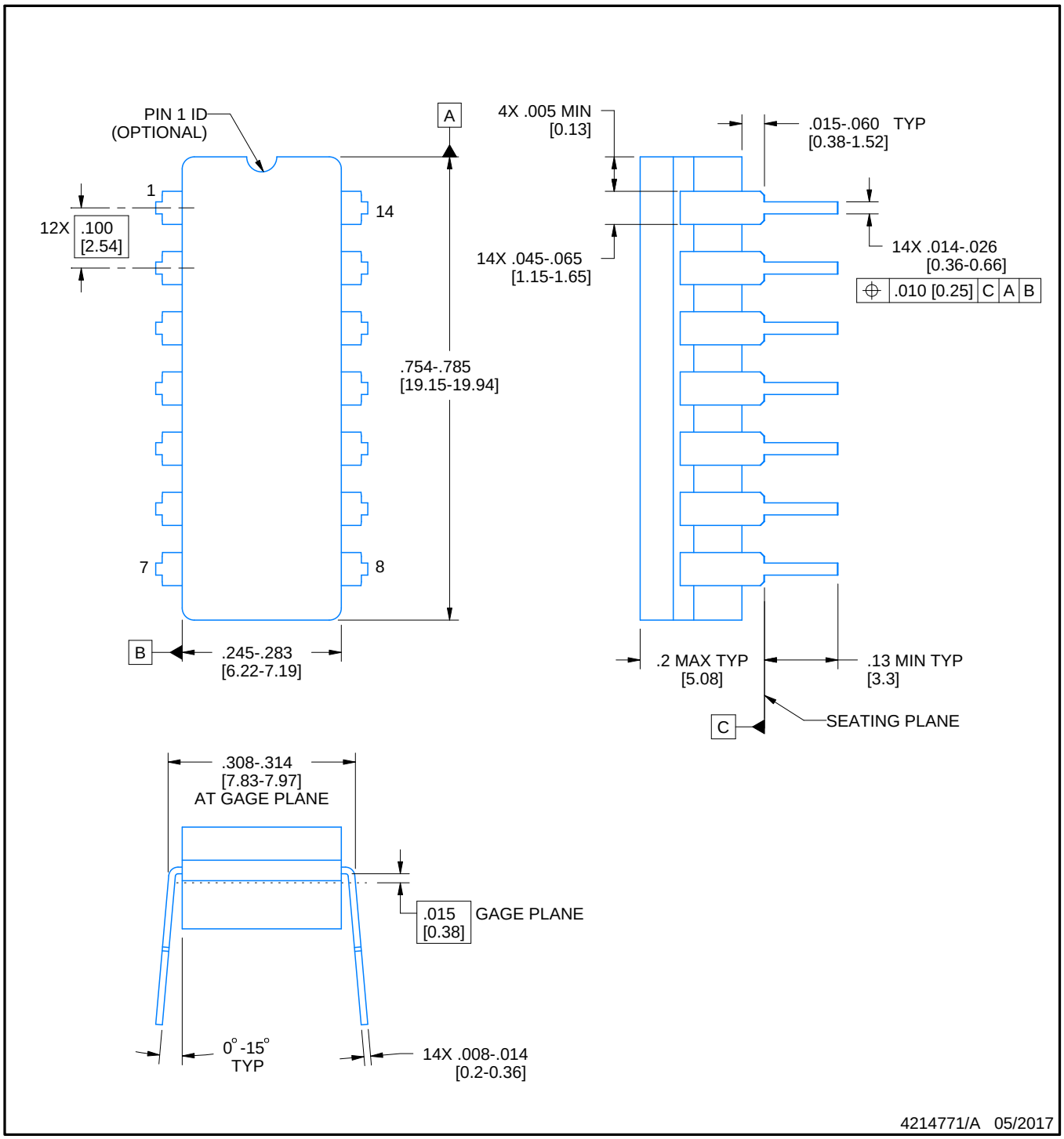


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

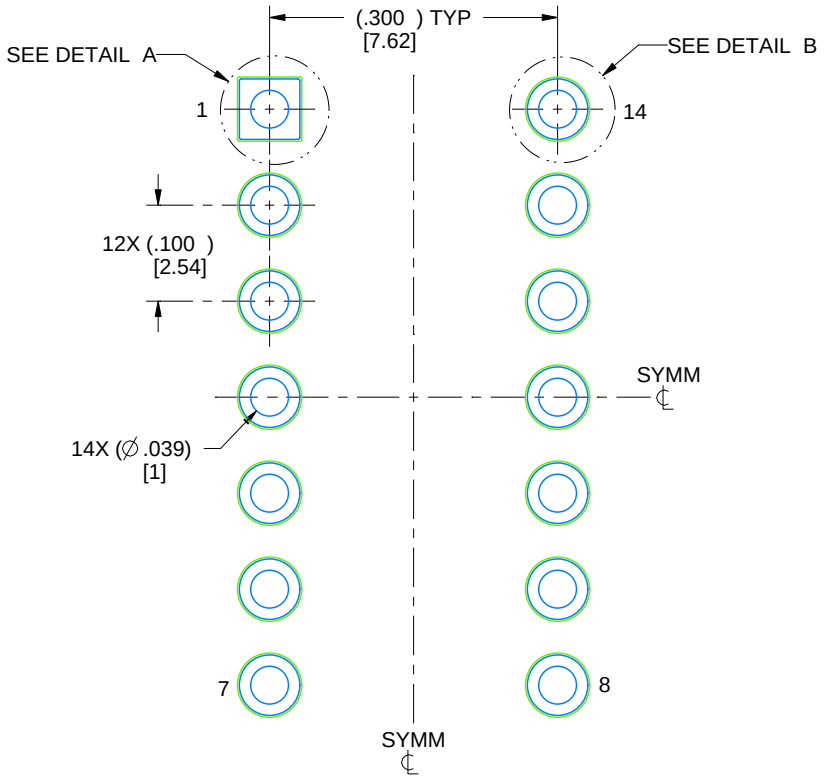
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

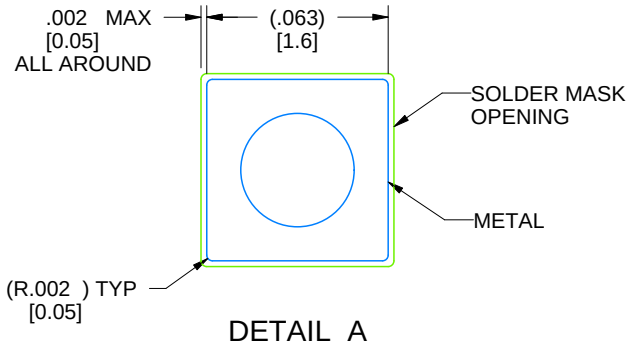
J0014A

CDIP - 5.08 mm max height

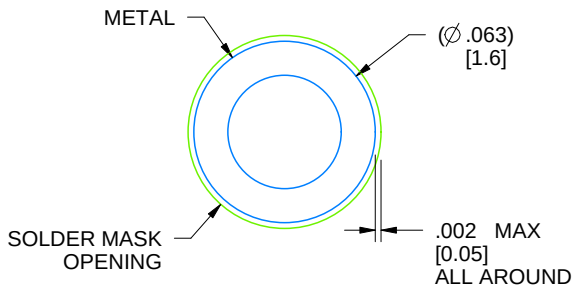
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



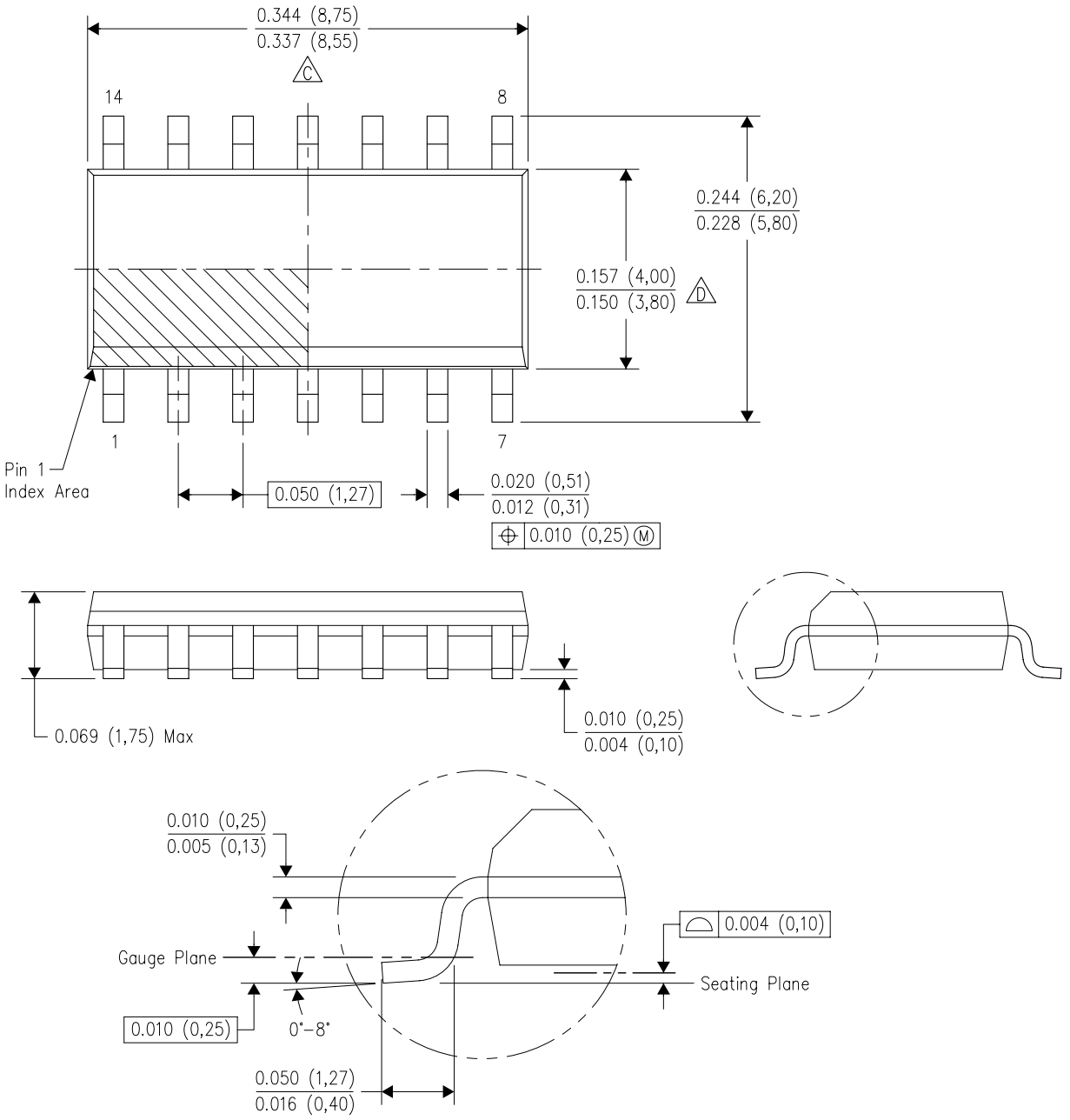
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

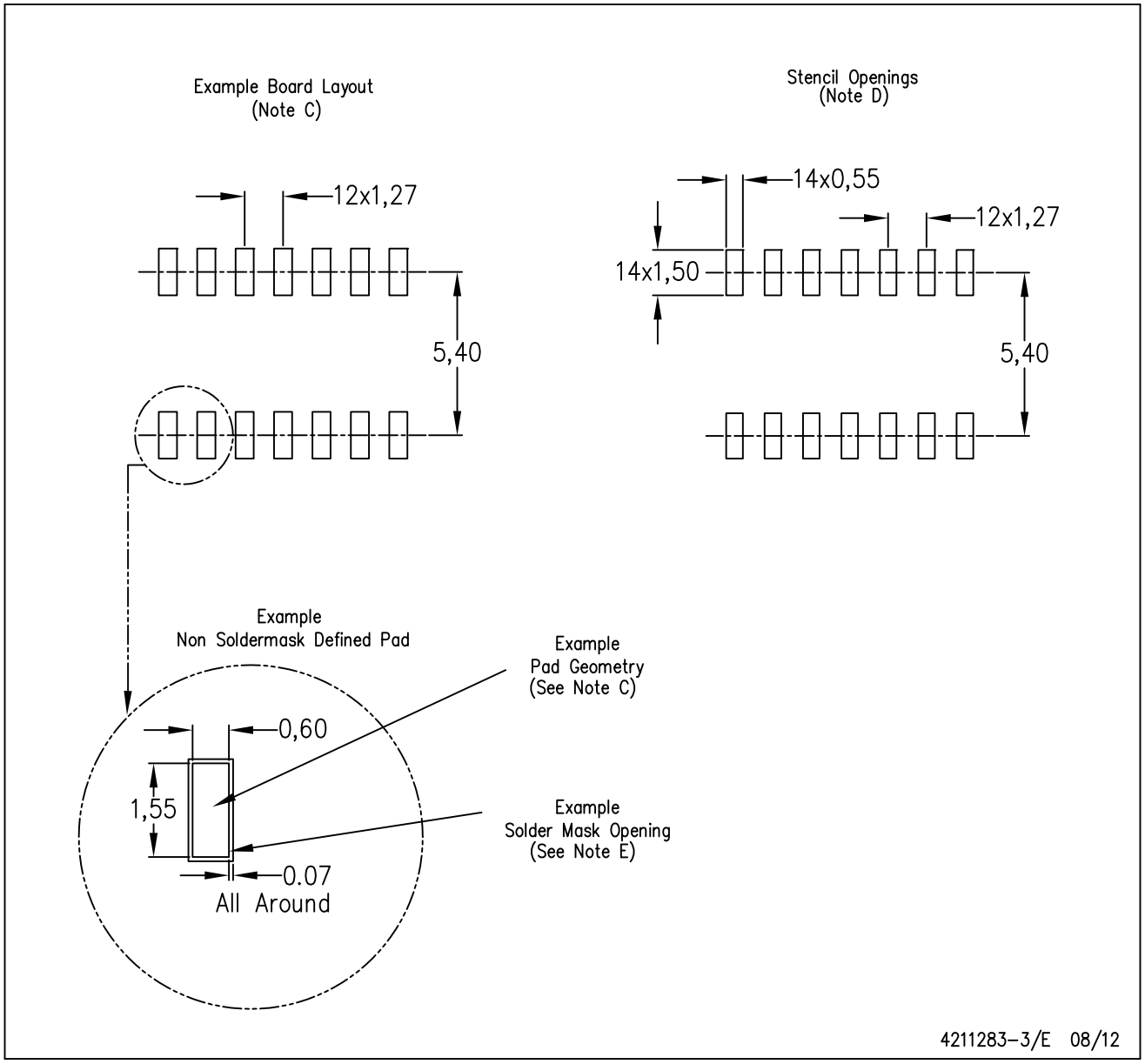
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

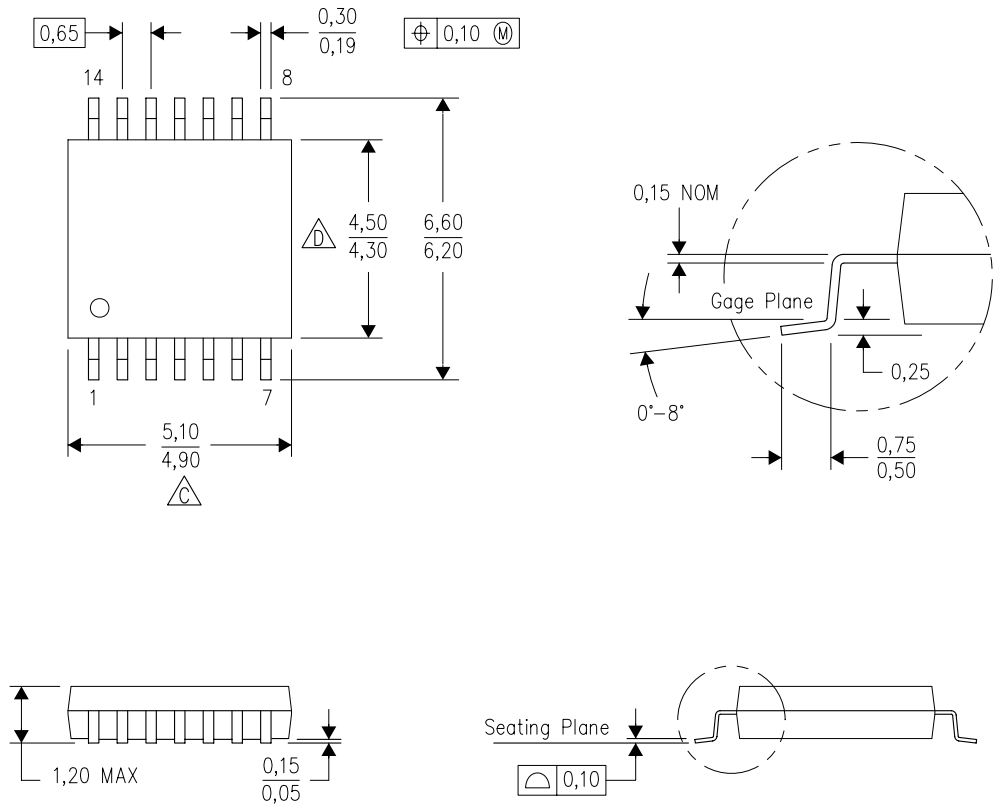
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



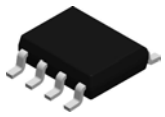
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

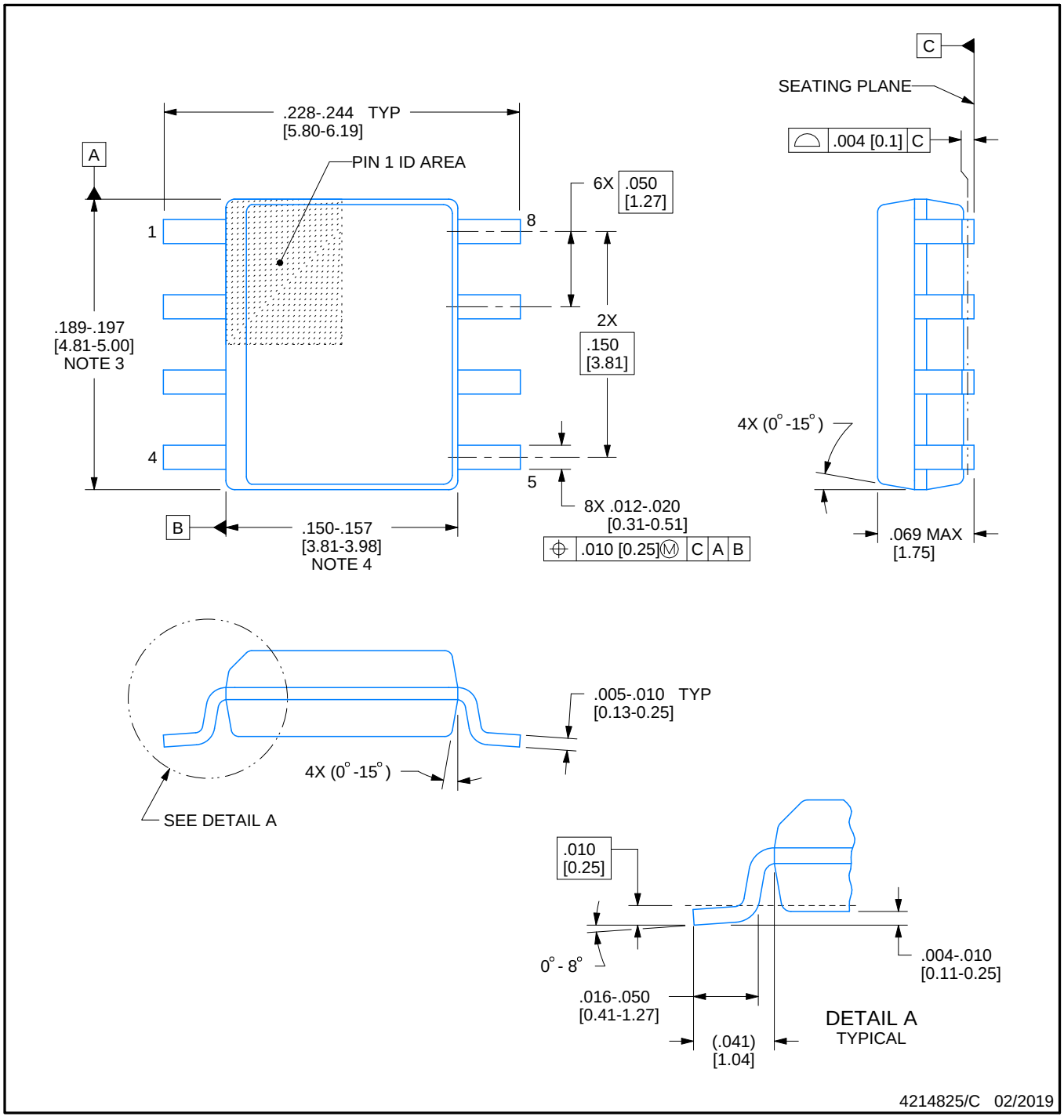


PACKAGE OUTLINE

D0008A

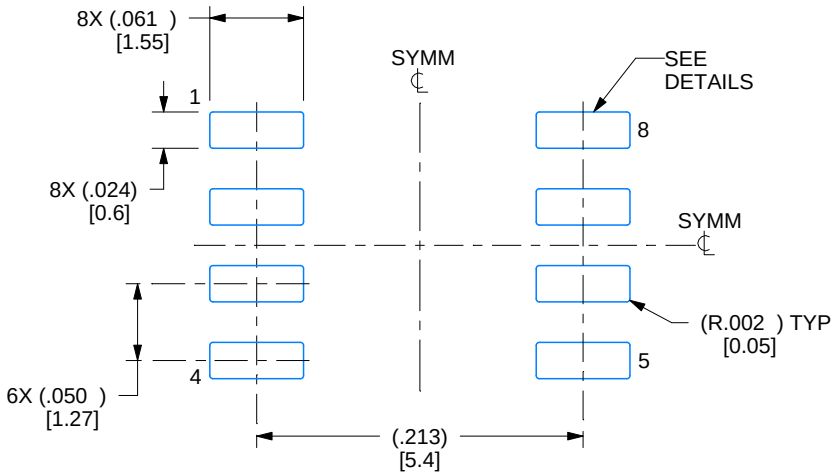
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

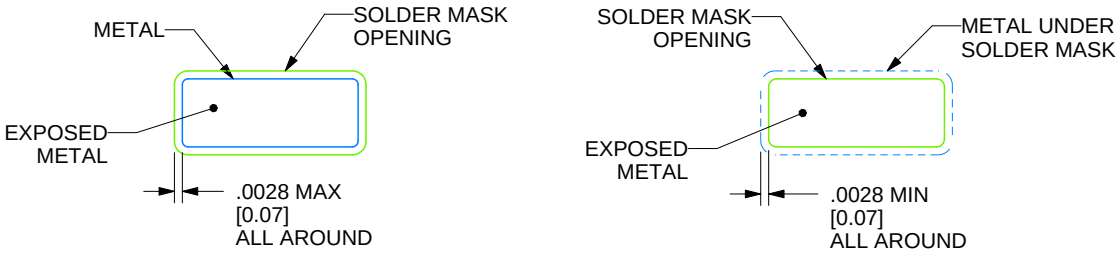


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

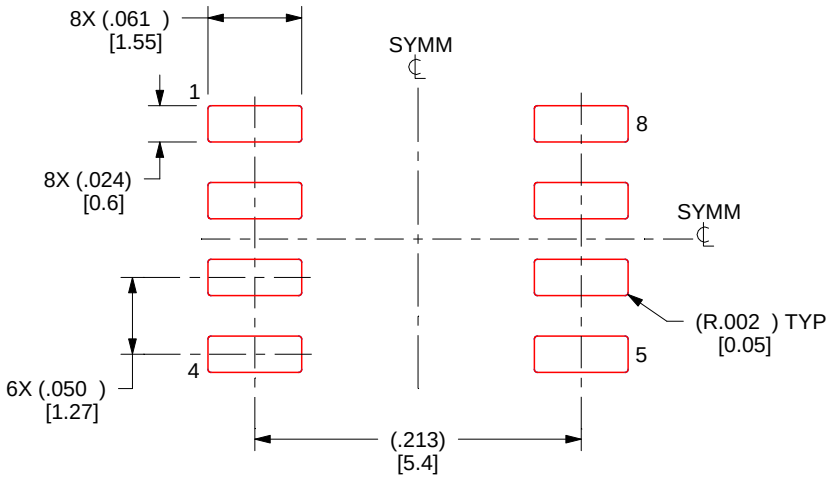
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

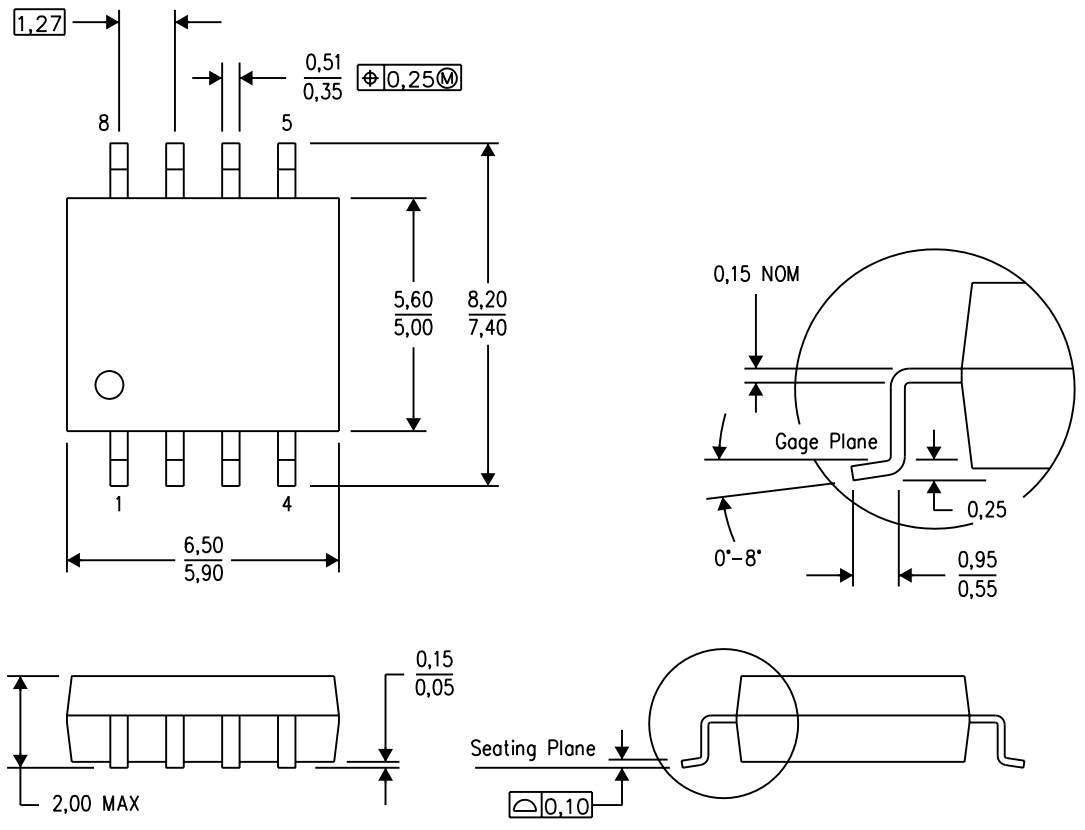
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

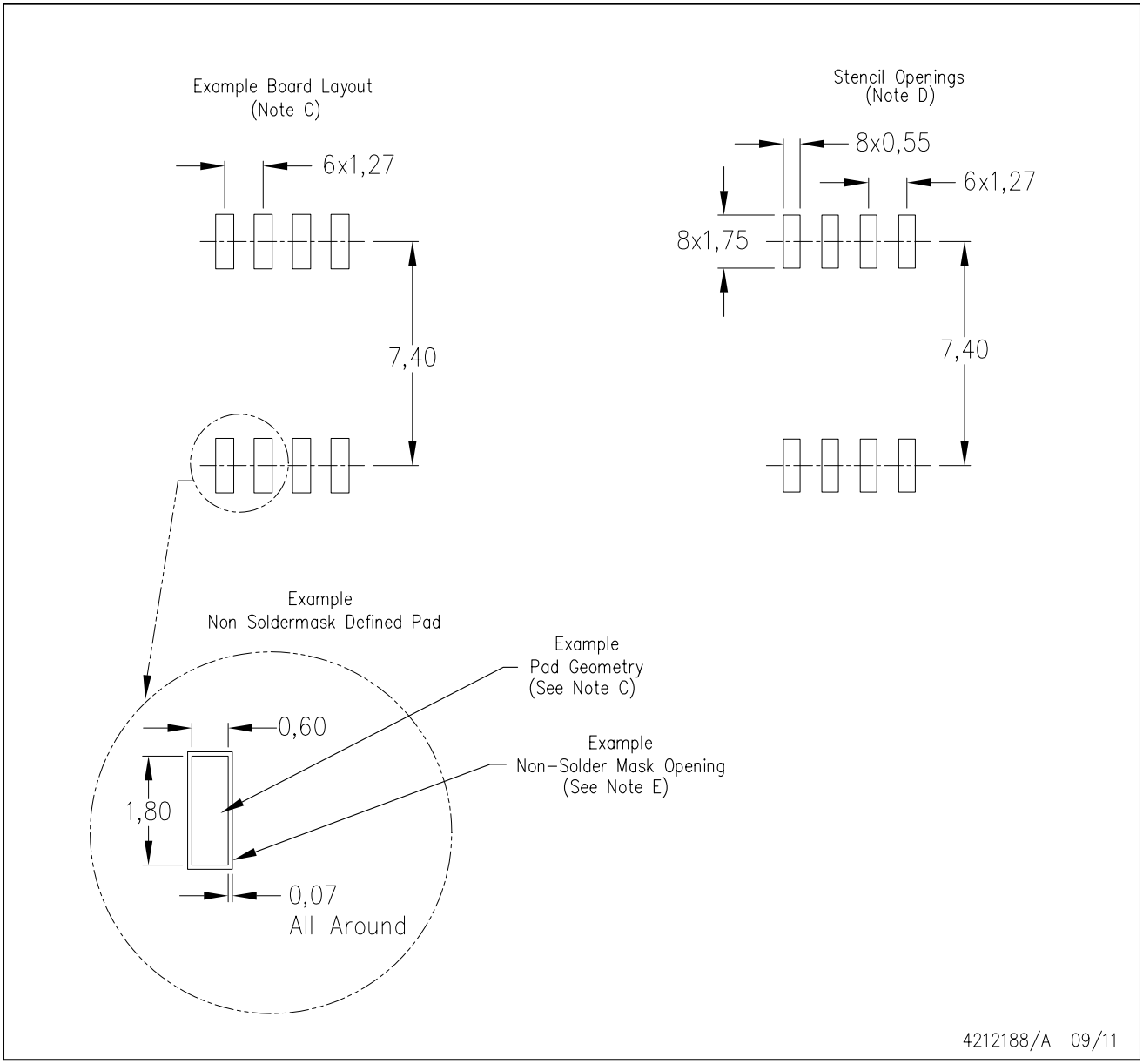
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

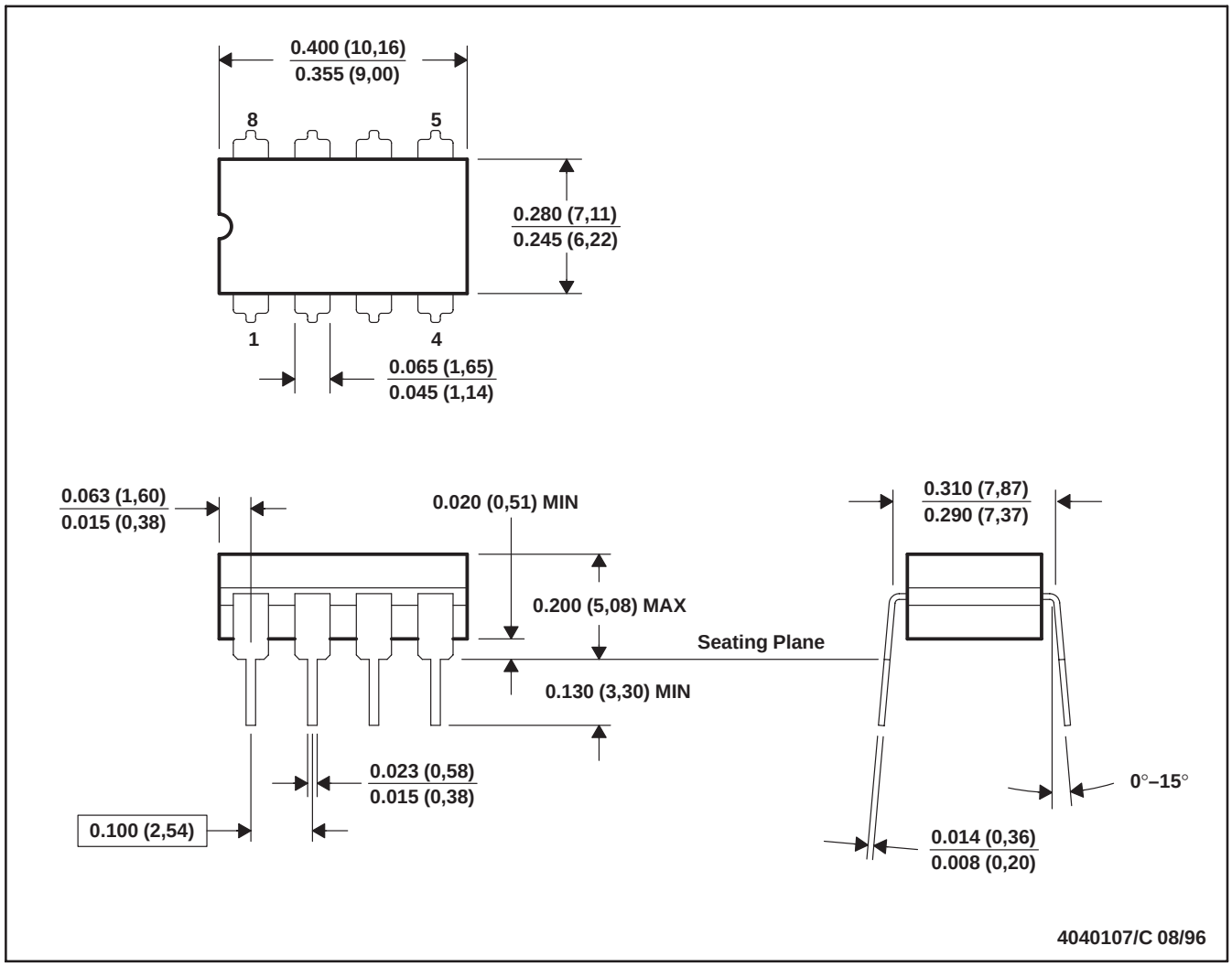
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

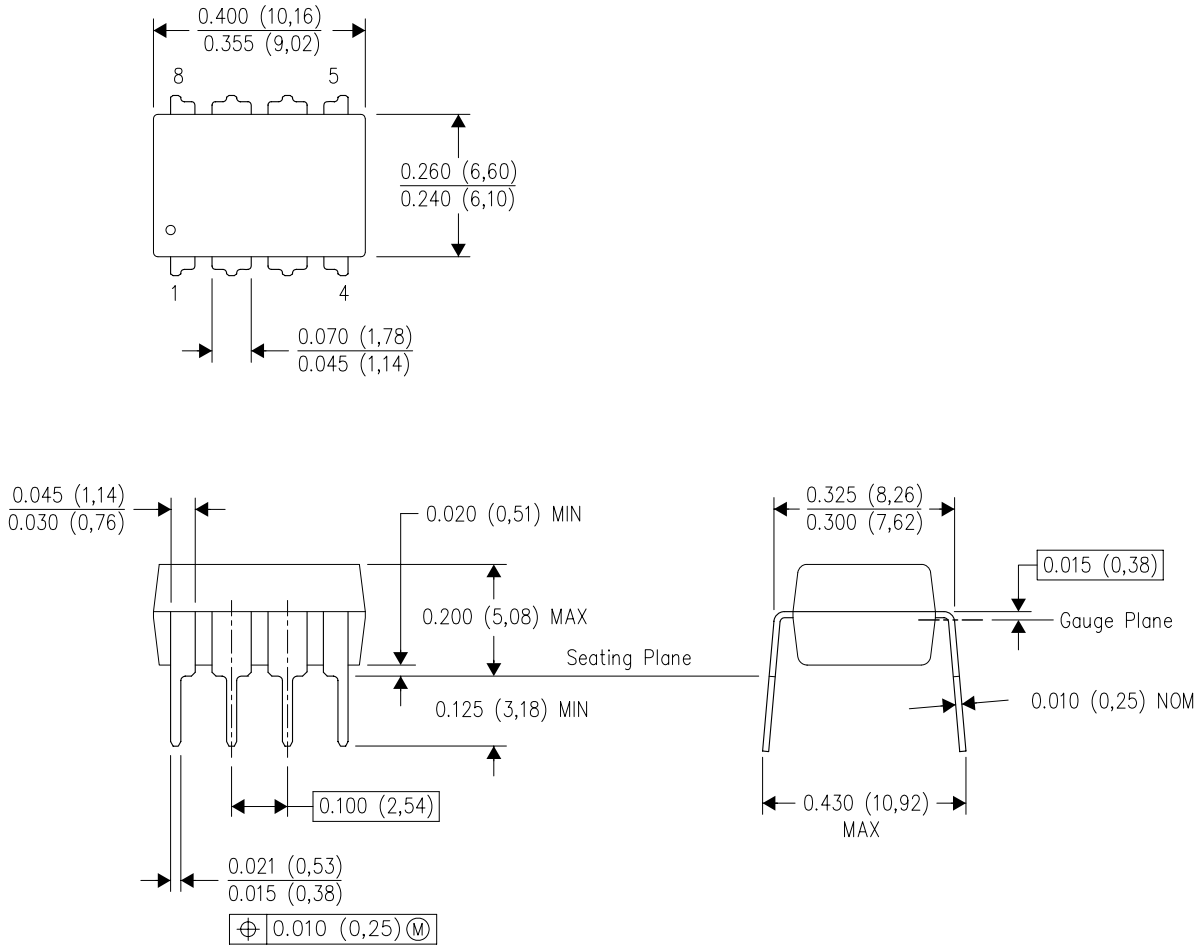
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

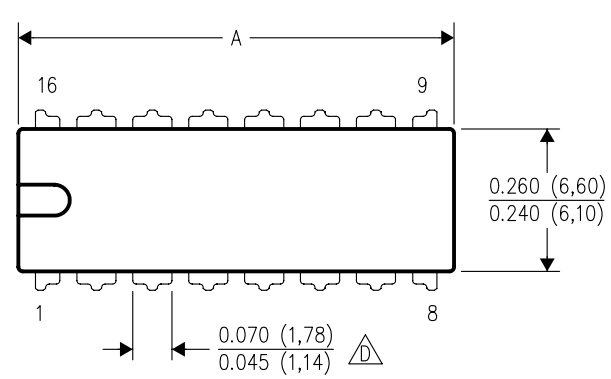


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

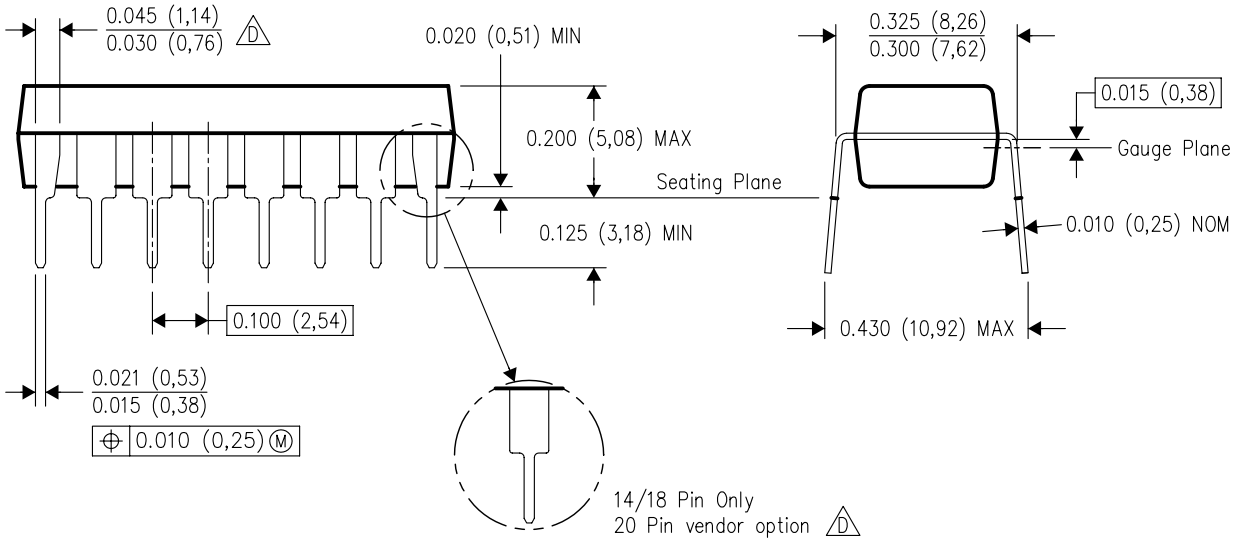
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

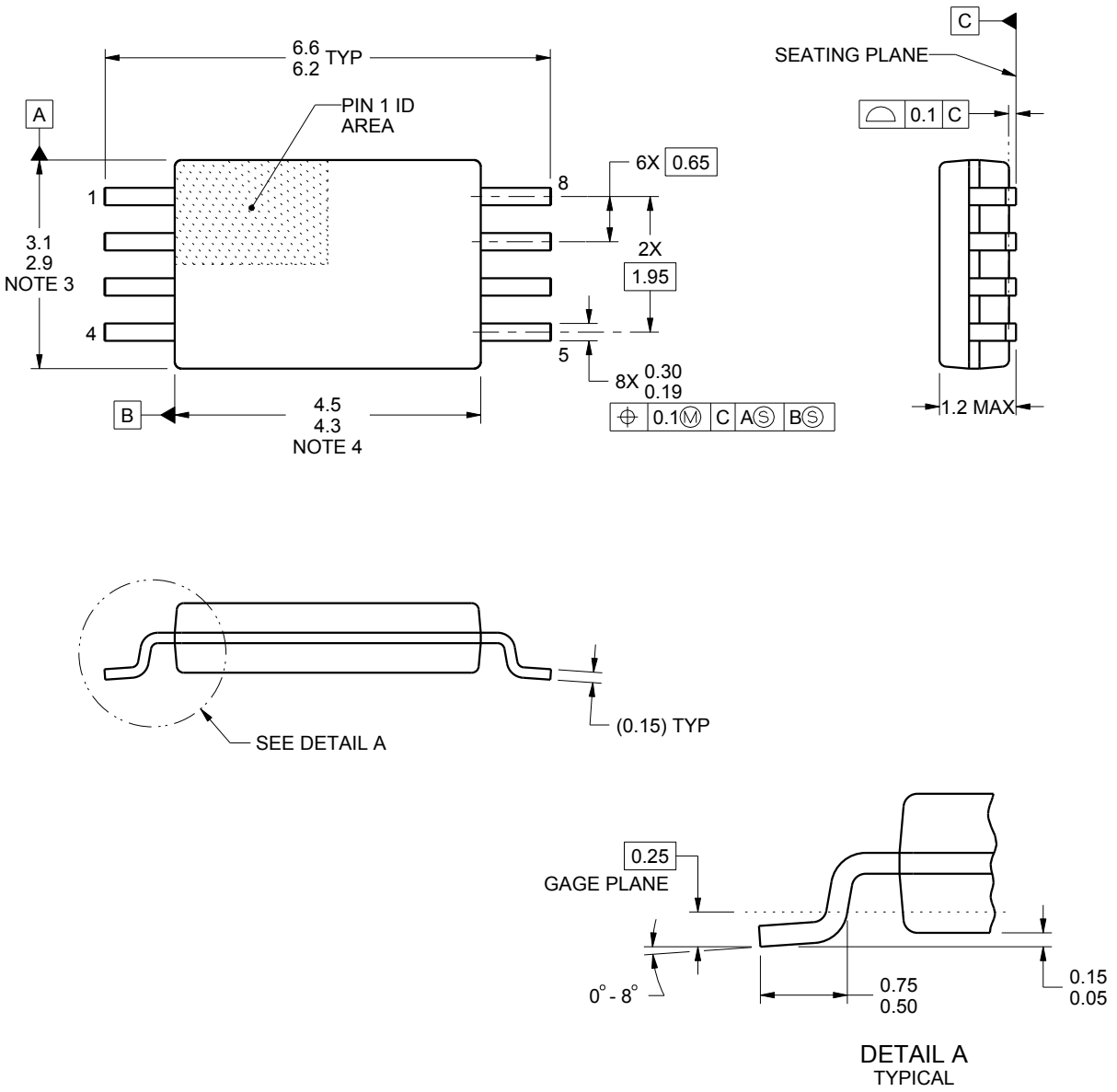
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

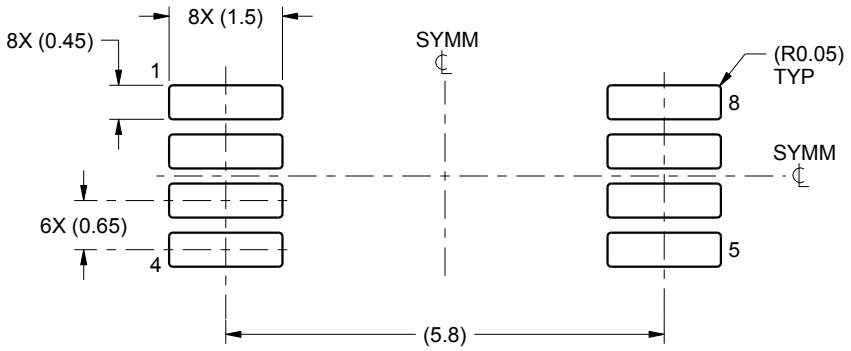
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

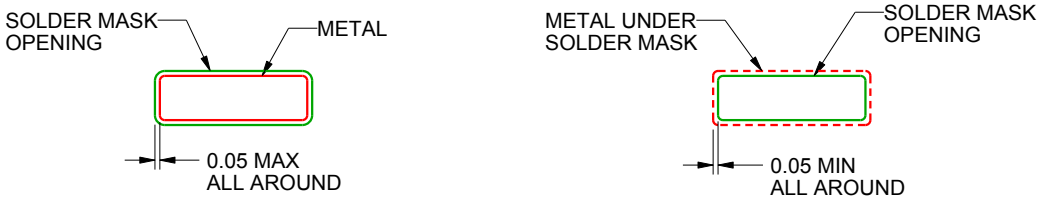


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

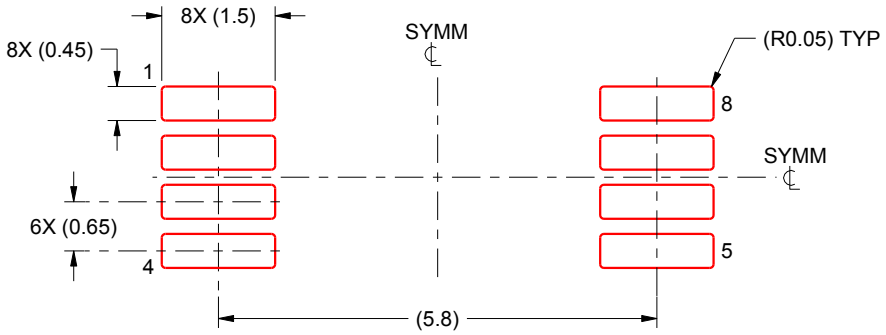


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

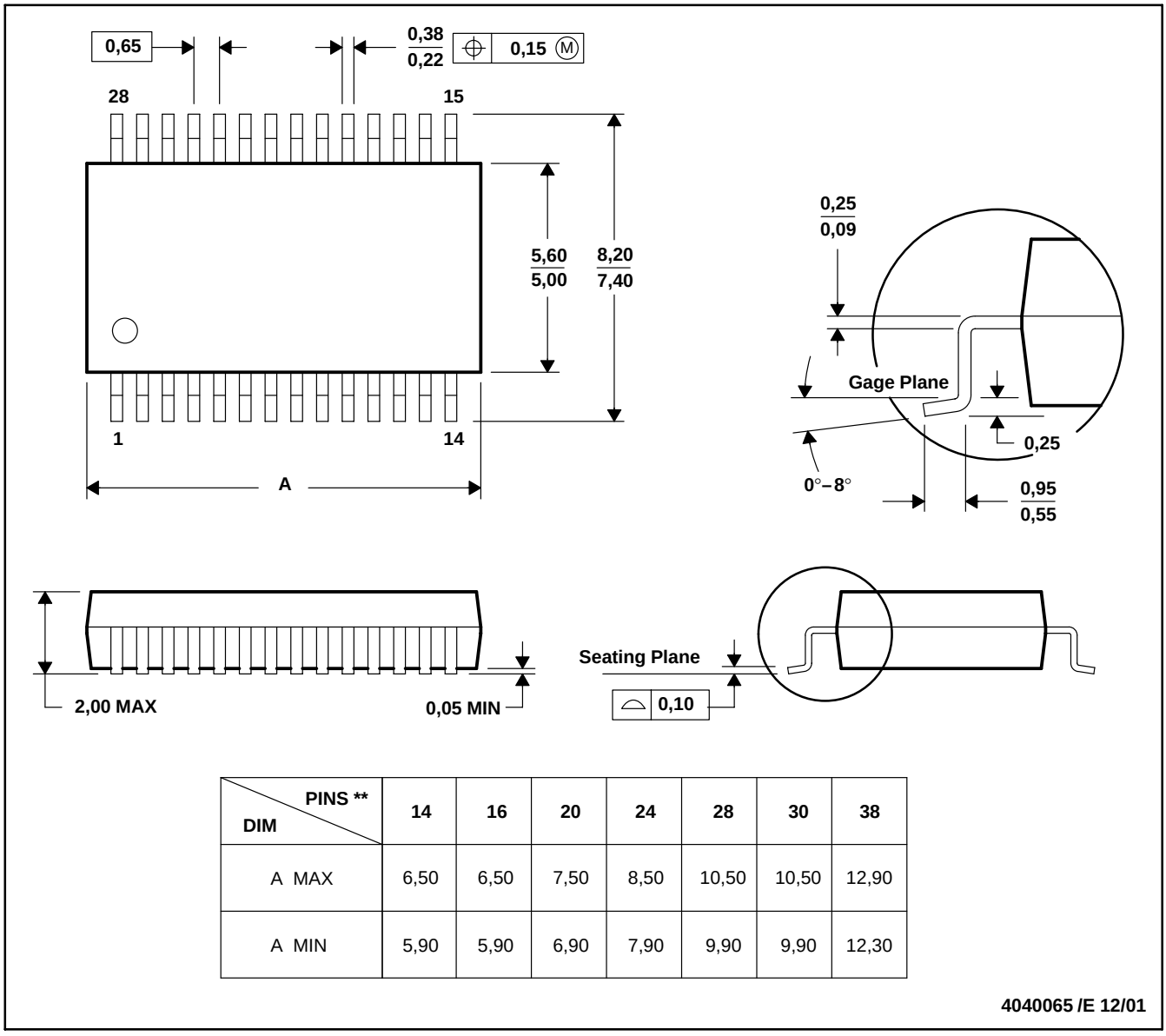
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

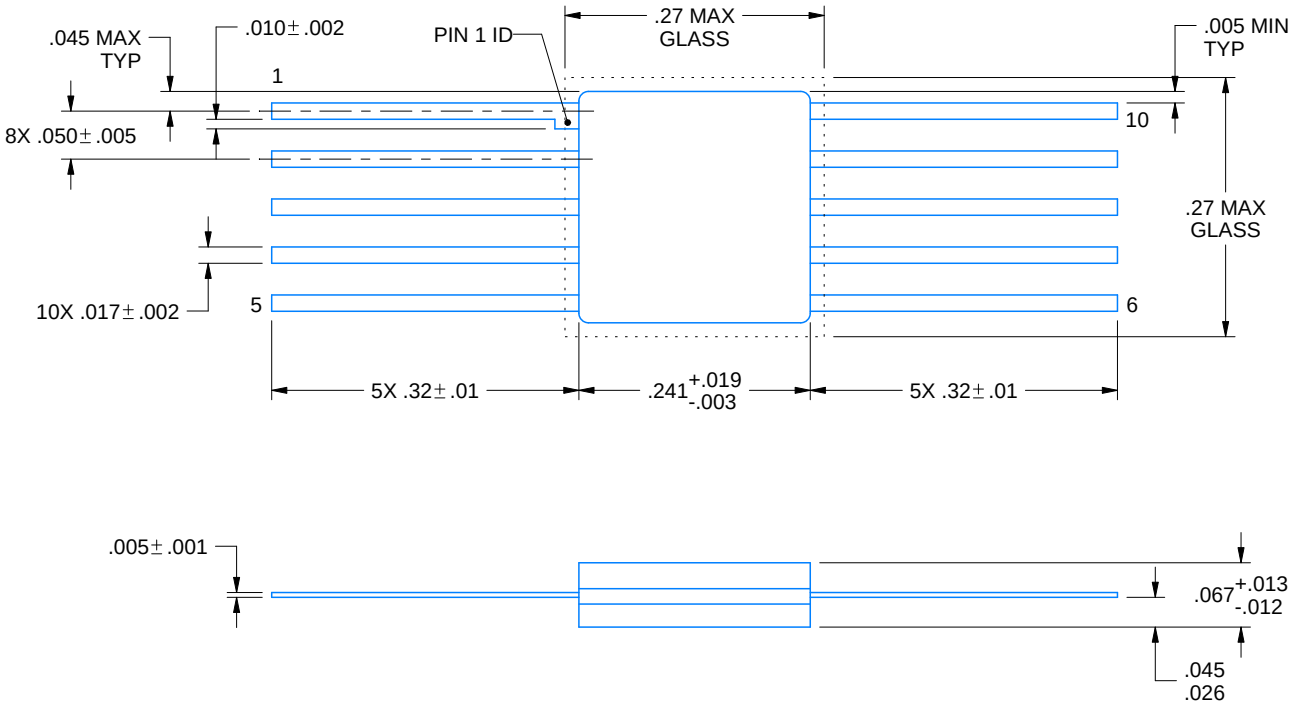
U0010A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



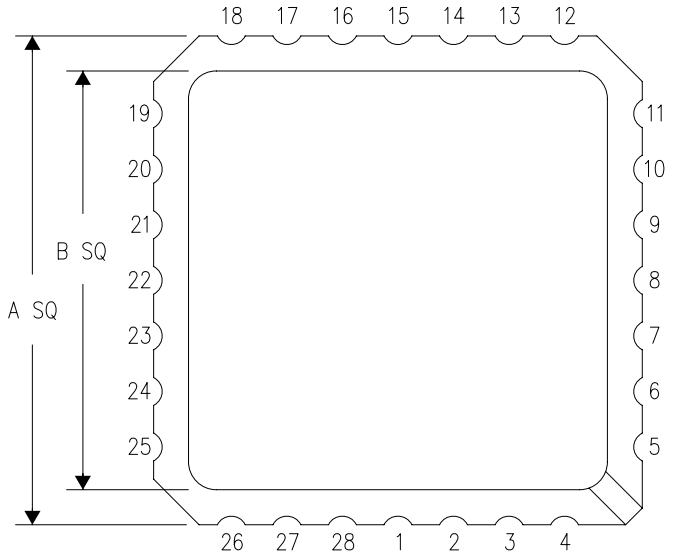
4225582/A 01/2020

NOTES:

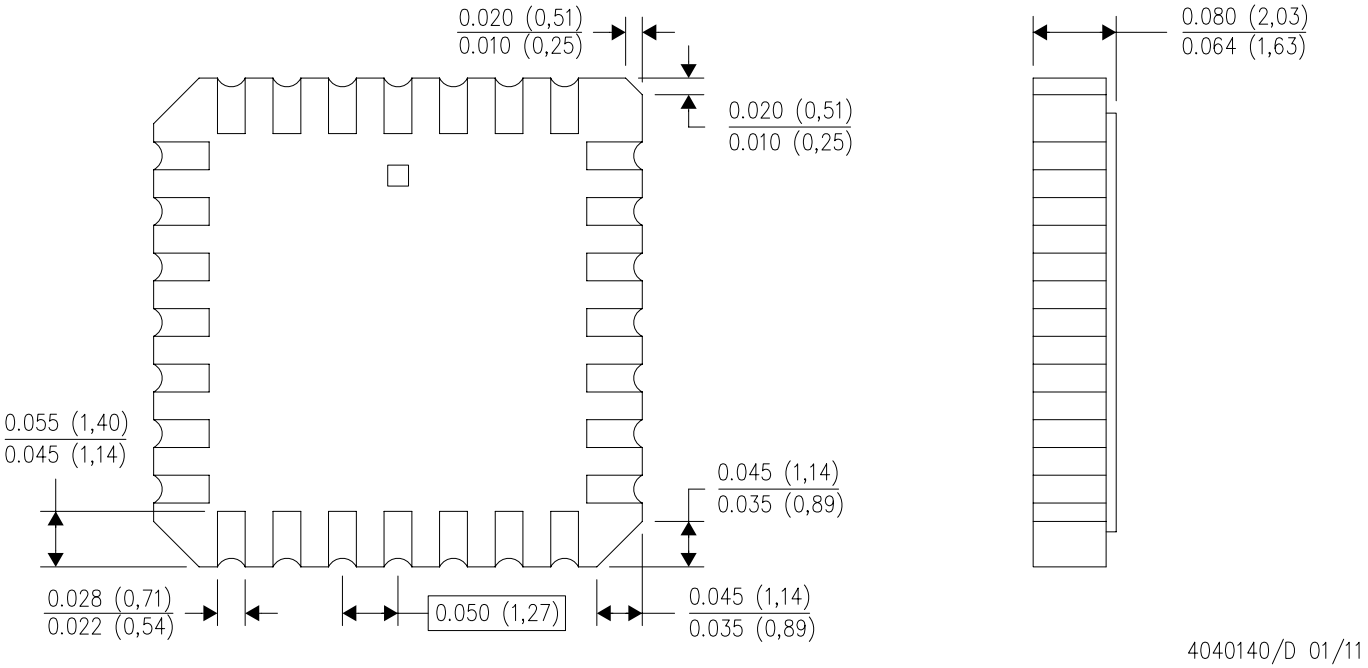
1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



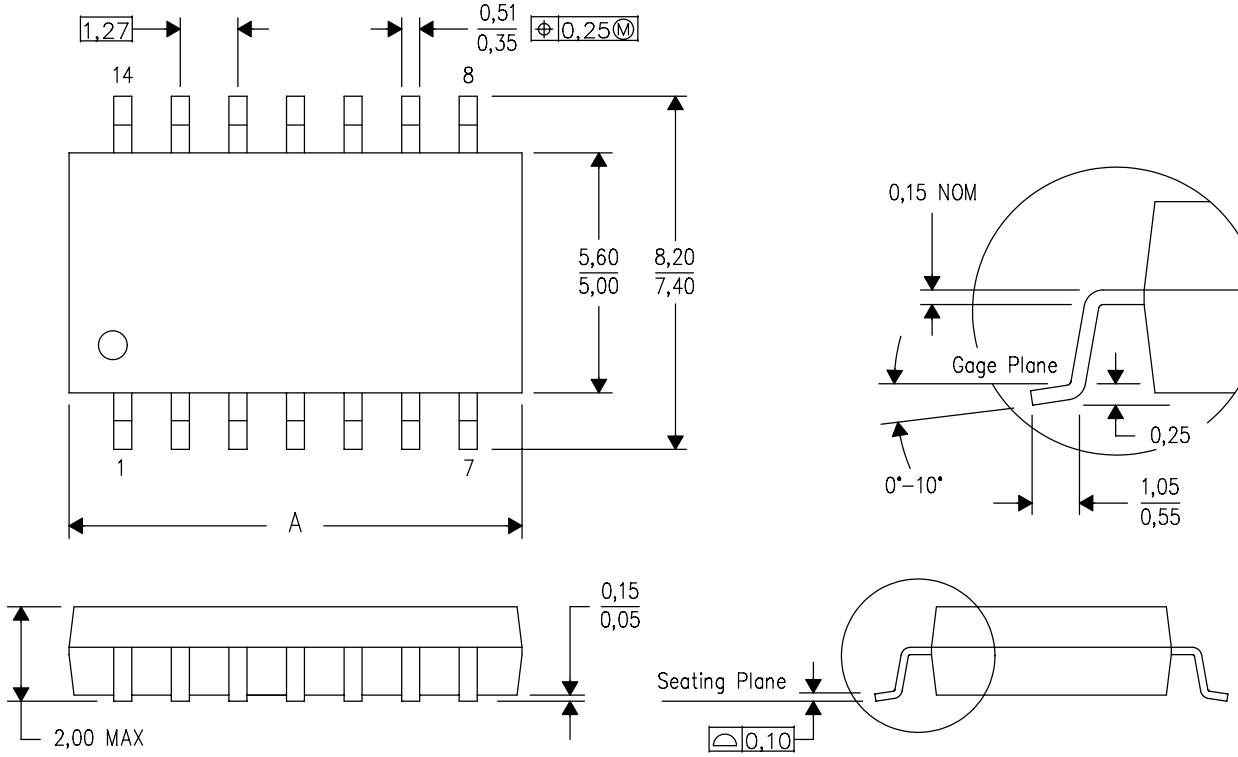
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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