TL7702B, TL7733B, and TL7705B Supply-Voltage Supervisors

1 Features

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- $\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1$ V
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- True and Complement Reset Outputs
- Externally Adjustable Pulse Duration

2 Applications

- Wireless communication systems
- Factory automation
- Building automation
- Servers
- Notebooks and Desktop computers
- STB and DVR

3 Description

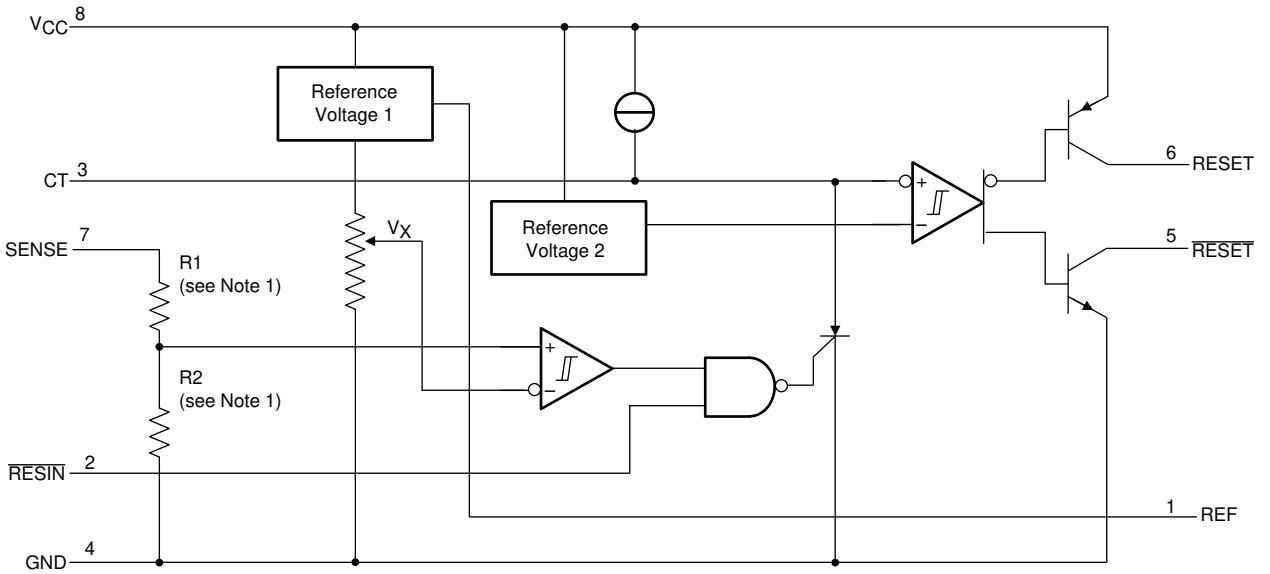
The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active.

The TL7702BC, TL7705BC, and TL7733BC are characterized for operation from 0°C to 70°C. The TL7702BI, TL7705BI, and TL7733BI are characterized for operation from –40°C to 85°C. The TL7705BQ is characterized for operation from –40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL77xxBD	SOIC (8)	4.90 mm × 3.91 mm
TL77xxBP	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision N (September 2016) to Revision O (December 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Corrected the $\overline{\text{RESIN}}$ pin description....3
- Corrected the I_{CC} parameter units from µA to mA in Electrical Characteristics Table....6

Changes from Revision M (May 2003) to Revision N (September 2016) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Deleted *Ordering Information* table; see POA at the end of the data sheet....1
- Deleted Lead temperature row....4
- Changed $R_{\theta JA}$ for D (SOIC) from 97 to 109.2 and for P (PDIP) from 85 to 51.4....5

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5 Pin Configuration and Functions

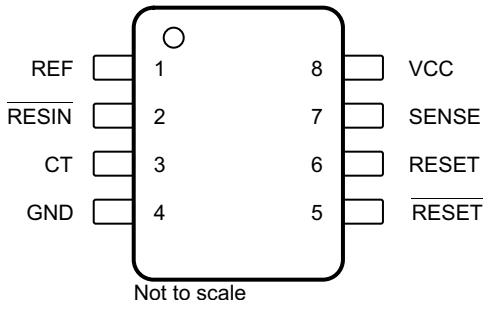


Figure 5-1. D or P Package 8-Pin SOIC or PDIP Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	3	O	Timing capacitor input. The timing capacitor determines the time delay that the reset outputs remain active after the voltage at the SENSE input exceeds the positive-going threshold value.
GND	4	—	Ground
REF	1	O	Reference voltage. See *Section 6.5* for reference voltage output and specification.
RESET	6	O	Active high reset. See Figure 6-1 for RESET function and timing.
$\overline{\text{RESET}}$	5	O	Active low reset. See Figure 6-1 for $\overline{\text{RESET}}$ function and timing.
$\overline{\text{RESIN}}$	2	I	Reset input. When the Reset Input is low, the RESET output goes high and the $\overline{\text{RESET}}$ goes low. When the Reset Input is high, the RESET and $\overline{\text{RESET}}$ outputs are allowed to trigger based on the SENSE voltage.
SENSE	7	I	Sense input. Voltage input to be supervised. See Figure 6-1 for SENSE function and timing.
VCC	8	—	Supply voltage. See *Section 6.3* for recommended voltage input range.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2), V_{CC}			20	V
Input voltage, V_I	$\overline{RESIN}$	–0.3	20	V
	SENSE	–0.3	20	
High-level output current, I_{OH} (RESET)			–30	mA
Low-level output current, I_{OL} ($\overline{RESET}$)			30	mA
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.6	18	V
V_{IH}	High-level input voltage	$\overline{RESIN}$	2	18	V
V_{IL}	Low-level input voltage	$\overline{RESIN}$	0	0.8	V
V_I	Input voltage	SENSE	0	18	V
I_{OH}	High-level output current	RESET		–20	mA
I_{OL}	Low-level output current	$\overline{RESET}$		20	mA
T_A	Operating free-air temperature	TL77xxBC	0	70	°C
		TL77xxBI	–40	85	
		TL7705BQ	–40	125	

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6.4 Thermal Information

THERMAL METRIC[1] [2]		TL77xxB		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.2	51.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	40.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.9	28.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.4	17.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.4	28.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

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6.5 Electrical Characteristics: TL77xxBC, TL77xxBI, and TL7705BQ

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC} – 1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{REF}	Reference voltage, REF		I_{ref} = –500 µA, T_A = 25°C	2.48	2.53	2.58	V
$V_{IT–}$	Negative-going input threshold voltage at SENSE input	TL7702B	T_A = 25°C	2.505	2.53	2.555	V
		TL7705B		4.5	4.55	4.6	
		TL7733B		3.03	3.08	3.13	
		TL7702B	T_A = full range(2)	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
		TL7733B		3	3.08	3.16	
V_{HYS}	Hysteresis, SENSE ($V_{IT+} – V_{IT–}$)	TL7702B	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
		TL7705B			30		
		TL7733B			10		
V_{RES}	Power-up reset voltage(3)		I_{OL} at $\overline{\text{RESET}}$ = 2 mA, T_A = 25°C			1	V
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 0.4 V to V_{CC}			–10	µA
		SENSE, TL7702B	V_I = V_{REF} to 18 V		–0.1	–2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V, see Figure 7-1			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0 V, see Figure 7-1			–50	µA
I_{CC}	Supply current		V_{SENSE} = 15 V, $\overline{\text{RESIN}}$ ≥ 2 V		1.8	3	mA
			V_{CC} = 18 V, T_A = full range(2)			3.5	

(1) All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and VCC to GND.
(2) Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –40°C to 125°C for the Q-suffix device.
(3) This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

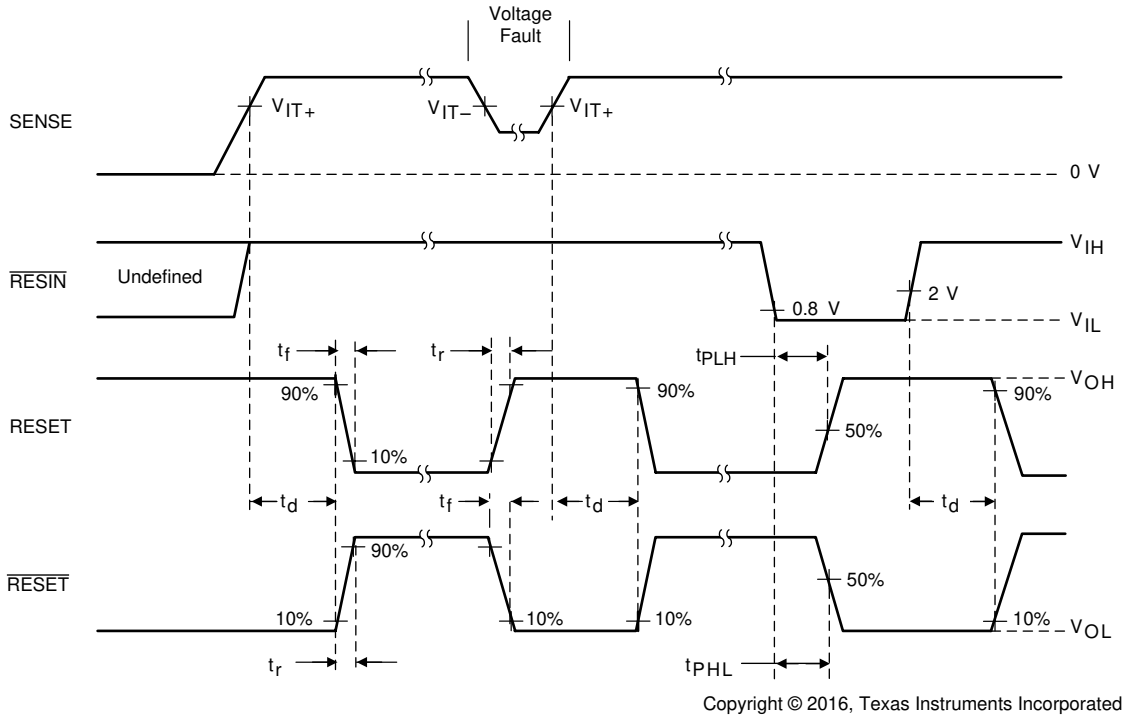
6.6 Switching Characteristics: TL77xxBC, TL77xxBI, and TL7705BQ

V_{CC} = 5 V, C_T open, T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from low-level to high-level output	$\overline{\text{RESIN}}$	RESET	See , Figure 6-1 Figure 6-2, Figure 7-1		270	500	ns
t_{PHL}	Propagation delay time from high-level to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	See Figure 6-1, Figure 6-2, Figure 7-2		270	500	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 7-3,Figure 7-4		150		ns
		SENSE				100		
t_r	Rise time		RESET	See Figure 6-1, Figure 7-1, Figure 7-2			75	ns
			$\overline{\text{RESET}}$			75	150	
t_f	Fall time		RESET	See Figure 6-1, Figure 7-1, Figure 7-2		150	200	ns
			$\overline{\text{RESET}}$				50	

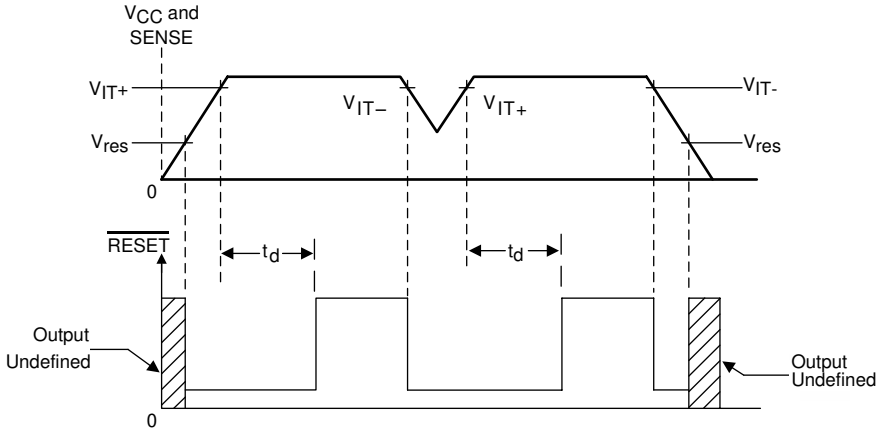
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6.7 Timing Diagrams



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Figure 6-1. TL7702B, TL7705B, and TL7733B Timing Diagram



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Figure 6-2. V_{IT} and V_{RES} Timing Diagram

6.8 Typical Characteristics

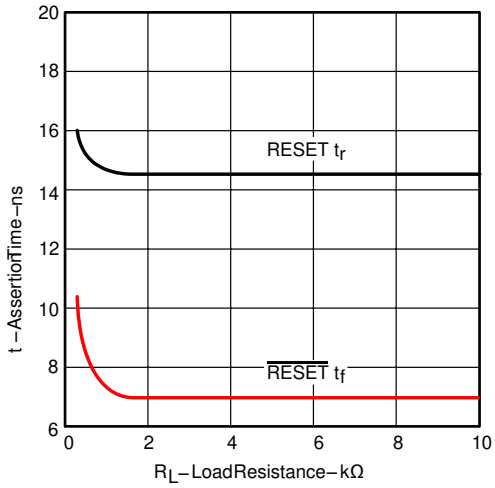


Figure 6-3. Assertion Time vs Load Resistance

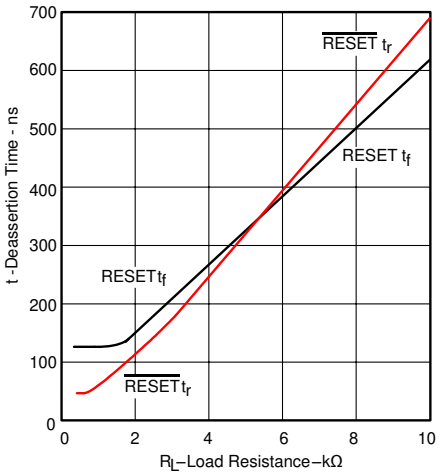


Figure 6-4. Deassertion Time vs Load Resistance

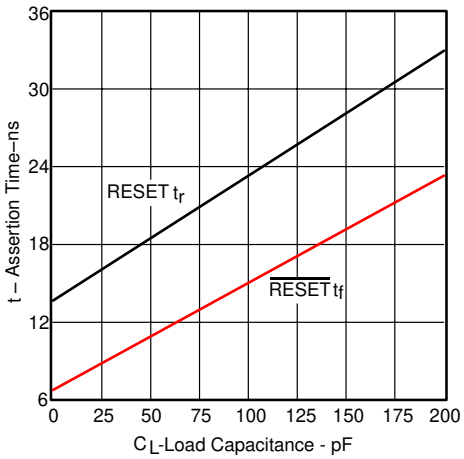


Figure 6-5. Assertion Time vs Load Capacitance

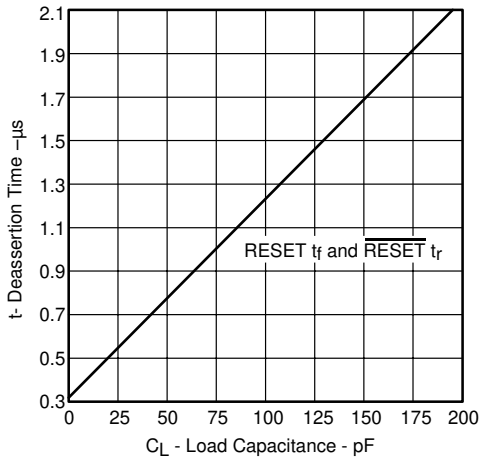
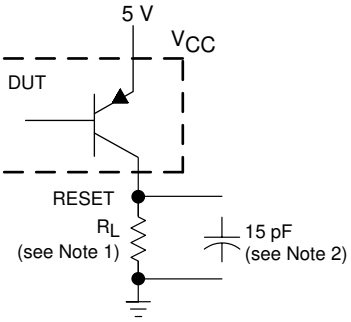


Figure 6-6. Deassertion Time vs Load Capacitance

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7 Parameter Measurement Information

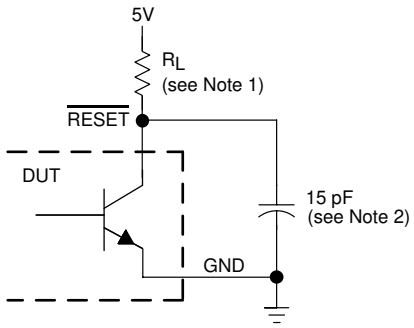


RESET OUTPUT CONFIGURATION

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A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

Figure 7-1. RESET Output Configuration



$\overline{\text{RESET}}$ OUTPUT CONFIGURATION

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A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

Figure 7-2. $\overline{\text{RESET}}$ Output Configuration

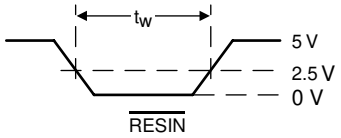


Figure 7-3. Input Pulse Definition RESIN

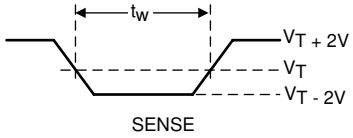


Figure 7-4. Input Pulse Definition SENSE

8 Detailed Description

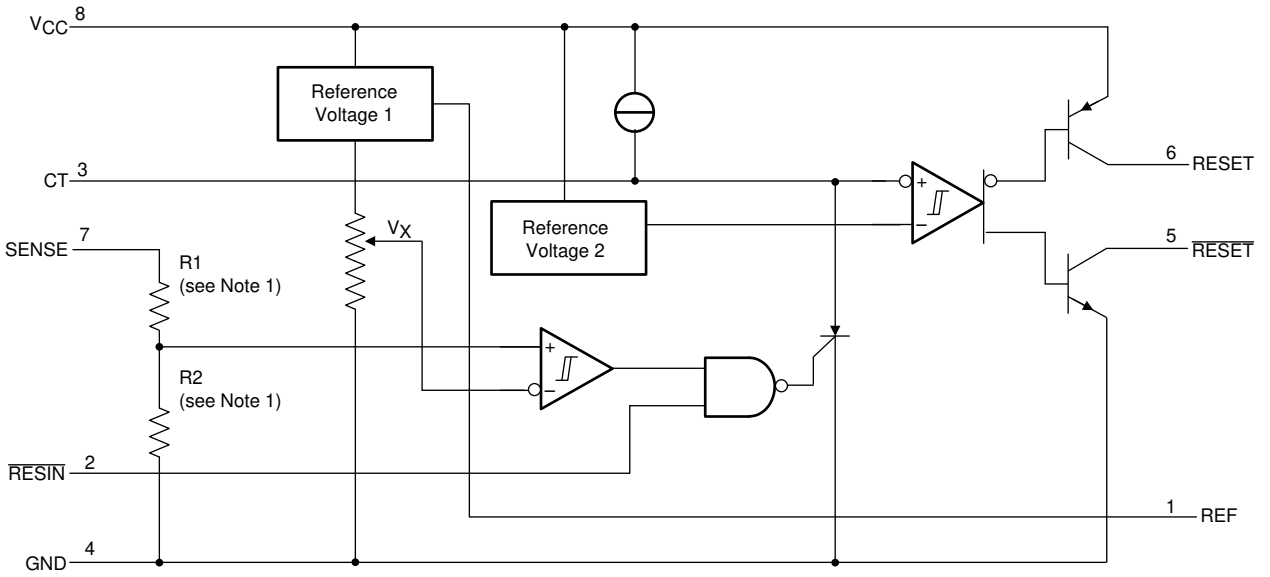
8.1 Overview

The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay-timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 µF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

8.2 Functional Block Diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



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8.3 Feature Description

8.3.1 Wide Supply-Voltage Range

The TL77xxB family operates using a wide supply voltage from 3.6 V to 18 V.

8.3.2 Adjustable Pulse Duration

The CT pin enables the ability to set a user-defined time delay in order to ensure that the fault condition is recognized. The external capacitor charges based on an internal current source until the voltage at the CT pin exceeds that of the internal reference voltage.

The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

The current source to charge the timing capacitor varies ±15%. Reference Voltage 2 is approximately 1.8 V and varies approximately ±5%. Once the timing capacitor charges, it discharges to about 0.6 V, not completely to 0 V.

8.4 Device Functional Modes

Figure 8-1 displays how the RESET and $\overline{\text{RESET}}$ output pins respond to the change in the the SENSE and $\overline{\text{RESIN}}$ input pins. When the $\overline{\text{RESIN}}$ pin is high, the RESET outputs are able to respond to a drop in the supply voltage at the SENSE pin. When the RESIN pin is low, the RESET and $\overline{\text{RESET}}$ pins are set HIGH and LOW respectively.

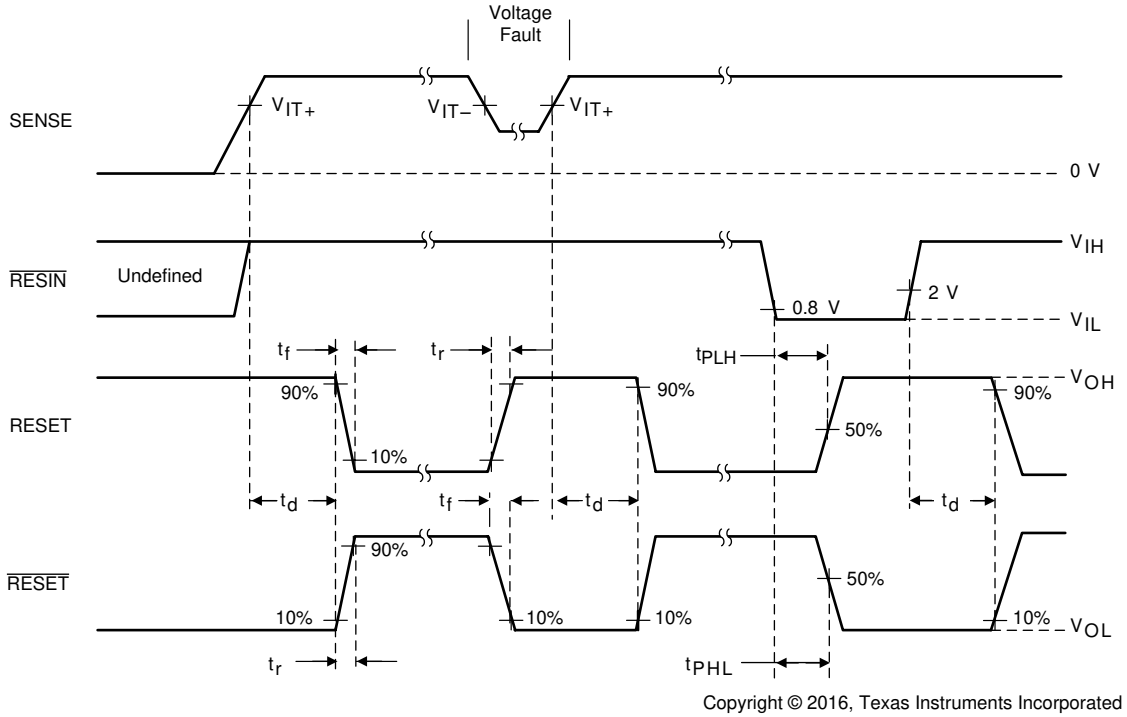


Figure 8-1. TL77xxB RESET and $\overline{\text{RESET}}$ Response and Timing

9 Application and Implementation

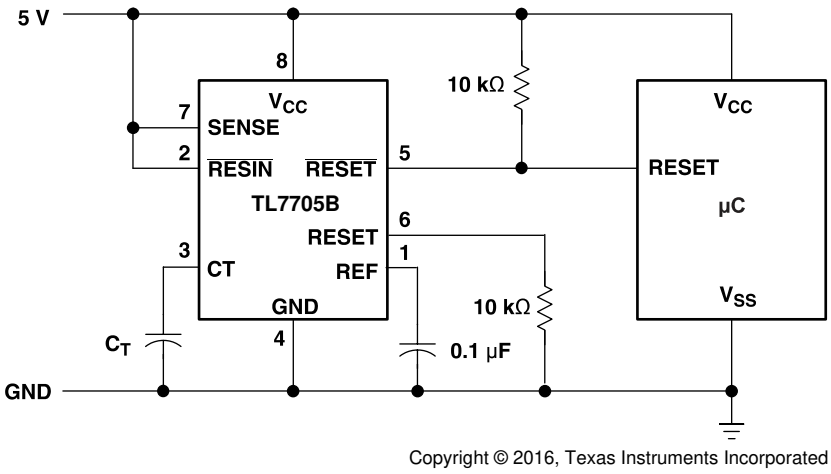
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Figure 9-1 shows an application where the TL7705B device is being used to sense the voltage supply for a microcontroller that is supplied with 5 V. If the voltage supply drops below the threshold voltage, the $\overline{\text{RESET}}$ pin is pulled LOW, signaling the microcontroller to reset.

9.2 Typical Application



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Figure 9-1. Reset Controller Schematic for a Microprocessor

9.2.1 Design Requirements

The external components required include the decoupling capacitor for the REF pin and the timing capacitor for the CT pin. Additionally, because the $\overline{\text{RESET}}$ output is open collector, a pullup resistor is required to ensure the correct HIGH level for the microcontroller RESET pin.

9.2.2 Detailed Design Procedure

TI recommends pullup and pulldown resistors of 10 kΩ.

To achieve a 2.6 ms time delay, use C_T = 0.1 μF.

Both outputs of the TL770xB must be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset

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9.2.3 Application Curve

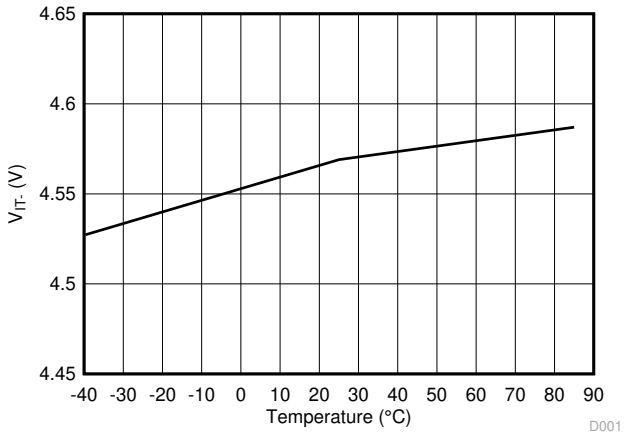


Figure 9-2. TL7705B Threshold Voltage vs Temperature

10 Power Supply Recommendations

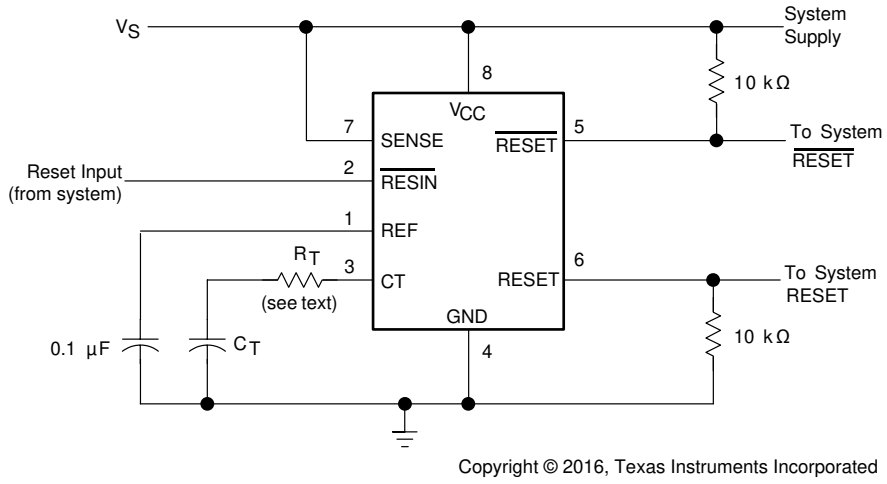


Figure 10-1. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC}, TI recommends a current-limiting resistor in series with C_T. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈7.1-V Zener), whichever is less. When the circuit then is subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC}. This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below $V_{T–}$.

Adding the external resistor, R_T, prevents false triggering. Its value is calculated as follows:

$$(V_{(CT)} – V_{T-}) / R_T \quad (1)$$

where

- $V_{(CT)} = V_{CC}$ or 7.1 V, whichever is less
- $V_{T–} = 4.55$ V (nom)
- R_T = value of series resistor required

For $V_{CC} = 5$ V

$$(5 – 4.55) / R_T < 1 \text{ mA} \quad (2)$$

Therefore,

$$R_T > 450\ \Omega \quad (3)$$

Using a 20%-tolerance resistor, R_T should be greater than 560 Ω.

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T, but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB must be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

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11 Layout

11.1 Layout Guidelines

Figure 11-1 shows an example layout for the TL7705B device. As the $\overline{\text{RESET}}$ and RESET pins are open collector outputs, place pullup and pulldown resistors on the $\overline{\text{RESET}}$ and RESET pins respectively. A capacitor must be placed on the REF pin to stabilize the reference. This can help to prevent false triggering if noise couples into the reference.

11.2 Layout Example

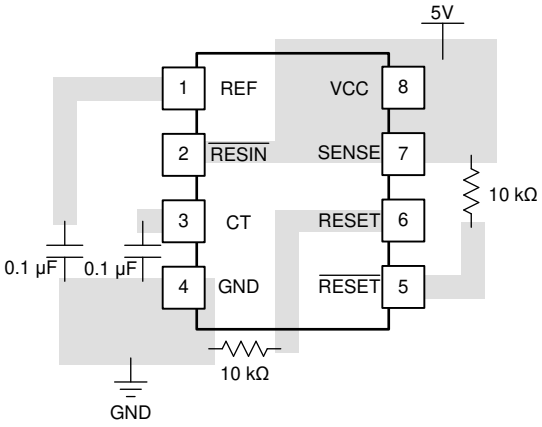


Figure 11-1. TL7705B Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL7702B	Click here	Click here	Click here	Click here	Click here
TL7705B	Click here	Click here	Click here	Click here	Click here
TL7733B	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7702BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7702BCP	Samples
TL7702BCPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7702BCP	Samples
TL7702BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7702BIP	Samples
TL7705BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7705BCP	Samples
TL7705BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7705BIP	Samples
TL7705BQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7705BQDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7705BQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7705BQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7733BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7733BCP	Samples
TL7733BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7733BIP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

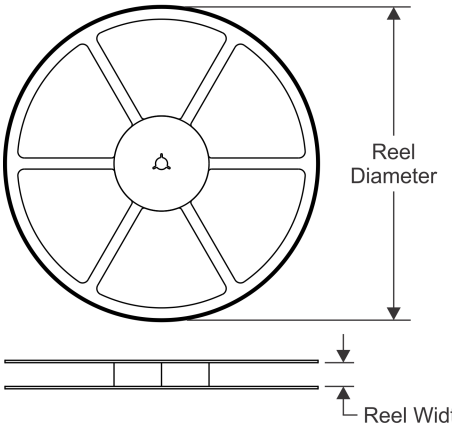
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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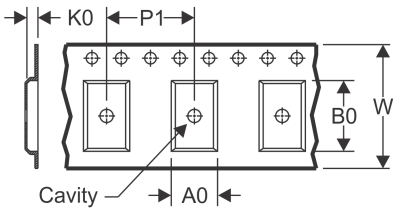
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

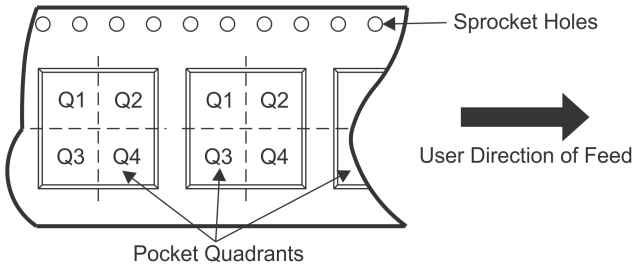


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

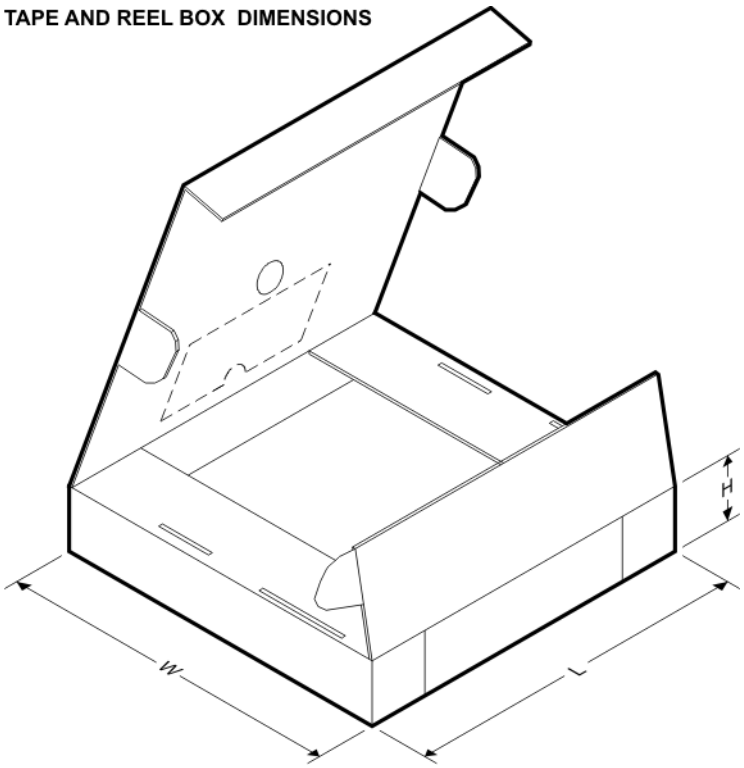
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

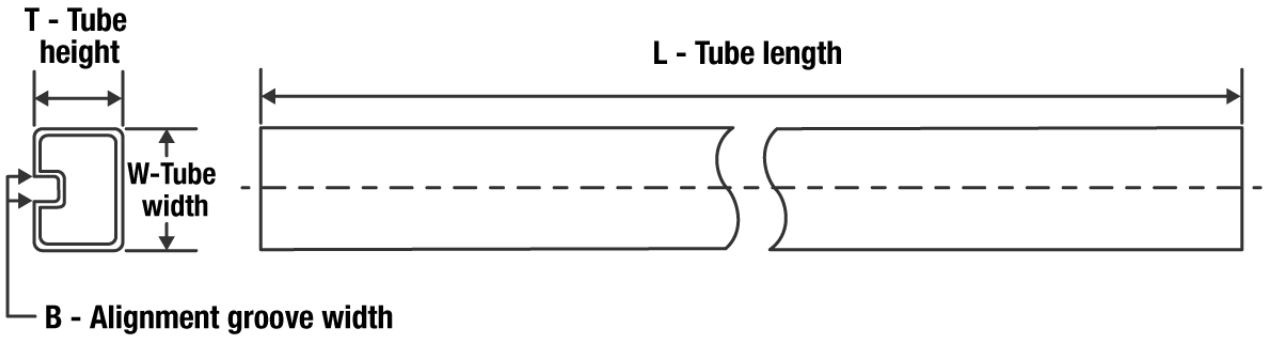
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

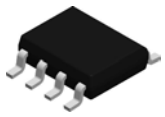
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7702BIDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7705BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7705BIDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7705BQDR	SOIC	D	8	2500	350.0	350.0	43.0
TL7705BQDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TL7733BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7733BIDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL7702BCD	D	SOIC	8	75	507	8	3940	4.32
TL7702BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7702BCPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL7702BID	D	SOIC	8	75	507	8	3940	4.32
TL7702BIP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BCD	D	SOIC	8	75	507	8	3940	4.32
TL7705BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BID	D	SOIC	8	75	507	8	3940	4.32
TL7705BIDE4	D	SOIC	8	75	507	8	3940	4.32
TL7705BIP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BQD	D	SOIC	8	75	505.46	6.76	3810	4
TL7705BQDG4	D	SOIC	8	75	505.46	6.76	3810	4
TL7733BCD	D	SOIC	8	75	507	8	3940	4.32
TL7733BCDE4	D	SOIC	8	75	507	8	3940	4.32
TL7733BCDG4	D	SOIC	8	75	507	8	3940	4.32
TL7733BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7733BID	D	SOIC	8	75	507	8	3940	4.32
TL7733BIDG4	D	SOIC	8	75	507	8	3940	4.32
TL7733BIP	P	PDIP	8	50	506	13.97	11230	4.32

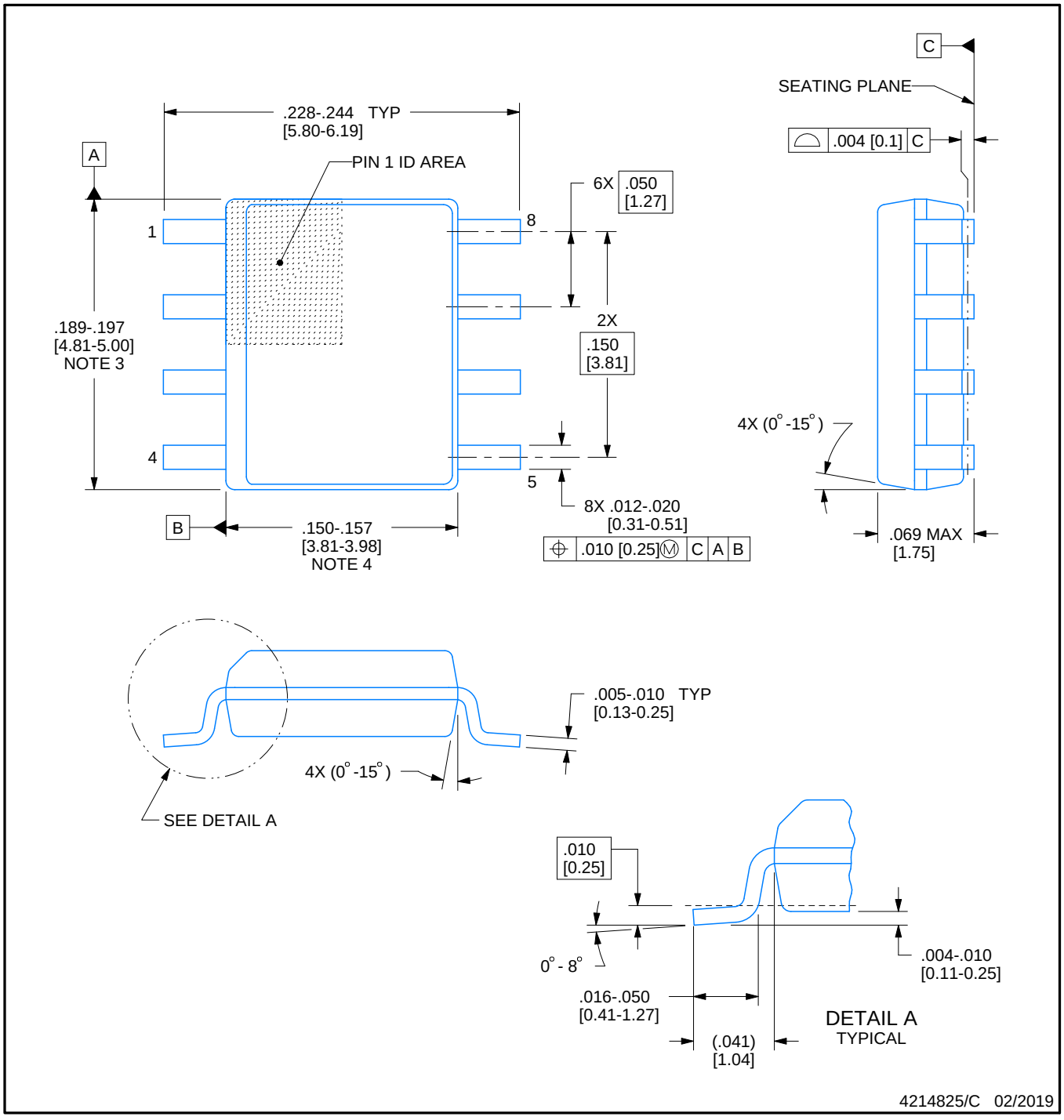


PACKAGE OUTLINE

D0008A

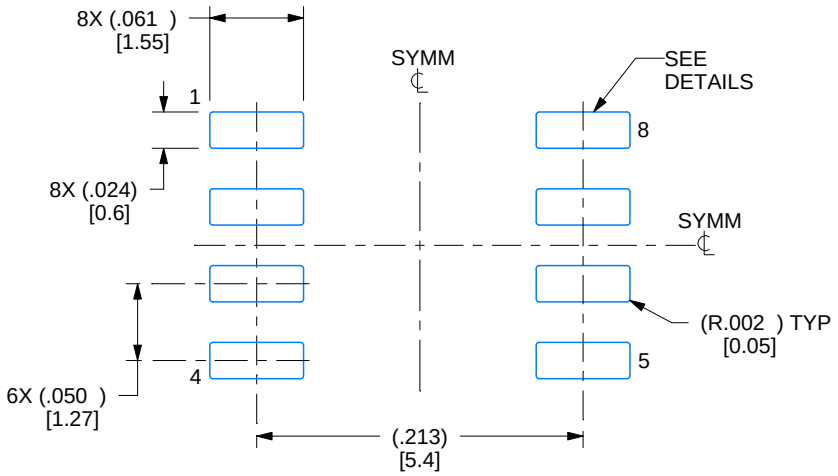
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

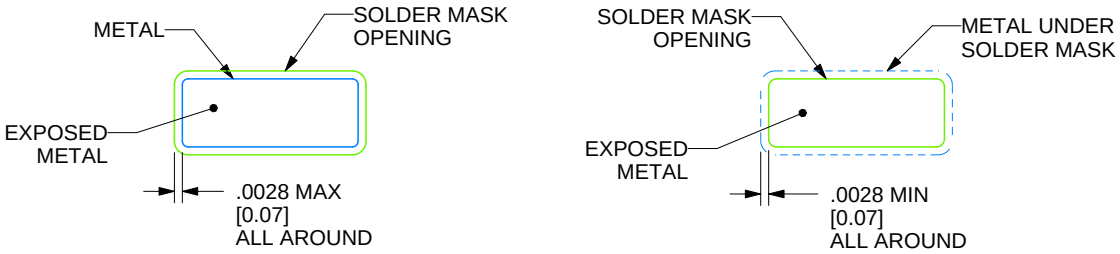


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

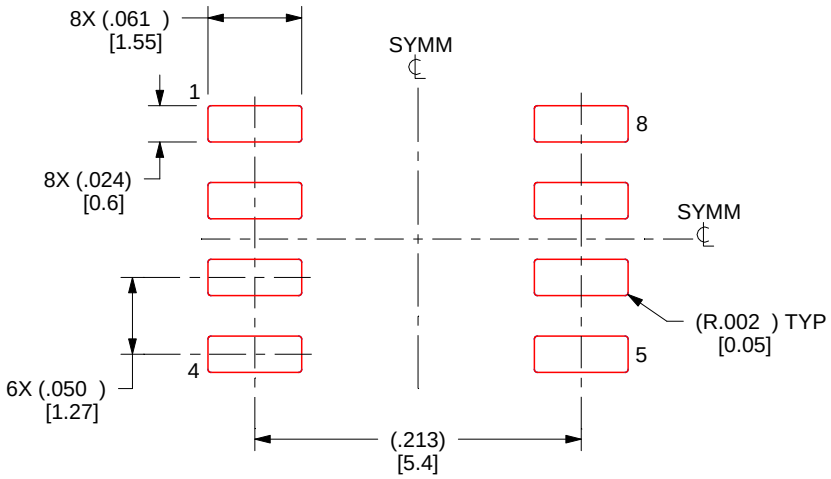
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



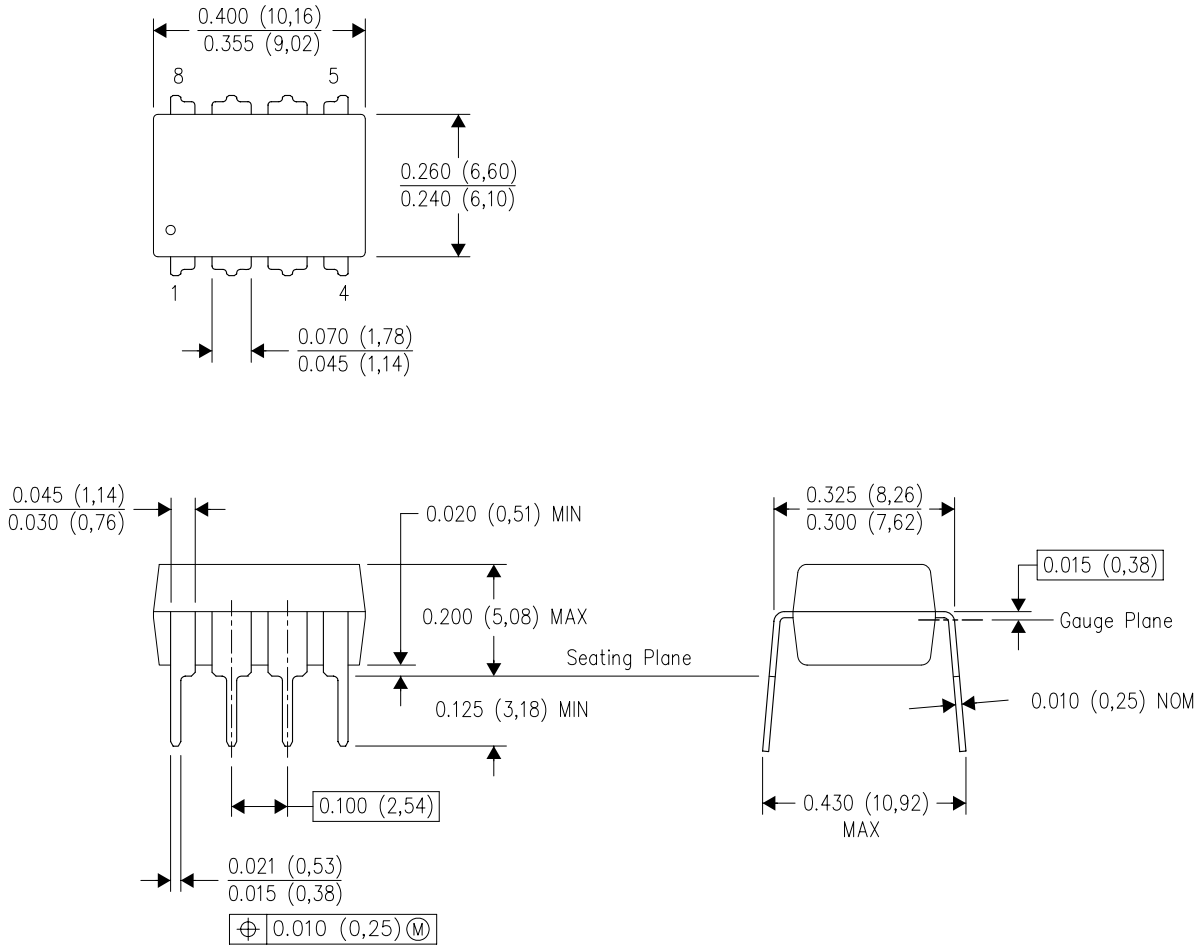
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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