TL720M05-Q1 Low-Dropout Voltage Regulator

1 Features

- Qualified for Automotive Applications
- Output Voltage of 5 V ±2%
- Very Low Current Consumption
- Very Low Dropout Voltage
- Short-Circuit Protection
- Reverse-Polarity Protection
- ESD Protection > 6 kV

2 Applications

- Qualified for Automotive Applications
- Cluster
- Body Control Modules

3 Description

The TL720M05-Q1 devices are monolithic integrated low-dropout voltage regulators offered in 3-pin TO packages. They regulate an input voltage up to 45 V to V_{OUT} of 5 V with 2% tolerance. The devices can drive loads up to 450 mA and are short-circuit proof. At overtemperature, the incorporated temperature protection turns off the TL720M05-Q1 devices.

The input capacitor (C_{IN}) compensates for line fluctuation. Using a resistor of approximately 1 Ω in series with C_{IN} dampens the oscillation of input inductivity and input capacitance. The output capacitor (C_{OUT}) stabilizes the regulation circuit. Output is stable at C_{OUT} ≥ 22 µF and ESR ≤ 5 Ω, within the operating temperature range.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor through a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against:

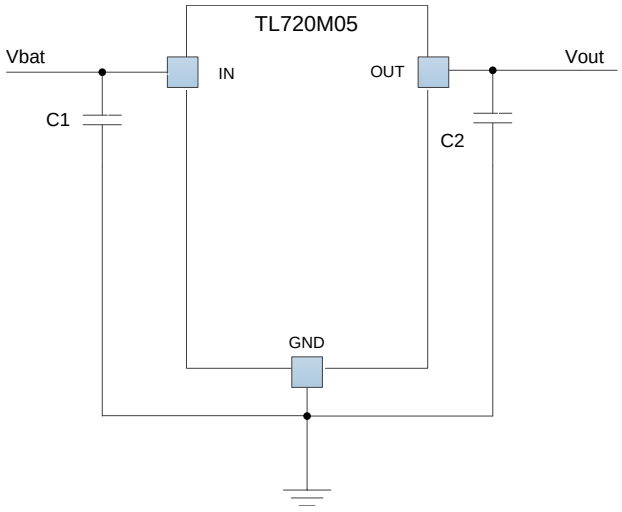
- Overload
- Overtemperature
- Reverse polarity

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL720M05-Q1	DDPAK/TO-263 (3)	10.18 mm × 8.41 mm
	TO-252 (3)	6.60 mm × 6.10 mm
	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2013) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

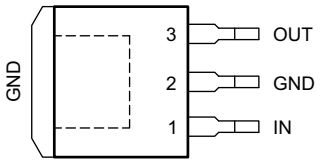
Changes from Revision F (May 2013) to Revision G — **Page**

- Removed Ordering Information table. ... 1

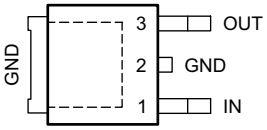
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5 Pin Configuration and Functions

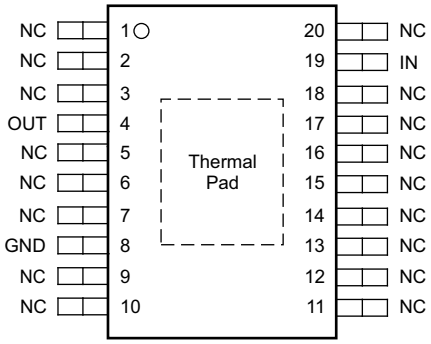
KTT Package
3-Pin TO-263
Top View



KVU Package
3-Pin TO-252
Top View



PWP Package(1)
20-Pin HTSSOP With PowerPAD
Top View



(1) NC - No internal connection

Pin Functions

PIN				I/O	DESCRIPTION
NAME	TO-263	TO-252	HTSSOP		
IN	1	1	19	I	Input voltage. Connect to ground as close to device as possible, through a ceramic capacitor.
GND	2	2	8	O	Ground. Internally connected to heatsink
OUT	3	3	4	O	Output. Connect to ground with ≥ 22-µF capacitor, ESR < 5 Ω at 10 kHz.
NC	—	—	1, 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14,15, 16, 17, 18, 20	—	Not connected

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Input voltage(2)	–42	45	V
V_O	Output voltage	–1	40	V
T_J	Operating virtual-junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±6000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	5.5		42	V
T_A	Operating free-air temperature	–40		125	°C
T_J	Operating virtual-junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TL720M05-Q1			UNIT
		KTT (TO-263)	KVU (TO-252)	PWP (HTSSOP)	
		3 PINS	3 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.2	45.3	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	36.8	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.9	30.8	19.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6	2.8	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.5	30.2	18.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	0.7	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953

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6.5 Electrical Characteristics

over recommended operating free-air temperature range, V_I = 13.5 V, T_J = −40°C to 150°C (unless otherwise noted) (see Figure 13)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 5 mA to 400 mA, V_I = 6 V to 28 V		4.9	5	5.1	V
		I_O = 5 mA to 200 mA, V_I = 6 V to 40 V		4.9	5	5.1	
I_O	Output current limit			450	700	950	mA
I_Q	Current consumption $I_q = I_I - I_O$	I_O = 1 mA	T_J = 25°C		100	220	µA
			$T_J \le$ 85°C		100	220	
		I_O = 250 mA			5	10	mA
		I_O = 400 mA			12	22	
V_{DO}	Dropout voltage(1)	I_O = 300 mA, $V_{do} = V_I - V_O$			250	500	mV
	Load regulation	I_O = 5 mA to 400 mA			15	30	mV
	Line regulation	ΔV_I = 8 to 32 V, I_O = 5 mA		–15	5	15	mV
PSRR	Power-supply ripple rejection	f_r = 100 Hz, V_r = 0.5 V_{pp}			60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift				0.5		mV/K

(1) Measured when the output voltage V_O has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

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6.6 Typical Characteristics

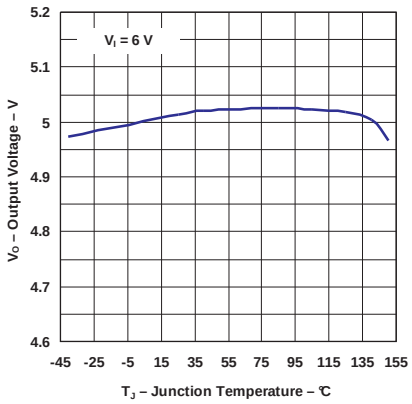


Figure 1. Output Voltage vs Junction Temperature

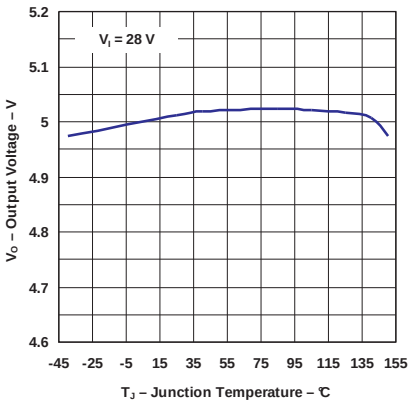


Figure 2. Output Voltage vs Junction Temperature

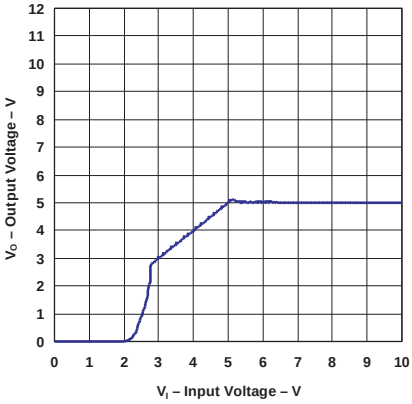


Figure 3. Output Voltage vs Input Voltage

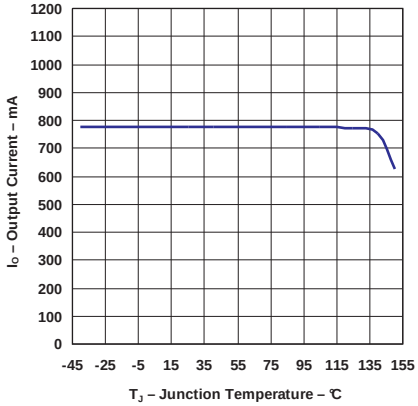


Figure 4. Output Current vs Junction Temperature

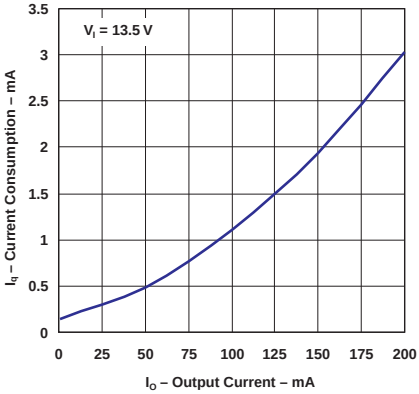


Figure 5. Current Consumption vs Output Current

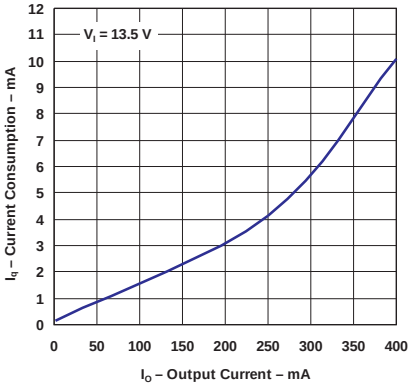


Figure 6. Current Consumption vs Output Current

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Typical Characteristics (continued)

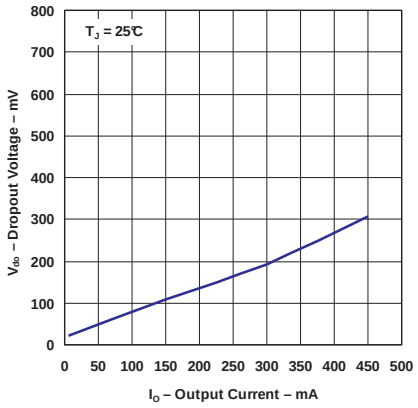


Figure 7. Dropout Voltage vs Output Current

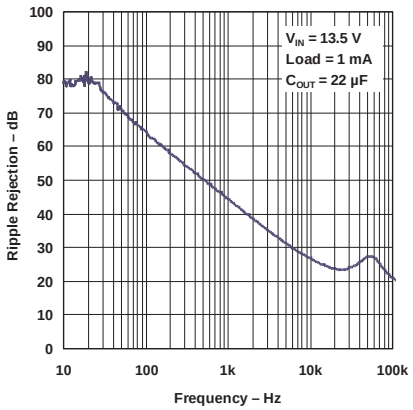


Figure 8. Power-Supply Ripple Rejection vs Frequency

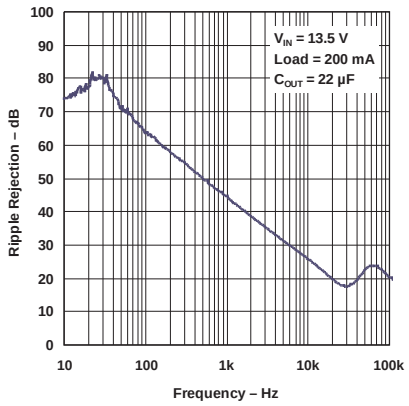


Figure 9. Power-Supply Ripple Rejection vs Frequency

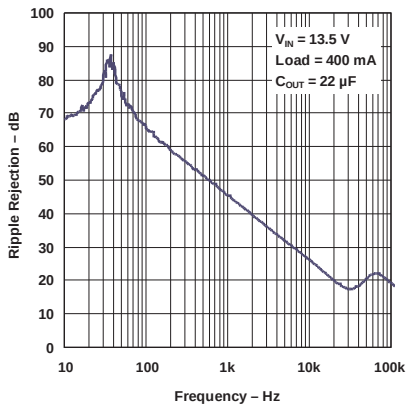


Figure 10. Power-Supply Ripple Rejection vs Frequency

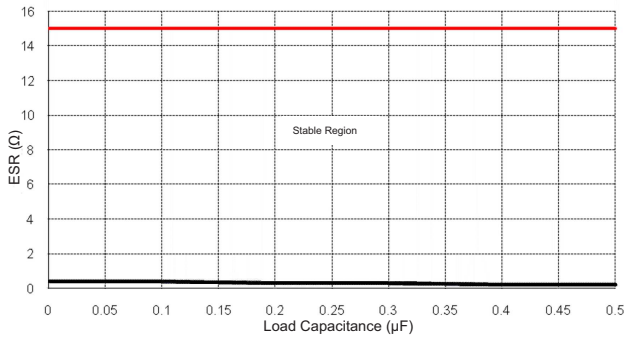


Figure 11. ESR Stability vs Load Current

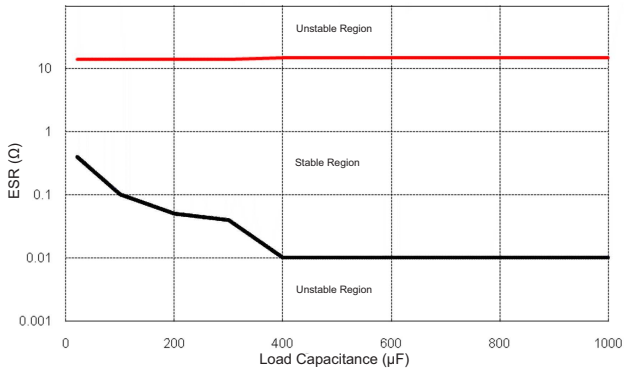


Figure 12. ESR Stability vs Load Capacitance

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7 Parameter Measurement Information

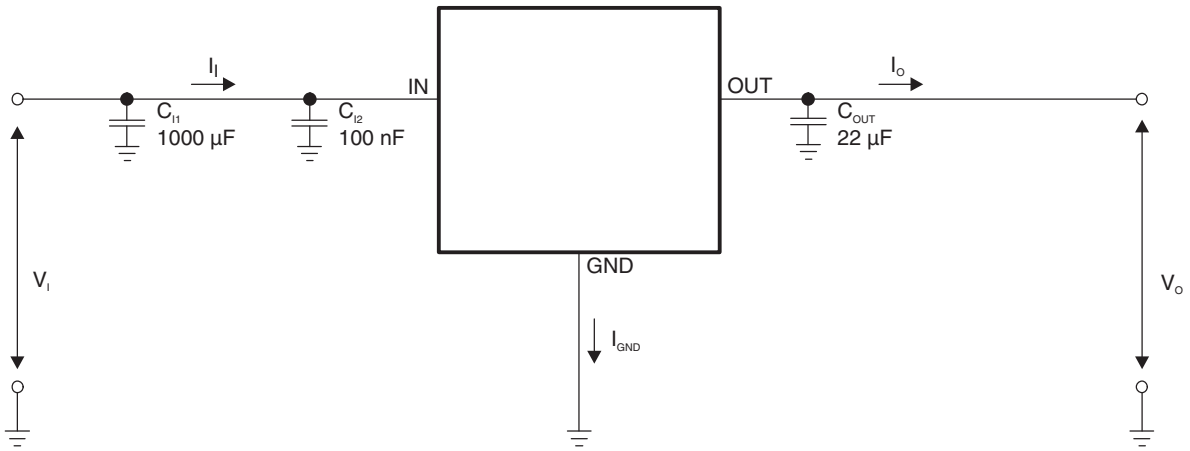


Figure 13. Test Circuit

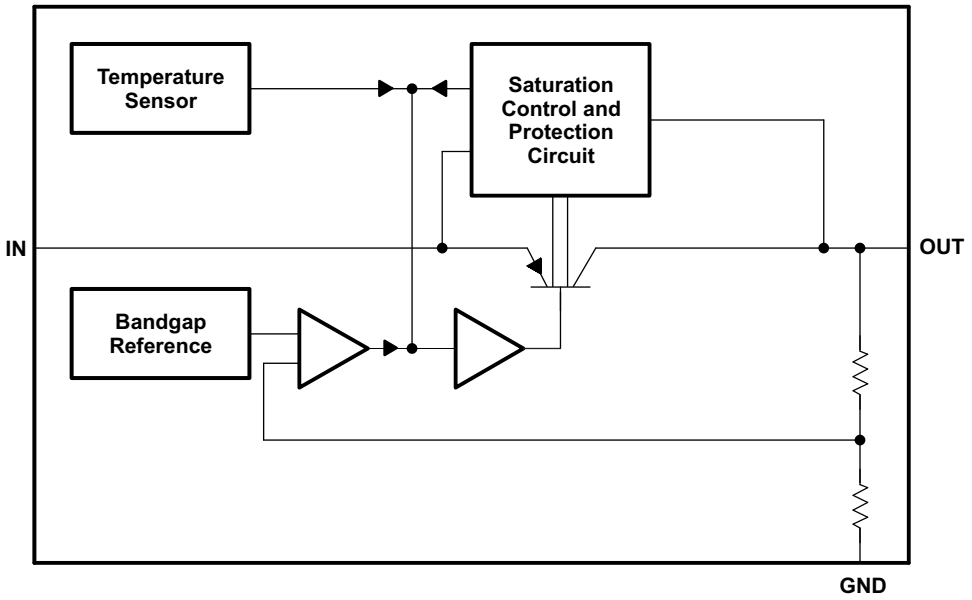
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8 Detailed Description

8.1 Overview

The TL720M05-Q1 device is a monolithic integrated low-dropout voltage regulator offered in a 3-pin TO package. The device regulates an input voltage up to 45 V to VOUT = 5 V (typical) with 2% tolerance. The device can drive loads up to 450 mA and is short-circuit proof. At overtemperature, the incorporated temperature protection turns off the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Regulated Output (OUT)

The OUT terminal is the regulated 5-V output. The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor through a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The output has current limitation. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current.

8.4 Device Functional Modes

8.4.1 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current and switch resistance. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

9.2 Typical Application

Figure 14 shows typical application circuits for the TL720M05-Q1 device.

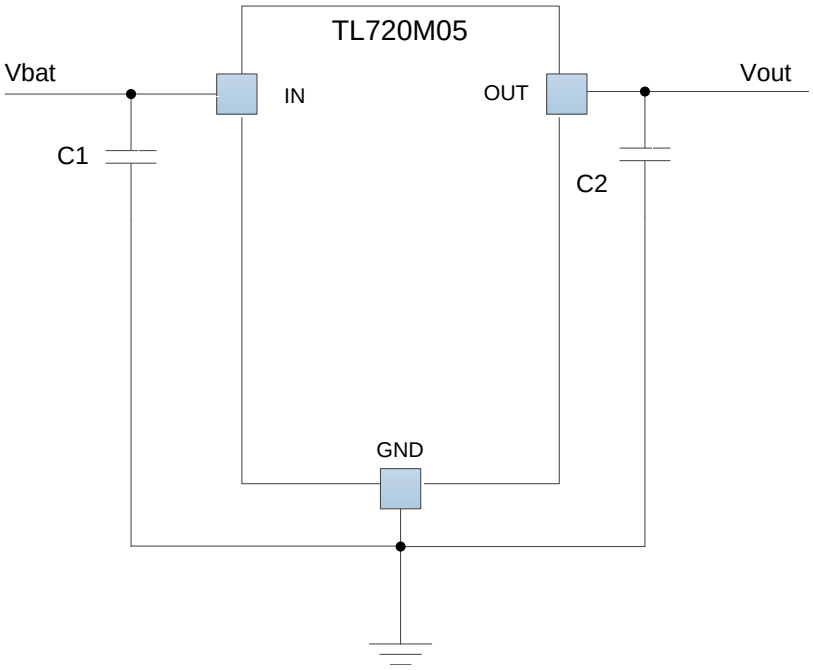


Figure 14. Typical Application Diagram

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 to 40 V
Output voltage	5 V
Output current rating	400 mA
Output capacitor range	10 to 500 µF
Output capacitor ESR range	1 mΩ to 20 Ω

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9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Output capacitor

9.2.2.1 Thermal Consideration

Calculate the power dissipated by the device according to the following formula:

$$P_T = I_O \times (V_I - V_O) + V_I \times I_Q$$

where

- PT = Total power dissipation of the device.
- I_O = output current
- V_I = input voltage
- V_O = output voltage

(1)

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (2)$$

9.2.3 Application Curves

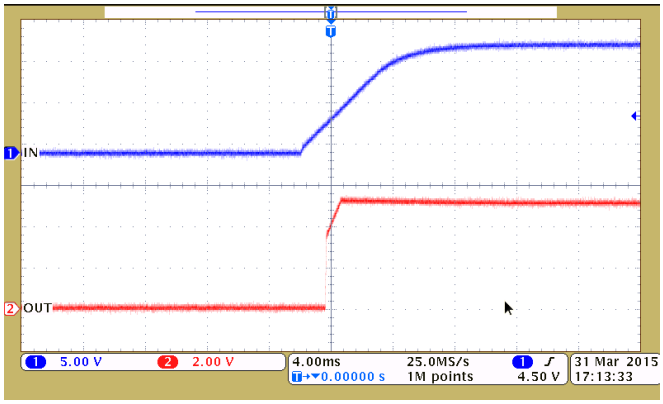


Figure 15. CH1: Vin, CH2: Vout Power Up Waveform (Load = 50 mA)

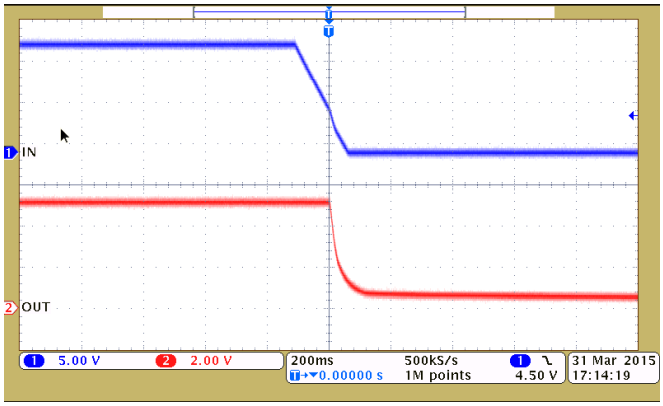


Figure 16. CH1: Vin, CH2: Vout Power Down Waveform (Load = 50mA)

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, TI recommends adding an electrolytic capacitor with a value of 47 µF and a ceramic bypass at the input.

11 Layout

11.1 Layout Guidelines

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor must be placed as close to the device as possible and on the same side of the PCB as the regulator.

11.2 Layout Example

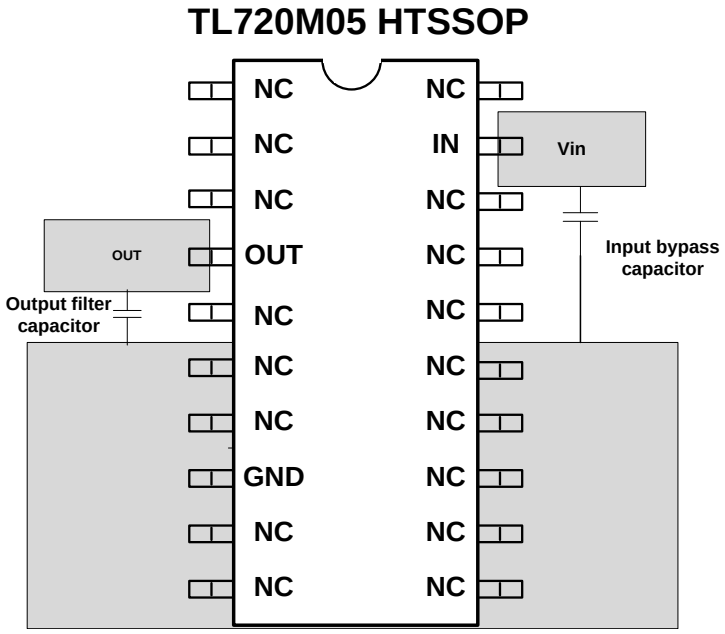


Figure 17. Layout Example Diagram

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *View LDO Noise Demystified* , SLAA412
- *View LDO PSRR Measurement Simplified*, SLAA414

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL720M05GQKVURQ1	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	720M05Q	Samples
TL720M05QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	T720M05Q	Samples
TL720M05QKVURQ1	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	720M05Q	Samples
TL720M05QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	720M05Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

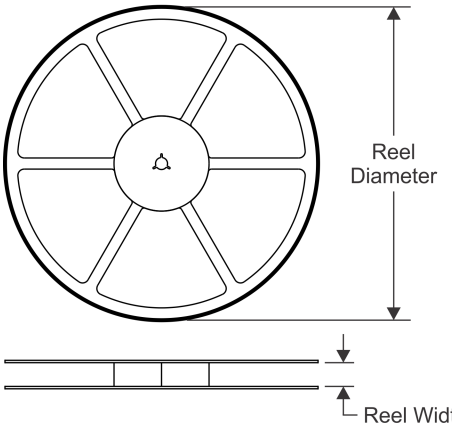
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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

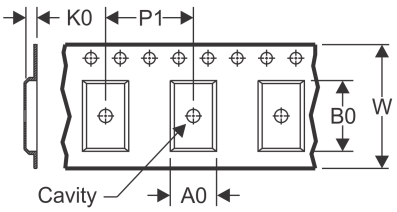
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

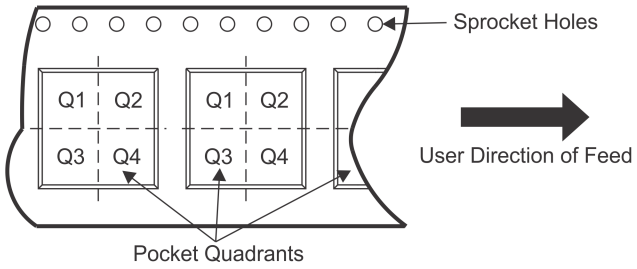


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

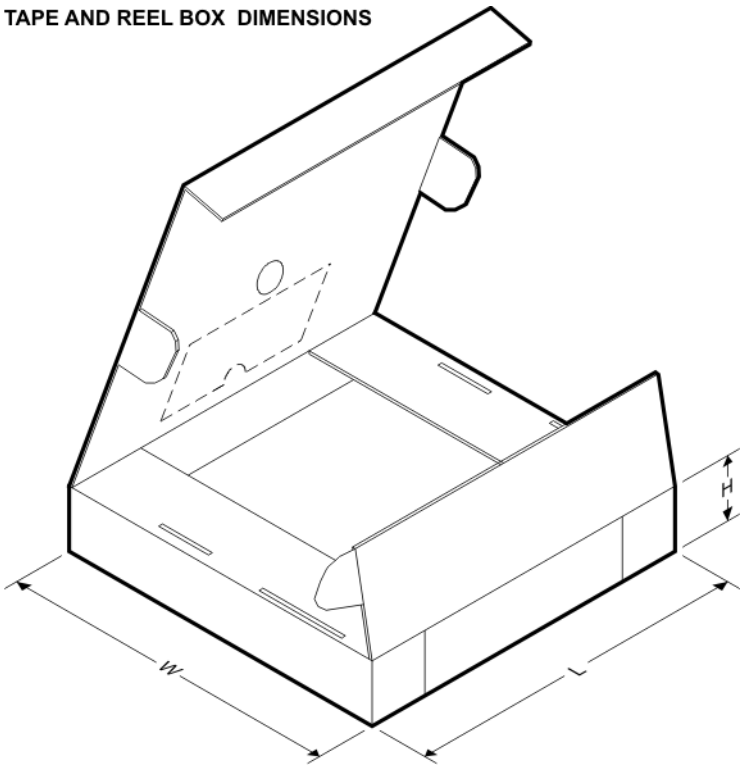
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL720M05GQKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL720M05QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL720M05QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



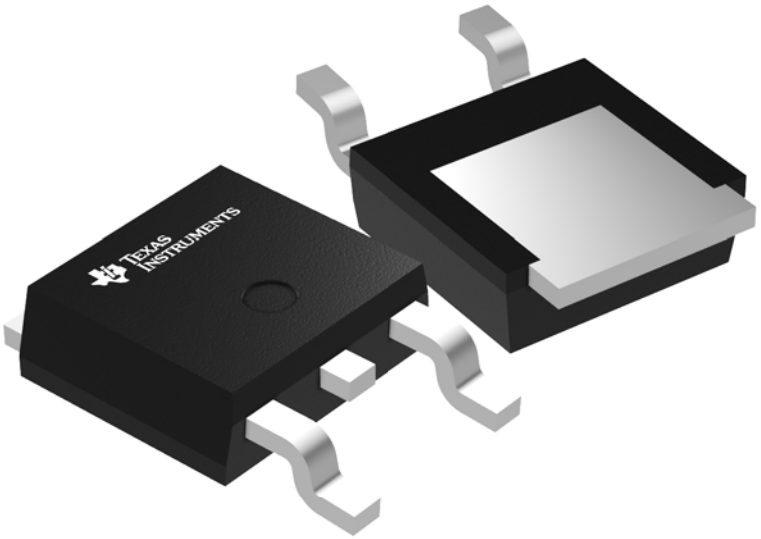
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL720M05GQKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL720M05QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL720M05QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

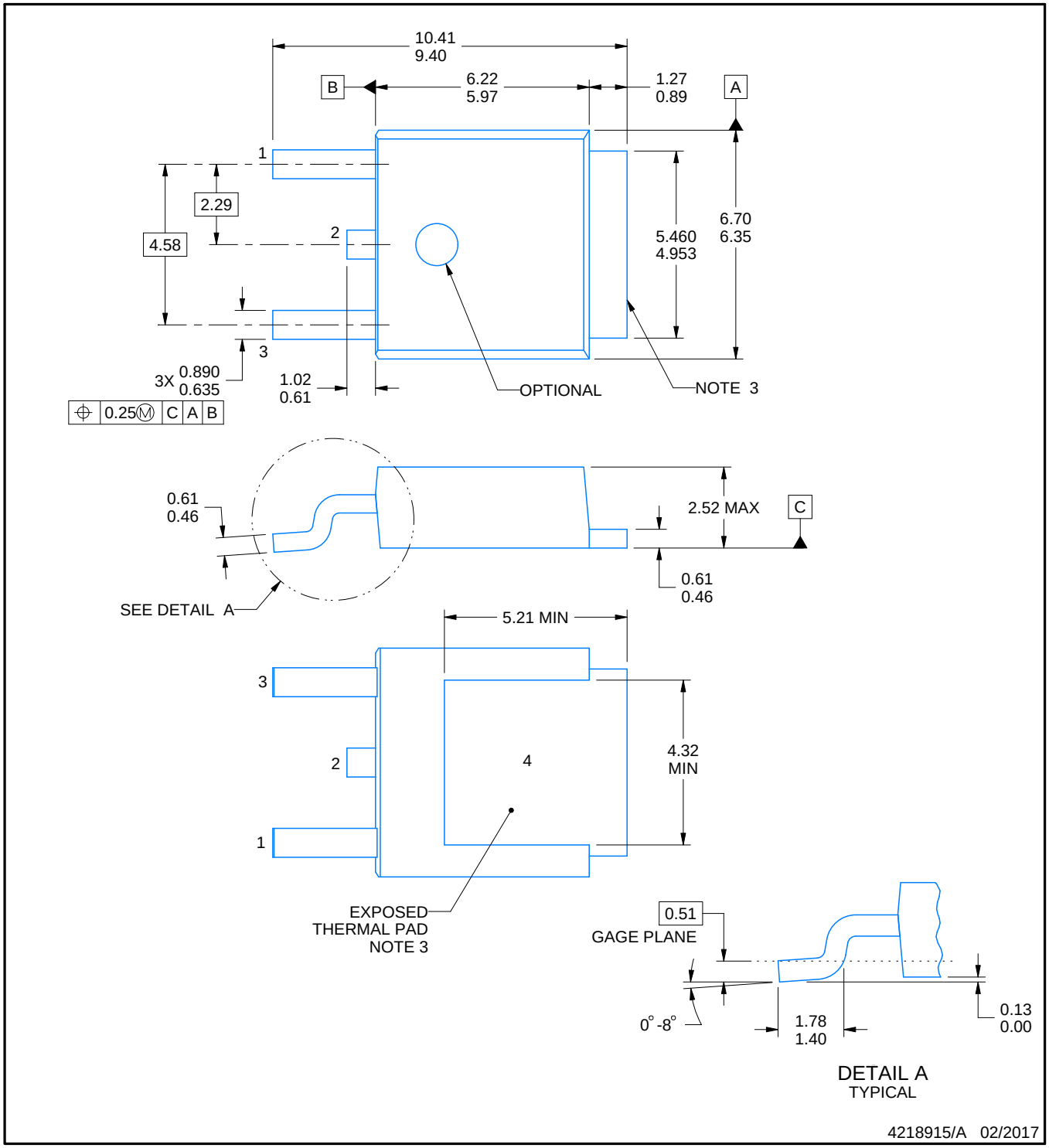


PACKAGE OUTLINE

KVU0003A

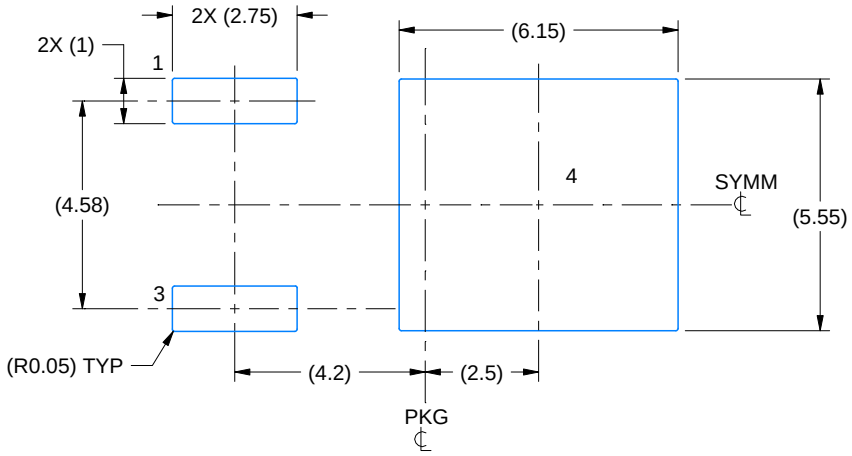
TO-252 - 2.52 mm max height

TO-252

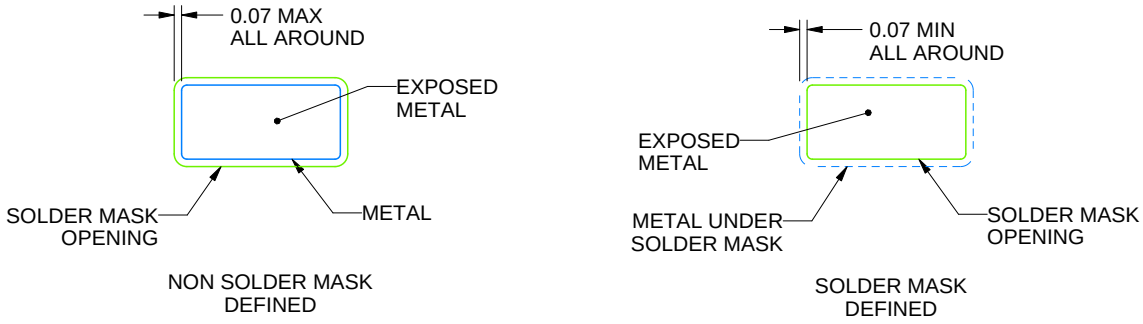


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

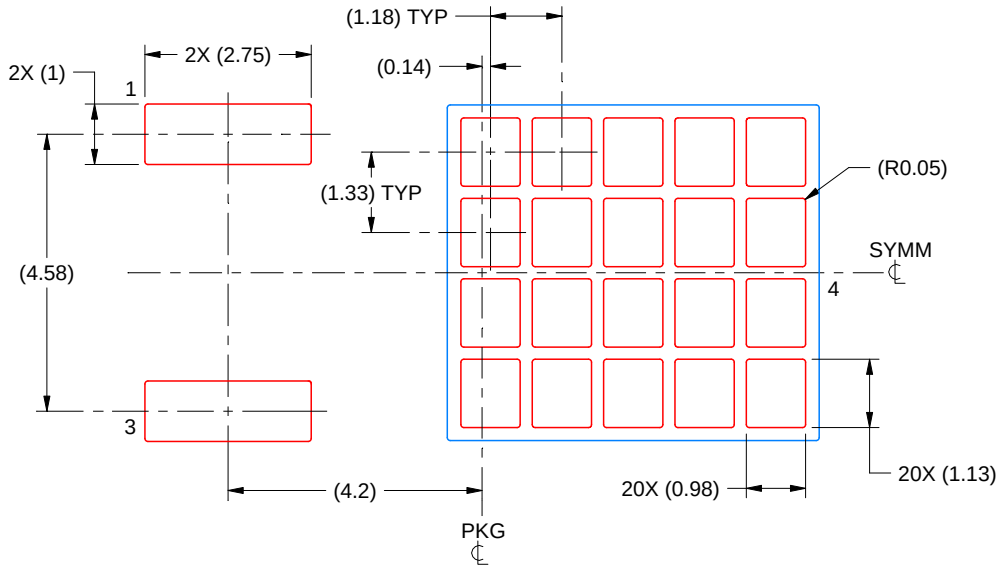
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

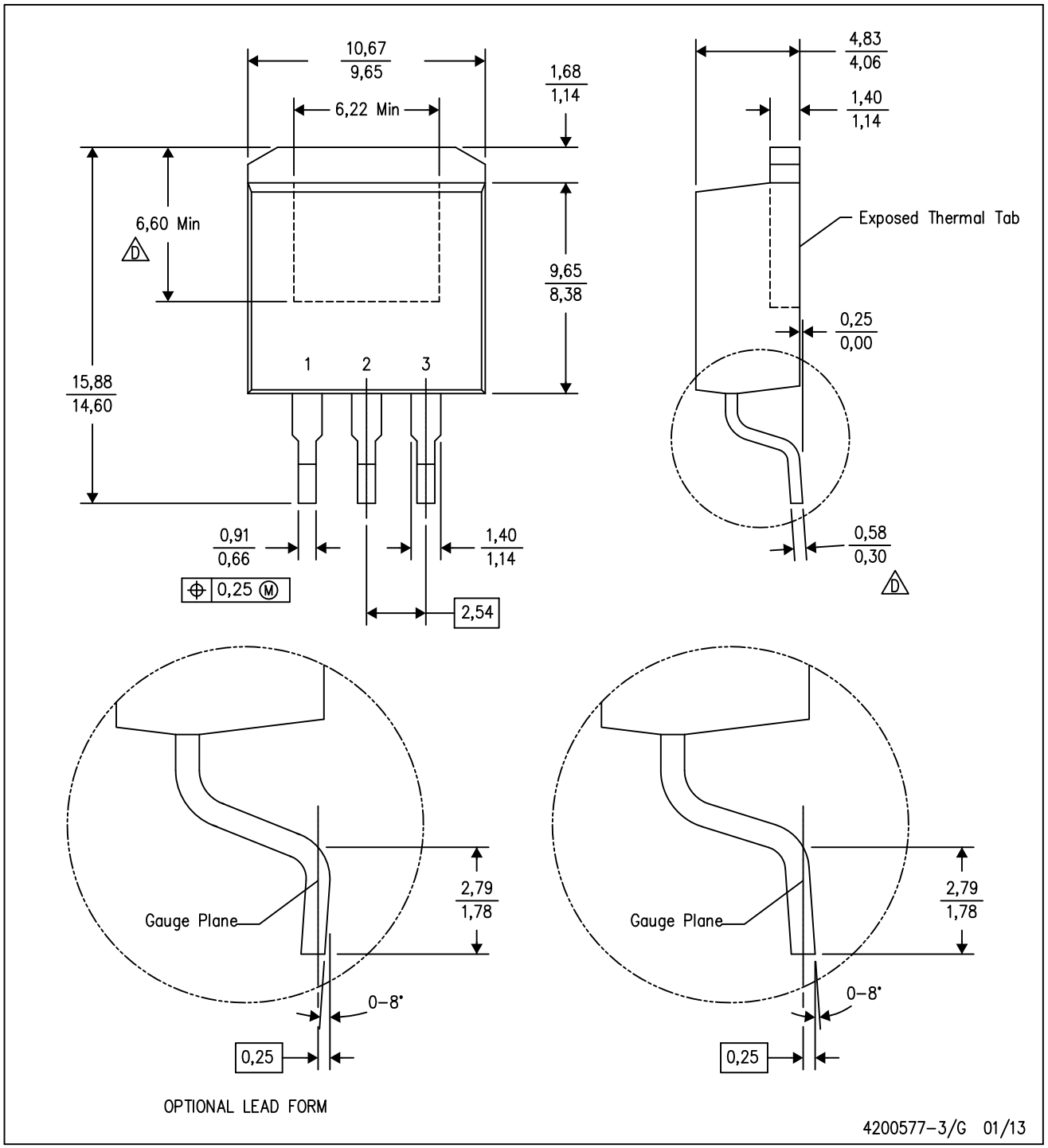
EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

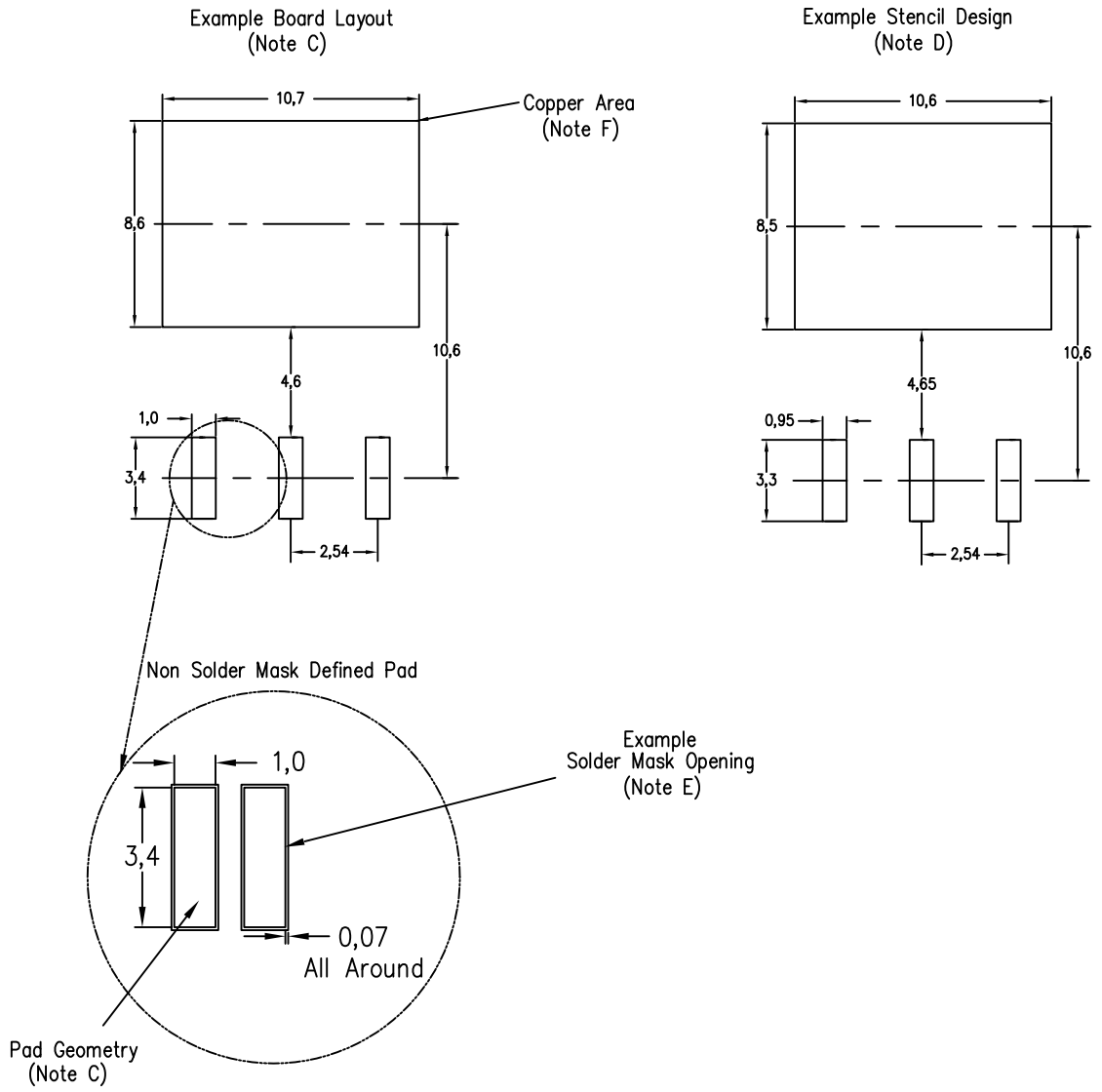
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



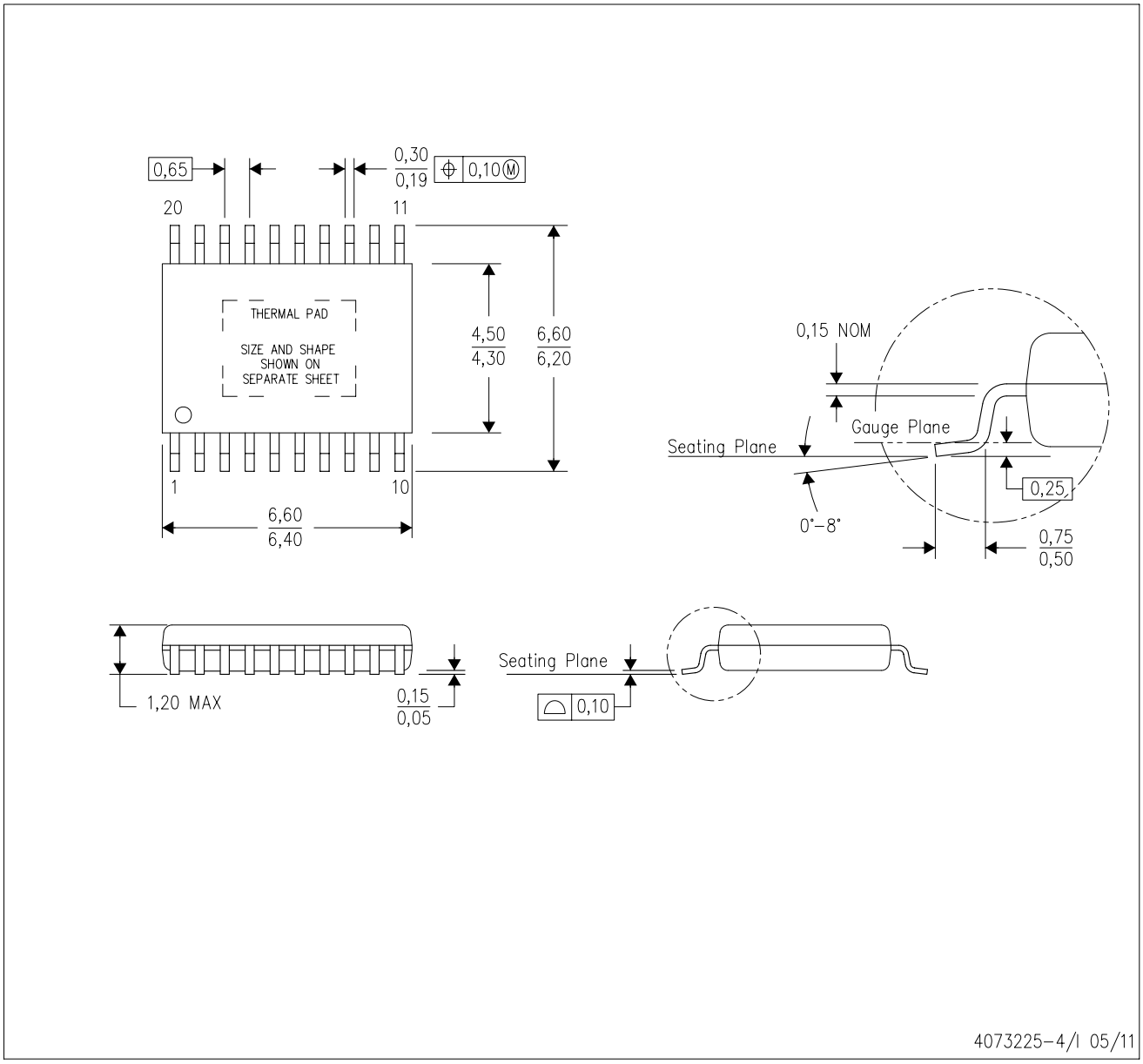
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

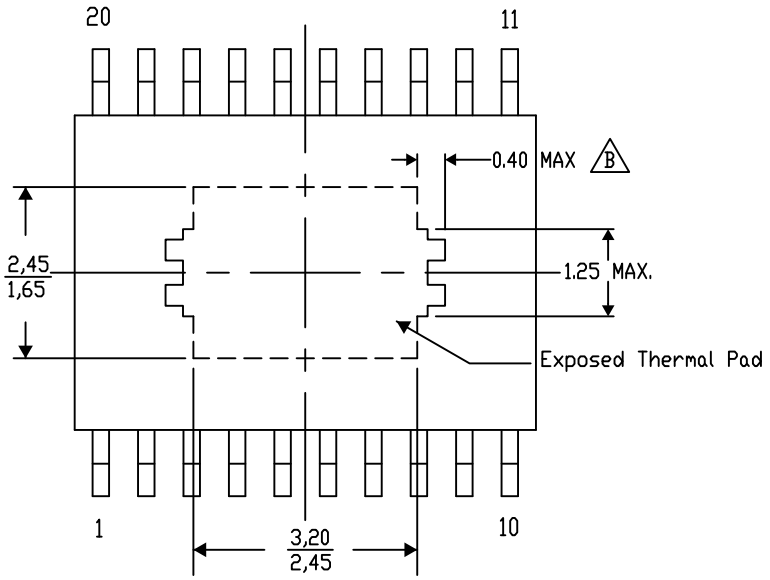
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

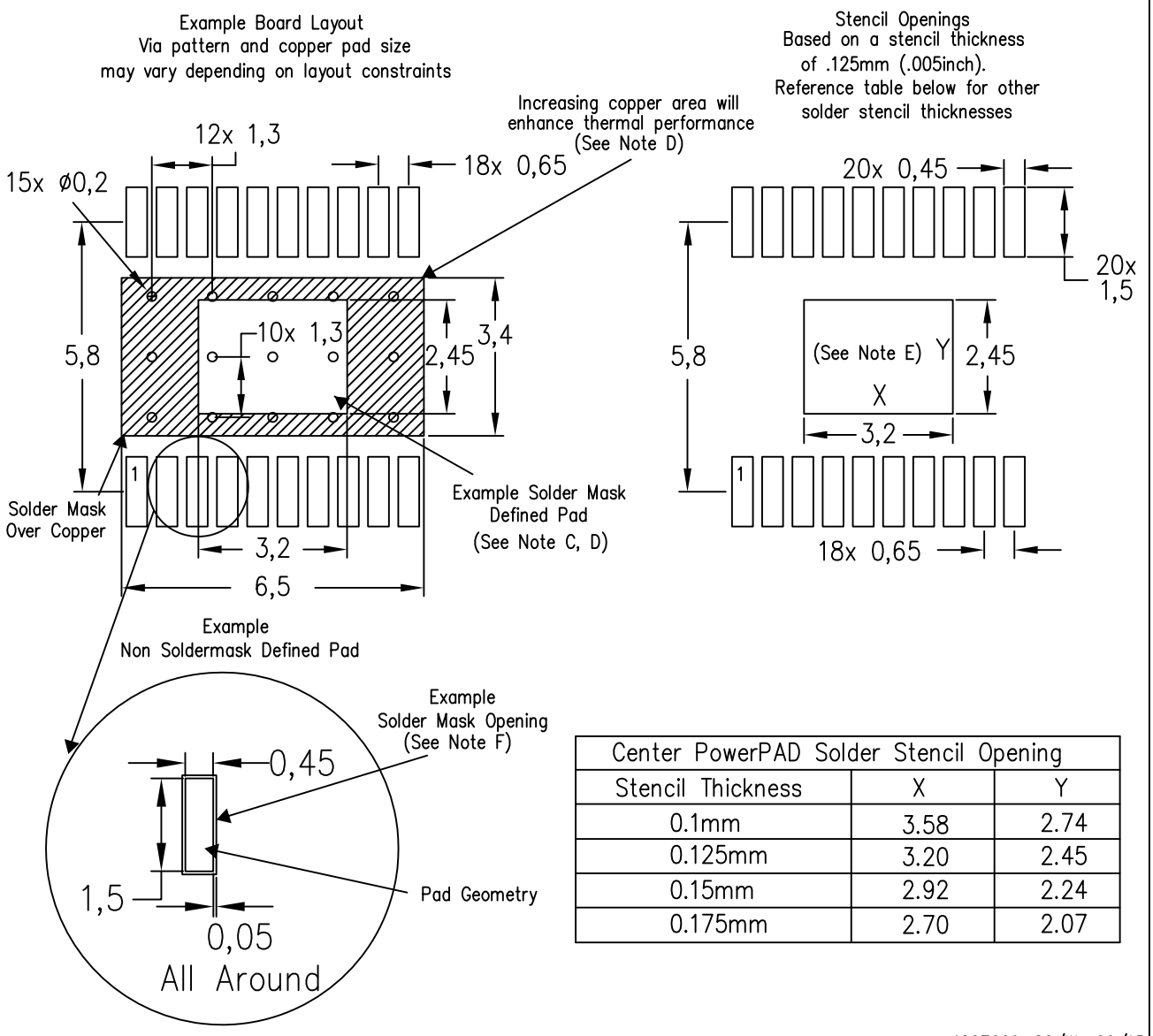
4206332–18/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.58	2.74
0.125mm	3.20	2.45
0.15mm	2.92	2.24
0.175mm	2.70	2.07

4207609–26/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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