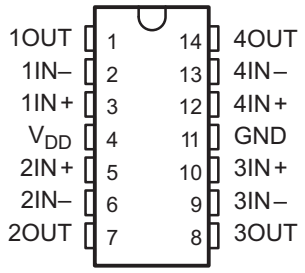
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

Check for Samples: TLC27M4, TLC27M4A, TLC27M4B, TLC27M4Y, TLC27M9

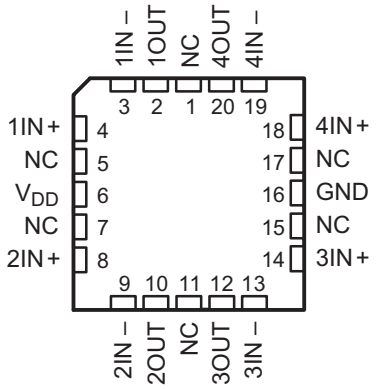
FEATURES

- **Trimmed Offset Voltage**
  - **TLC27M9 . . . 900 µV Max at T_A = 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 µV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **–40°C to 85°C . . . 4 V to 16 V**
  - **–55°C to 125°C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/√Hz at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at T_A = 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, N, OR PW PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)



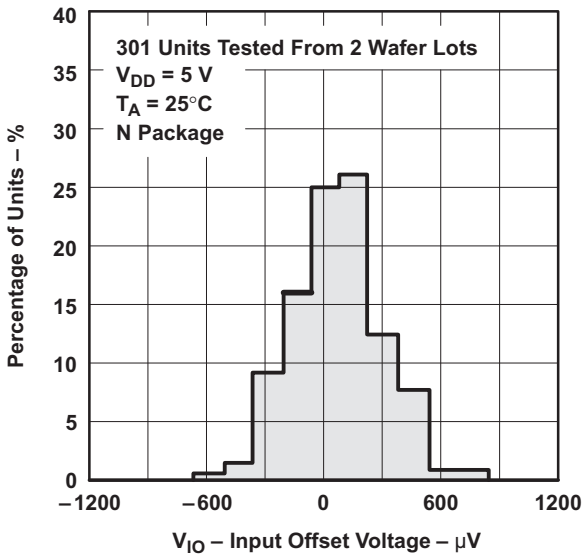
NC – No internal connection

DESCRIPTION

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption.

DISTRIBUTION OF TLC27M9 INPUT OFFSET VOLTAGE



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Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single-supply operation, and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27M4 and TLC27M9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE					CHIP FORM (Y)
		SMALL OUTLINE (D)(1)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)(1)	
0°C to 70°C	900 µV	TLC27M9CD	—	—	TLC27M9CN	—	—
	2 mV	TLC27M4BCD	—	—	TLC27M4BCN	—	—
	5 mV	TLC27M4ACD	—	—	TLC27M4ACN	—	—
	10 mV	TLC27M4CD	—	—	TLC27M4CN	TLC27M4CPW	TLC27M4Y
–40°C to 85°C	900 µV	TLC27M9ID	—	—	TLC27M9IN	—	—
	2 mV	TLC27M4BID	—	—	TLC27M4BIN	—	—
	5 mV	TLC27M4AID	—	—	TLC27M4AIN	—	—
	10 mV	TLC27M4ID	—	—	TLC27M4IN	TLC27M41PW	—
–55°C to 125°C	900 µV	TLC27M9MD	TLC27M9MFK	TLC27M9MJ	TLC27M9MN	—	—
	10 mV	TLC27M4MD	TLC27M4MFK	TLC27M4MJ	TLC27M4MN	—	—

(1) The D and PW package is available taped and reeled. Add R suffix to the device type (e.g., TLC279CDR).

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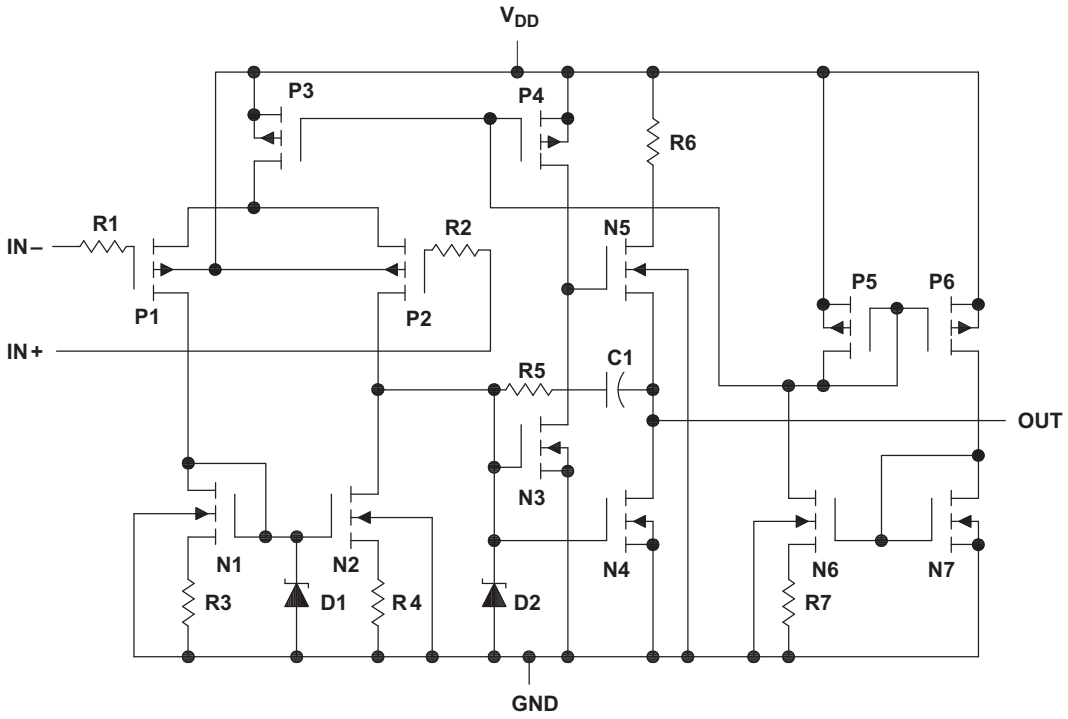
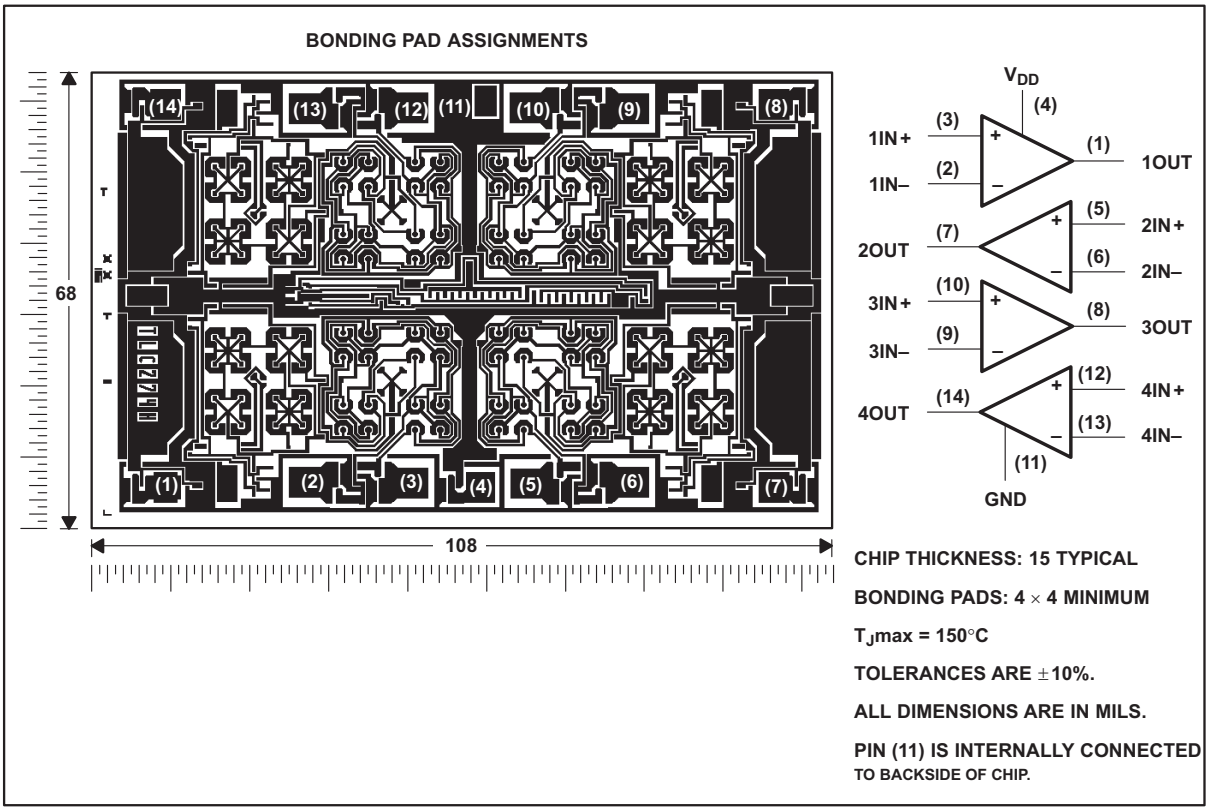
EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



TLC27M4Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC27M4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
Supply voltage, V_{DD}[2]		18	V
Differential input voltage, V_{ID}[3]		±VDD	
Input voltage range, V_I (any input)		–0.3 V to V_{DD}	
Input current, I_I		±5	mA
Output current, I_O (each output)		±30	mA
Total current into V_{DD}		45	mA
Total current out of GND		45	mA
Duration of short-circuit current at (or below) 25°C[4]		unlimited	
Continuous total dissipation		See Dissipation Rating Table	
Operating free-air temperature, T_A	C suffix	0 to 70	°C
	I suffix	–40 to 85	°C
	M suffix	–55 to 125	°C
Storage temperature range		–65 to 150	°C
Case temperature for 60 seconds: FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATINGS

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	—
PW	700 mW	5.6 mW/°C	448 mW	—	—

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common mode input voltage, V_{IC}	V_{DD} = 5 V	–0.2	3.5	–0.2	3.5	0	3.5	V
	V_{DD} = 10 V	–0.2	8.5	–0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

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ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		250	2000	µV
					Full range			3000	
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (2)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (2)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (3)				25°C	–0.2 to 4	–0.3 to 4.2		V
					Full range	–0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	µA
					0°C		500	1280	
					70°C		340	880	

(1) Full range is 0°C to 70°C.
(2) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(3) This range also applies to each input individually.

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ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	2000	µV
					Full range			3000	
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (2)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (2)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (3)				25°C	–0.2 to 9	–0.3 to 9.2		V
					Full range	–0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					0°C	7.8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					0°C	15	320		
					70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					0°C	60	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	µA
					0°C		690	1600	
					70°C		440	1120	

(1) Full range is 0°C to 70°C.
(2) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(3) This range also applies to each input individually.

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ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		250	2000	µV
					Full range			3000	
		TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (2)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (2)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (3)				25°C	–0.2 to 4	–0.3 to 4.2		V
					Full range	–0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					–40°C	3	3.9		
					85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					–40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					–40°C	15	270		
					85°C	15	130		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	91		dB
					–40°C	60	90		
					85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					–40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	µA
					–40°C		630	1600	
					85°C		320	800	

(1) Full range is –40°C to 85°C.
(2) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(3) This range also applies to each input individually.

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ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			7	
		TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	2000	µV
					Full range			3500	
		TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		µV/°C
I_{IO}	Input offset current (2)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (2)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (3)				25°C	–0.2 to 9	–0.3 to 9.2		V
					Full range	–0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					–40°C	7.8	8.7		
					85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					–40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					–40°C	15	390		
					85°C	15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					–40°C	60	93		
					85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					–40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	µA
					–40°C		900	1800	
					85°C		410	1040	

(1) Full range is –40°C to 85°C.
(2) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(3) This range also applies to each input individually.

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ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLC27M4M TLC27M9M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	µV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.7		µV/°C
I_{IO}	Input offset current (2)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (2)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		9	35	nA
V_{ICR}	Common-mode input voltage range (3)				25°C	0 to 4	–0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					–55°C	3	3.9		
					125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					–55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					–55°C	15	270		
					125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	91		dB
					–55°C	60	89		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					–55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	µA
					–55°C		680	1760	
					125°C		280	720	

(1) Full range is –55°C to 125°C.
(2) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(3) This range also applies to each input individually.

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ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLC27M4M TLC27M9M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	µV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (2)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (2)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (3)				25°C	0 to 9	–0.3 to 9.2		V
					Full range	–0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					–55°C	7.8	8.6		
					125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					–55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					–55°C	15	420		
					125°C	15	190		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					–55°C	60	93		
					125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					–55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	µA
					–55°C		980	2000	
					125°C		360	960	

(1) Full range is –55°C to 70°C.
(2) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(3) This range also applies to each input individually.

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ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC27M4Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage	T_A = 25°C to 70°C			1.7		µV/°C
I_{IO}	Input offset current(1)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.1		pA
I_{IB}	Input bias current(1)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.6		pA
V_{ICR}	Common-mode input voltage range(2)			–0.2 to 4	–0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 100 kΩ	3.2	3.9		V
V_{OL}	Low-level output voltage	V_{ID} = –100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V,	R_L= 100 kΩ	25	170		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	70	93		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	V_{IC} = 2.5 V,		420	1120	µA

(1) The typical values of input bias current and input offset current below 5 pA were determined mathematically
(2) This range also applies to each input individually.

ELECTRICAL CHARACTERISTICS

V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC27M4Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage	T_A = 25°C to 70°C			1.7		µV/°C
I_{IO}	Input offset current(1)	V_O = 5 V,	V_{IC} = 5 V		0.1		pA
I_{IB}	Input bias current(1)	V_O = 5 V,	V_{IC} = 5 V		0.6		pA
V_{ICR}	Common-mode input voltage range(2)			–0.2 to 9	–0.3 to 9.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 100 kΩ	8	8.7		V
V_{OL}	Low-level output voltage	V_{ID} = –100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V,	R_L= 100 kΩ	25	275		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	70	93		dB
I_{DD}	Supply current (four amplifiers)	V_O = 5 V, No load	V_{IC} = 5 V,		570	1200	µA

(1) The typical values of input bias current and input offset current below 5 pA were determined mathematically.
(2) This range also applies to each input individually.

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OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF	25°C		525		kHz
				0°C		610		
				70°C		400		
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF	25°C		635		kHz
				0°C		710		
				70°C		510		
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

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OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				–40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				–40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				–40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF	25°C		525		kHz
				–40°C		770		
				85°C		370		
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				–40°C		43°		
				85°C		38°		

OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				–40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				–40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				–40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF	25°C		635		kHz
				–40°C		880		
				85°C		480		
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				–40°C		46°		
				85°C		41°		

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OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4M TLC27M9M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				–55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				–55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		56		kHz
				–55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF	25°C		525		kHz
				–55°C		850		
				125°C		330		
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				–55°C		44°		
				125°C		36°		

OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4M TLC27M9M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				–55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				–55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				–55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF	25°C		635		kHz
				–55°C		960		
				125°C		440		
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				–55°C		47°		
				125°C		39°		

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OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC27M4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		0.43		V/µs
			V_{IPP} = 2.5 V		0.40		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1		55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF		525		kHz
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3		40°		

OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC27M4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		0.62		V/µs
			V_{IPP} = 5.5 V		0.56		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1		35		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF		635		kHz
φ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3		43°		

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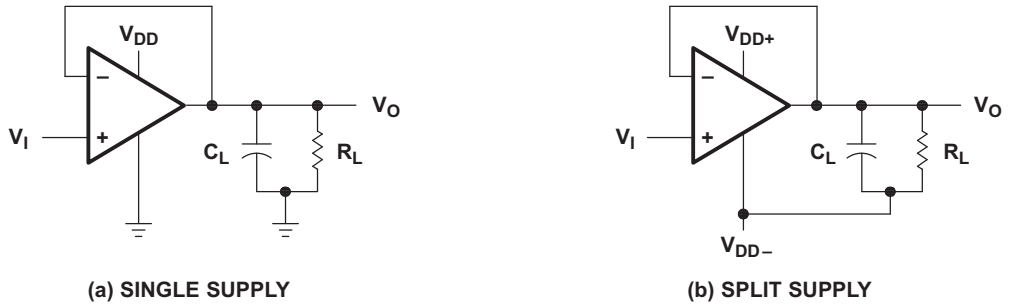
PARAMETER MEASUREMENT INFORMATION

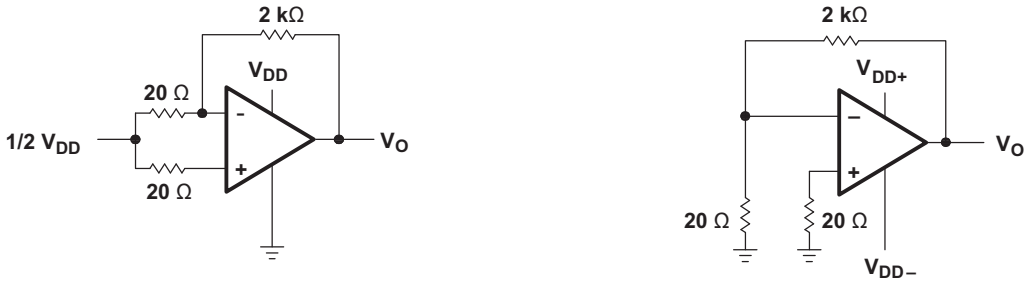
Single-Supply versus Split-Supply Test Circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



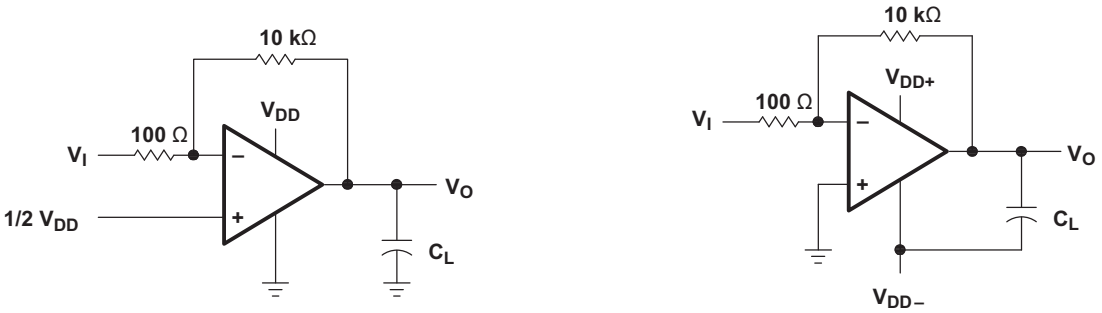
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION (continued)

Input Bias Current

Because of the high input impedance of the TLC27M4 and TLC27M9 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution—many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current; the voltage drop across the series resistor is measured and the bias current is calculated. This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

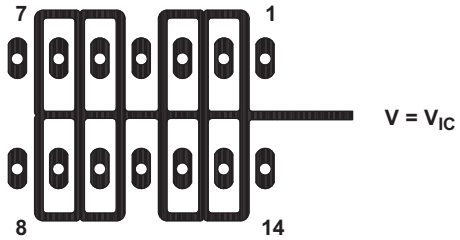


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

Low-Level Output Voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figure 14 through Figure 19 in the *Typical Characteristics* of this data sheet.

Input Offset Voltage Temperature Coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

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PARAMETER MEASUREMENT INFORMATION (continued)

Full-Power Response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output, while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

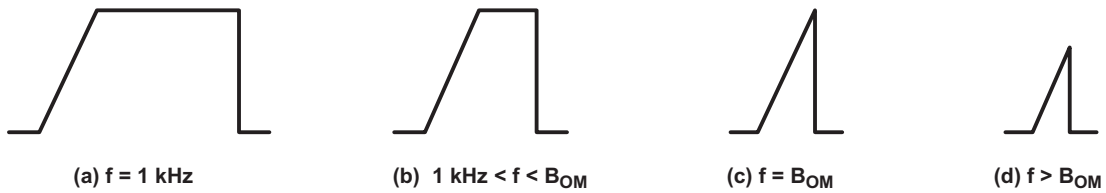

Figure 5. Full-Power-Response Output Signal

Test Time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Differential voltage amplification	vs Supply voltage vs Free-air temperature Free vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity gain bandwidth	vs Free-air temperature Free vs Supply voltage	30 31
	Phase shift	vs Frequency	32, 33
φ_m	Phase margin	vs Supply voltage vs Free-air temperature Free vs Load capacitance	34 35 36
Vn	Equivalent input noise voltage	vs Frequency	37

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TYPICAL CHARACTERISTICS

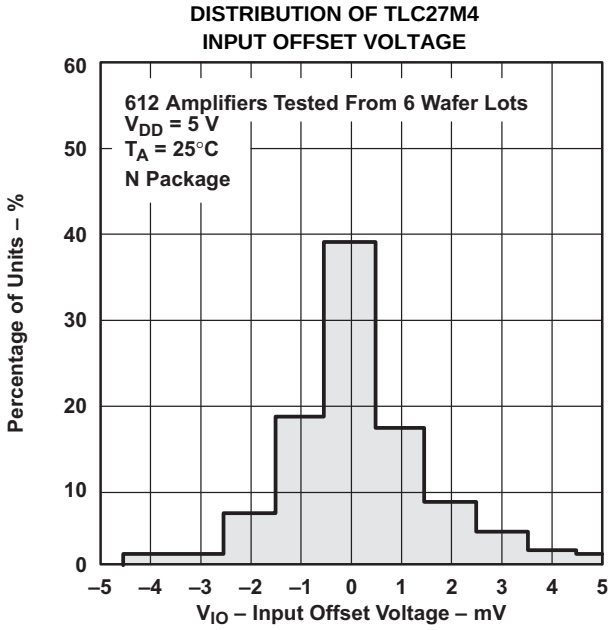
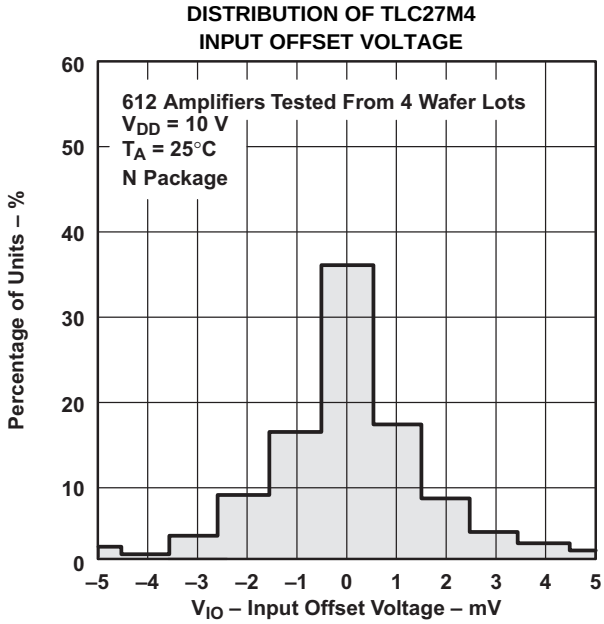


Figure 6.



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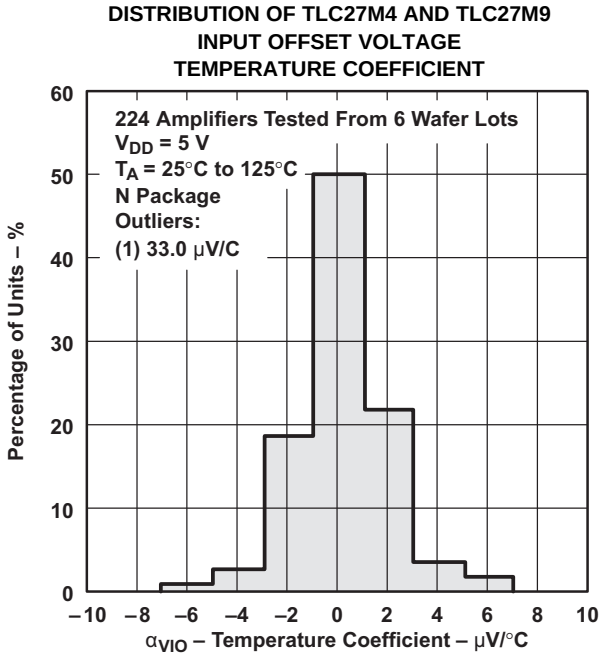

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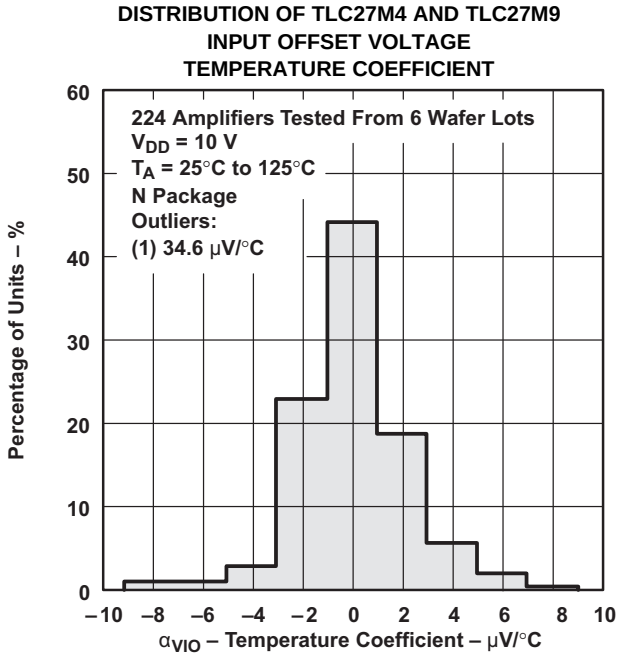
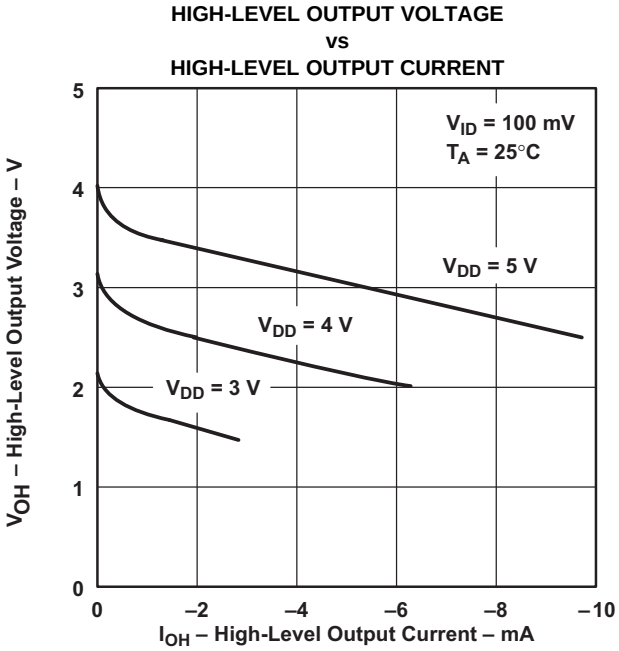


Figure 9.

TYPICAL CHARACTERISTICS (1)



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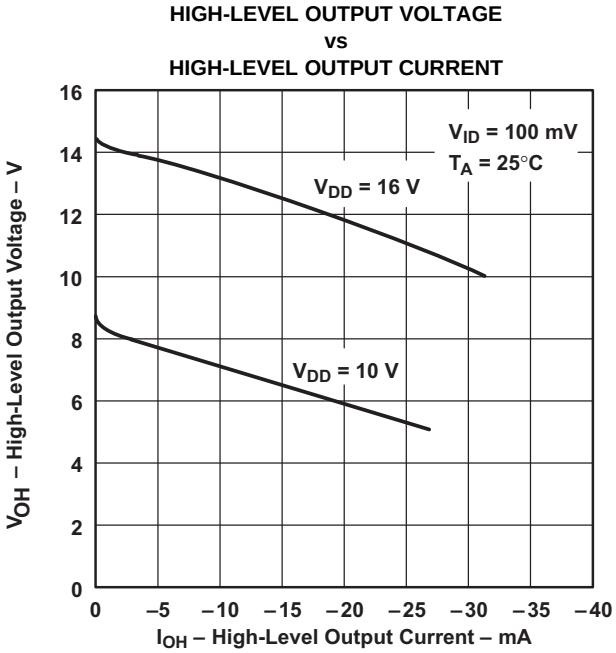

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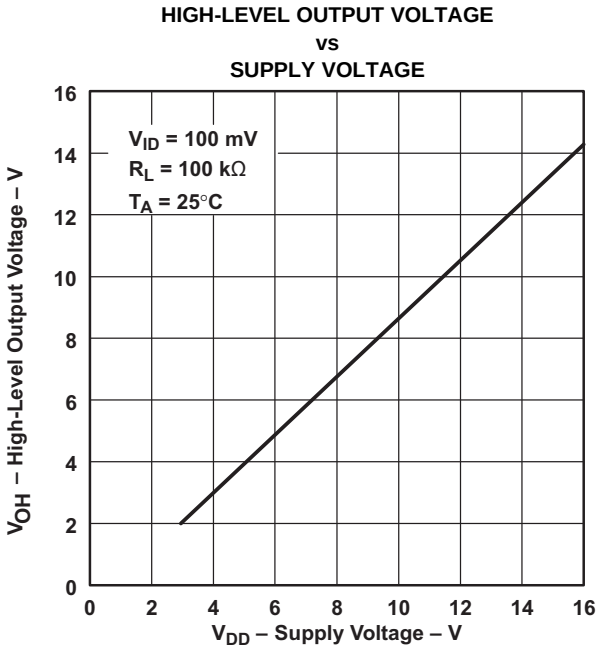

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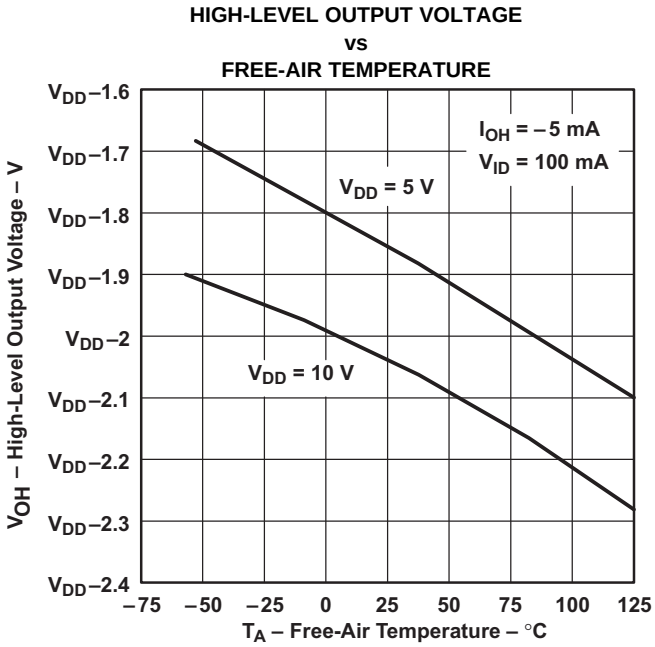

Figure 13.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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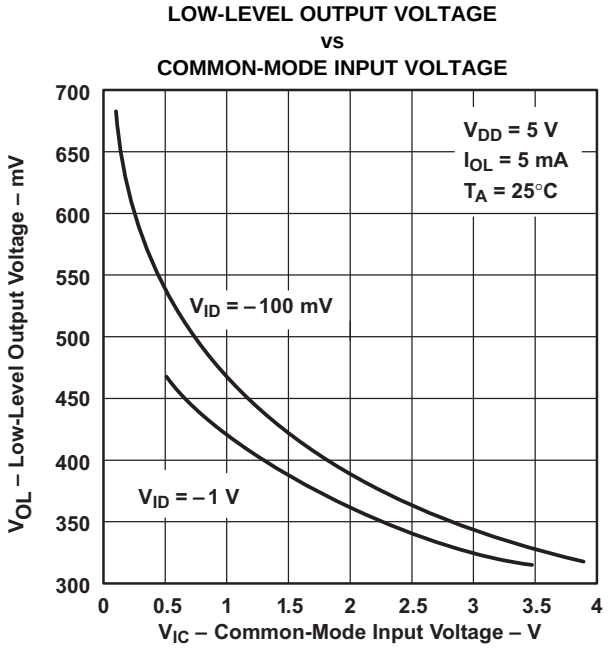
TYPICAL CHARACTERISTICS (1)



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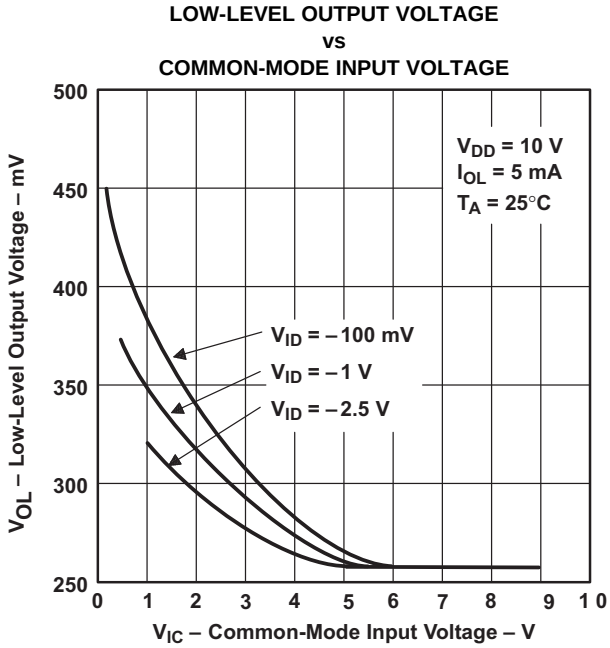

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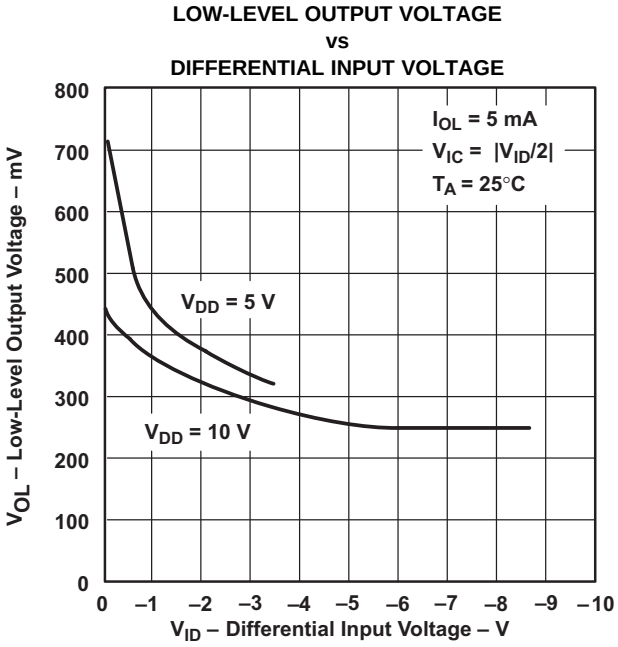

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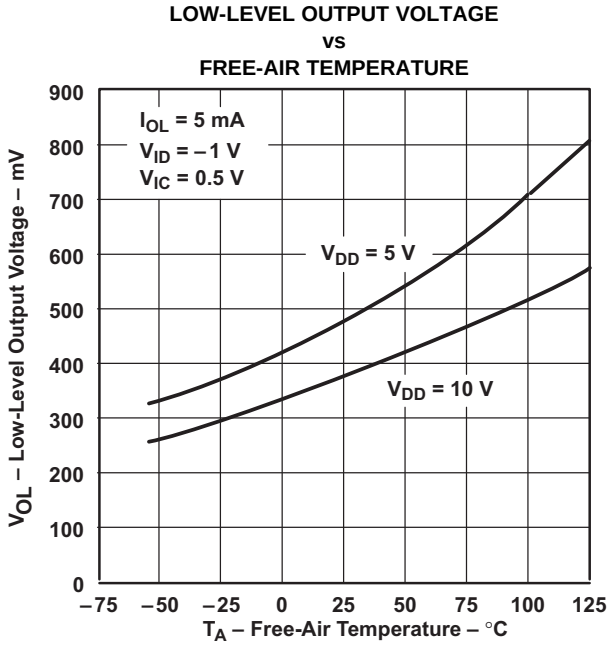

Figure 17.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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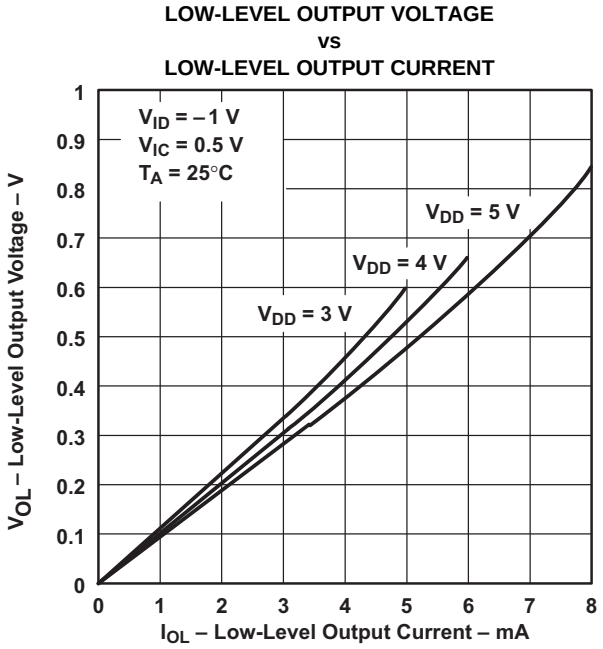

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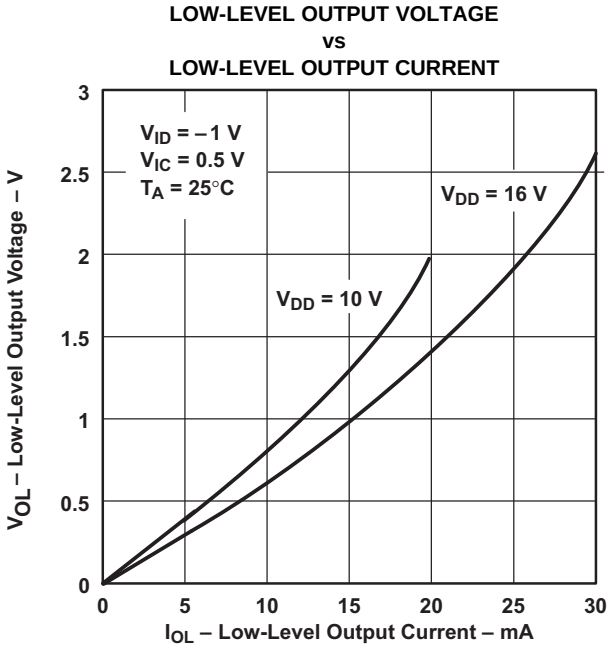

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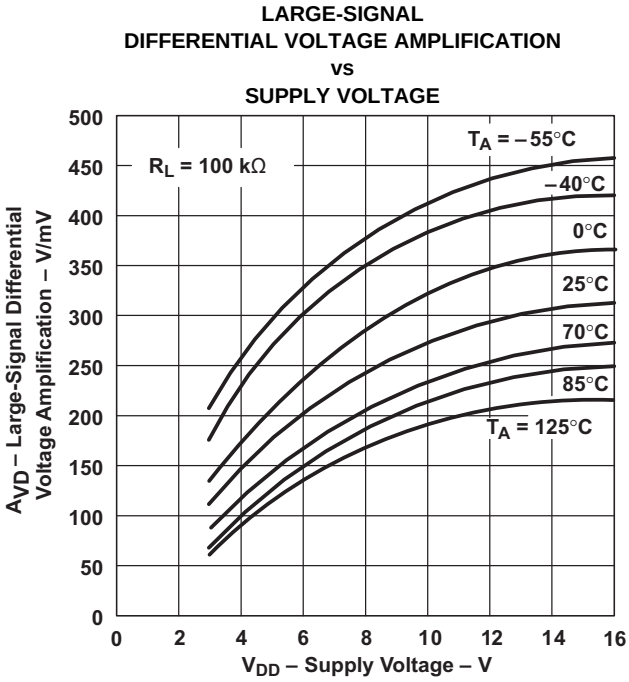

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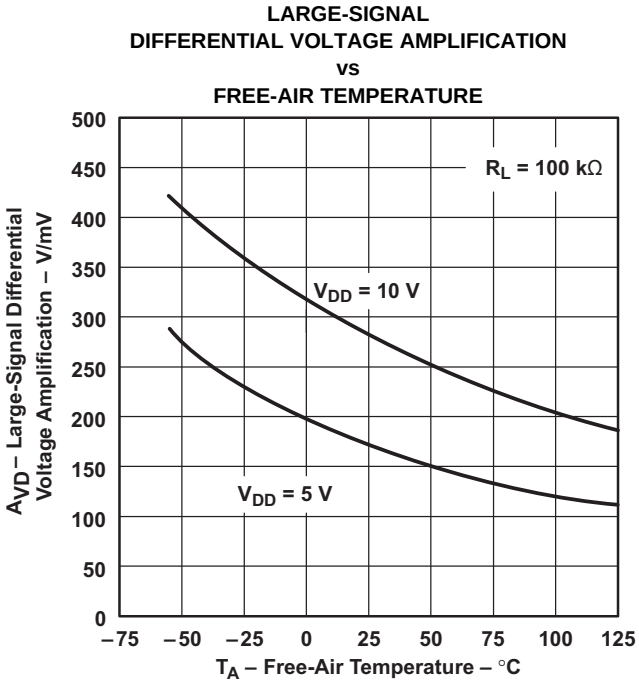

Figure 21.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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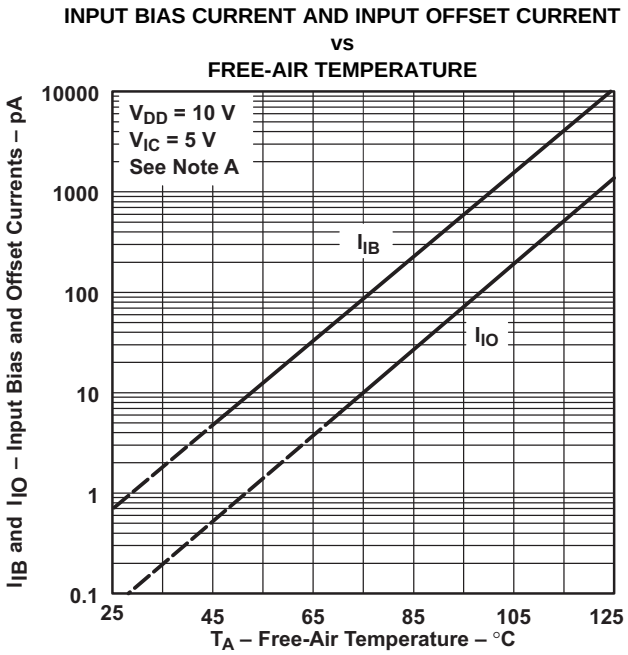
TYPICAL CHARACTERISTICS (1)



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22.

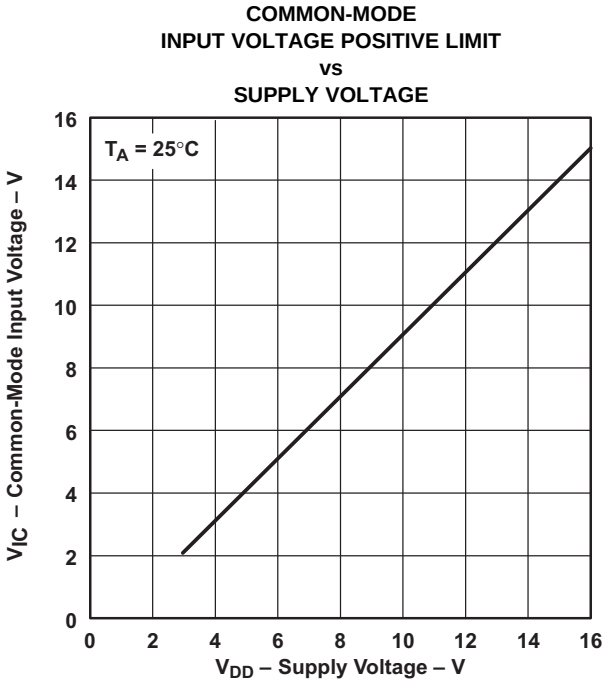
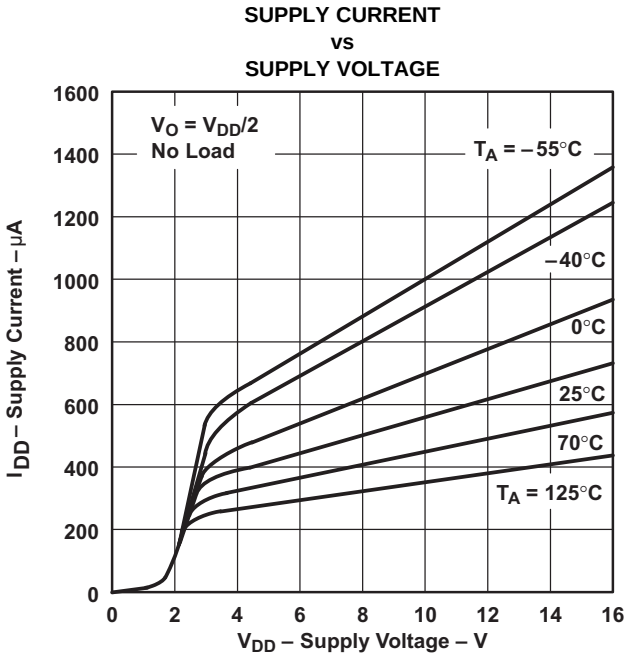


Figure 23.



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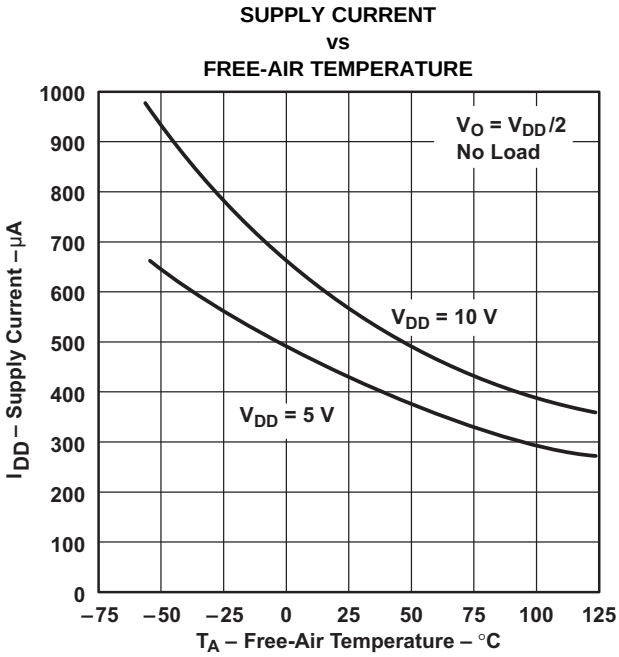

Figure 25.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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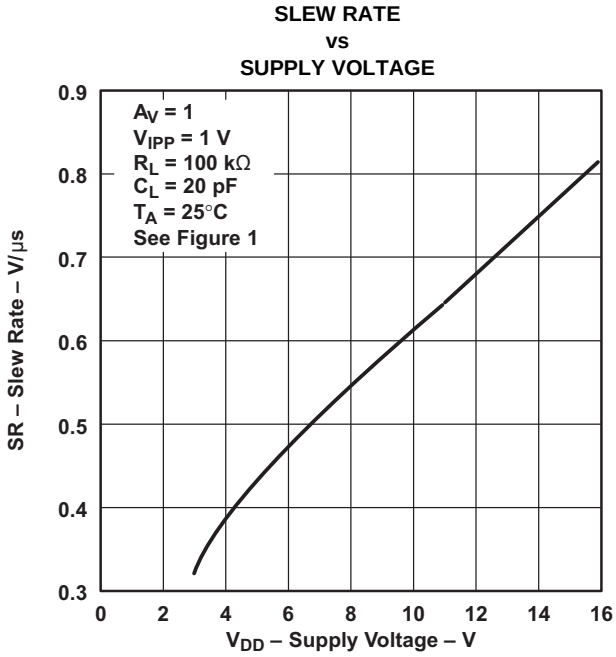

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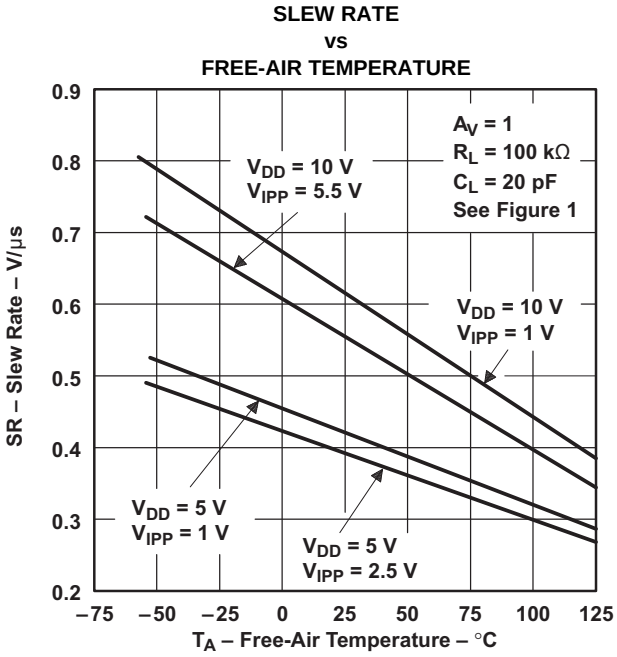
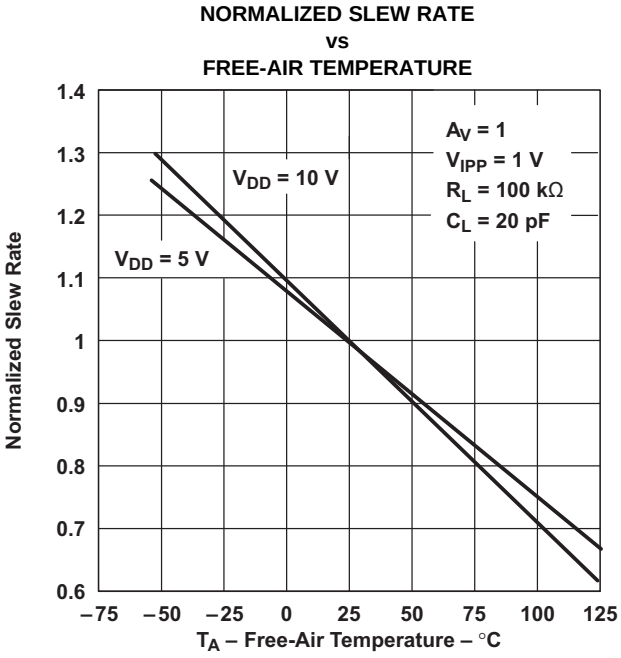


Figure 27.



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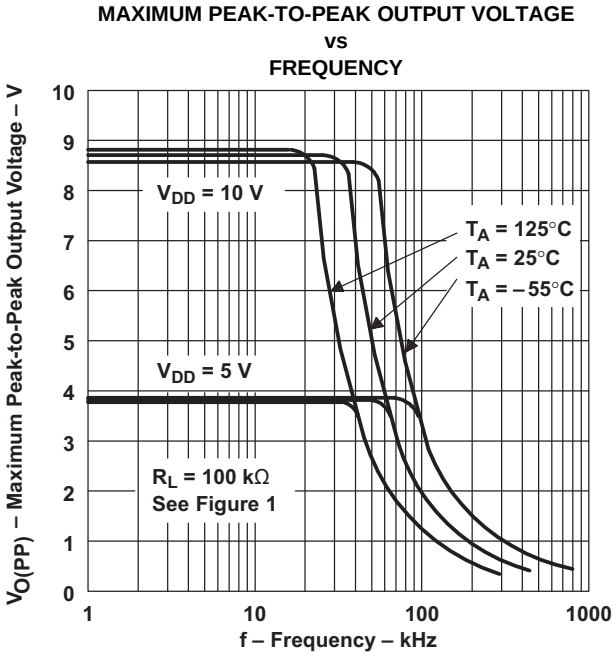

Figure 29.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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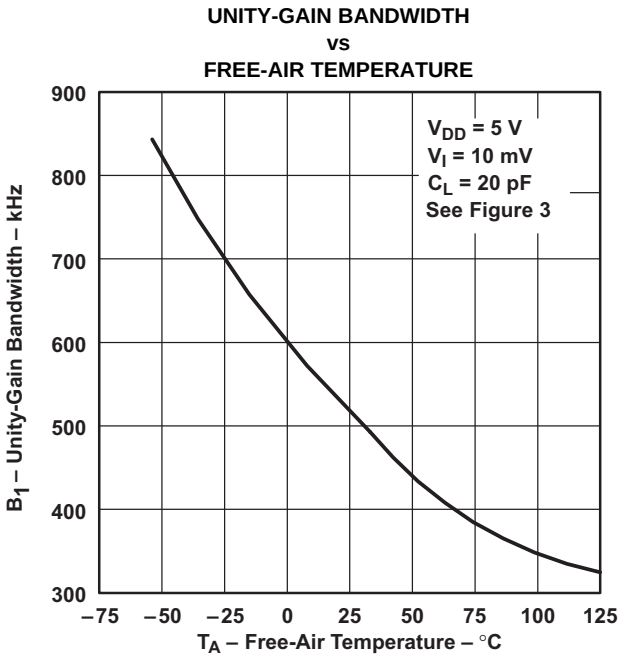
TYPICAL CHARACTERISTICS (1)



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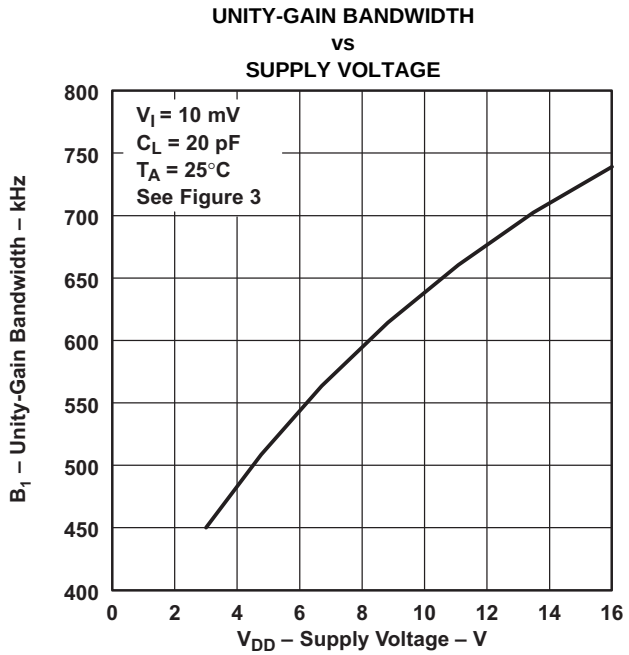

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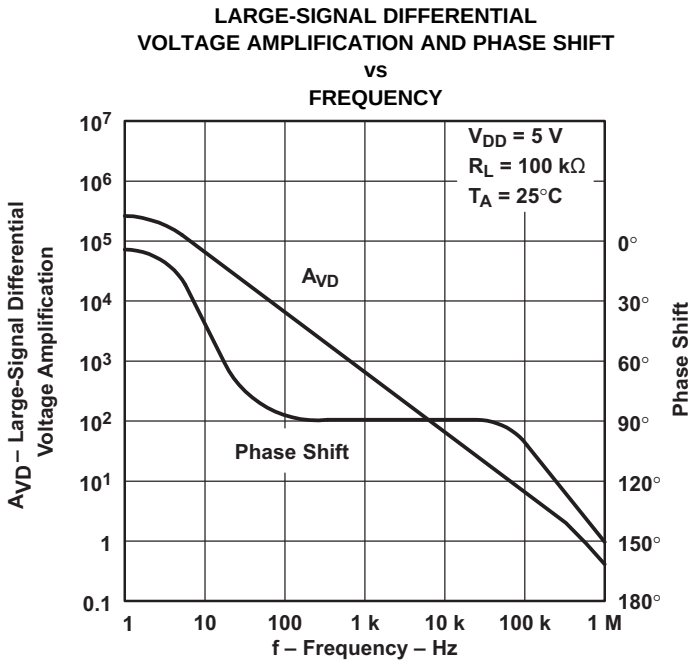


Figure 32.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (1)

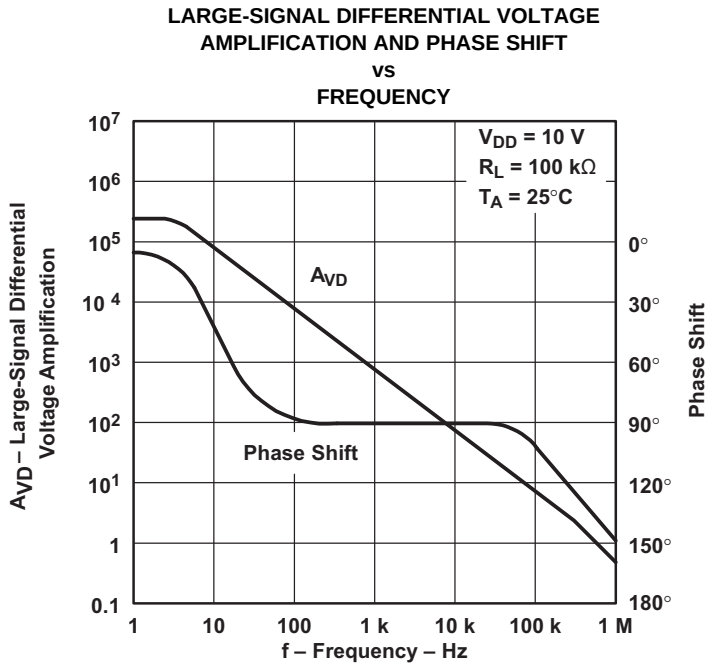
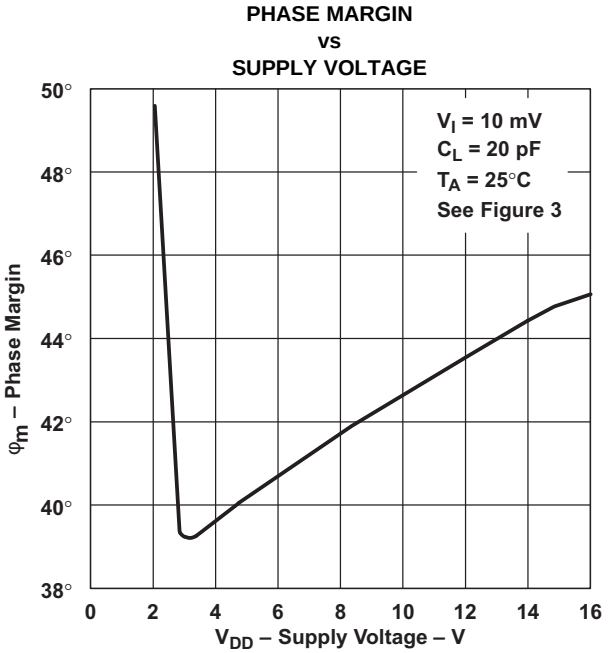


Figure 33.



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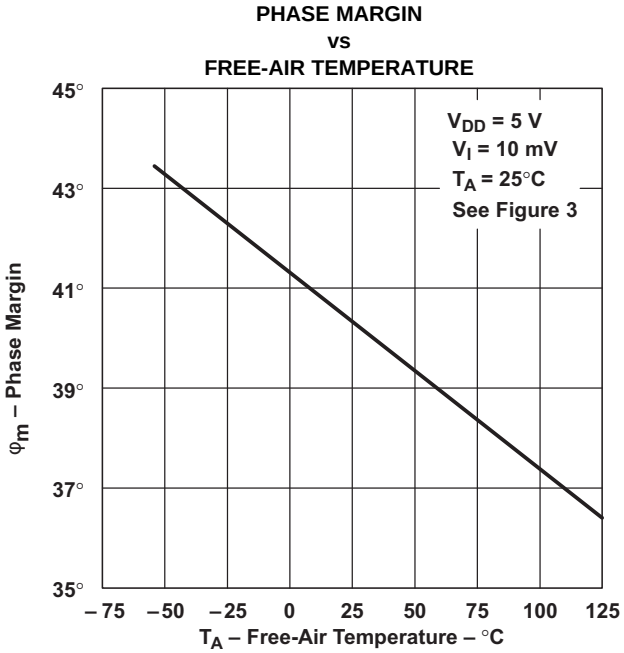

Figure 35.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

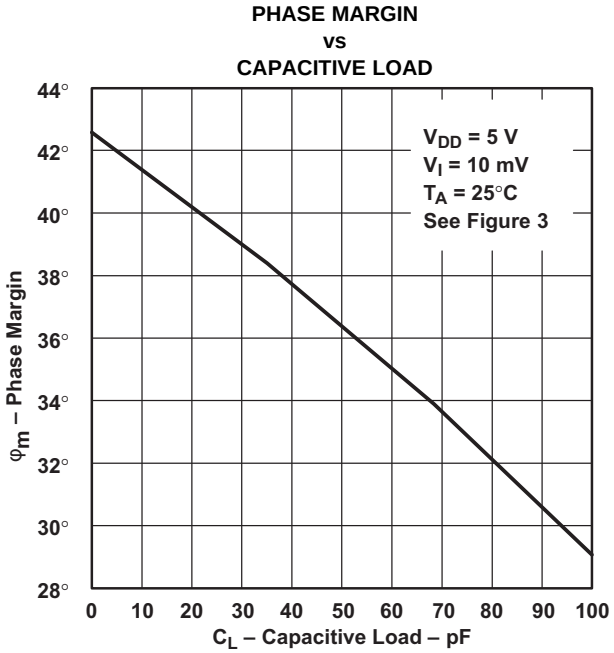


Figure 36.

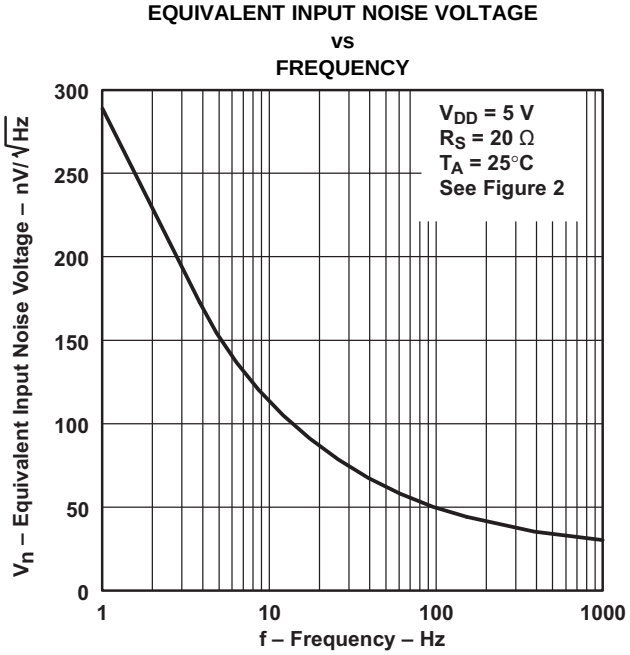


Figure 37.

APPLICATION INFORMATION

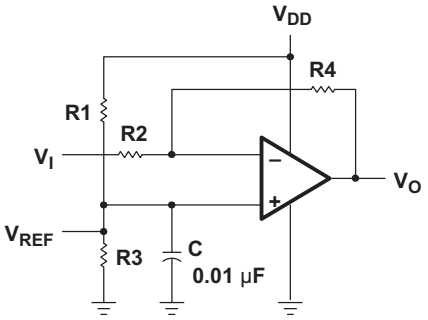
Single-Supply Operation

While the TLC27M4 and TLC27M9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I) \frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference

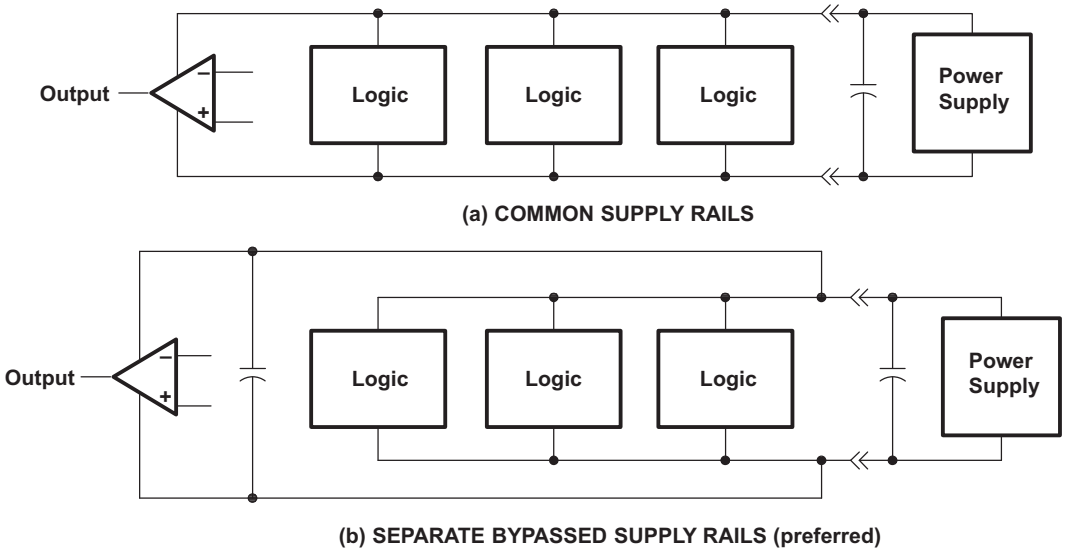


Figure 39. Common Versus Separate Supply Rails

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Input Characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the *Parameter Measurement Information* section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as unity-gain followers to avoid possible oscillation.

Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

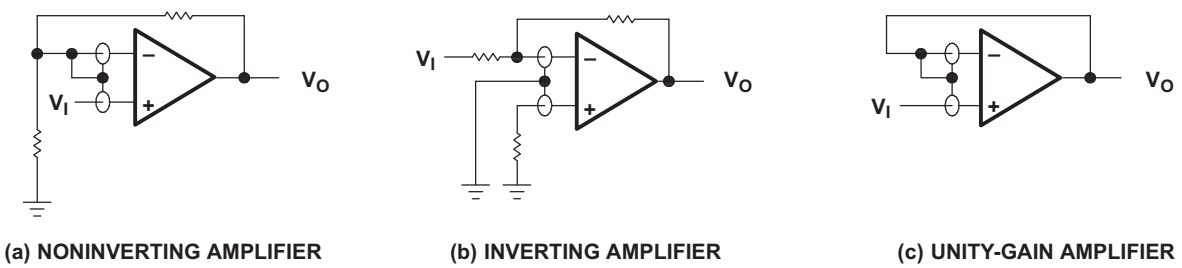

Figure 40. Guard-Ring Schemes

Output Characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see *typical characteristics*). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

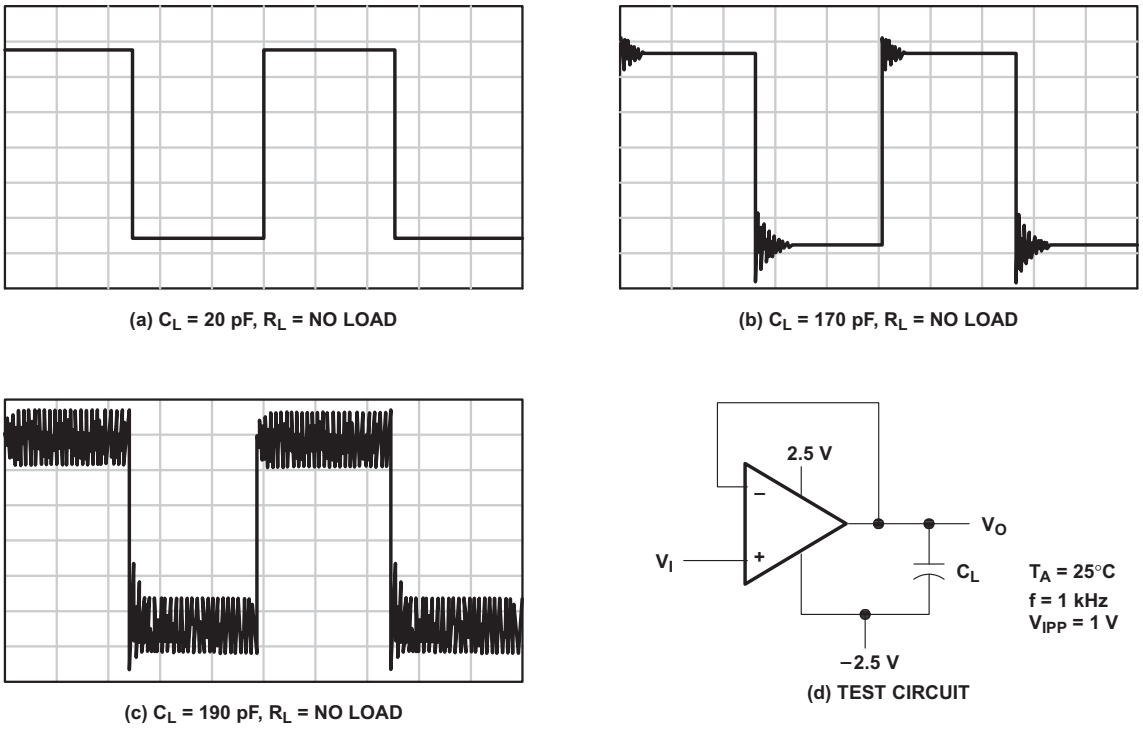

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (RP) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of RP, a voltage offset from 0 V at the output occurs. Second, pullup resistor RP acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

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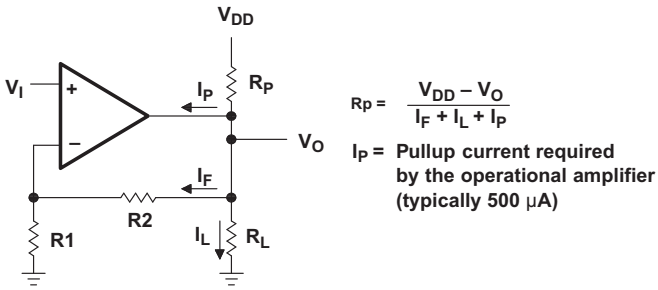

Figure 42. Resistive Pullup to Increase V_{OH}

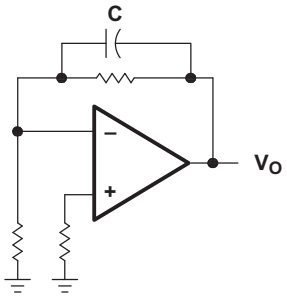

Figure 43. Compensation for Input Capacitance

Feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

Electrostatic Discharge Protection

The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

Latch-Up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand —100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground; it can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

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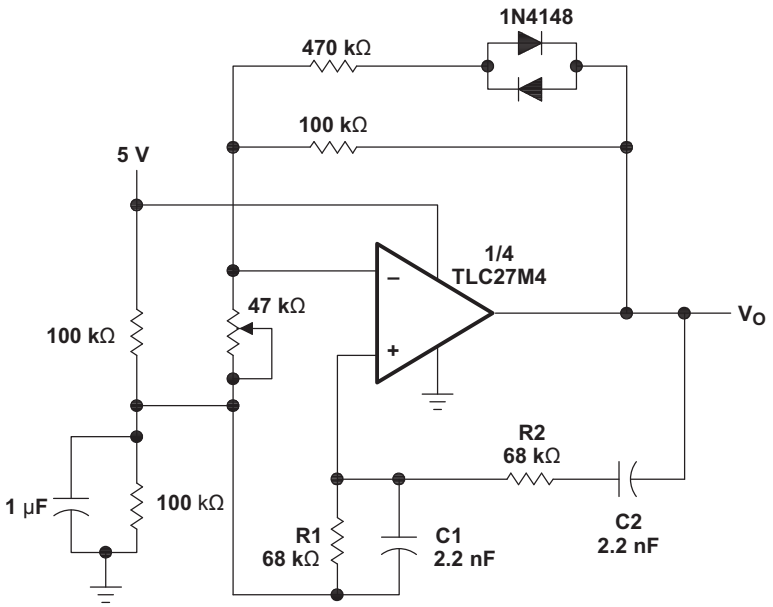

NOTE: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Figure 44. Wien Oscillator

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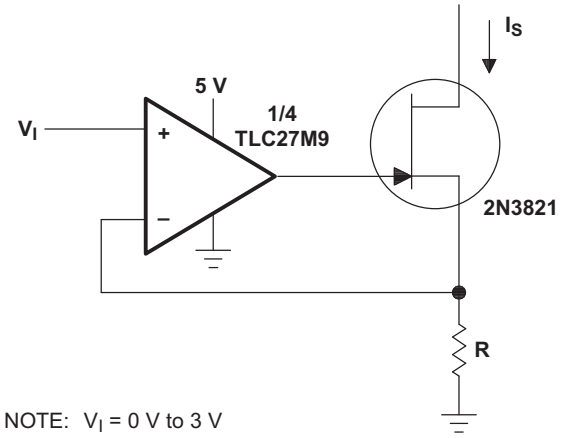
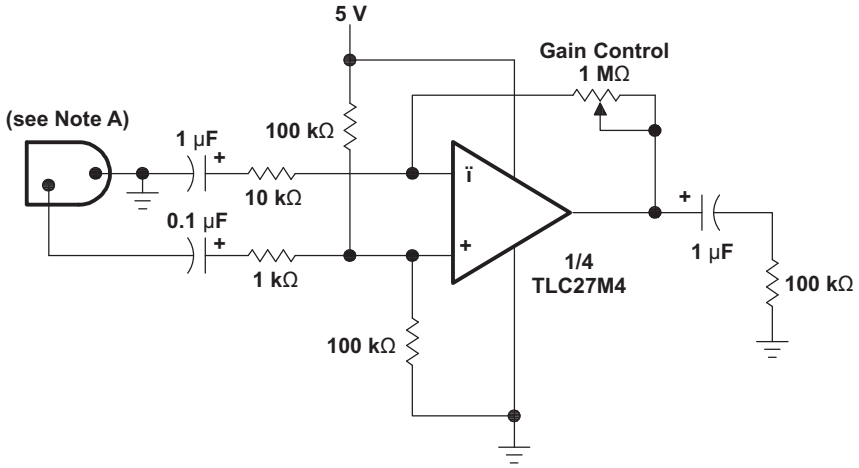


NOTE: V_I = 0 V to 3 V

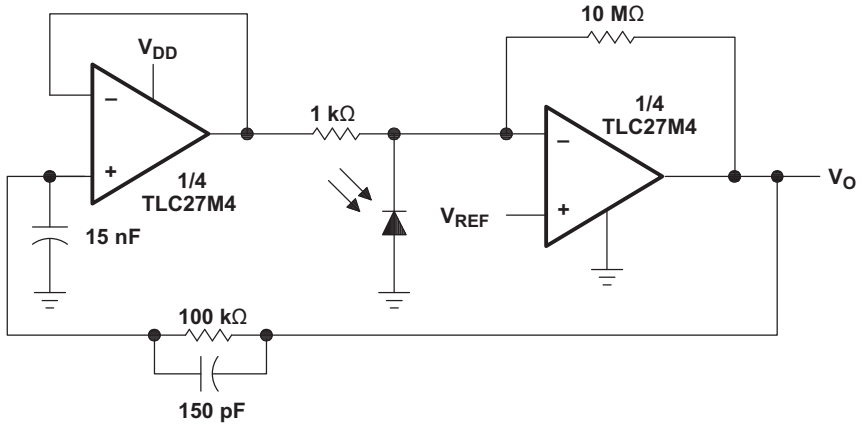
$$I_S = \frac{V_I}{R}$$

Figure 45. Precision Low-Current Sink



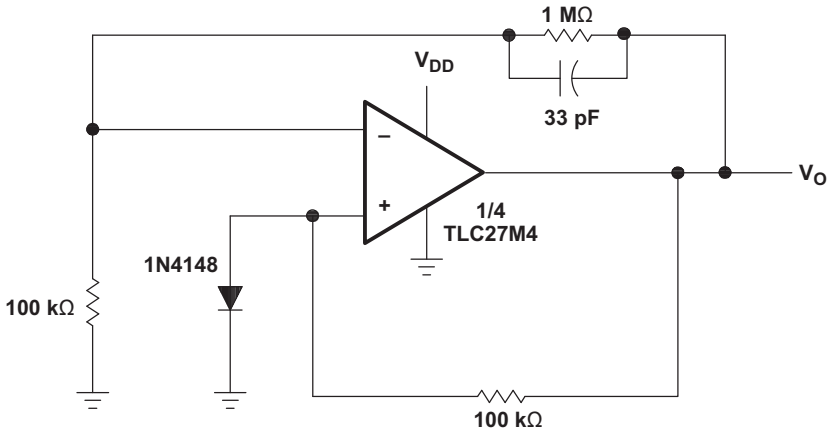
NOTE A: Low to medium impedance dynamic mike

Figure 46. Microphone Preamplifier



NOTE: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} – 2 V

Figure 47. Photo-Diode Amplifier With Ambient Light Rejection



NOTE: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

Figure 48. Low-Power Voltage Regulator

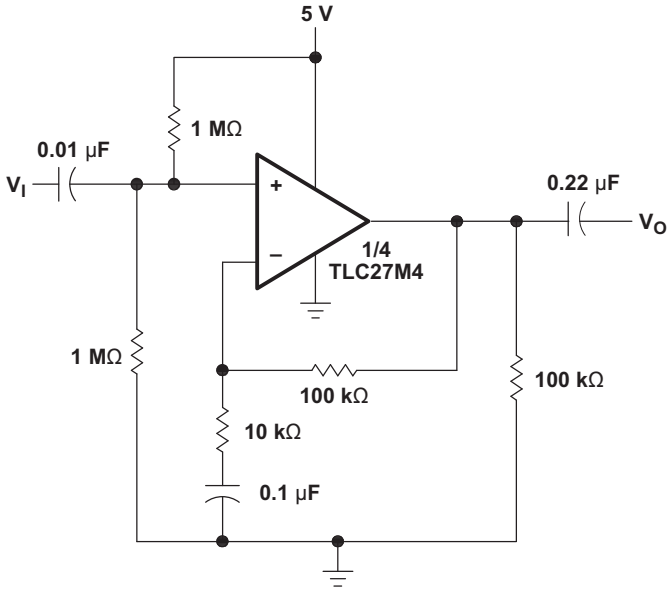


Figure 49. Single-Rail AC Amplifier

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27M4ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M4AC	Samples
TLC27M4ACDG4	ACTIVE	SOIC	D	14	50	TBD	Call TI	Call TI	0 to 70		Samples
TLC27M4ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M4AC	Samples
TLC27M4ACDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70		Samples
TLC27M4ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27M4ACN	Samples
TLC27M4ACNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27M4ACN	Samples
TLC27M4AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M4AI	Samples
TLC27M4AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M4AI	Samples
TLC27M4AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27M4AIN	Samples
TLC27M4AINE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	-40 to 85		Samples
TLC27M4BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M4BC	Samples
TLC27M4BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M4BC	Samples
TLC27M4BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27M4BCN	Samples
TLC27M4BID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M4BI	Samples
TLC27M4BIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M4BI	Samples
TLC27M4BIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27M4BIN	Samples
TLC27M4CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M4C	Samples
TLC27M4CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M4C	Samples
TLC27M4CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M4C	Samples
TLC27M4CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27M4CN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27M4CNS	ACTIVE	SO	NS	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M4	Samples
TLC27M4CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M4	Samples
TLC27M4CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M4	Samples
TLC27M4ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27M4I	Samples
TLC27M4IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27M4I	Samples
TLC27M4IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27M4I	Samples
TLC27M4IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27M4I	Samples
TLC27M4IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27M4IN	Samples
TLC27M4IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P27M4I	Samples
TLC27M4IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P27M4I	Samples
TLC27M9CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M9C	Samples
TLC27M9CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M9C	Samples
TLC27M9CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27M9C	Samples
TLC27M9CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27M9CN	Samples
TLC27M9ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27M9I	Samples
TLC27M9IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27M9I	Samples
TLC27M9IDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TLC27M9IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27M9IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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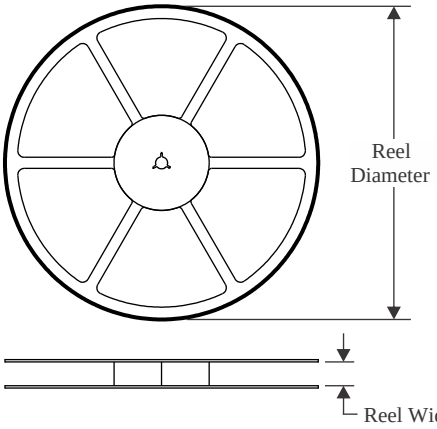
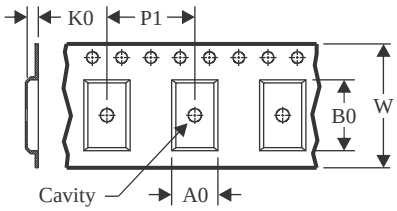
TAPE AND REEL INFORMATION

REEL DIMENSIONS

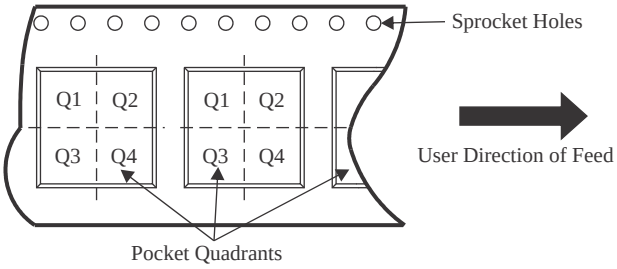


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

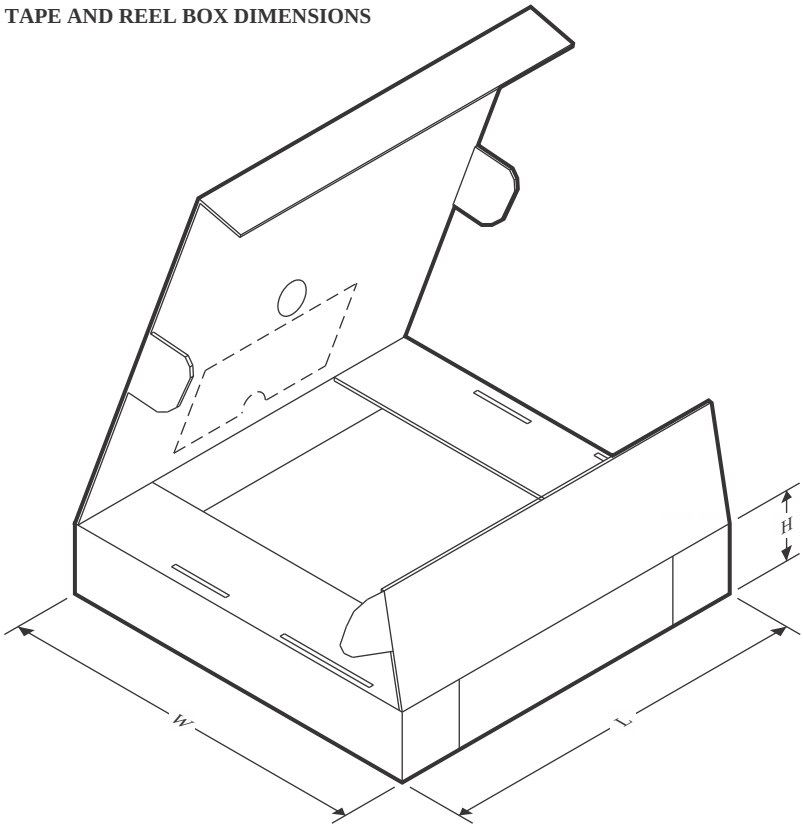
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27M4ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M4AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M4BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M4BIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M4CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M4CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC27M4CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC27M4IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M4IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC27M9CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27M9IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

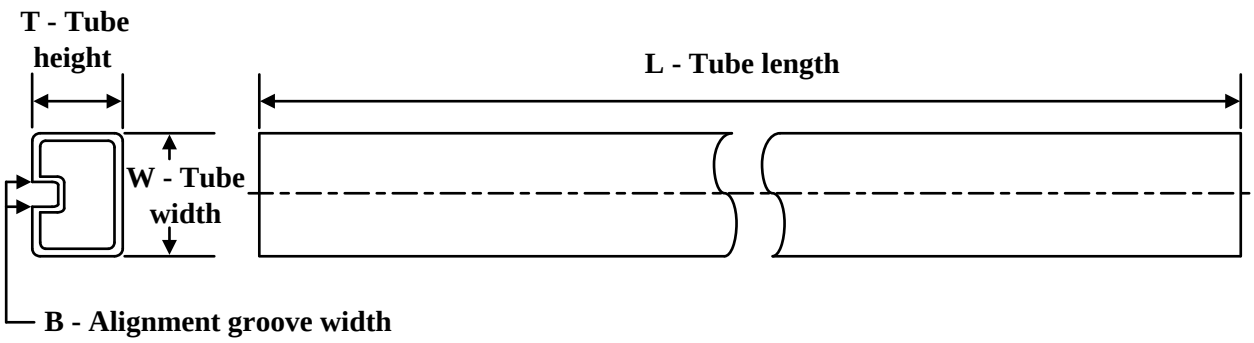
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27M4ACDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M4AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M4BCDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M4BIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M4CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M4CNSR	SO	NS	14	2000	356.0	356.0	35.0
TLC27M4CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC27M4IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M4IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC27M9CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27M9IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



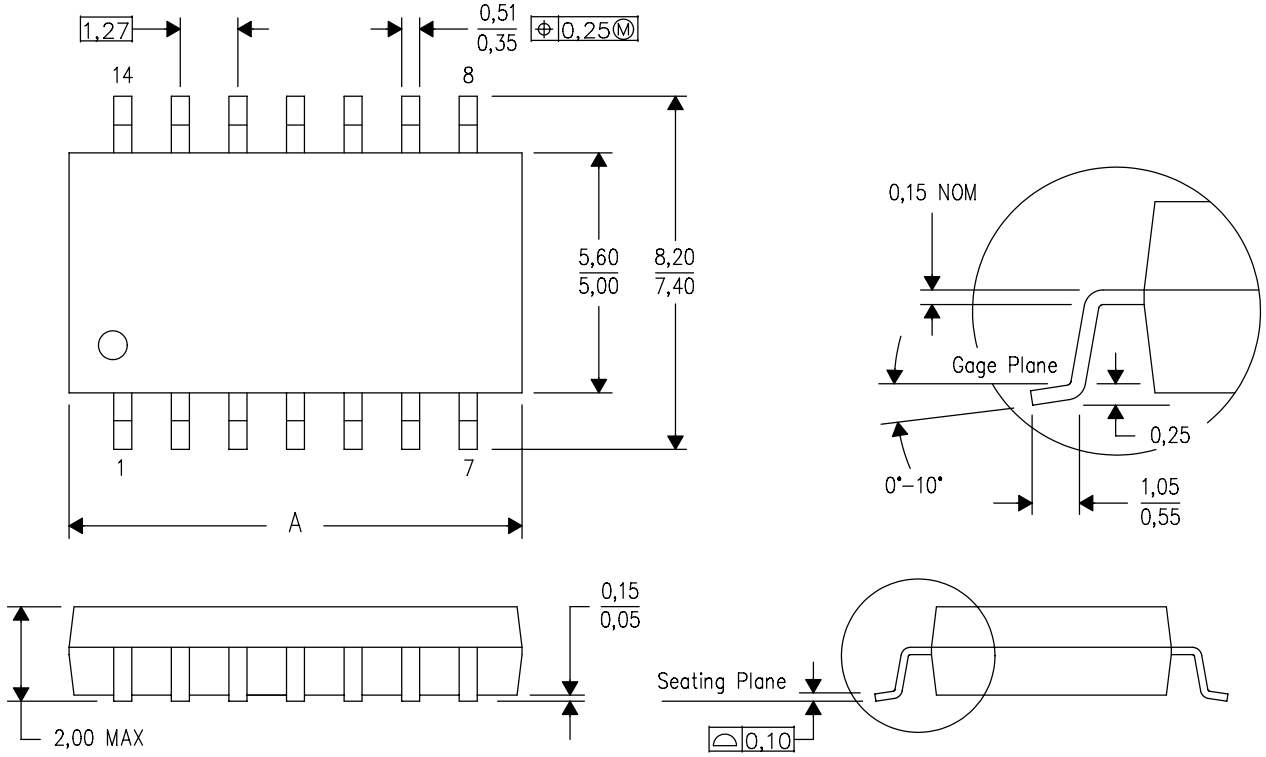
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27M4ACD	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4ACN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4ACNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4AID	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4BCD	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4BCN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4BID	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4BIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4CNS	NS	SOP	14	50	530	10.5	4000	4.1
TLC27M4ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4IDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M4IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M4IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC27M9CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M9CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27M9ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC27M9IN	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

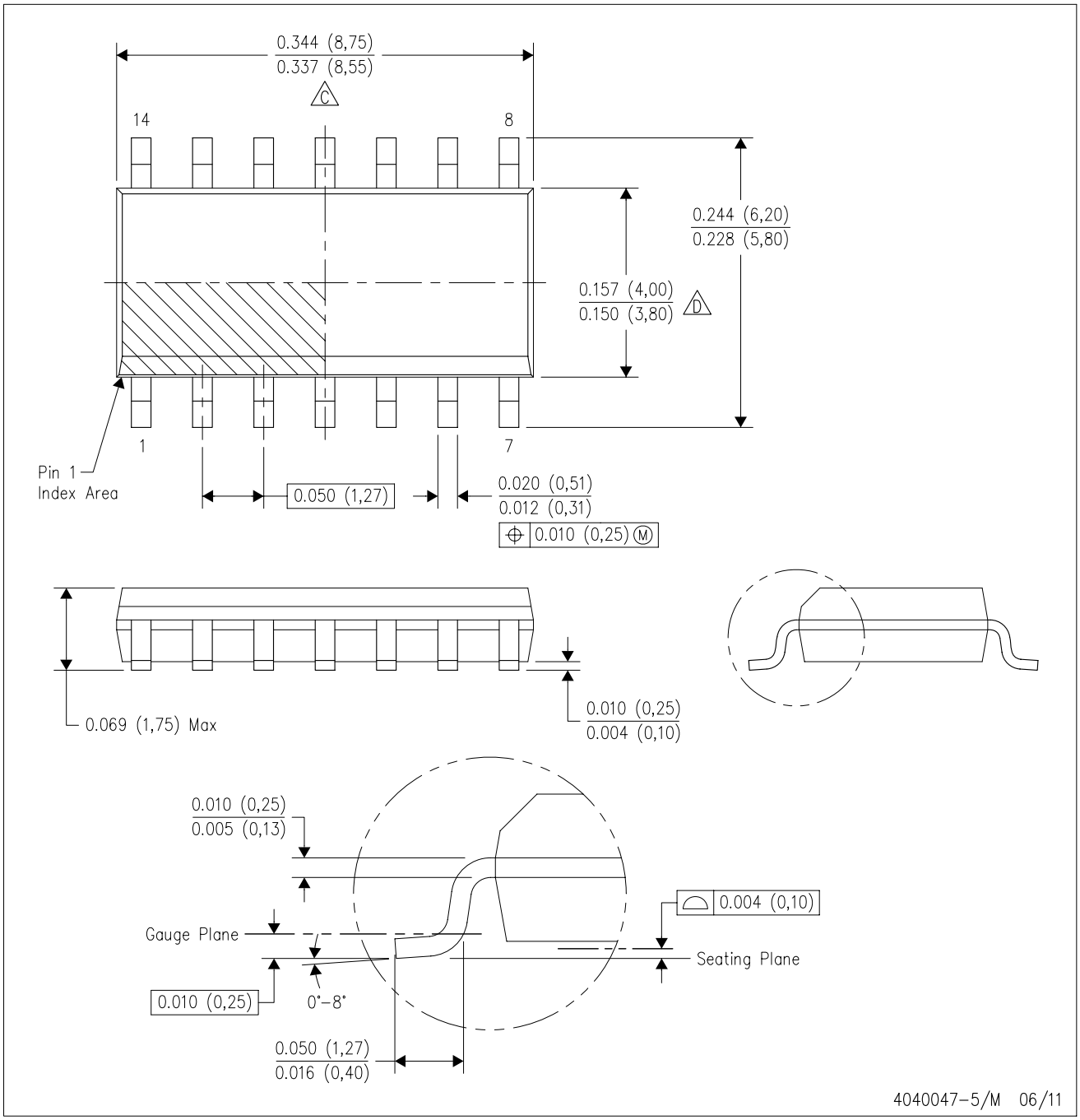


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

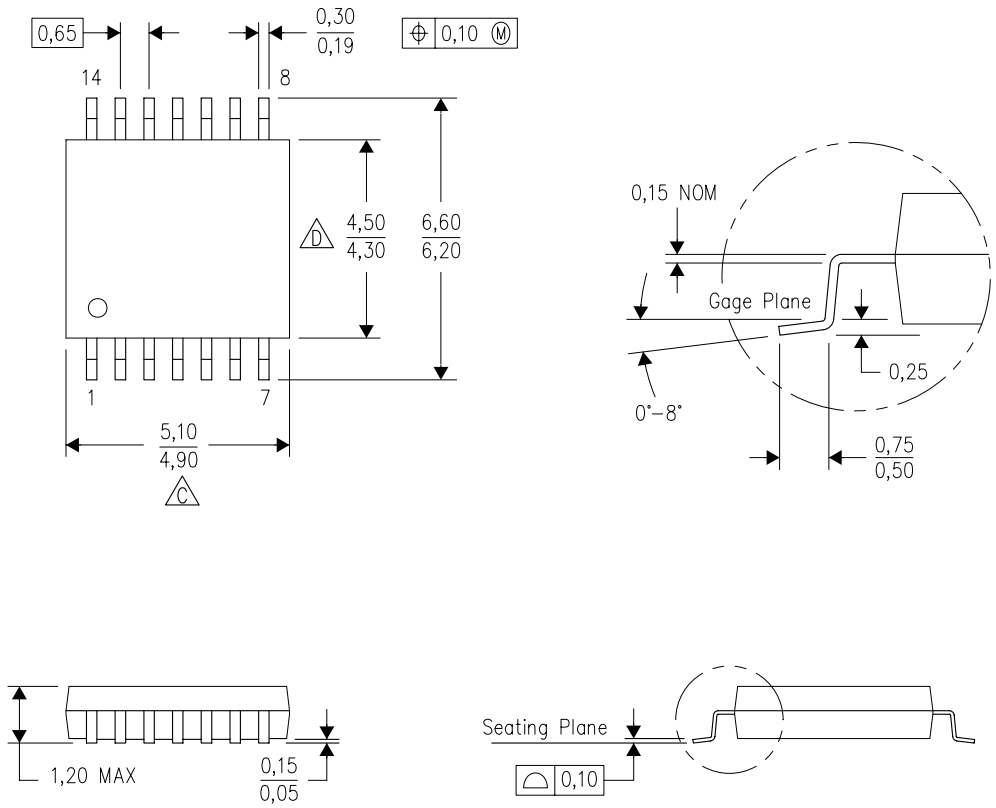
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

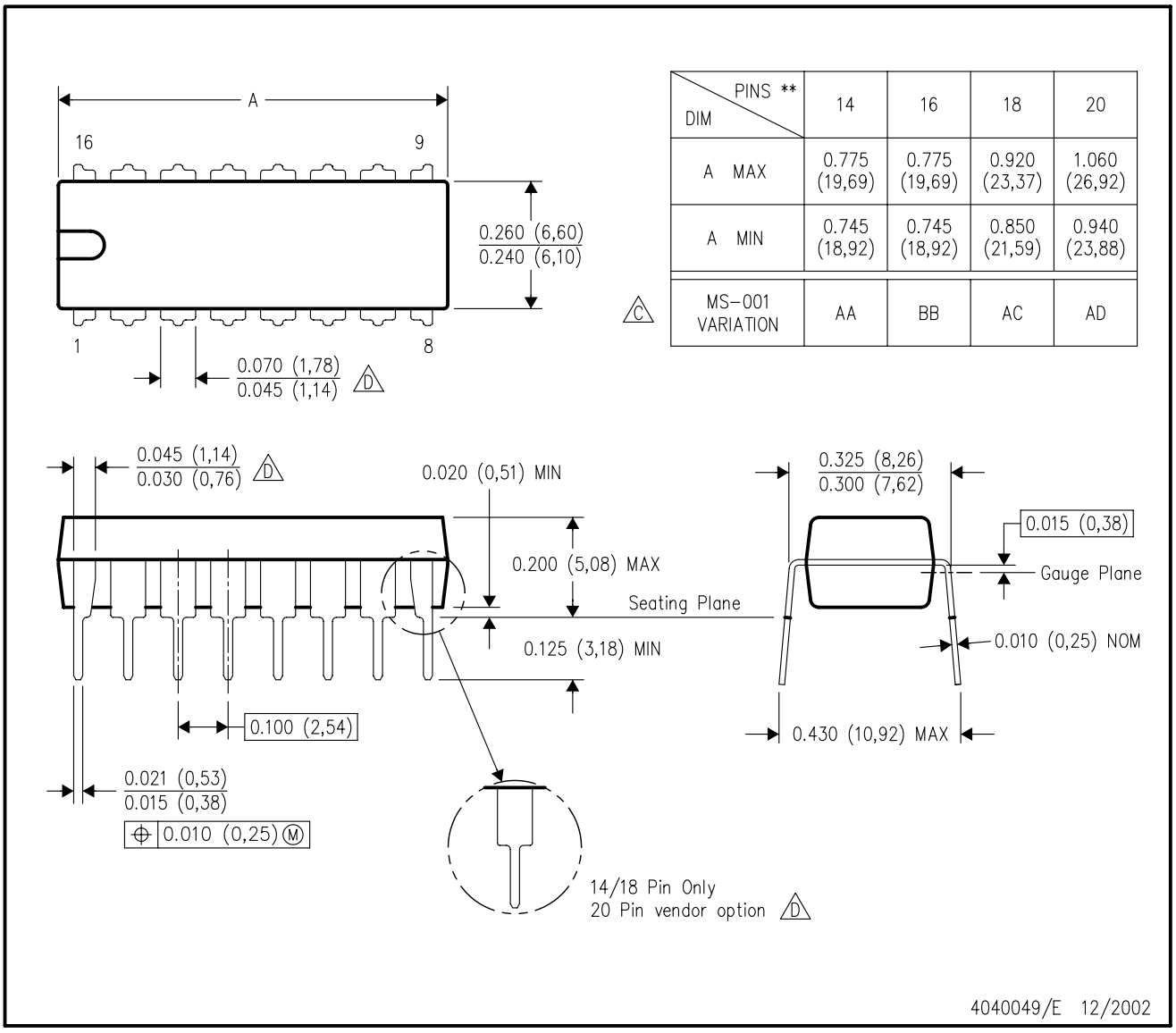
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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