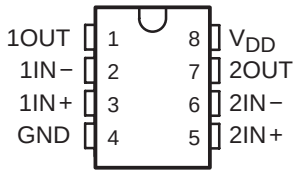
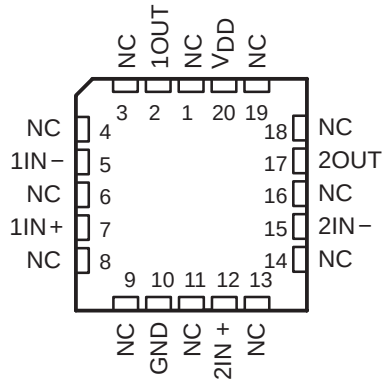
- **Trimmed Offset Voltage: TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **−40°C to 85°C . . . 4 V to 16 V**
  - **−55°C to 125°C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Ultra-Low Power . . . Typically 95 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC − No internal connection

description

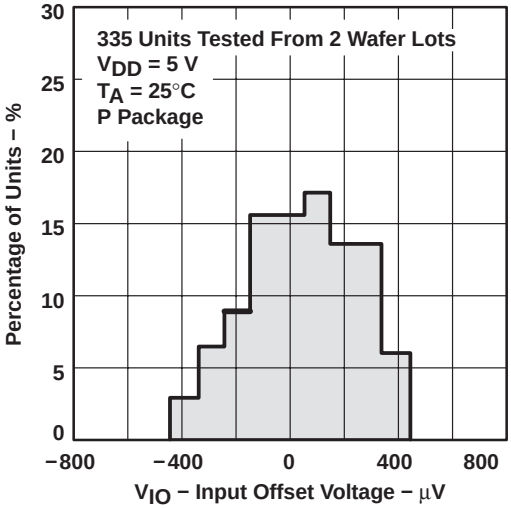
The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV 2 mV 5 mV 10 mV	TLC27L7CD TLC27L2BCD TLC27L2ACD TLC27L2CD	—	—	TLC27L7CP TLC27L2BCP TLC27L2ACP TLC27L2CP
−40°C to 85°C	500 μV 2 mV 5 mV 10 mV	TLC27L7ID TLC27L2BID TLC27L2AID TLC27L2ID	—	—	TLC27L7IP TLC27L2BIP TLC27L2AIP TLC27L2IP
−55°C to 125°C	500 μV 10 mV	TLC27L7MD TLC27L2MD TLC27L2MDRG4	TLC27L7MFK TLC27L2MFK	TLC27L7MJG TLC27L2MJG	TLC27L7MP TLC27L2MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L7CDR).

DISTRIBUTION OF TLC27L7 INPUT OFFSET VOLTAGE



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description (continued)

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

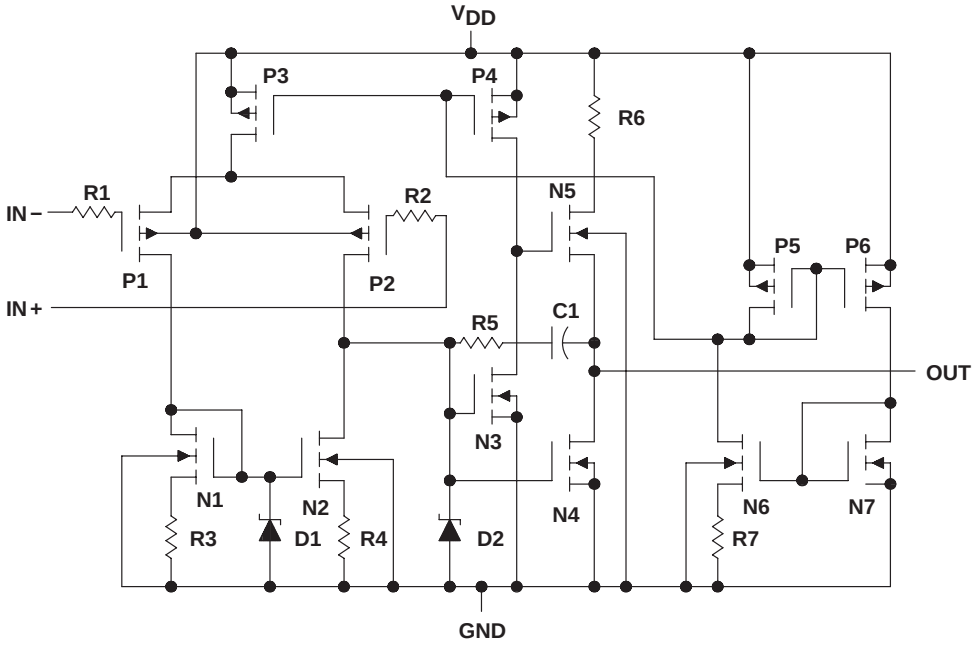
A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-Suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} . . . . . 45 mA
Total current out of GND . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
M suffix . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8 mW/°C	640 mW	520 mW	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		204	2000	µV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	700		V/mV
					0°C	50	700		
					70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	µA
					0°C		24	42	
					70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		235	2000	µV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					0°C	50	1025		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	µA
					0°C		36	66	
					70°C		22	40	

† Full range is 0°C to 70°C.

NOTES: 4 The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5 This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		240	2000	µV
					Full range			3500	
		TLC27L7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−40°C	3	4.1		
					85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	480		V/mV
					−40°C	50	900		
					85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					−40°C	60	95		
					85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	µA
					−40°C		31	54	
					85°C		15	26	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		235	2000	µV
					Full range			3500	
		TLC27L7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	µA
					−40°C		49	86	
					85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2M TLC27L7M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	µV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6	60	pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−55°C	3	4.1		
					125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	500		V/mV
					−55°C	25	1000		
					125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					−55°C	60	95		
					125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	µA
					−55°C		35	60	
					125°C		14	24	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2M TLC27L7M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	µV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7	60	pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	µA
					−55°C		56	96	
					125°C		18	30	

† Full range is −55 °C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/µs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				−40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		29°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/µs
				−40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M TLC27L7M MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				−55°C		0.04		
				125°C		0.02		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

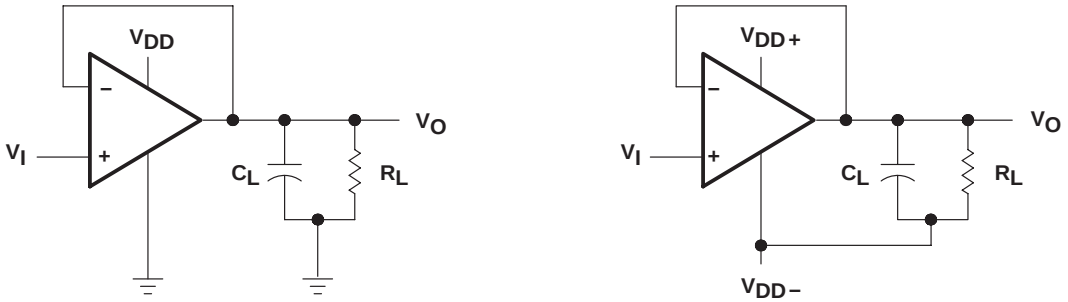
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M TLC27L7M MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/µs
				−55°C		0.06		
				125°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

PARAMETER MEASUREMENT INFORMATION

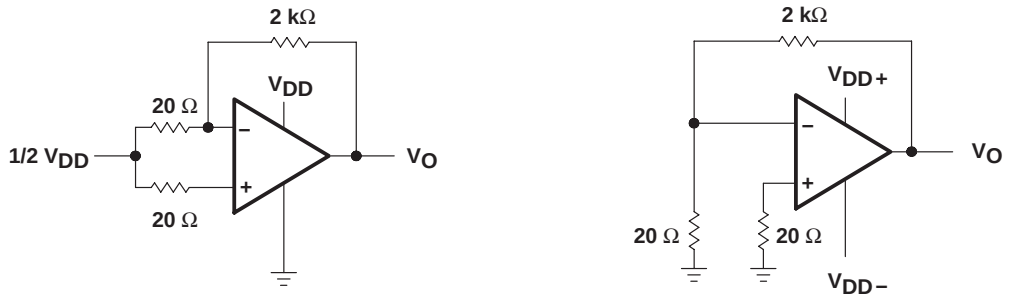
single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown in Figure 1. The use of either circuit gives the same result.



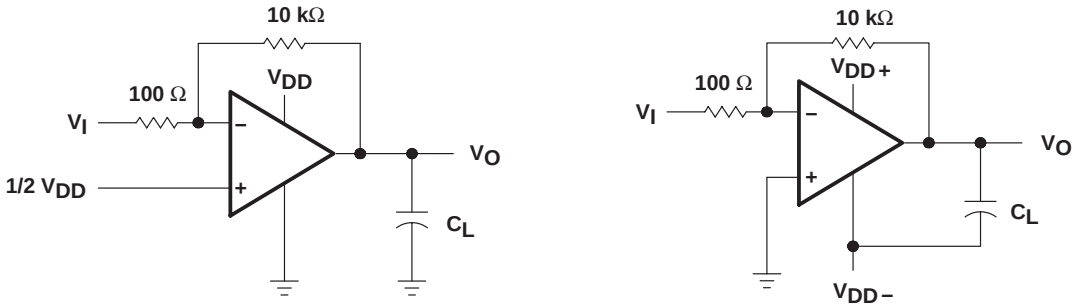
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources.Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

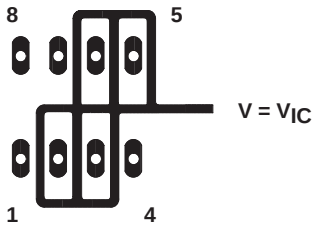


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figure 14 through Figure 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

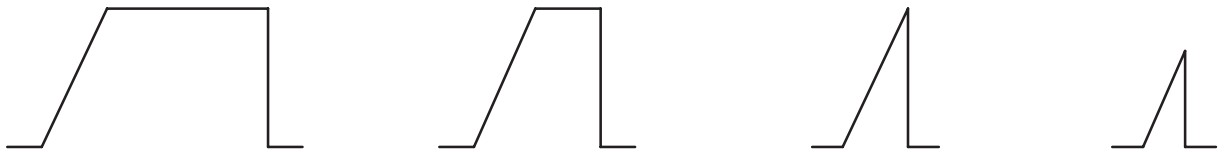
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (see Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 kHz **(b) B_{OM} > f > 100 kHz** **(c) f = B_{OM}** **(d) f > B_{OM}**

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Differential input voltage vs Free-air temperature vs Low-level output current	14,16 15,17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive Load	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

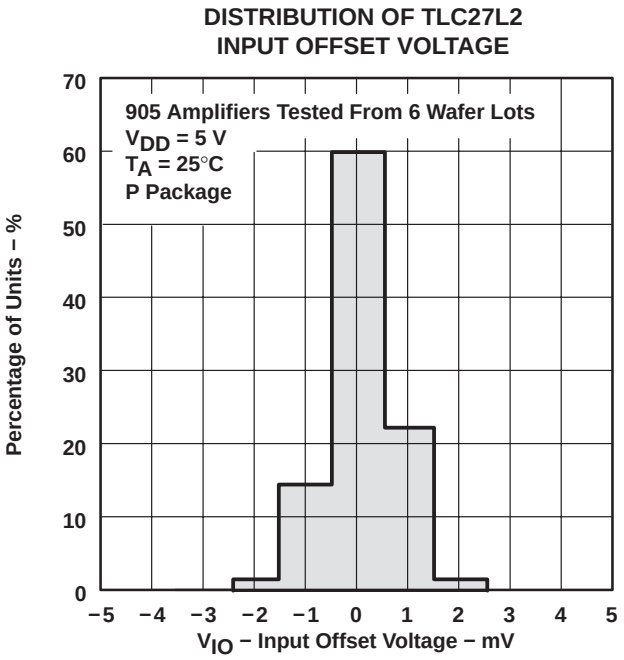


Figure 6

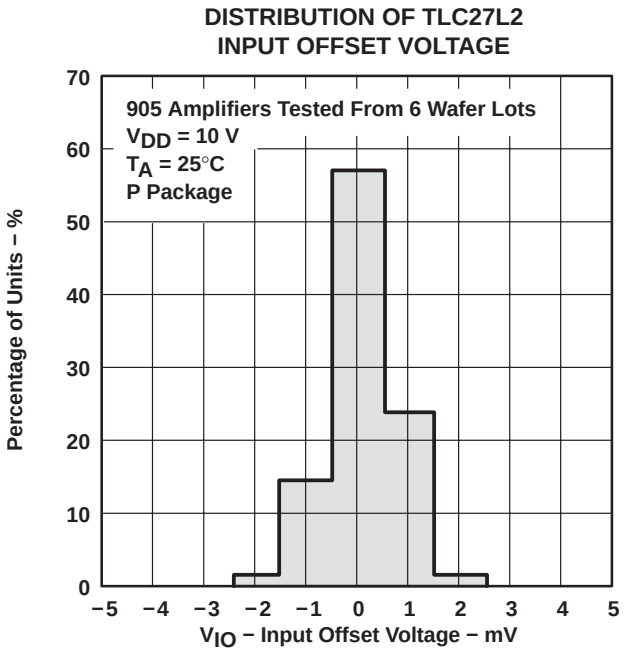


Figure 7

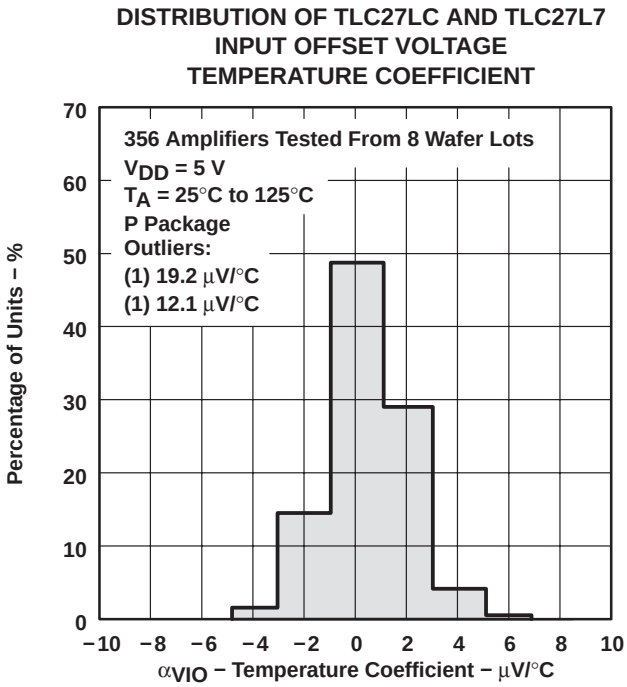


Figure 8

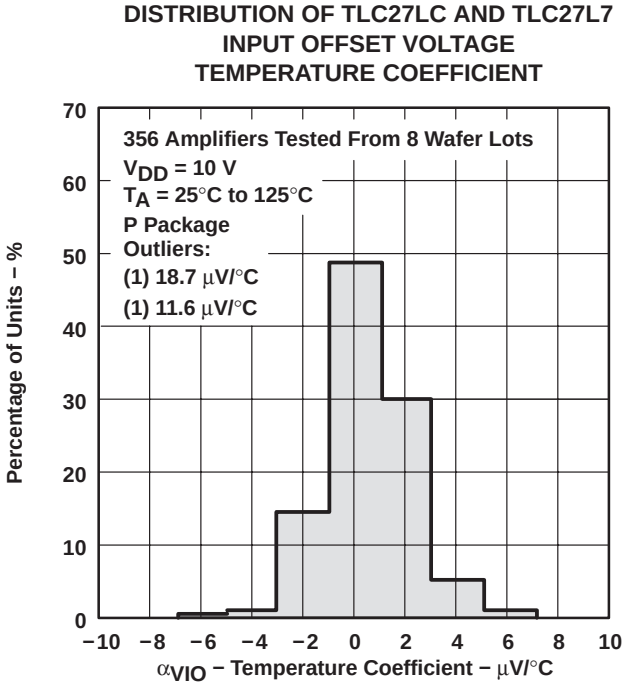


Figure 9

TYPICAL CHARACTERISTICS†

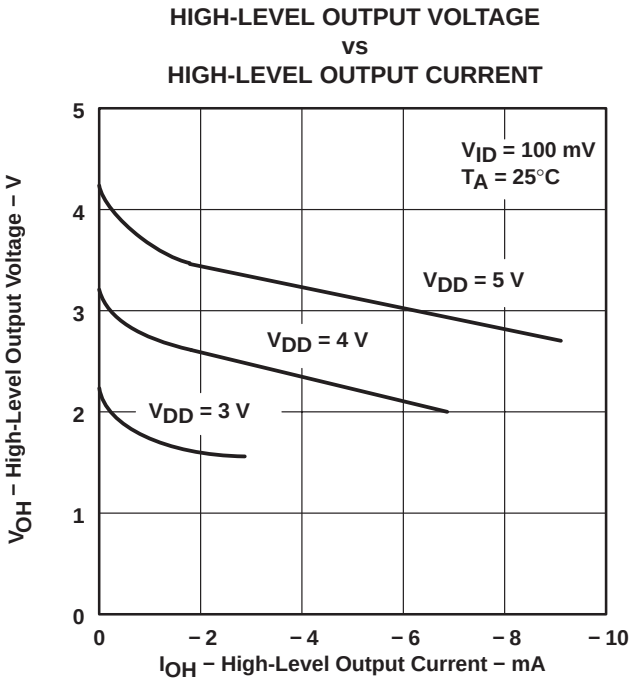


Figure 10

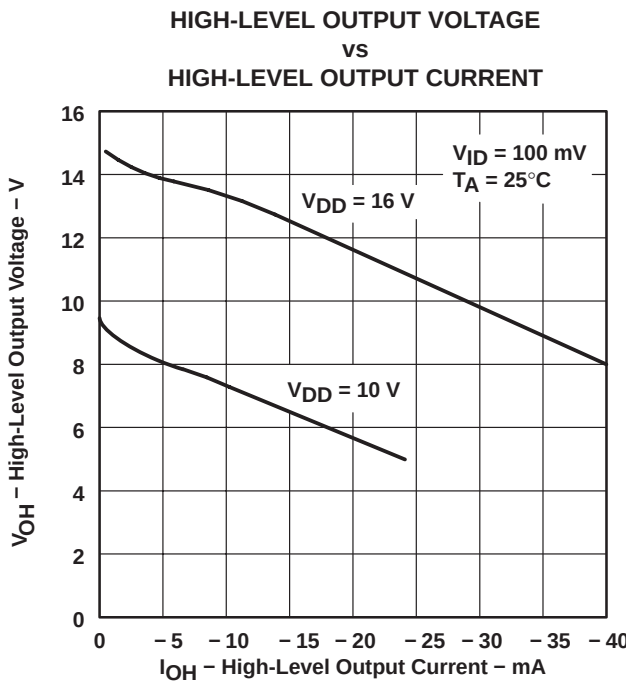


Figure 11

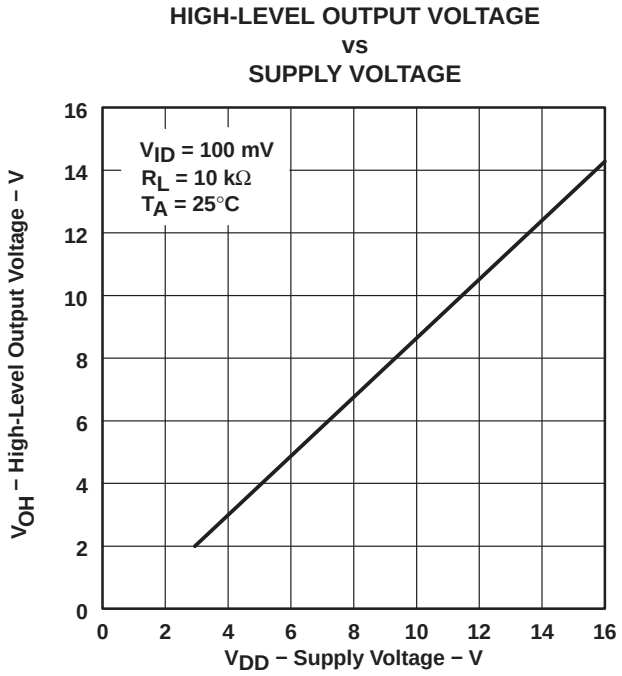


Figure 12

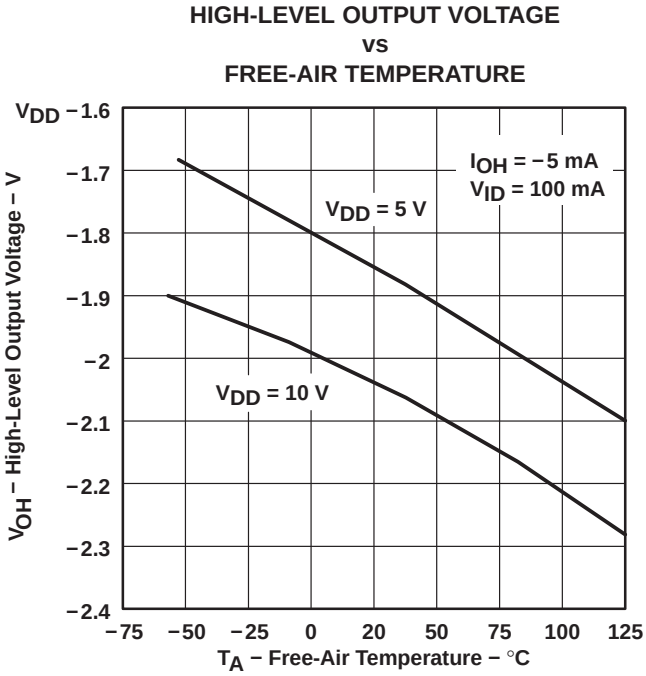


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

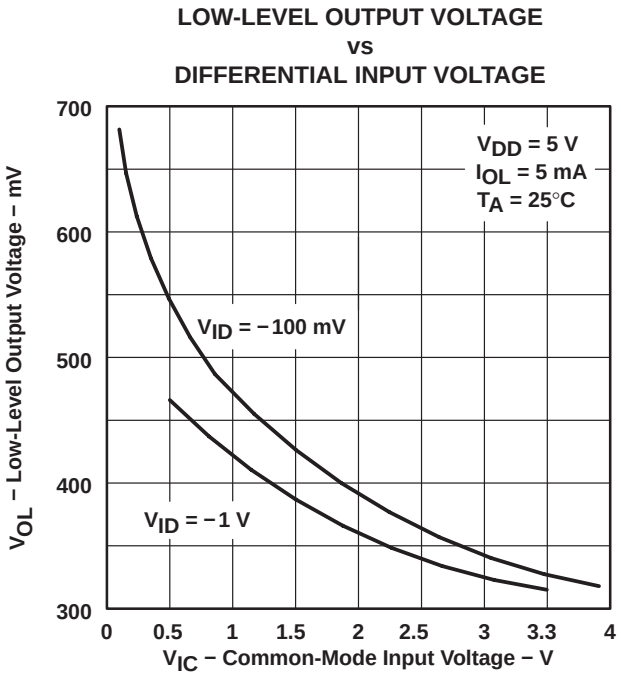


Figure 14

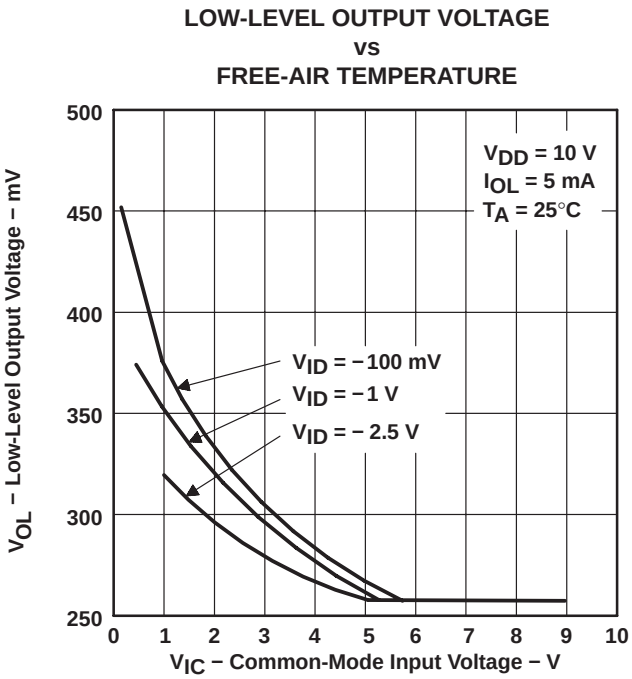


Figure 15

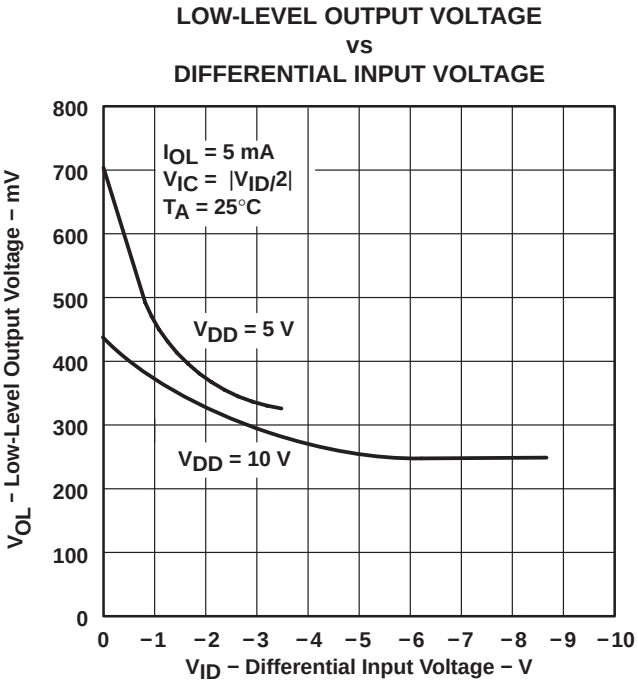


Figure 16

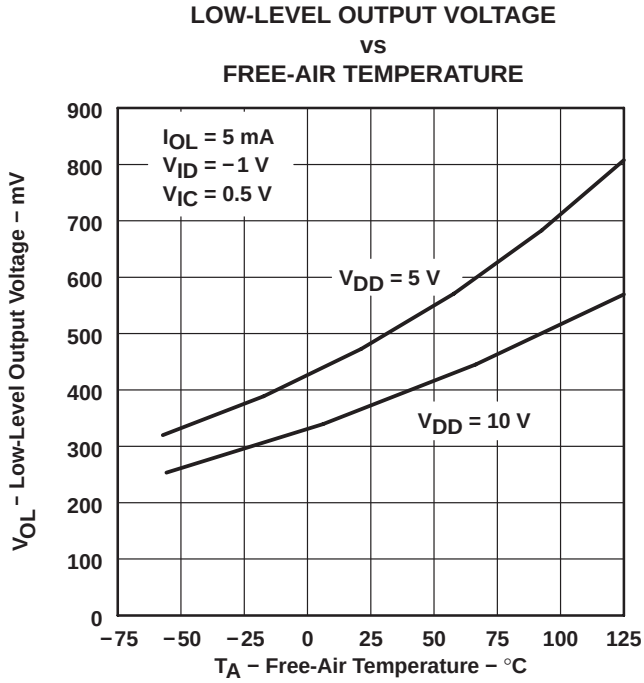


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

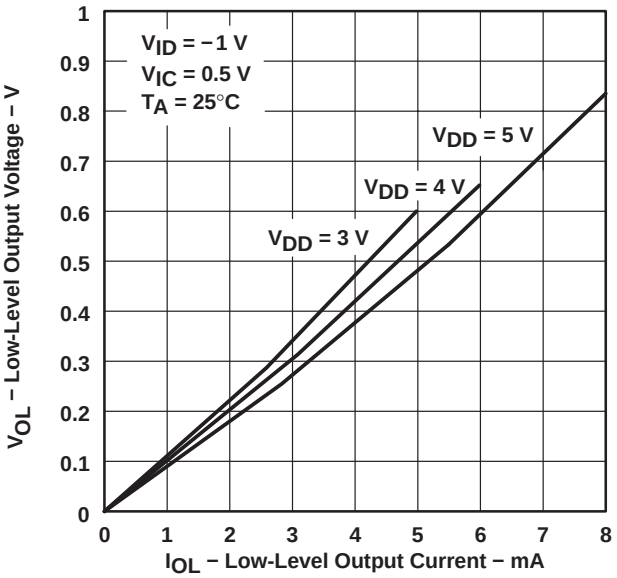


Figure 18

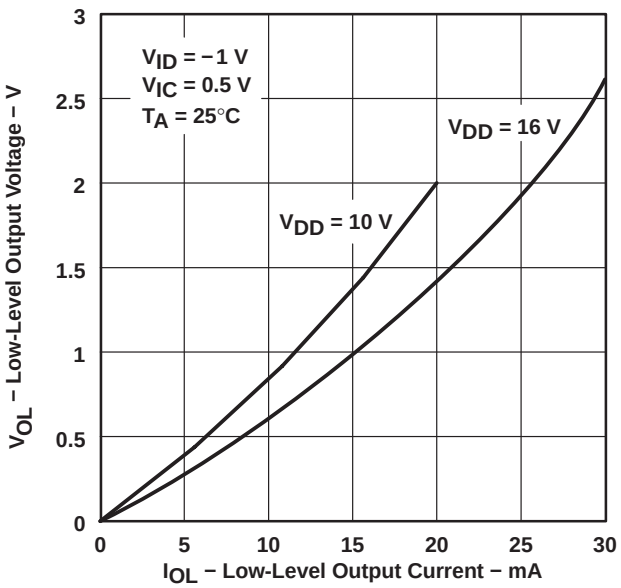


Figure 19

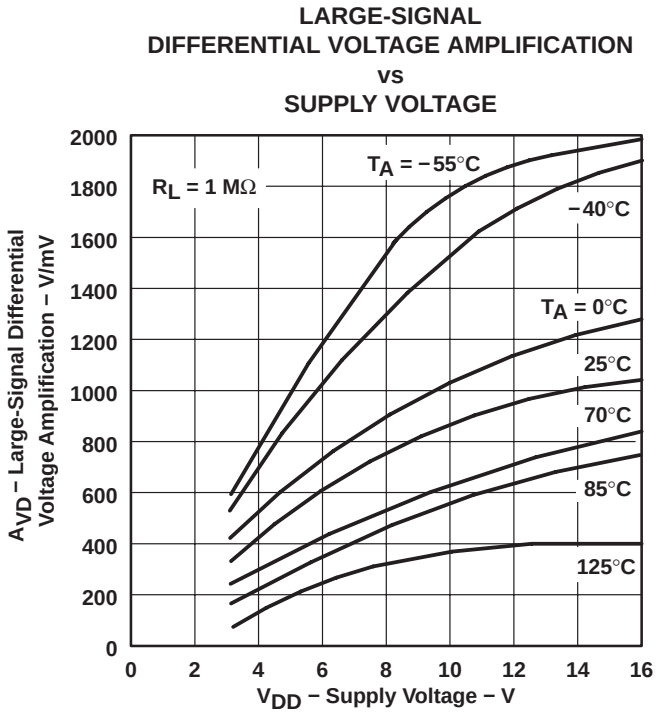


Figure 20

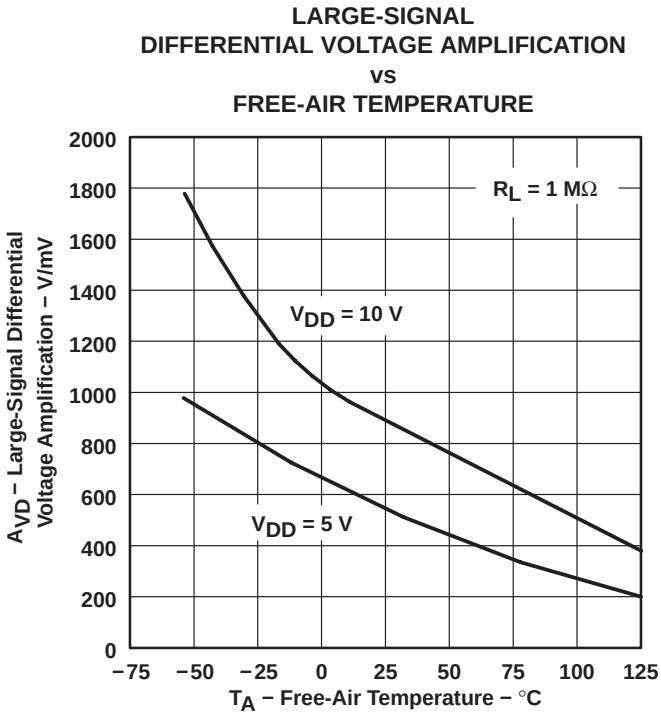
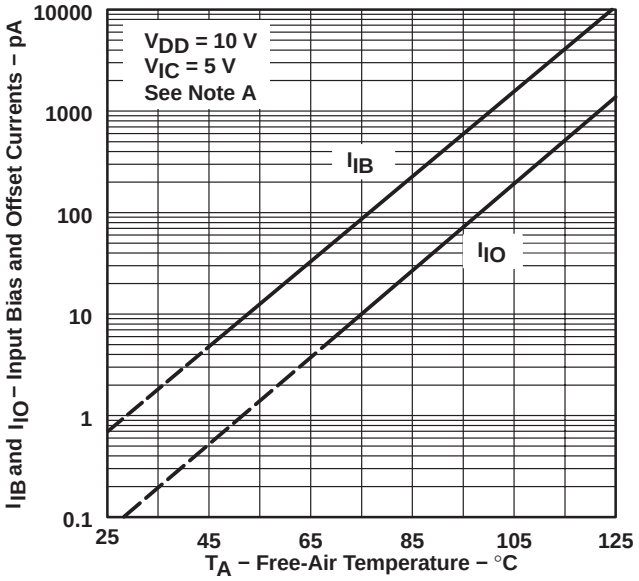


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

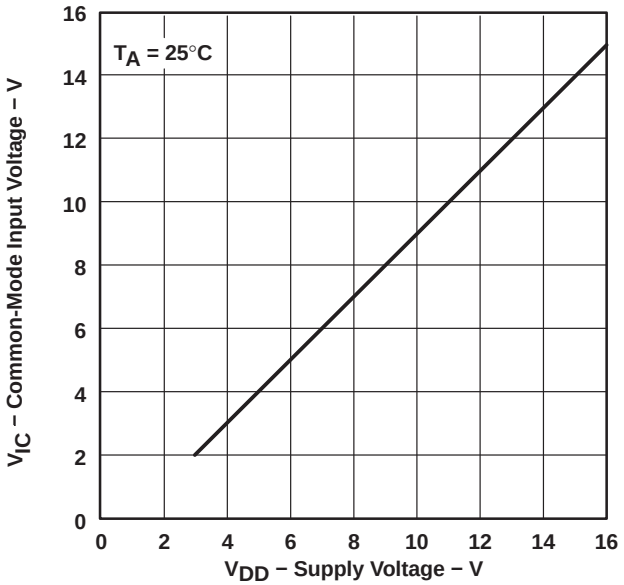


Figure 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

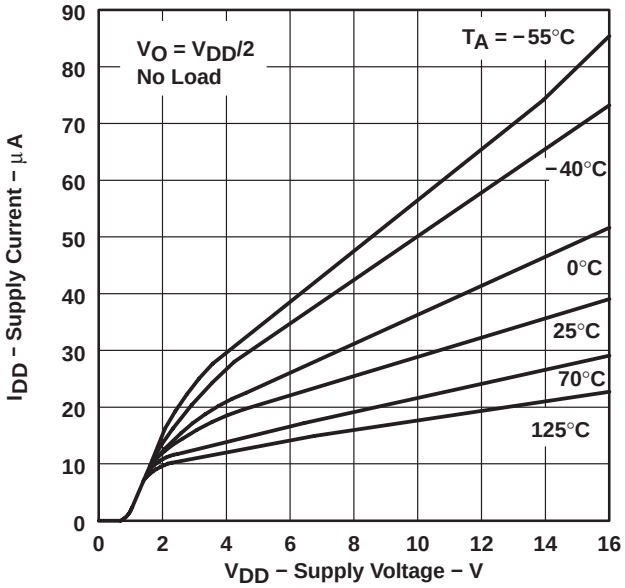


Figure 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

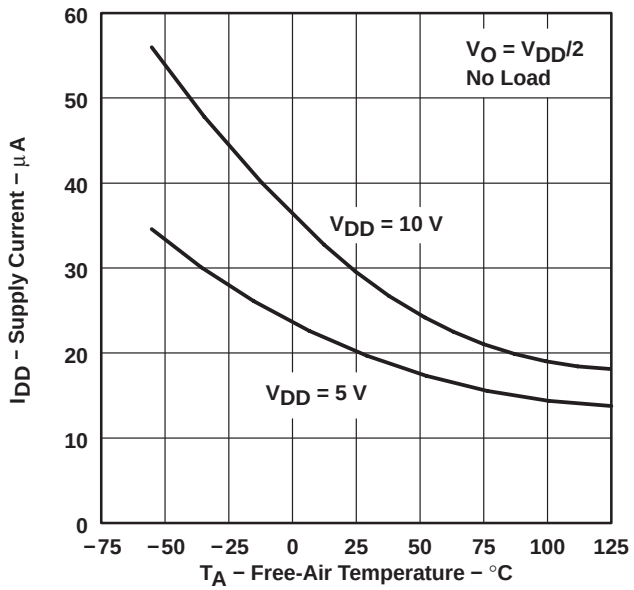


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs SUPPLY VOLTAGE

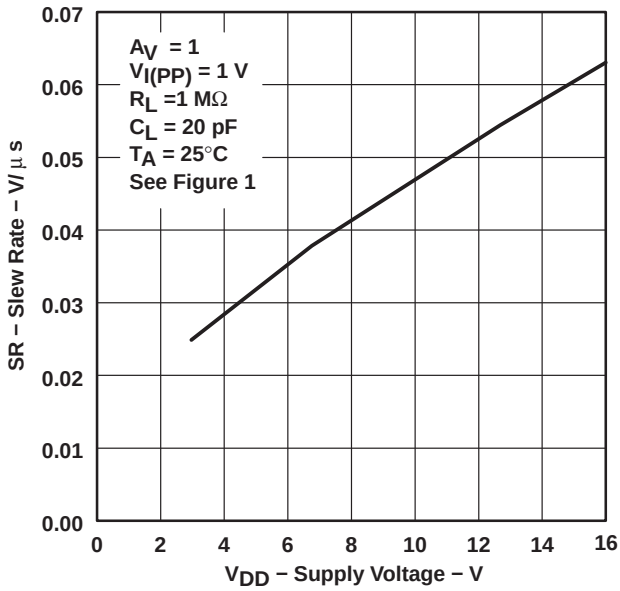


Figure 26

SLEW RATE vs FREE-AIR TEMPERATURE

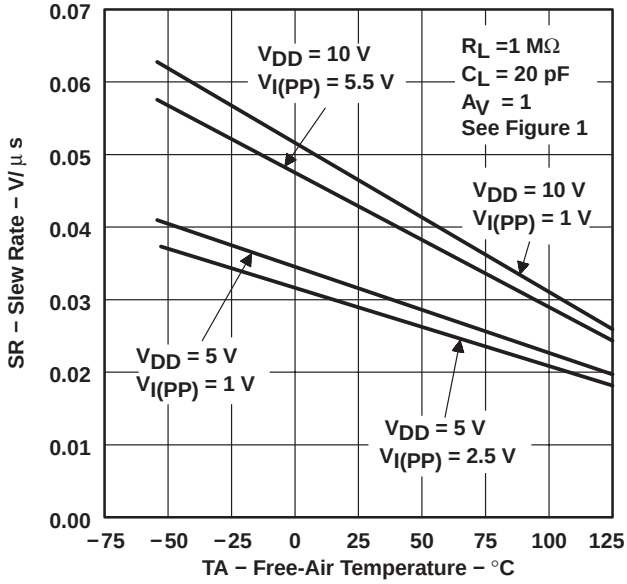


Figure 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

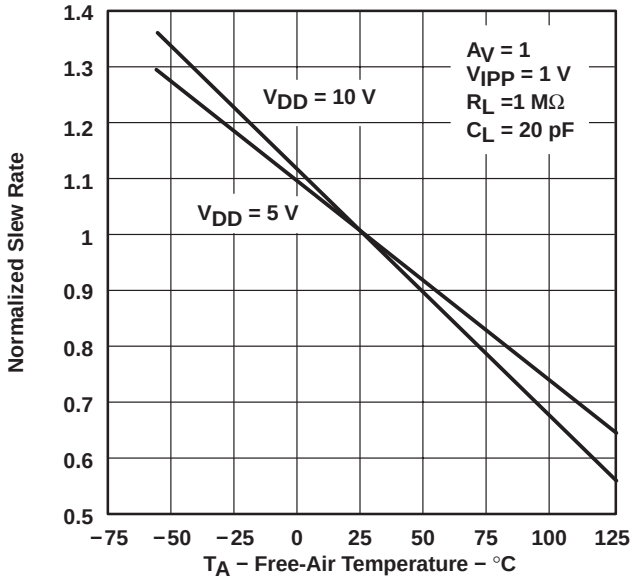


Figure 28

MAXIMUM-PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

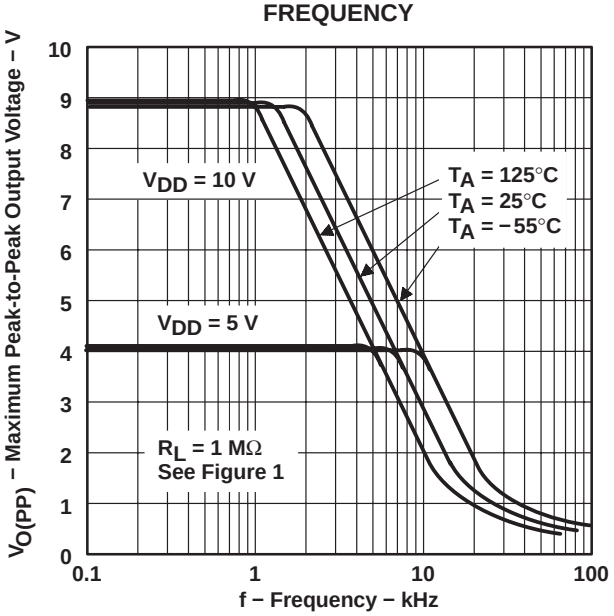


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

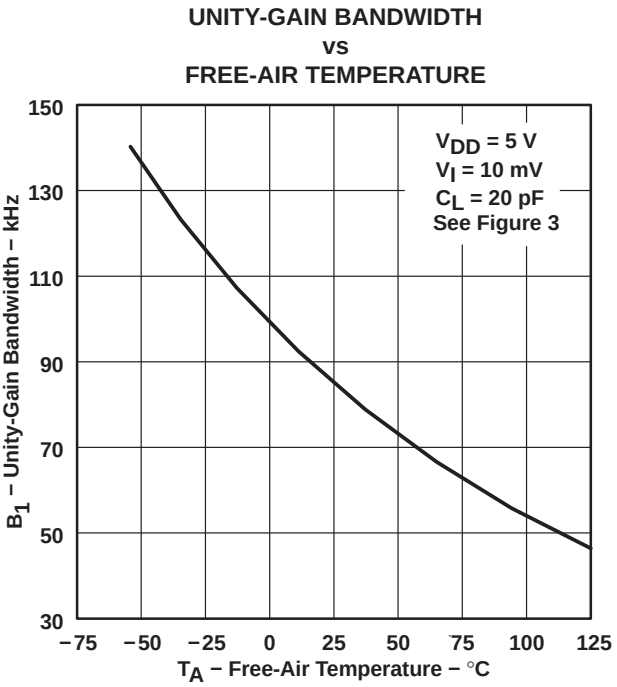


Figure 30

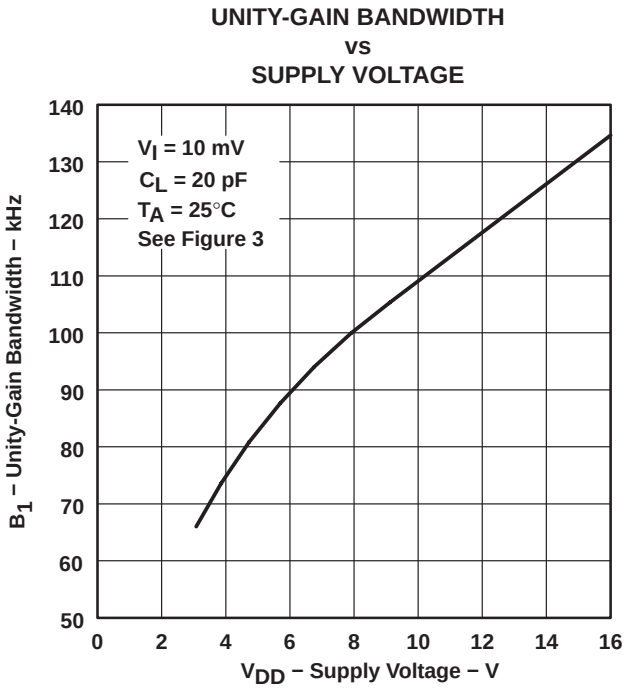


Figure 31

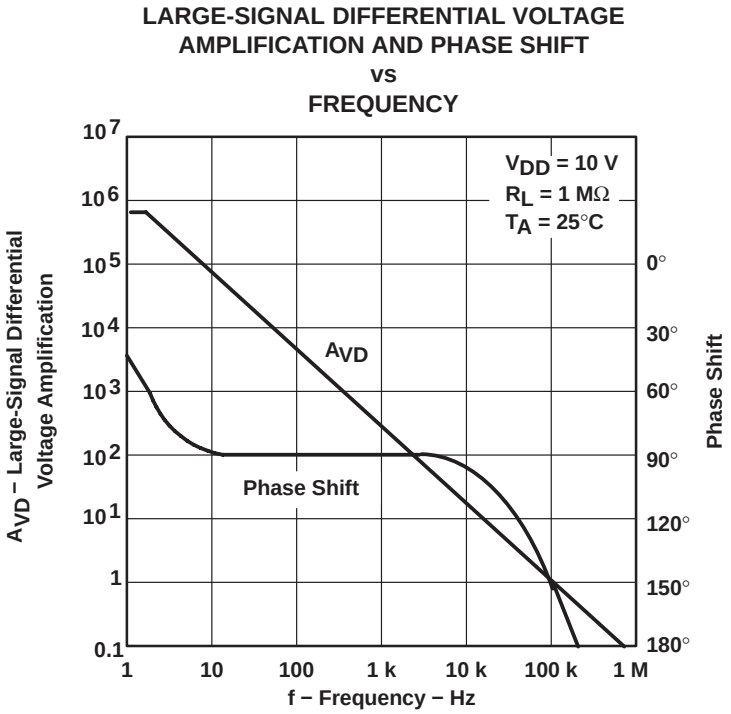


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

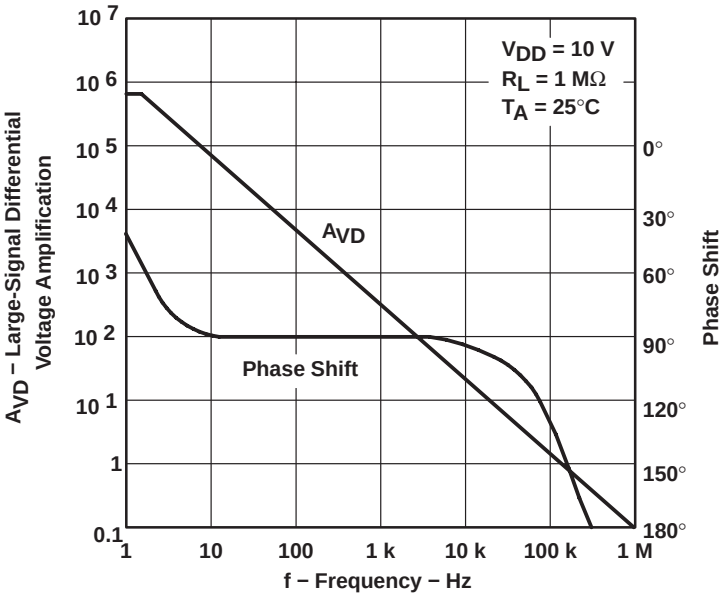


Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

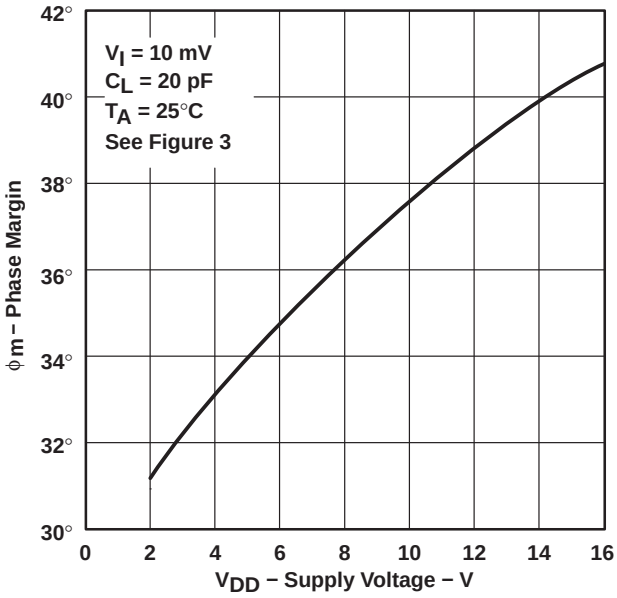


Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

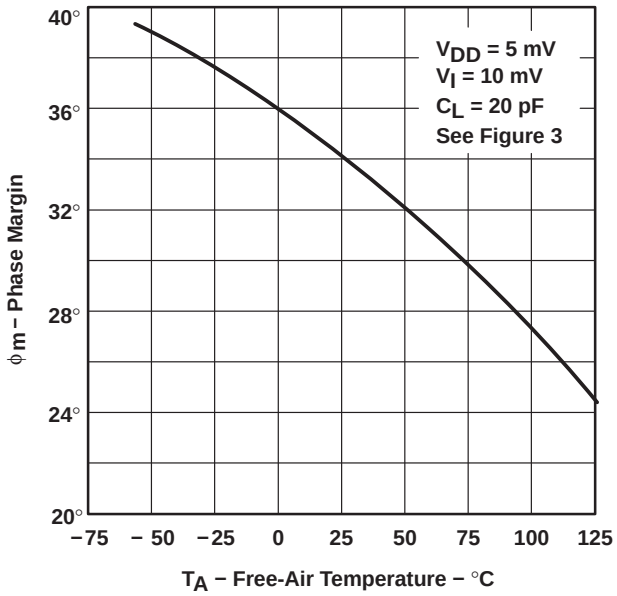


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs CAPACITIVE LOAD

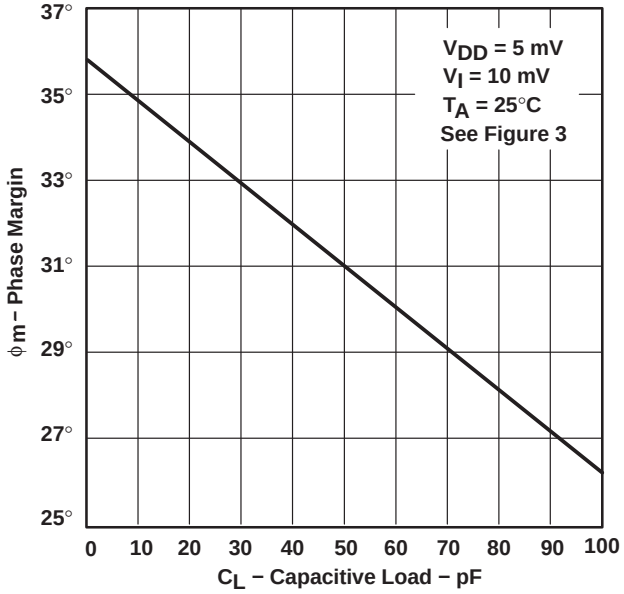


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

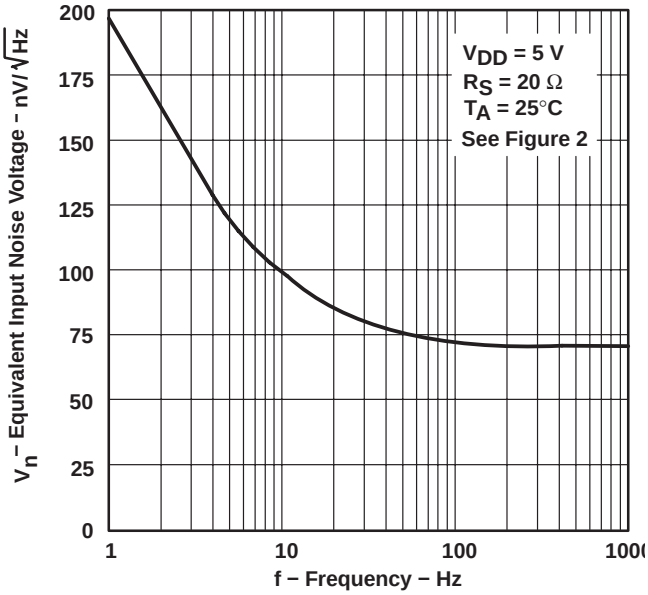


Figure 37

APPLICATION INFORMATION

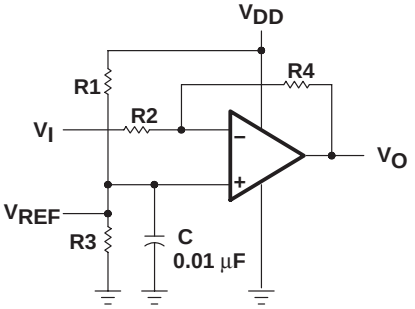
single-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference

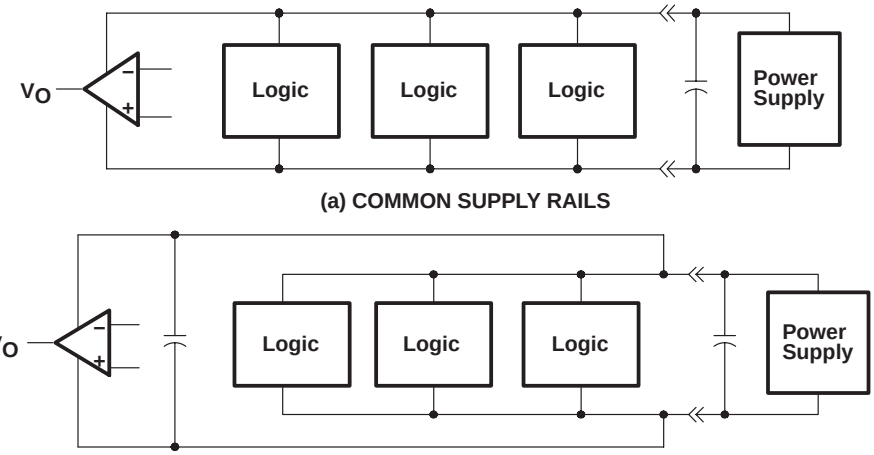


Figure 39. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} −1 V at T_A = 25°C and at V_{DD} −1.5 V at all other temperatures.

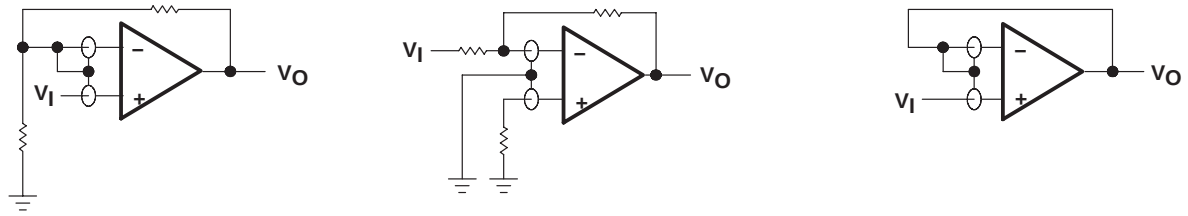
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the *Parameter Measurement Information* section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER **(b) INVERTING AMPLIFIER** **(c) UNITY-GAIN AMPLIFIER**

Figure 40. Guard-Ring Schemes

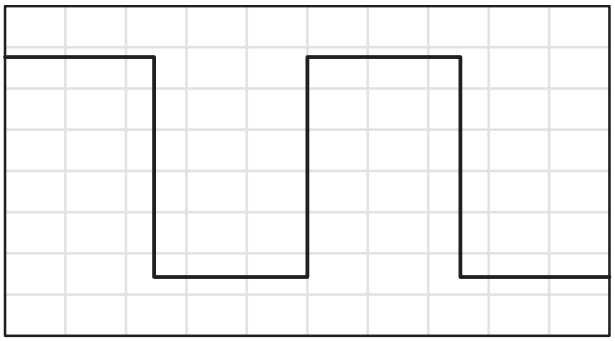
output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

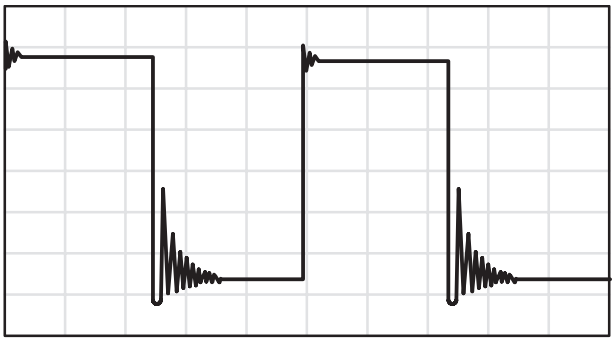
All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

APPLICATION INFORMATION

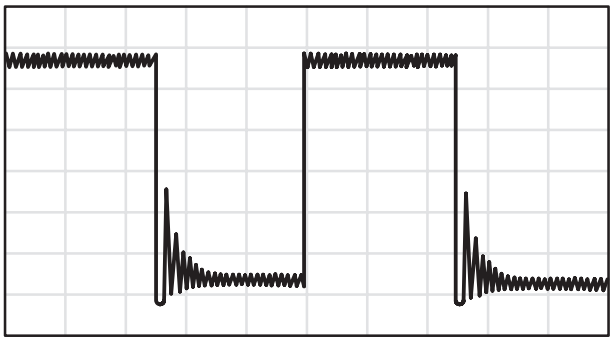
output characteristics (continued)



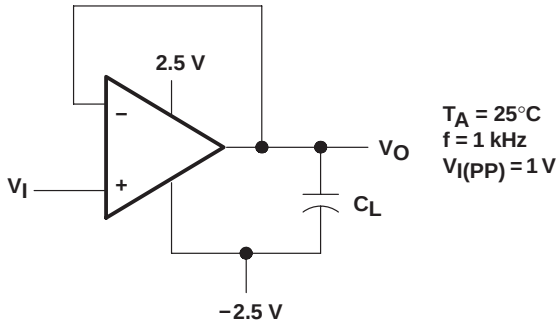
(a) C_L = 20 pF, R_L = NO LOAD



(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD



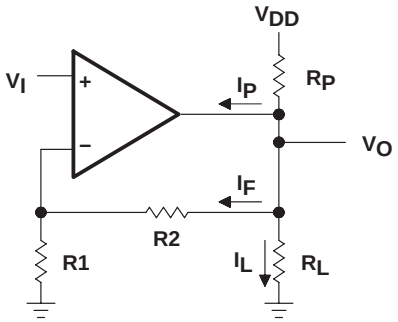
(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 μA)

Figure 42. Resistive Pullup to Increase V_{OH}

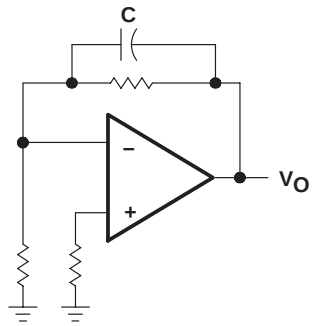


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

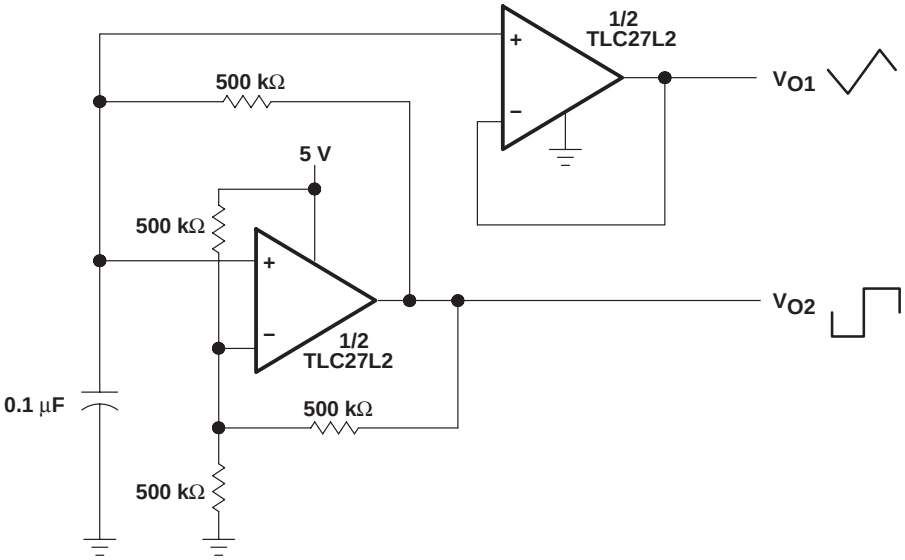
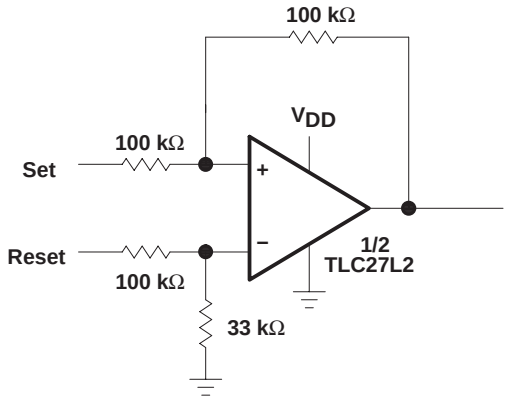


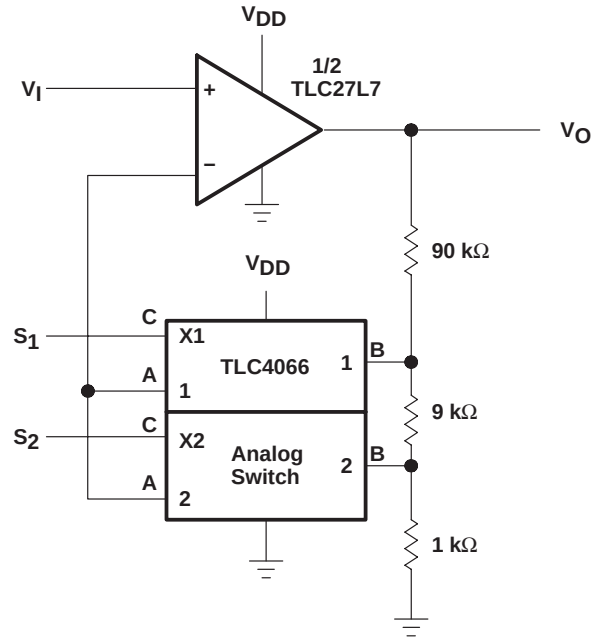
Figure 44. Multivibrator



NOTE: V_{DD} = 5 V to 16 V

Figure 45. Set/Reset Flip-Flop

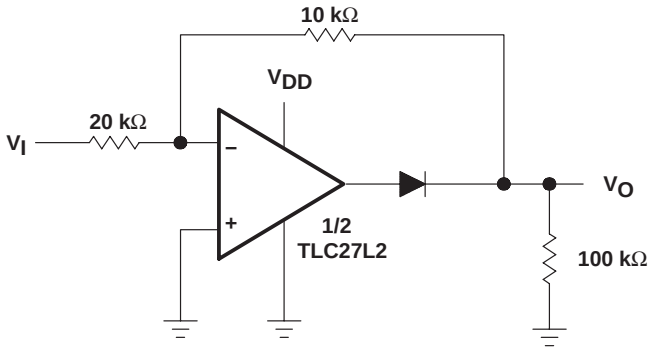
APPLICATION INFORMATION



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

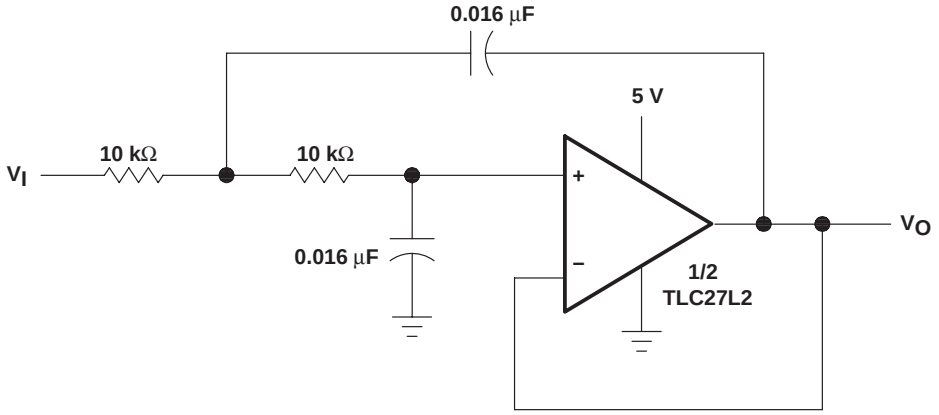
Figure 46. Amplifier With Digital Gain Selection



NOTE: V_{DD} = 5 V to 16 V

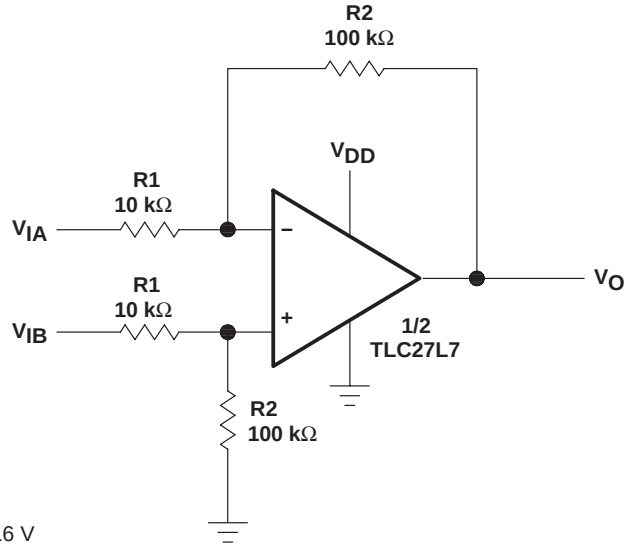
Figure 47. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE: Normalized to f_c = 1 kHz and R_L = 10 kΩ

Figure 48. Two-Pole Low-Pass Butterworth Filter



NOTE: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}\left(V_{IB} - V_{IA}\right)$$

Figure 49. Difference Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27L2ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2AC	Samples
TLC27L2ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2AC	Samples
TLC27L2ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2AC	Samples
TLC27L2ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L2AC	Samples
TLC27L2ACPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2A	Samples
TLC27L2AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2AI	Samples
TLC27L2AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2AI	Samples
TLC27L2AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2AI	Samples
TLC27L2AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L2AI	Samples
TLC27L2BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2BC	Samples
TLC27L2BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2BC	Samples
TLC27L2BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2BC	Samples
TLC27L2BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L2BC	Samples
TLC27L2BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2BI	Samples
TLC27L2BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2BI	Samples
TLC27L2BIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2BI	Samples
TLC27L2BIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L2BI	Samples
TLC27L2CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2C	Samples
TLC27L2CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2C	Samples
TLC27L2CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27L2CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L2CP	Samples
TLC27L2CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L2CP	Samples
TLC27L2CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2	Samples
TLC27L2CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2	Samples
TLC27L2CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2	Samples
TLC27L2ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2I	Samples
TLC27L2IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2I	Samples
TLC27L2IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2I	Samples
TLC27L2IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2I	Samples
TLC27L2IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L2IP	Samples
TLC27L2IPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y27L2	Samples
TLC27L2IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y27L2I	Samples
TLC27L2MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27L2M	Samples
TLC27L2MDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		27L2M	Samples
TLC27L2MDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27L2M	Samples
TLC27L7CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L7C	Samples
TLC27L7CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L7C	Samples
TLC27L7CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L7CP	Samples
TLC27L7CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L7	Samples
TLC27L7CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L7	Samples
TLC27L7ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L7I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27L7IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L7I	Samples
TLC27L7IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L7I	Samples
TLC27L7IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L7I	Samples
TLC27L7IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L7IP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC27L2, TLC27L2M :

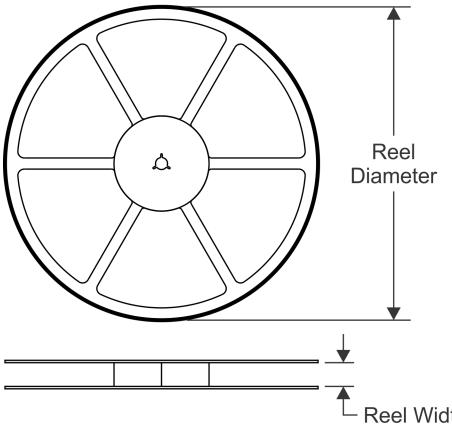
- Catalog : TLC27L2
- Military : TLC27L2M

NOTE: Qualified Version Definitions:

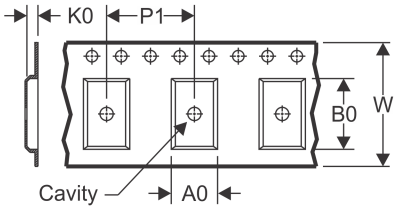
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

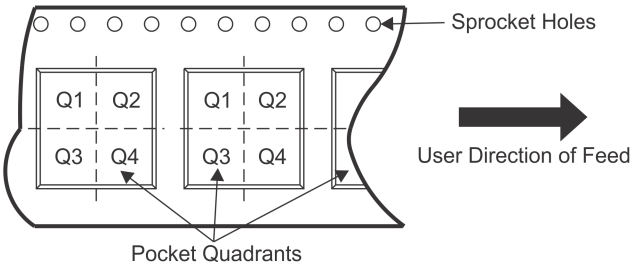


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

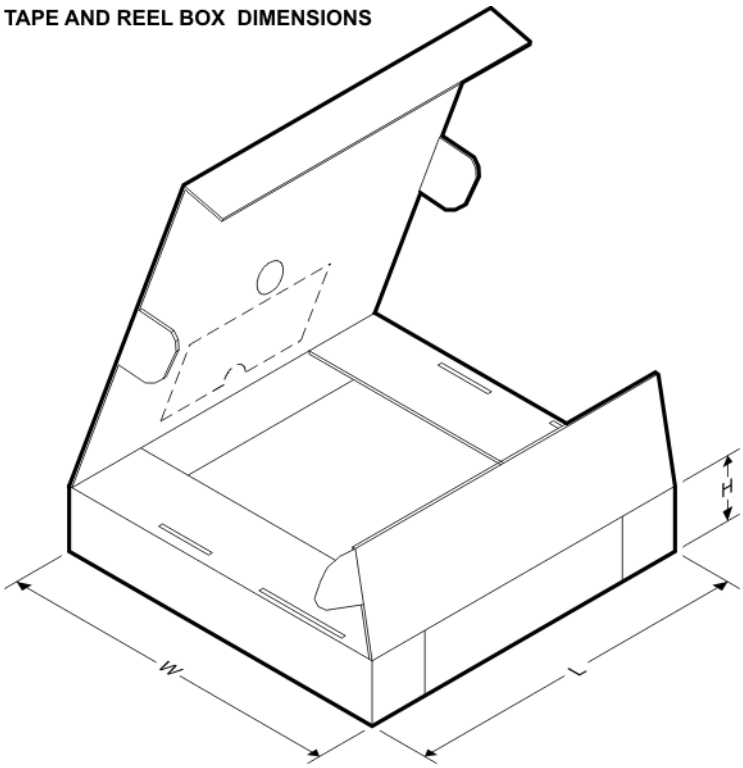
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27L2ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TLC27L2CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC27L2IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC27L2MDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L7CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L7CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TLC27L7IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

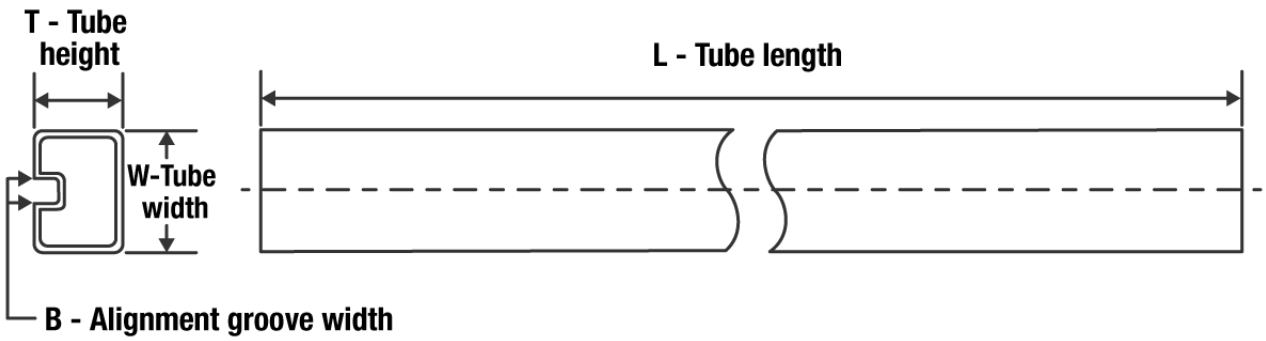
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27L2ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L2AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L2BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L2BIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L2CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L2CPSR	SO	PS	8	2000	853.0	449.0	35.0
TLC27L2CPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLC27L2IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L2IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLC27L2MDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TLC27L7CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC27L7CPSR	SO	PS	8	2000	853.0	449.0	35.0
TLC27L7IDR	SOIC	D	8	2500	340.5	336.1	25.0

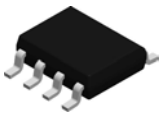
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27L2ACD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2ACD	D	SOIC	8	75	507	8	3940	4.32
TLC27L2ACDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2ACDG4	D	SOIC	8	75	507	8	3940	4.32
TLC27L2ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2ACPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2AID	D	SOIC	8	75	507	8	3940	4.32
TLC27L2AID	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2BCD	D	SOIC	8	75	507	8	3940	4.32
TLC27L2BCD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2BCP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2BID	D	SOIC	8	75	507	8	3940	4.32
TLC27L2BID	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2BIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2CD	D	SOIC	8	75	507	8	3940	4.32
TLC27L2CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2CDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2CDG4	D	SOIC	8	75	507	8	3940	4.32
TLC27L2CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2ID	D	SOIC	8	75	507	8	3940	4.32
TLC27L2IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2IDG4	D	SOIC	8	75	507	8	3940	4.32
TLC27L2IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2IPW	PW	TSSOP	8	150	530	10.2	3600	3.5

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27L2MD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L2MDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L7CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L7CD	D	SOIC	8	75	507	8	3940	4.32
TLC27L7CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L7CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L7ID	D	SOIC	8	75	507	8	3940	4.32
TLC27L7ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L7IDG4	D	SOIC	8	75	507	8	3940	4.32
TLC27L7IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L7IP	P	PDIP	8	50	506	13.97	11230	4.32

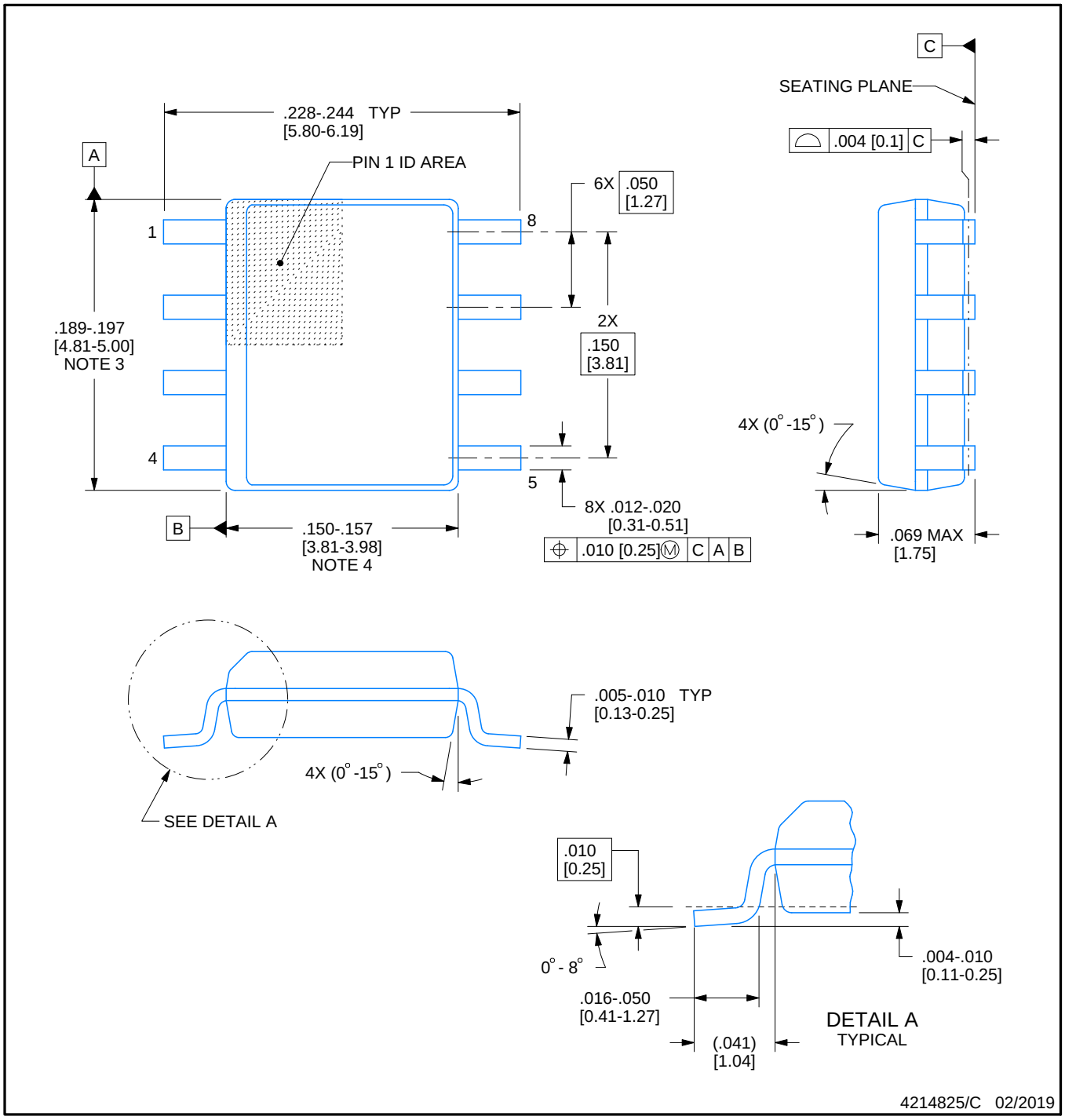


PACKAGE OUTLINE

D0008A

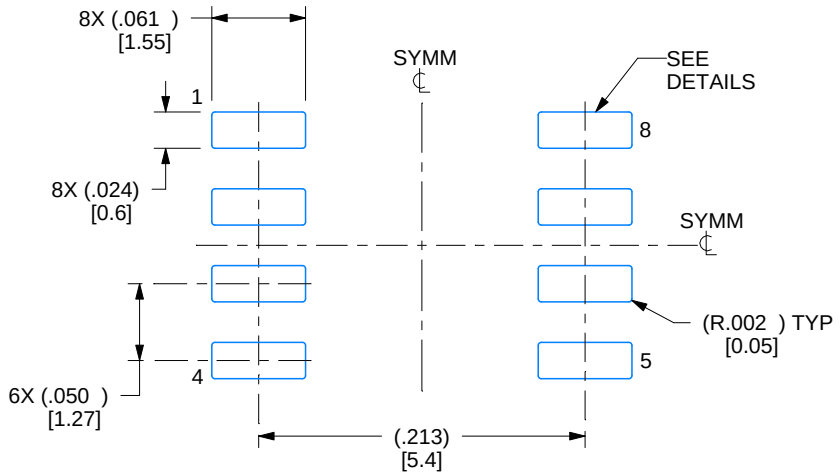
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

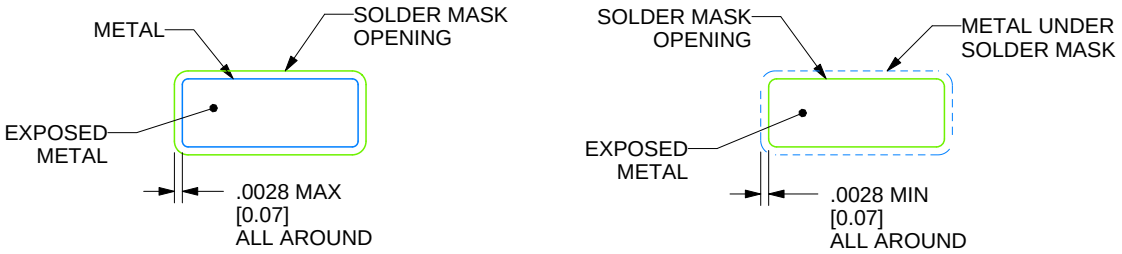


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

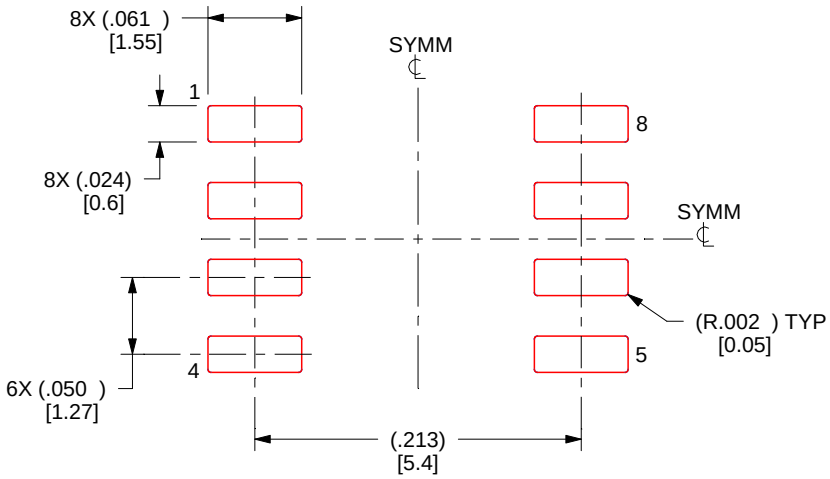


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

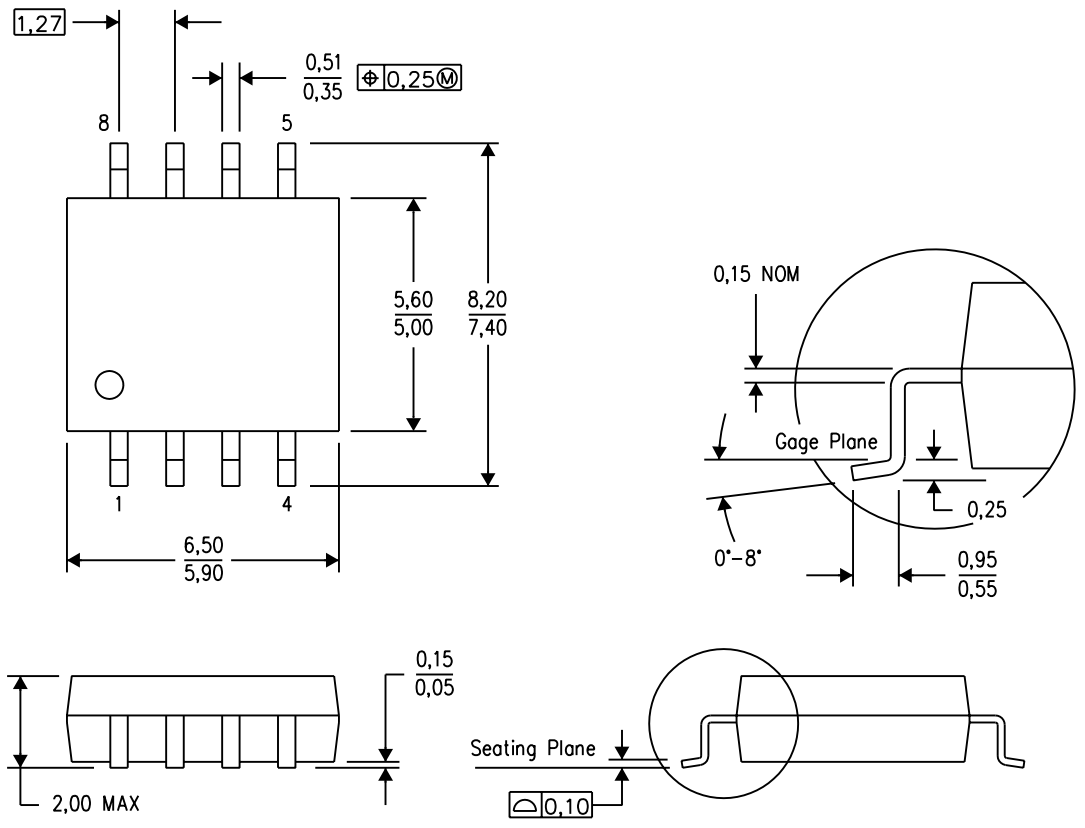
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

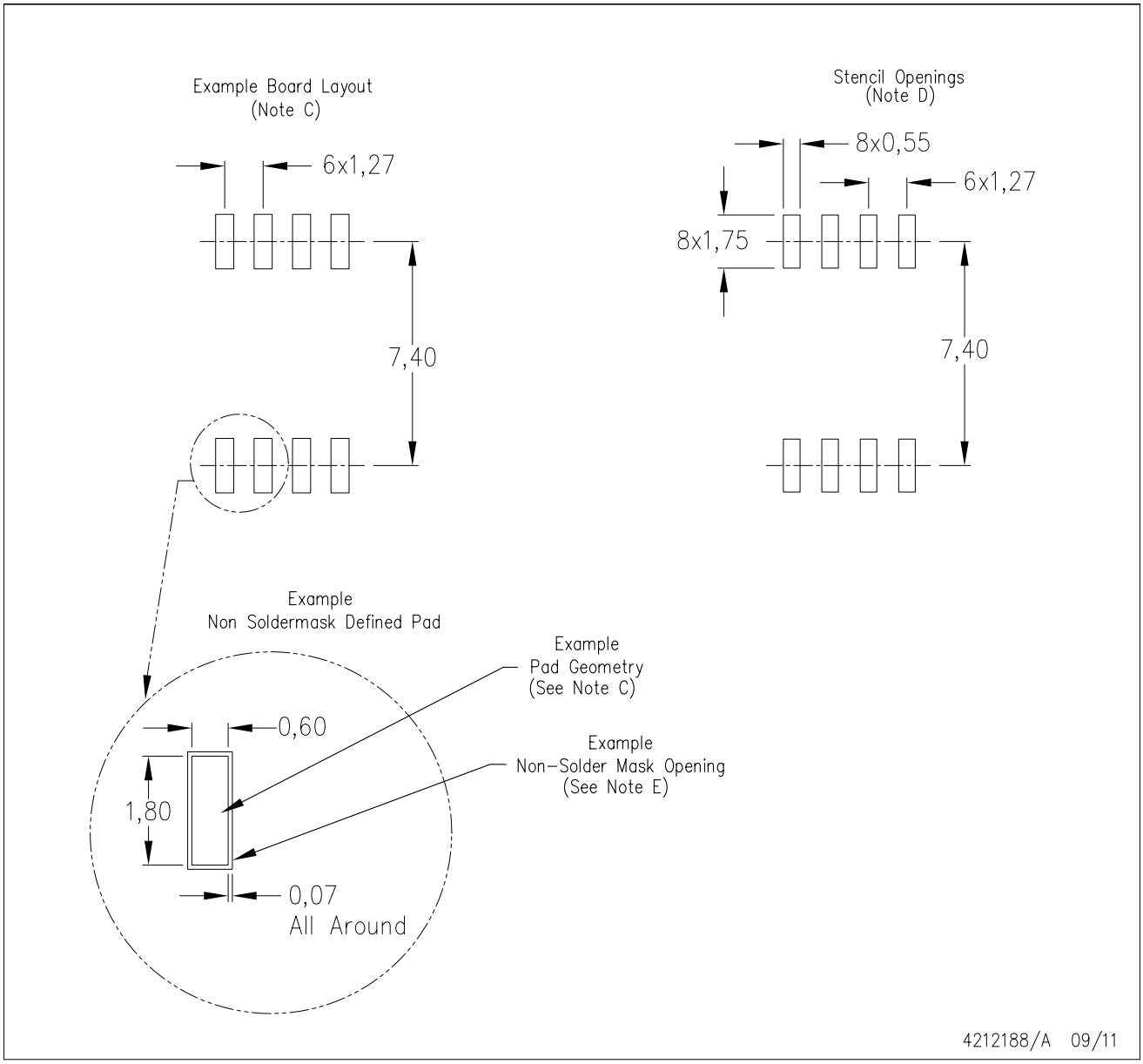
MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



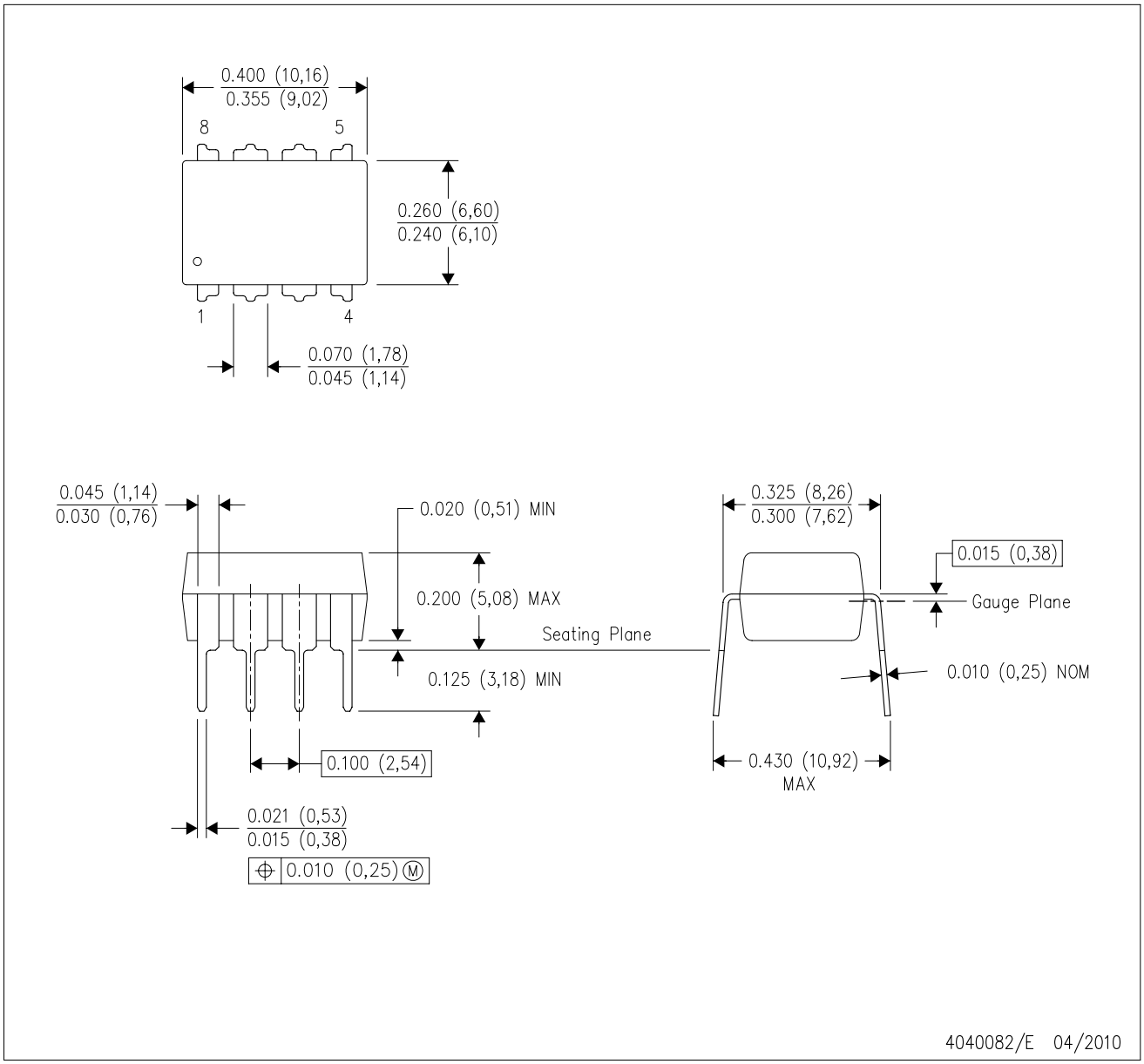
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE

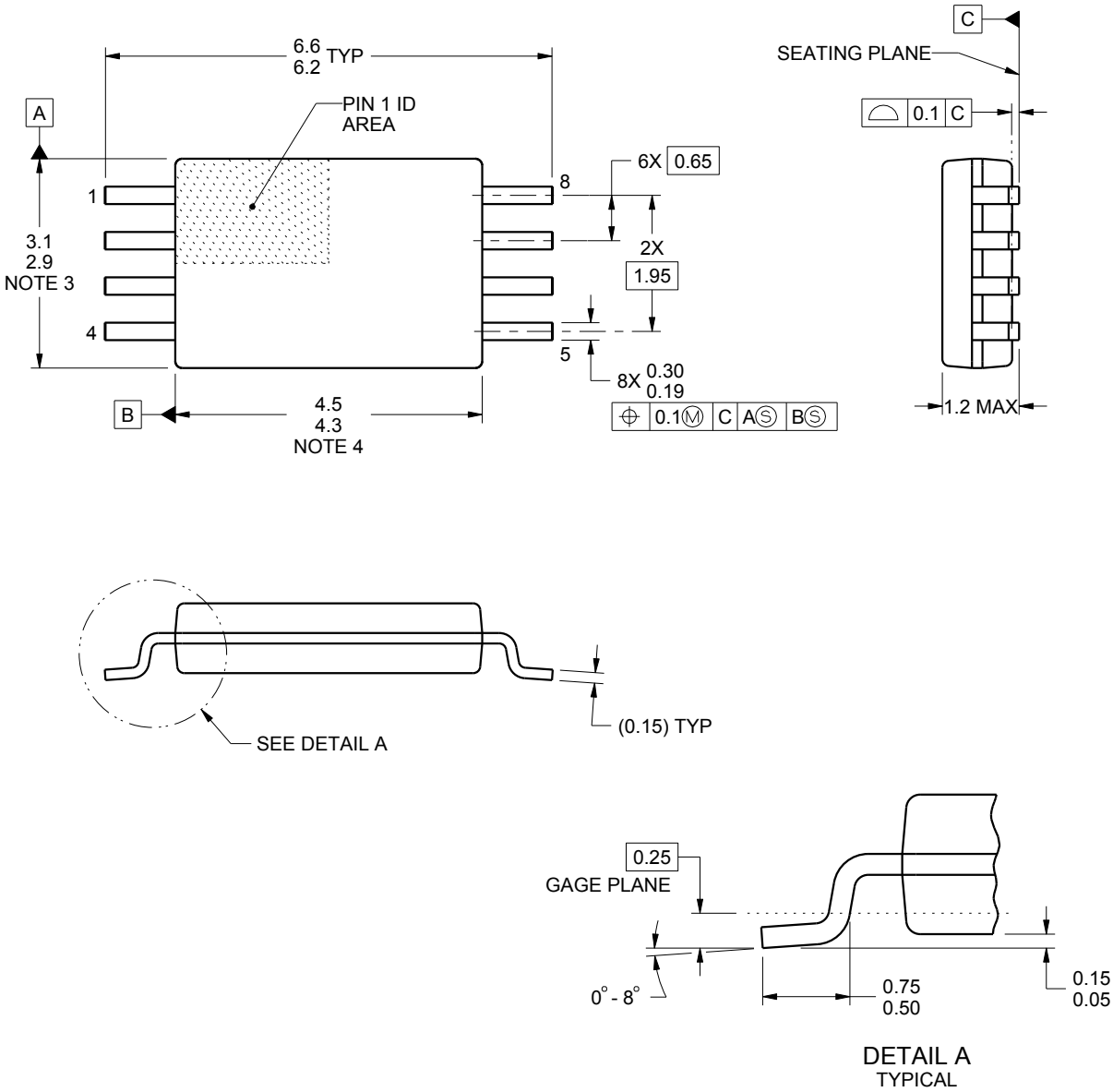


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

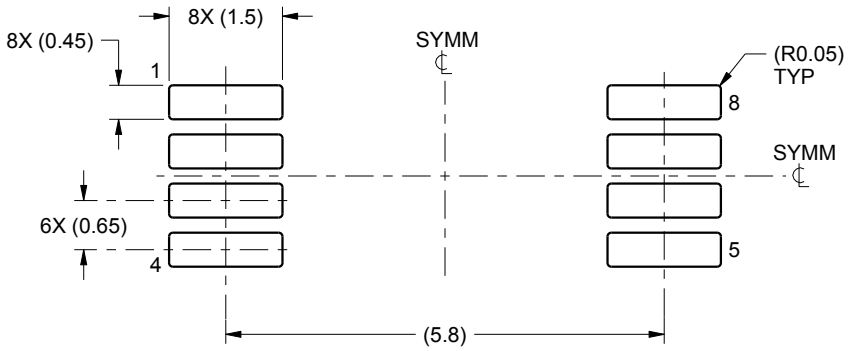


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

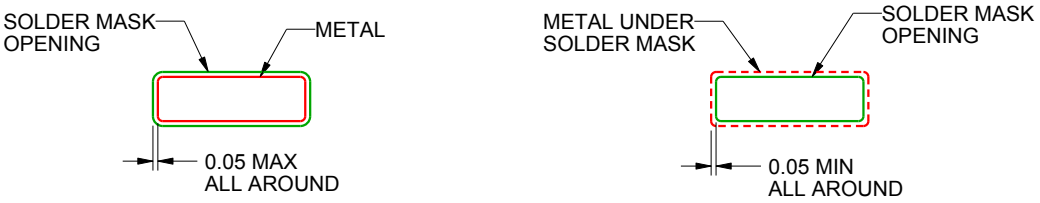


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

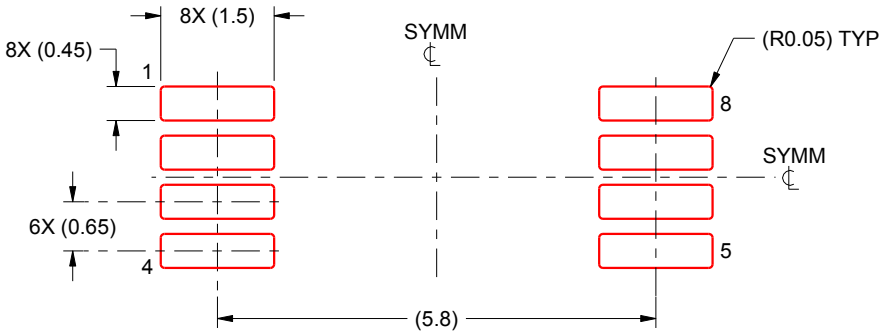
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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