- **8-Bit Resolution**
- **2.7-V to 3.6-V V_{CC}**
- **Easy Microprocessor Interface or Stand-Alone Operation**
- **Operates Ratiometrically or With V_{CC} Reference**
- **4- or 8-Channel Multiplexer Options With Address Logic**
- **Input Range 0 V to V_{CC} With V_{CC} Reference**
- **Remote Operation With Serial Data Link**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μs at $f_{(CLK)}$ = 250 kHz**
- **Functionally Equivalent to the ADC0834 and ADC0838 at 3-V Supply Without the Internal Zener Regulator Network**
- **Total Unadjusted Error . . . ±1 LSB**

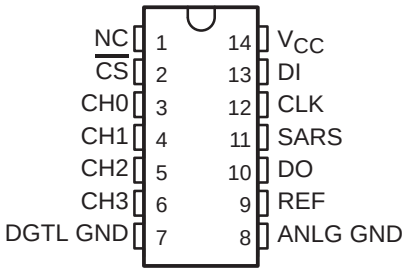
description

These devices are 8-bit successive-approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

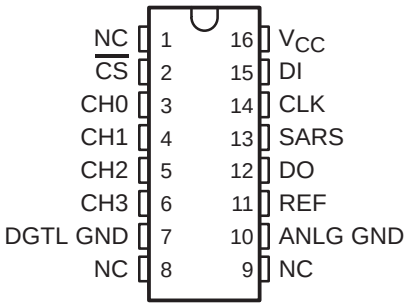
The TLV0834 (4-channel) and TLV0838 (8-channel) multiplexer is software-configured for single-ended or differential inputs as well as pseudodifferential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding of any smaller analog voltage span to the full 8 bits of resolution.

The TLV0834C and TLV0838C are characterized for operation from 0°C to 70°C. The TLV0834I and TLV0838I are characterized for operation from –40°C to 85°C.

TLV0834 . . . D OR N PACKAGE
(TOP VIEW)

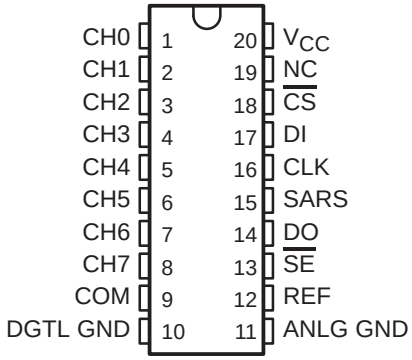


TLV0834 . . . PW PACKAGE
(TOP VIEW)



NC – No internal connection

TLV0838 . . . PW, DW, OR N PACKAGE
(TOP VIEW)

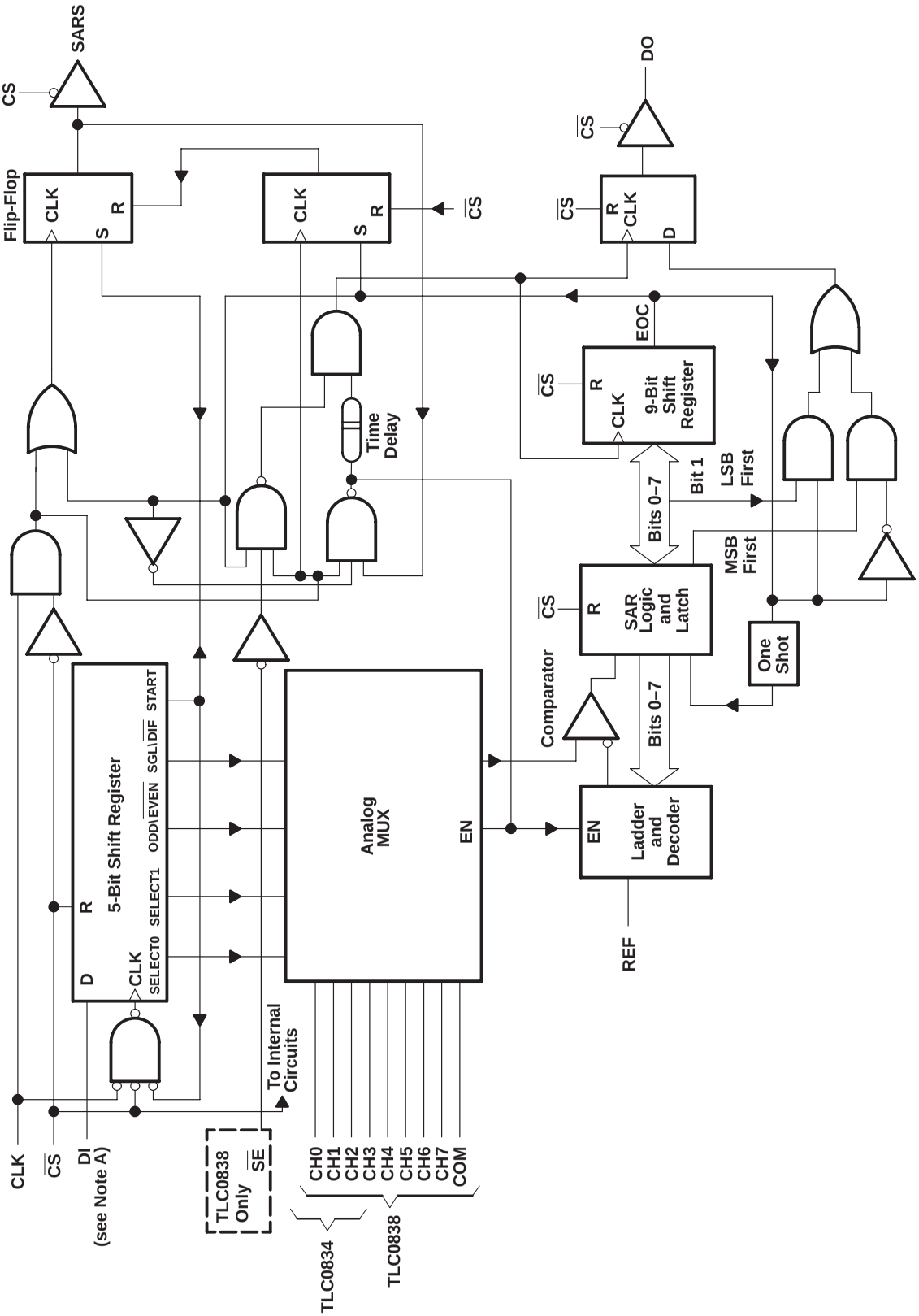


AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE (D)	SMALL OUTLINE (DW)	PLASTIC DIP (N)		TSSOP (PW)	
0°C to 70°C	TLV0834CD	TLV0838CDW	TLV0834CN	TLV0838CN	TLV0834CPW	TLV0838CPW
–40°C to 85°C	TLV0834ID	TLV0838IDW	TLV0834IN	TLV0838IN	TLV0834IPW	TLV0838IPW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



NOTE A: For the TLC0834, DI is input directly to the D input of SELECT1; SELECT0 is forced to a high.

functional description

The TLV0834 and TLV0838 use a sample-data-comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of $\overline{SE}$, an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single ended), to an adjacent input (differential), or to a common terminal (pseudo differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (–) polarity. When the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial-data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer-addressing sequence. The multiplexer address shifts into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs . For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the TLV0838 can be used for a pseudodifferential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

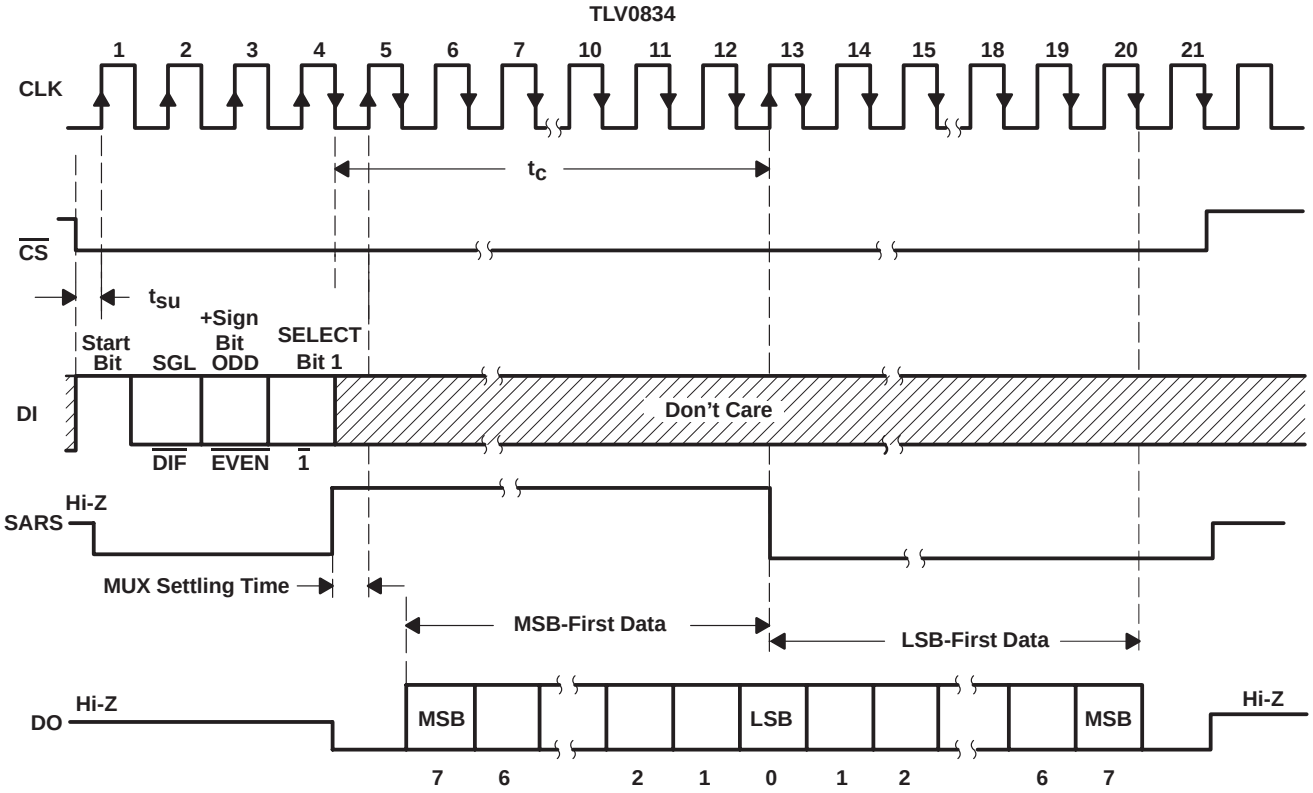
A conversion is initiated by setting $\overline{CS}$ low, which enables all logic circuits. $\overline{CS}$ must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer-address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR status output (SARS) goes high to indicate that a conversion is in progress, and DI to the multiplexer shift register is disabled for the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. DO comes out of the high-impedance state and provides a leading low for one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive-ladder output. As the conversion proceeds, conversion data is simultaneously output from DO, with the most significant bit (MSB) first. After eight clock periods, the conversion is complete and SARS goes low.

The TLV0834 outputs the least-significant-bit (LSB) first data after the MSB-first data stream. When $\overline{SE}$ is held high on the TLV0838, the value of the LSB remains on the data line. When $\overline{SE}$ is forced low, the data is then clocked out as LSB-first data. (To output LSB first, $\overline{SE}$ must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When $\overline{CS}$ goes high, all internal registers are cleared. At this time, the output circuits go to the high-impedance state. If another conversion is desired, $\overline{CS}$ must make a high-to-low transition followed by address information.

DI and DO can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer-addressing interval and DO is still in the high-impedance state.

sequence of operation



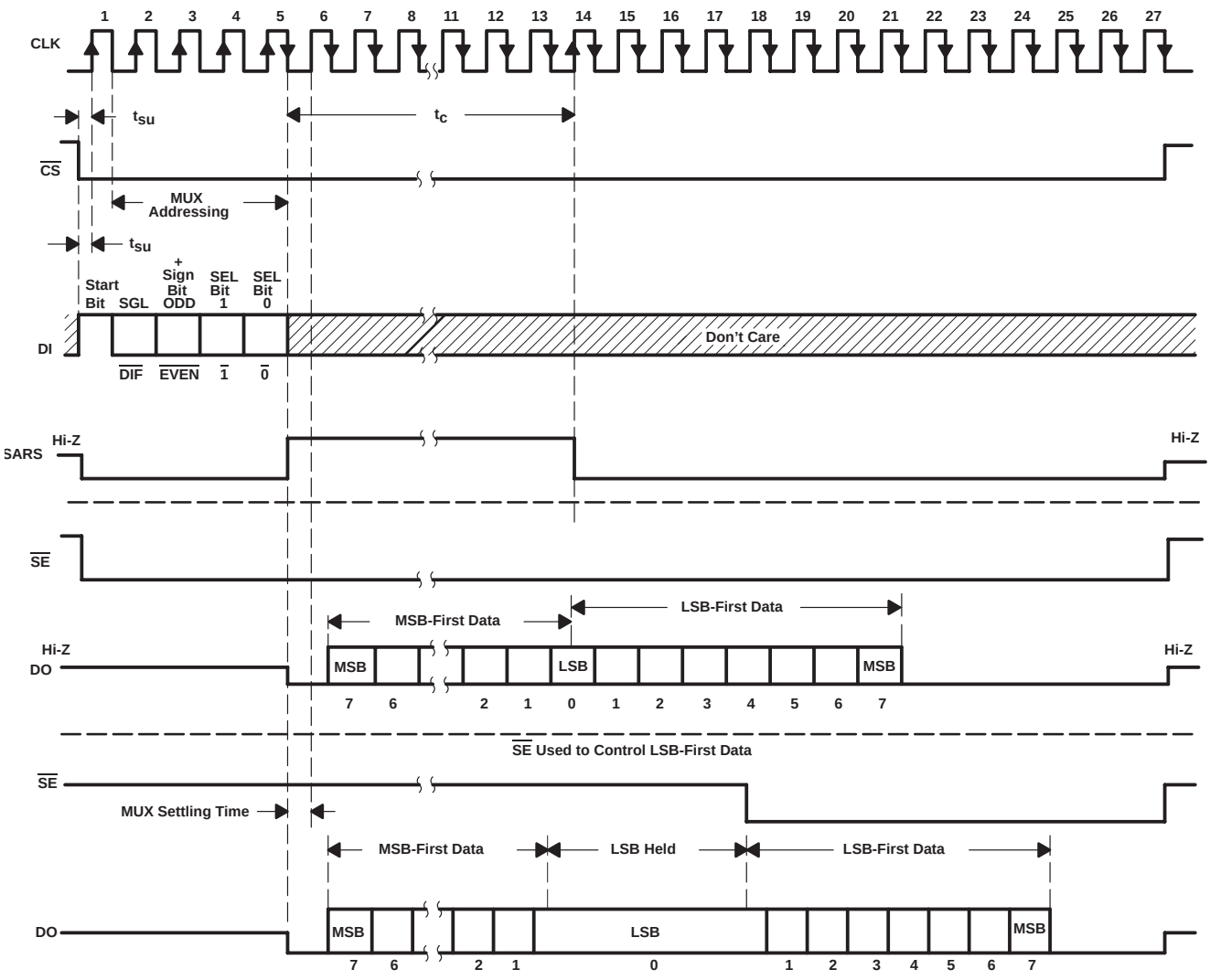
TLV0834 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/$\overline{\text{DIF}}$	ODD/$\overline{\text{EVEN}}$	SELECT BIT 1	CH0	CH1	CH2	CH3
L	L	L	+	–		
L	L	H			+	–
L	H	L	–	+		
L	H	H			–	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, – or + = terminal polarity for the selected input channel

sequence of operation (continued)

TLV0838



TLV0838 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/$\overline{\text{DIF}}$	ODD/$\overline{\text{EVEN}}$	SELECT		0		1		2		3		
		1	0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
L	L	L	L	+	–							
L	L	L	H			+	–					
L	L	H	L					+	–			
L	L	H	H							+	–	
L	H	L	L	–	+							
L	H	L	H			–	+					
L	H	H	L					–	+			
L	H	H	H							–	+	
H	L	L	L	+								–
H	L	L	H			+						–
H	L	H	L					+				–
H	L	H	H							+		–
H	H	L	L		+							–
H	H	L	H				+					–
H	H	H	L						+			–
H	H	H	H								+	–

H = high level, L = low level, – or + = polarity of external input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: Logic . . . . . –0.3 V to V_{CC} + 0.3 V
Analog . . . . . –0.3 V to V_{CC}+ 0.3 V
Input current, I_I . . . . . ±5 mA
Total input current . . . . . ±20 mA
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see clock frequency operating conditions)		2.7	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Clock frequency, $f_{(CLK)}$	V_{CC} = 2.7 V	10		250	kHz
Clock frequency, $f_{(CLK)}$	V_{CC} = 3.3 V	10		600	kHz
Clock duty cycle (see Note 2)		40%		60%	
Pulse duration, $\overline{CS}$ high, t_w		220			ns
Setup time, $\overline{CS}$ low, $\overline{SE}$ low, or data valid before CLK↑, t_{su}		350			ns
Hold time, data valid after CLK↑, t_h		90			ns
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. When a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 µs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 3.3 V, $f_{(CLK)}$ = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†	C SUFFIX			I SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 3 V, I_{OH} = –360 µA	2.8			2.4			V
		V_{CC} = 3 V, I_{OH} = –10 µA	2.9			2.8			
V_{OL}	Low-level output voltage	V_{CC} = 3 V, I_{OL} = 1.6 mA			0.34			0.4	V
I_{IH}	High-level input current	V_{IH} = 3.6 V		0.005	1		0.005	1	µA
I_{IL}	Low-level input current	V_{IL} = 0		–0.005	–1		–0.005	–1	µA
I_{OH}	High-level output (source) current	At V_{OH}, DO = 0 V, T_A = 25°C	–6.5	–15		–6.5	–15		mA
I_{OL}	Low-level output (sink) current	A t V_{OL}, DO = V_{CC}, T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO or SARS)	V_O = 3.3 V, T_A = 25°C		0.01	3		0.01	3	µA
		V_O = 0, T_A = 25°C		–0.01	–3		–0.01	–3	
C_i	Input capacitance						5		pF
C_o	Output capacitance						5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 3.3 V, $f_{(CLK)}$ = 250 kHz (unless otherwise noted) (continued)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IC}	Common-mode input voltage		See Note 3	−0.05 to V_{CC} + 0.05			V
$I_{I(stdby)}$	Standby input current (see Note 4)	On channel	V_I = 3.3 V			1	µA
		Off channel	V_I = 0			−1	
		On channel	V_I = 0			−1	
		Off channel	V_I = 3.3 V			1	
$r_{i(REF)}$	Input resistance to REF			1.3	2.4	5.9	kΩ

total device

PARAMETER		MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current		0.2	0.75	mA

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 3. When channel IN– is more positive than channel IN+, the digital output code is 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (3 V) because high-level analog input voltage (3.6 V) can, especially at high temperatures, cause the input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code is correct. To achieve an absolute 0- to 3.3-V input range requires a minimum V_{CC} of 3.25 V for all variations of temperature and load.

4. Standby input currents go in or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics, V_{CC} = 3.3 V, $f_{(CLK)}$ = 250 kHz, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS§	MIN	TYP	MAX	UNIT
	Supply-voltage variation error		V_{CC} = 3 V to 3.6 V		±1/16	±1/4	LSB
	Total unadjusted error (see Note 5)		V_{ref} = 3.3 V, T_A = MIN to MAX			±1	LSB
	Common-mode error		Differential mode		±1/16	±1/4	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 6)	MSB-first data	C_L = 100pF			500	ns
		LSB-first data				200	
t_{dis}	Output disable time, DO or SARS after CS↑		C_L = 10 pF, R_L = 10 kΩ			80	ns
			C_L = 100 pF, R_L = 2 kΩ			250	
t_c	Conversion time (multiplexer-addressing time not included)					8	clock periods

§ All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The MSB-first data is output directly from the comparator and, therefore, requires additional delay to allow for comparator response time.

PARAMETER MEASUREMENT INFORMATION

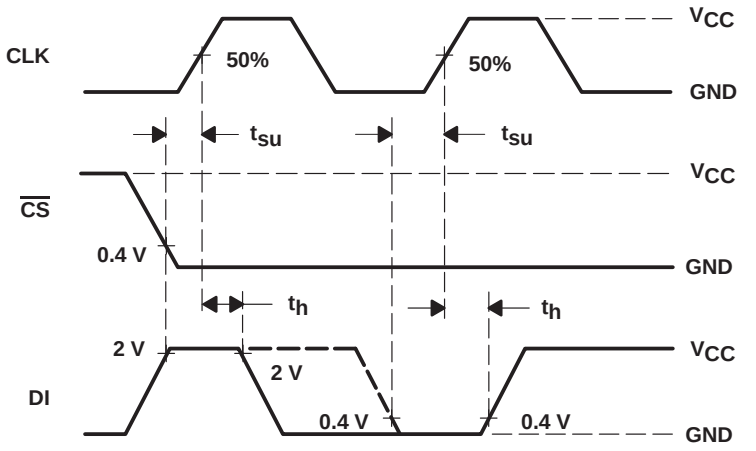


Figure 1. Data-Input Timing

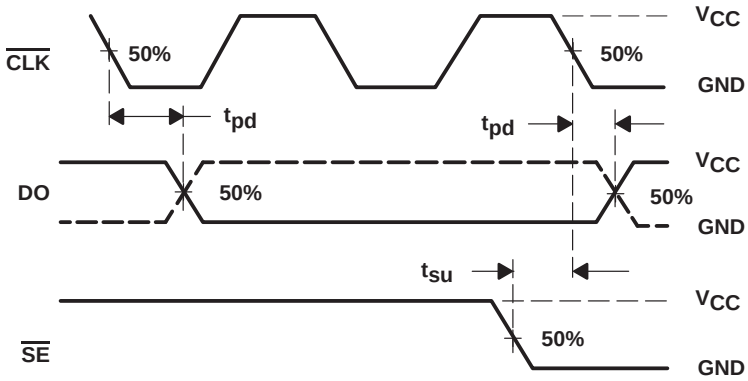
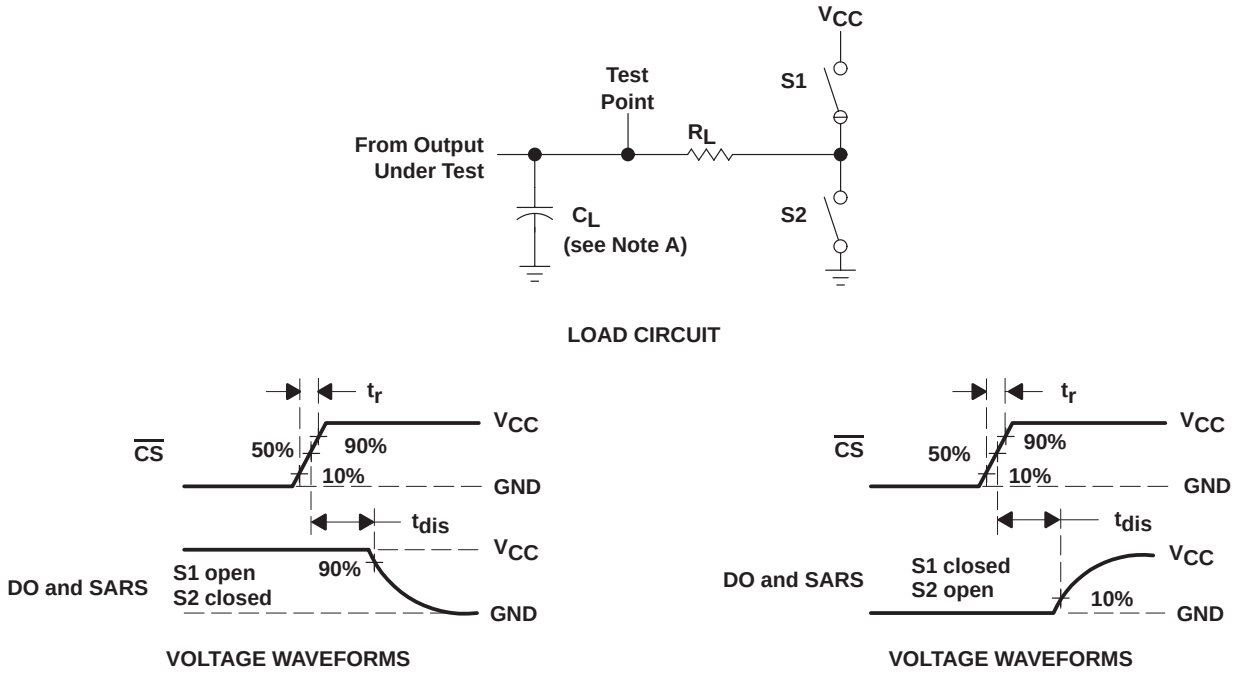


Figure 2. Data-Output Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR vs REFERENCE VOLTAGE

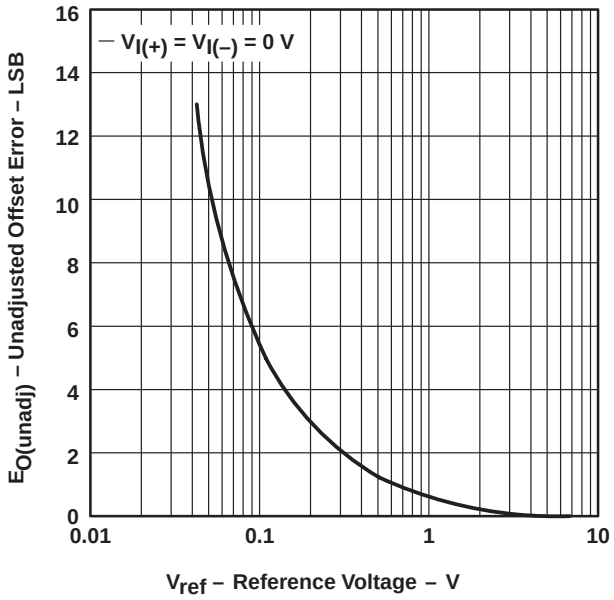


Figure 4

LINEARITY ERROR vs REFERENCE VOLTAGE

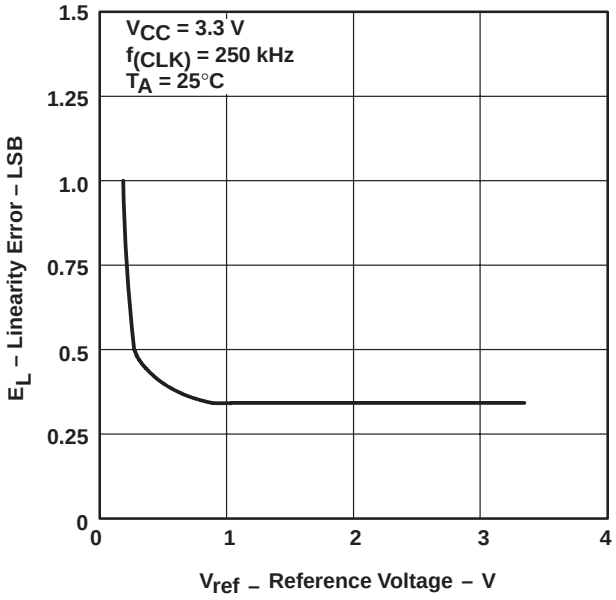


Figure 5

LINEARITY ERROR vs FREE-AIR TEMPERATURE

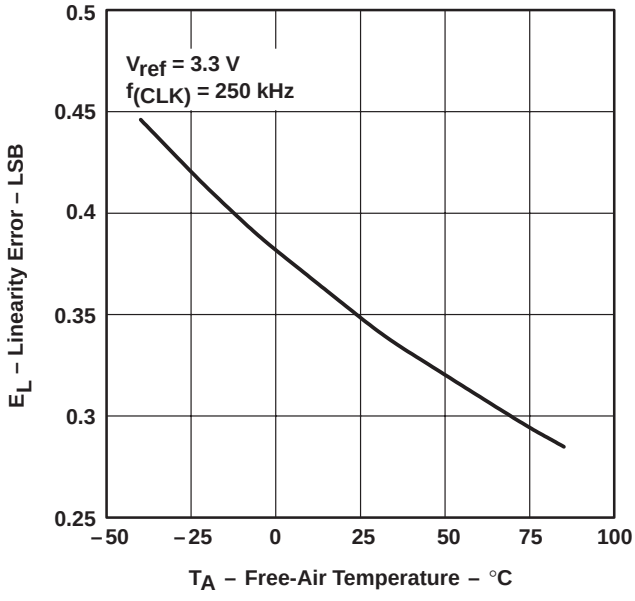


Figure 6

LINEARITY ERROR vs CLOCK FREQUENCY

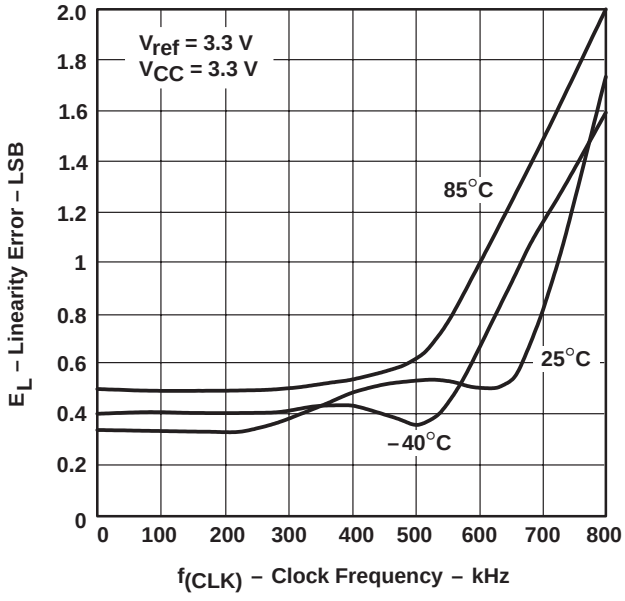


Figure 7

TYPICAL CHARACTERISTICS

TLV0831
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

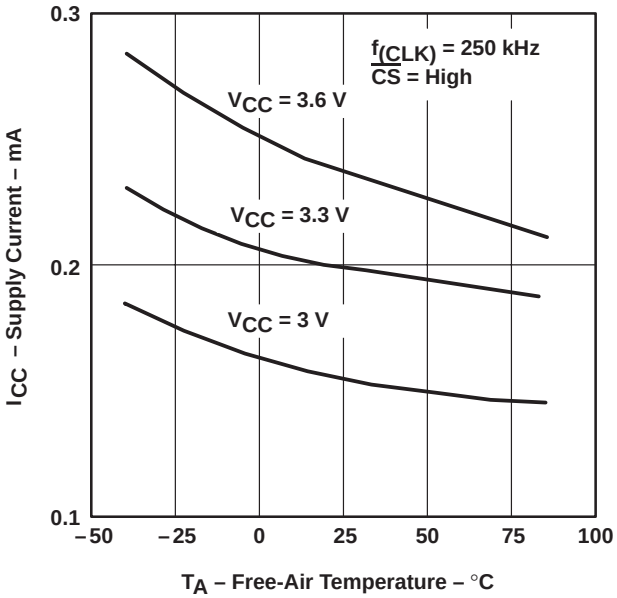


Figure 8

TLV0831
SUPPLY CURRENT
vs
CLOCK FREQUENCY

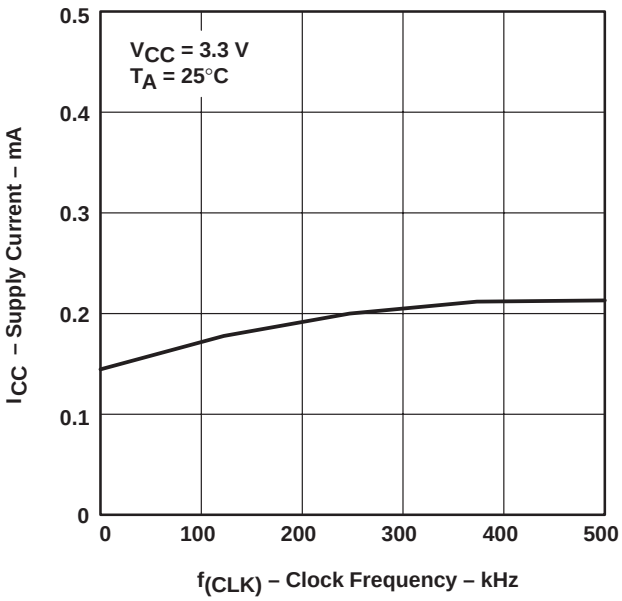


Figure 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

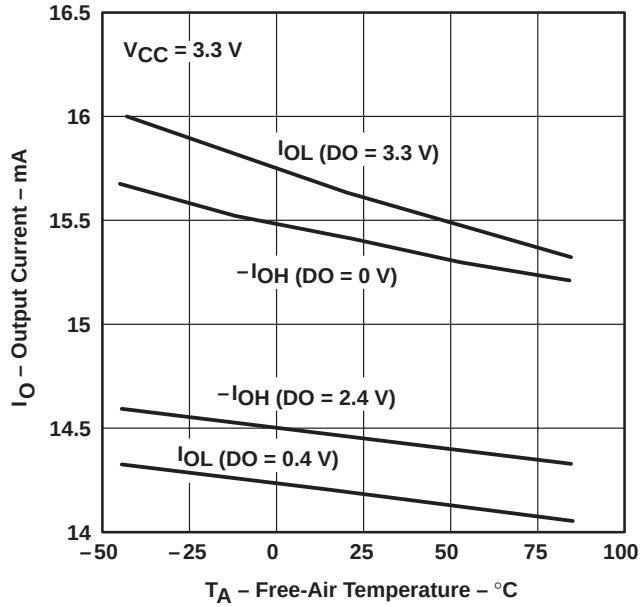


Figure 10

TYPICAL CHARACTERISTICS

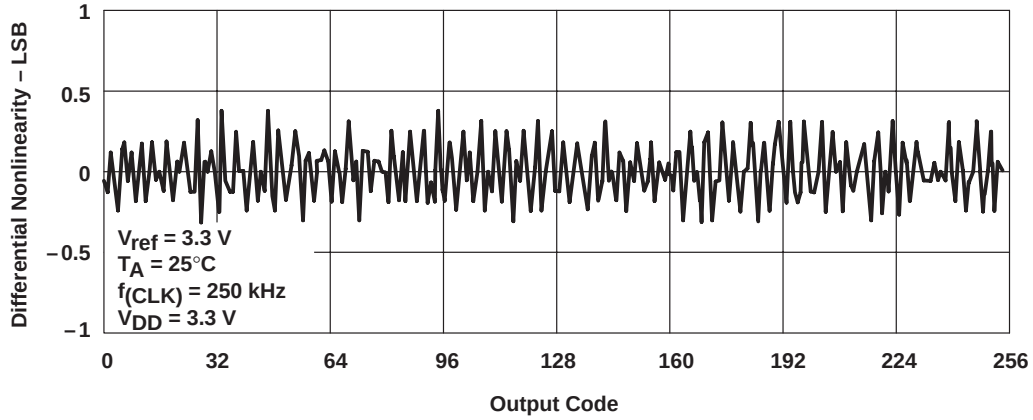


Figure 11. Differential Nonlinearity With Output Code

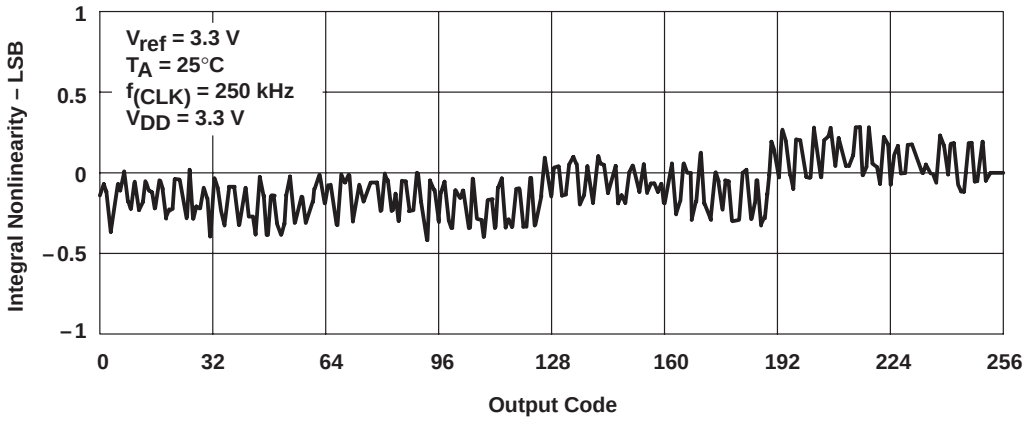


Figure 12. Integral Nonlinearity With Output Code

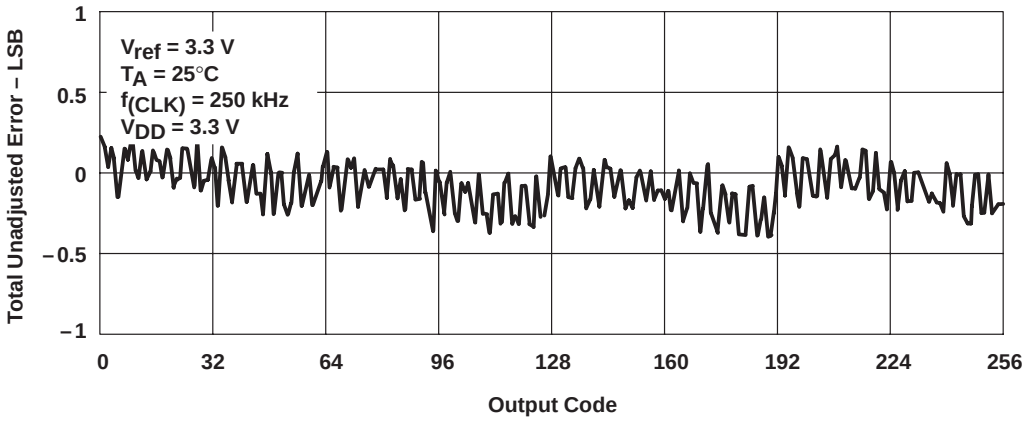


Figure 13. Total Unadjusted Error With Output Code

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV0834CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0834C	Samples
TLV0834CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0834C	Samples
TLV0834CPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV0834	Samples
TLV0834CPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV0834	Samples
TLV0834ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0834I	Samples
TLV0834IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0834I	Samples
TLV0834IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLV0834IN	Samples
TLV0834IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY0834	Samples
TLV0834IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY0834	Samples
TLV0834IPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY0834	Samples
TLV0838CDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0838C	Samples
TLV0838CDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0838C	Samples
TLV0838CDWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0838C	Samples
TLV0838CN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type		TLV0838CN	Samples
TLV0838CPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV0838C	Samples
TLV0838CPWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV0838C	Samples
TLV0838CPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV0838C	Samples
TLV0838IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0838I	Samples
TLV0838IDWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0838I	Samples
TLV0838IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLV0838I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV0838IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV0838I	Samples
TLV0838IPWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV0838I	Samples
TLV0838IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV0838I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

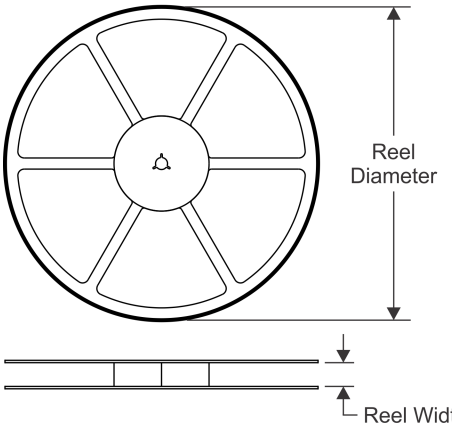
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

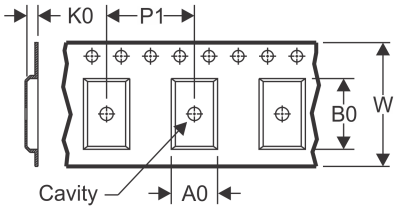
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

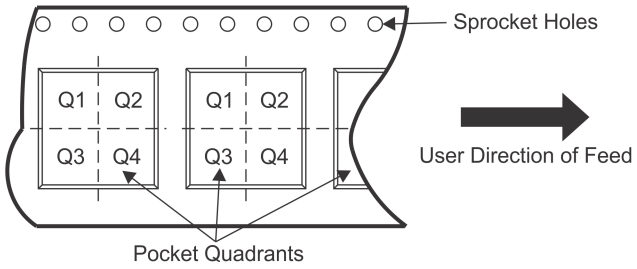


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

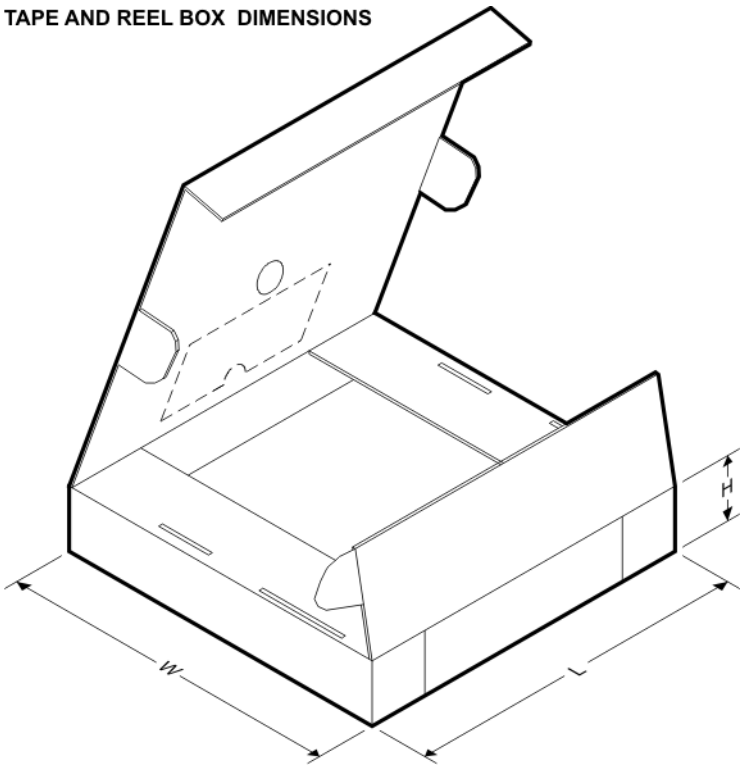
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV0834CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV0834CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV0834IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV0834IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV0838CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV0838CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV0838IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV0838IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

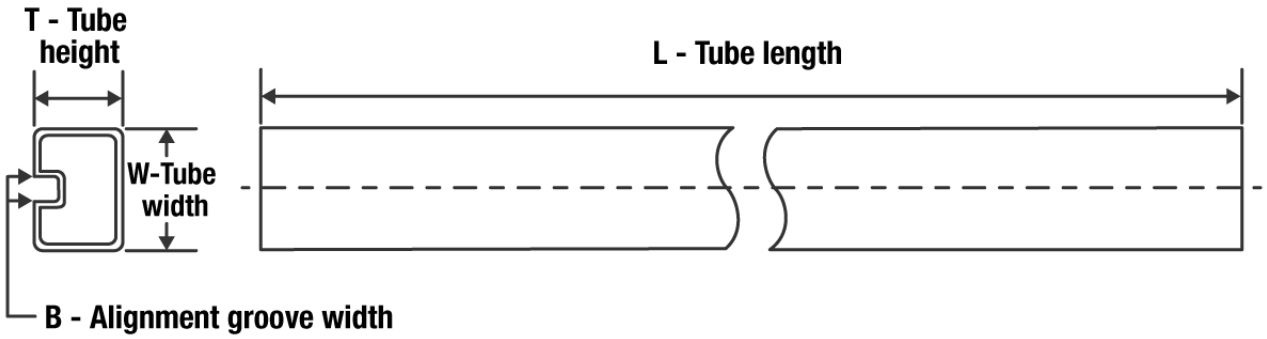
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV0834CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV0834CPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
TLV0834IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV0834IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
TLV0838CDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLV0838CPWR	TSSOP	PW	20	2000	350.0	350.0	43.0
TLV0838IDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLV0838IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0

TUBE



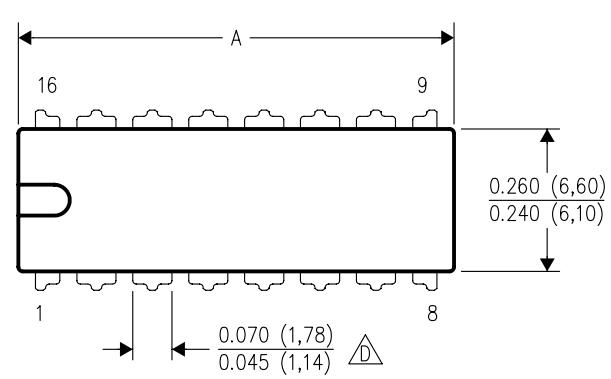
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV0834CD	D	SOIC	14	50	505.46	6.76	3810	4
TLV0834CPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV0834ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV0834IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV0834IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV0838CDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV0838CN	N	PDIP	20	20	506	13.97	11230	4.32
TLV0838CPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV0838CPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV0838IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV0838IDWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV0838IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV0838IPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

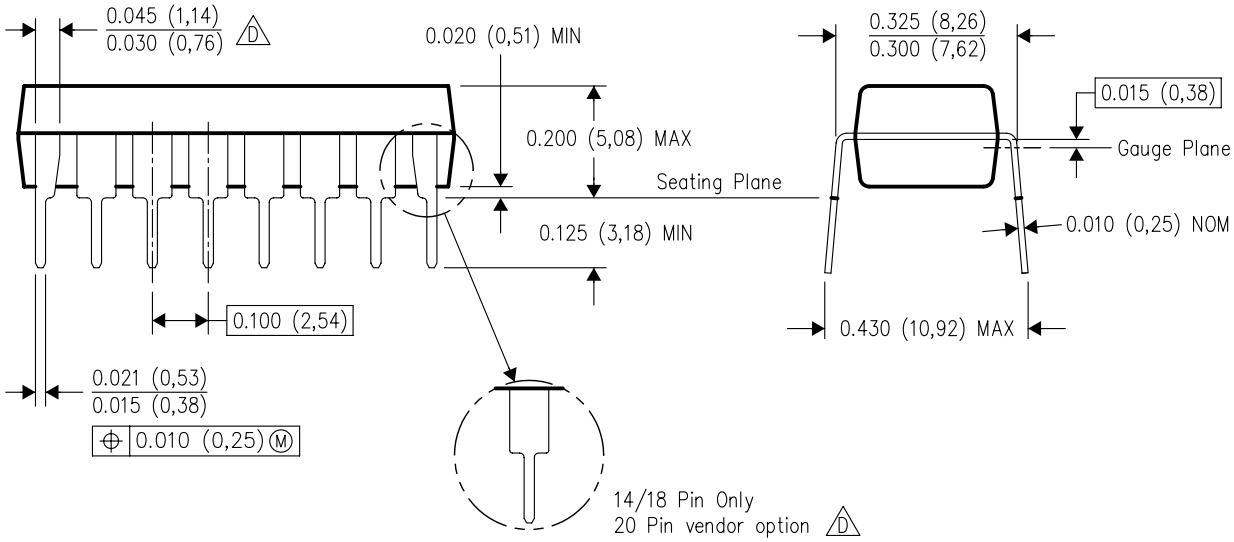
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

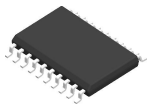


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

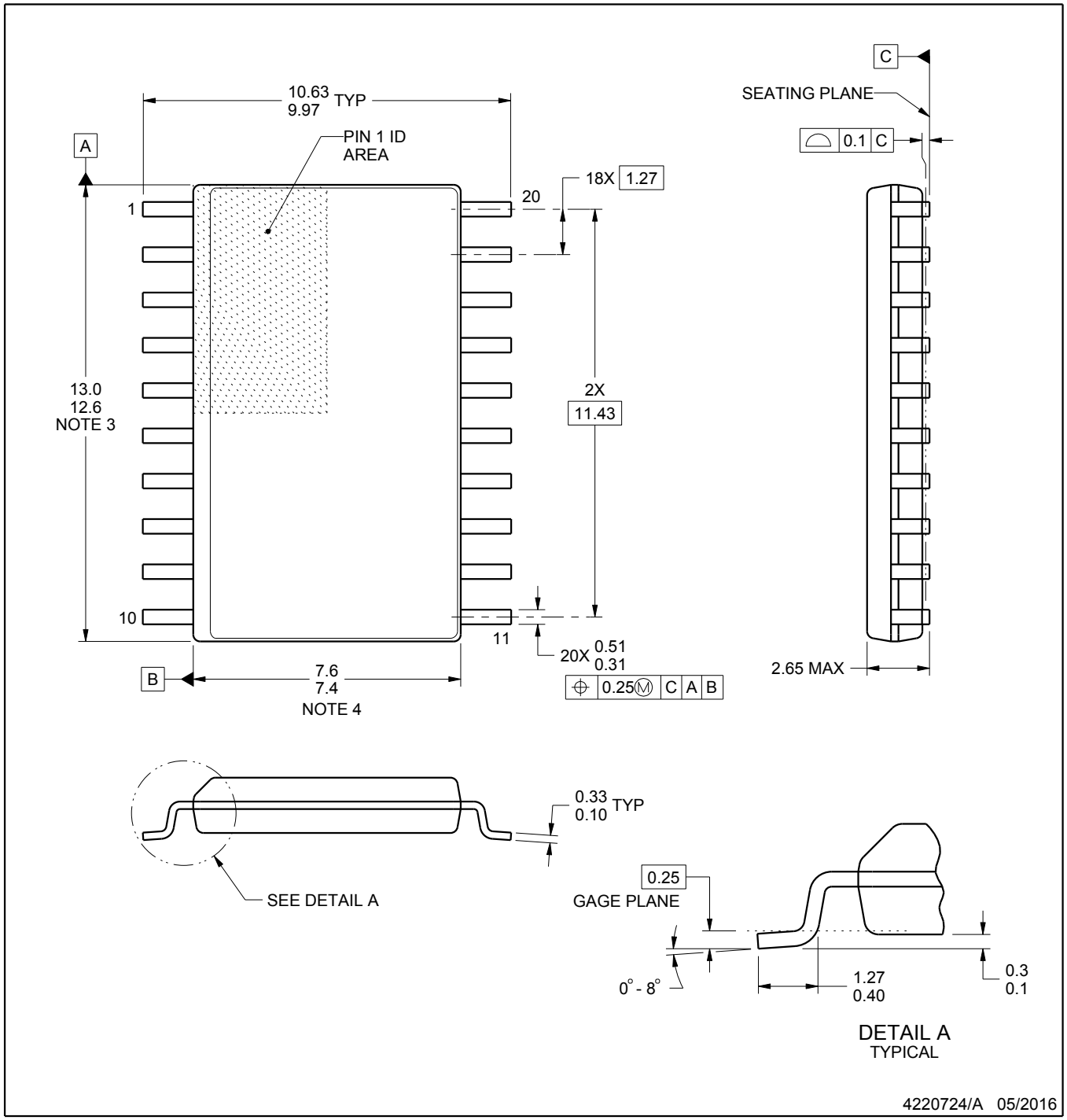


PACKAGE OUTLINE

DW0020A

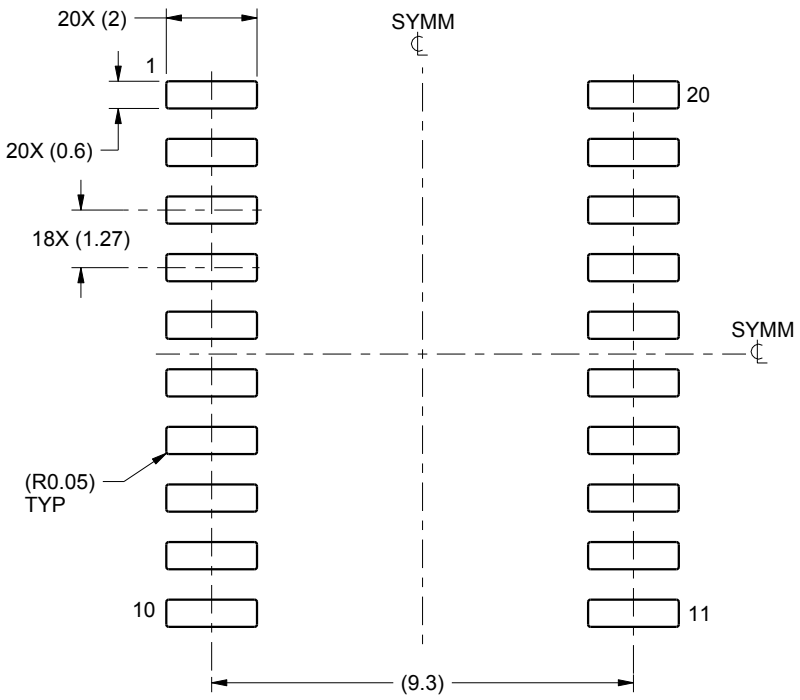
SOIC - 2.65 mm max height

SOIC

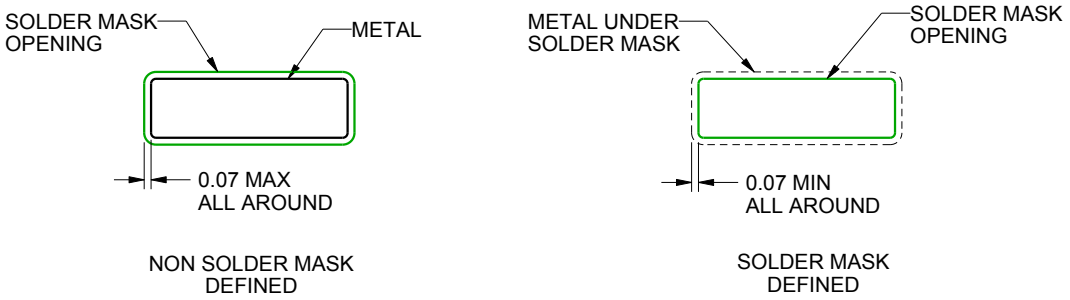


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

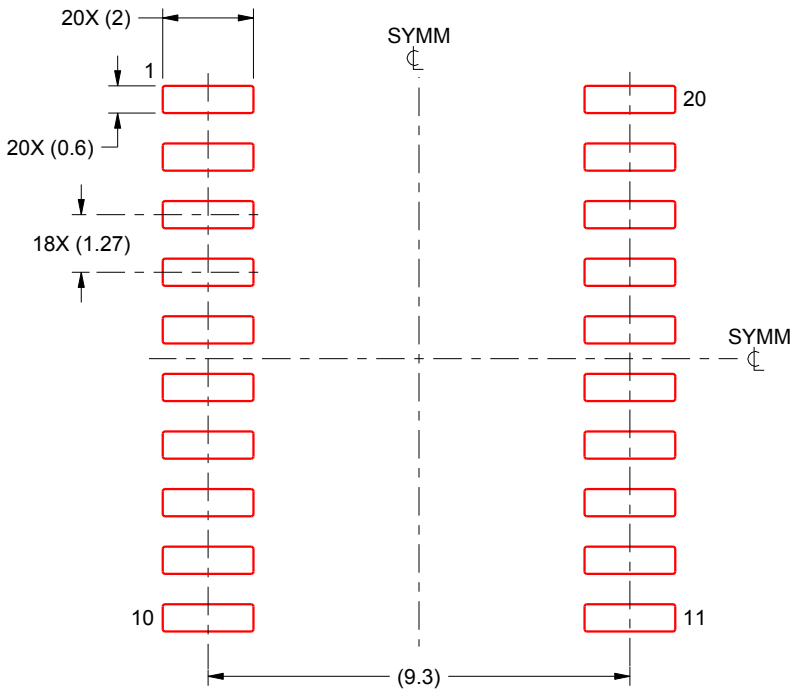


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



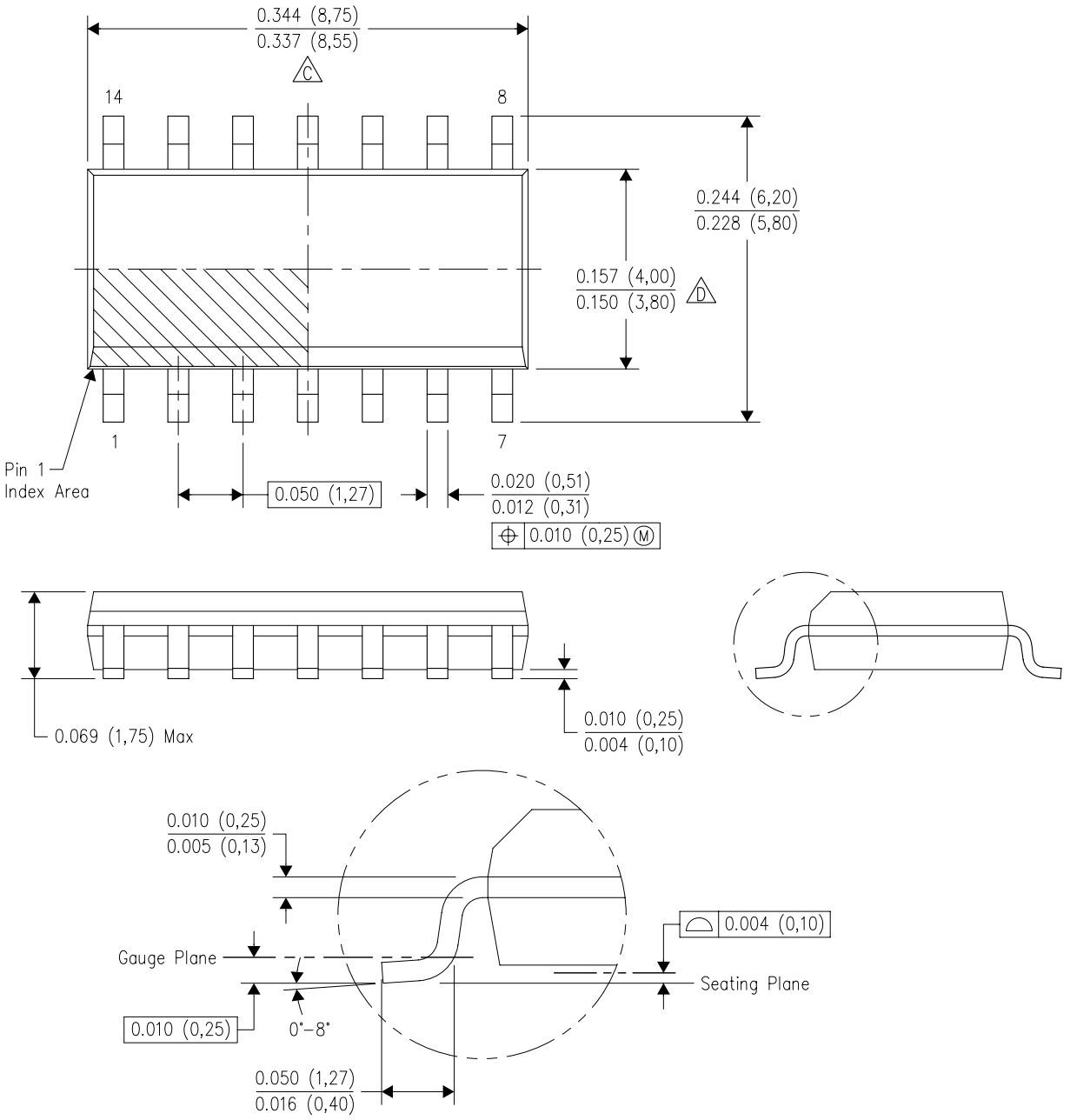
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

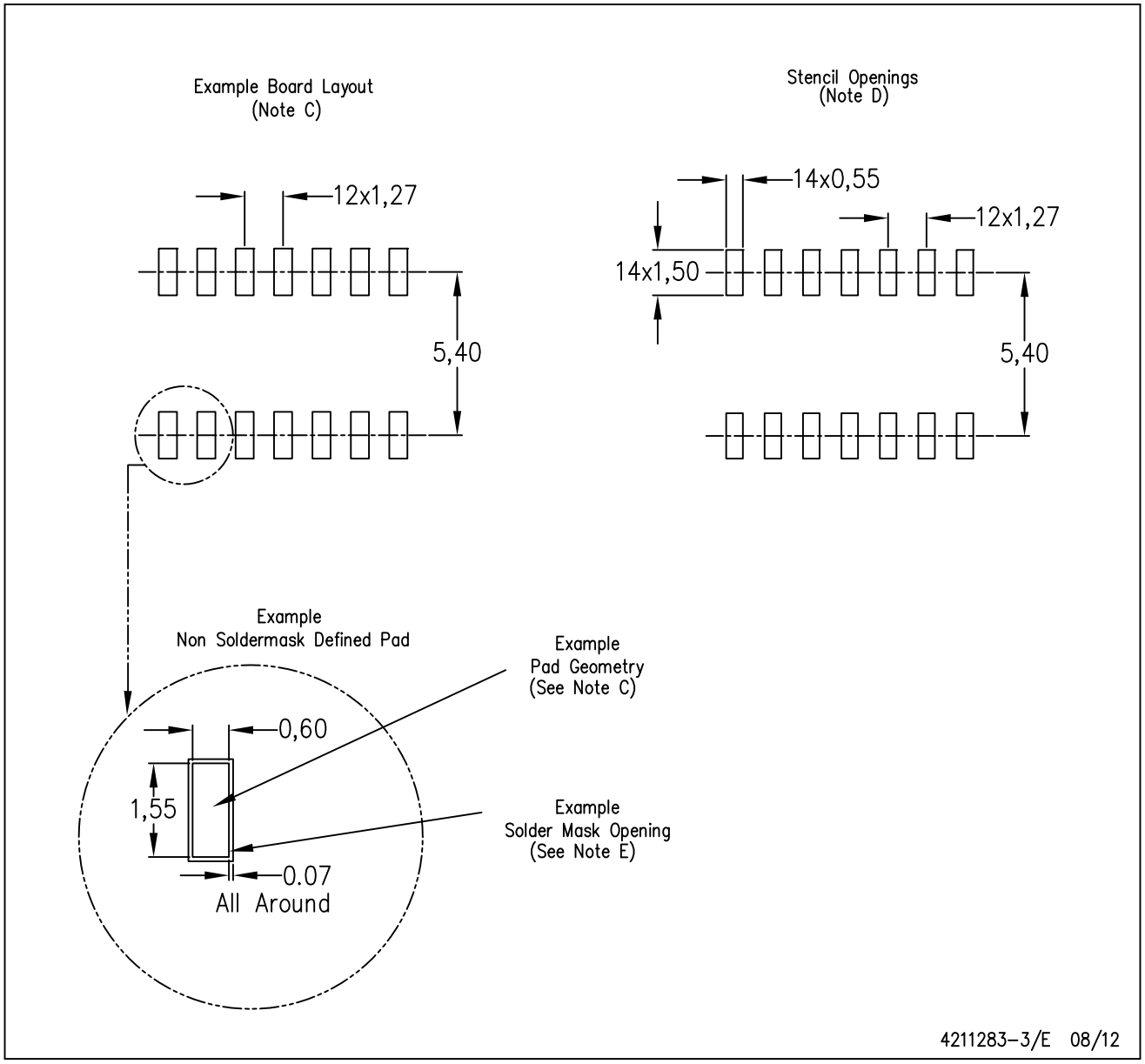
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



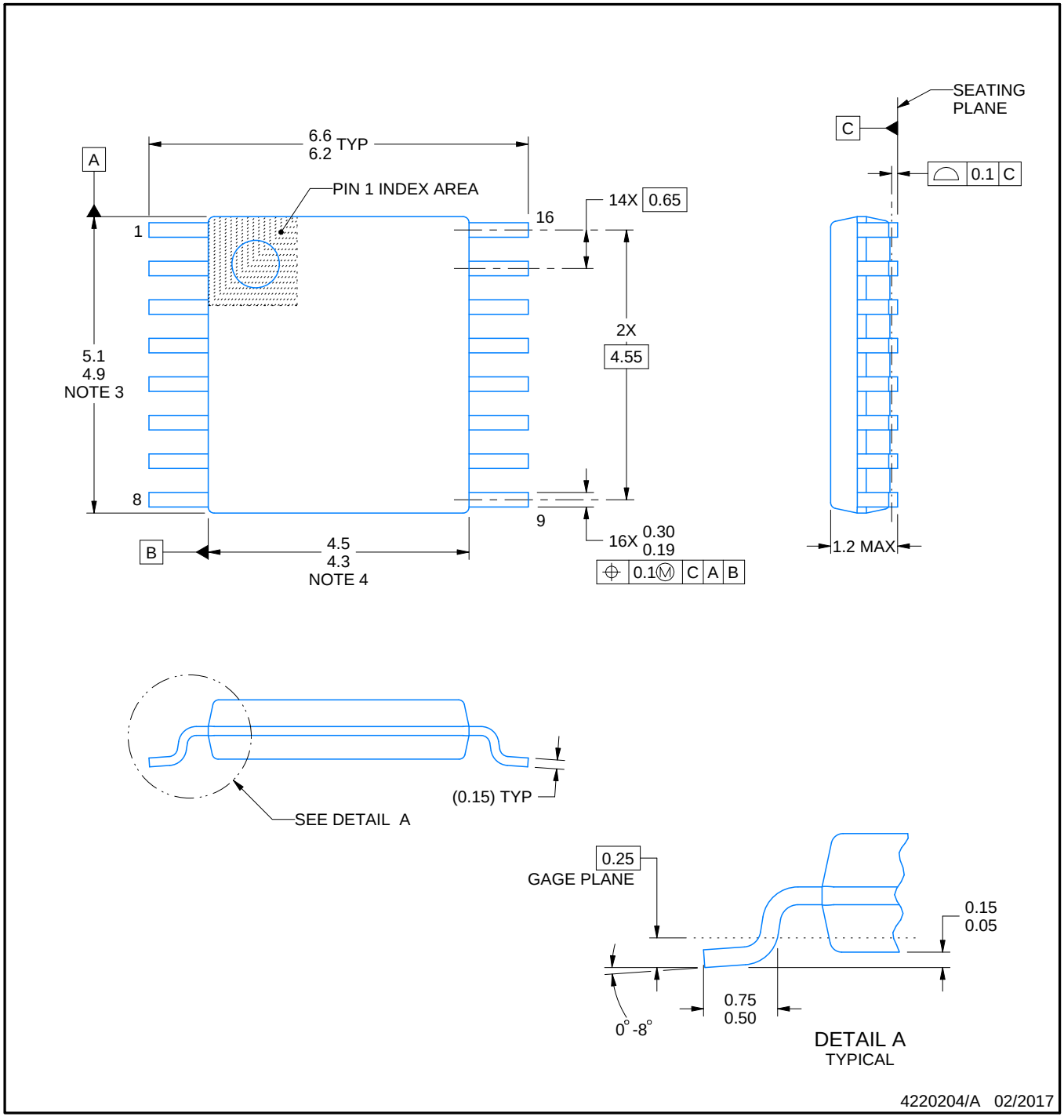
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

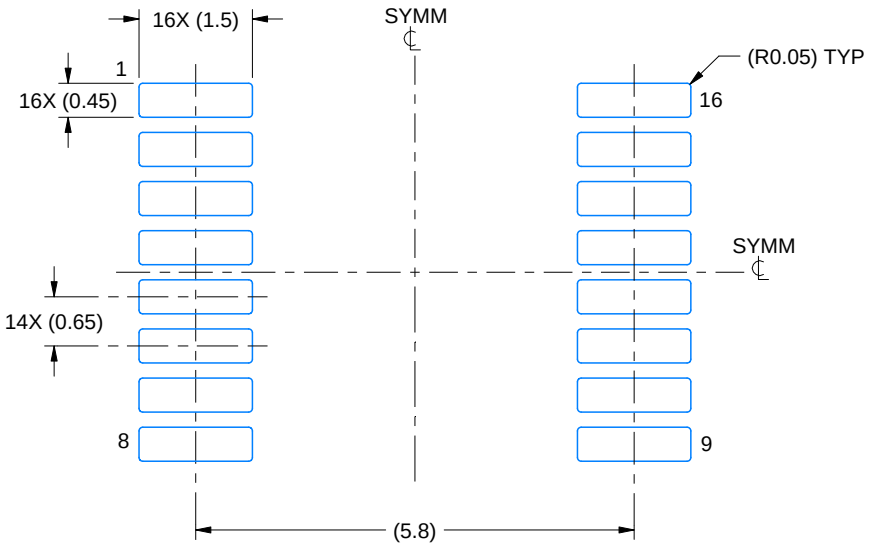
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

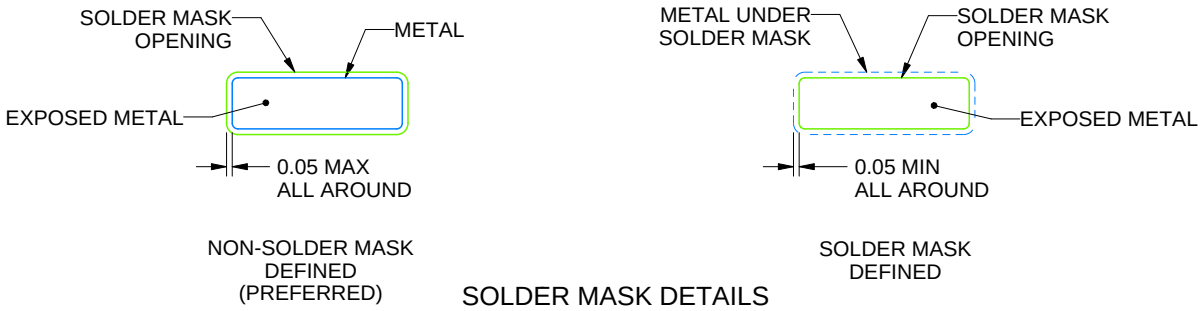


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

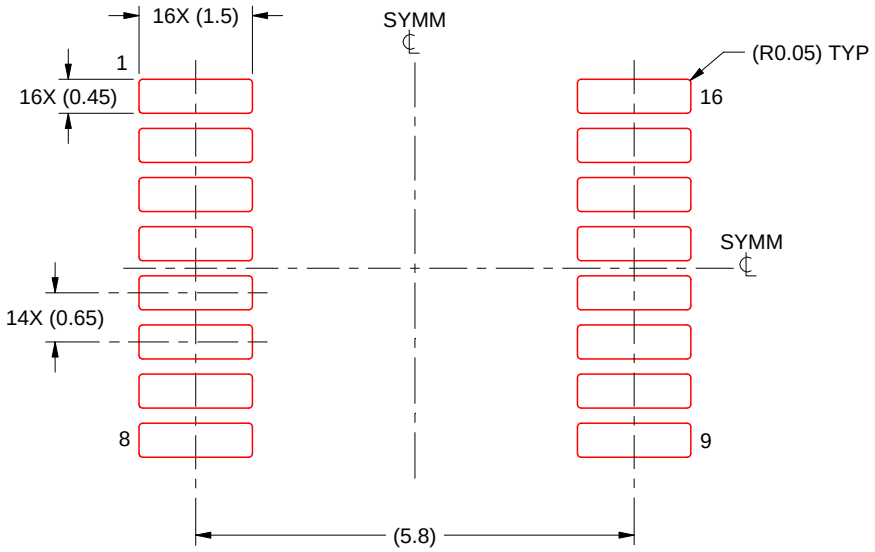


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

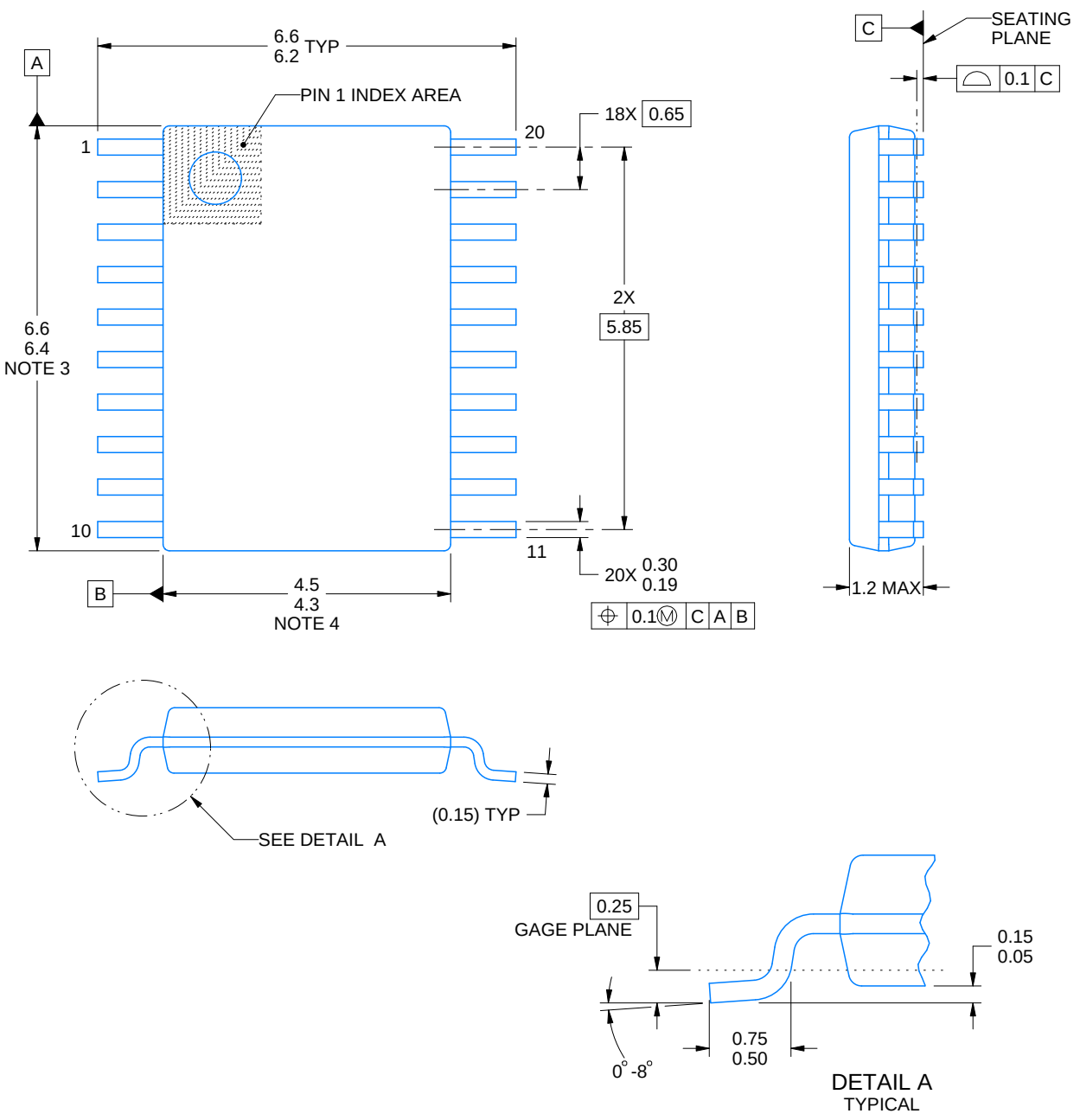
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

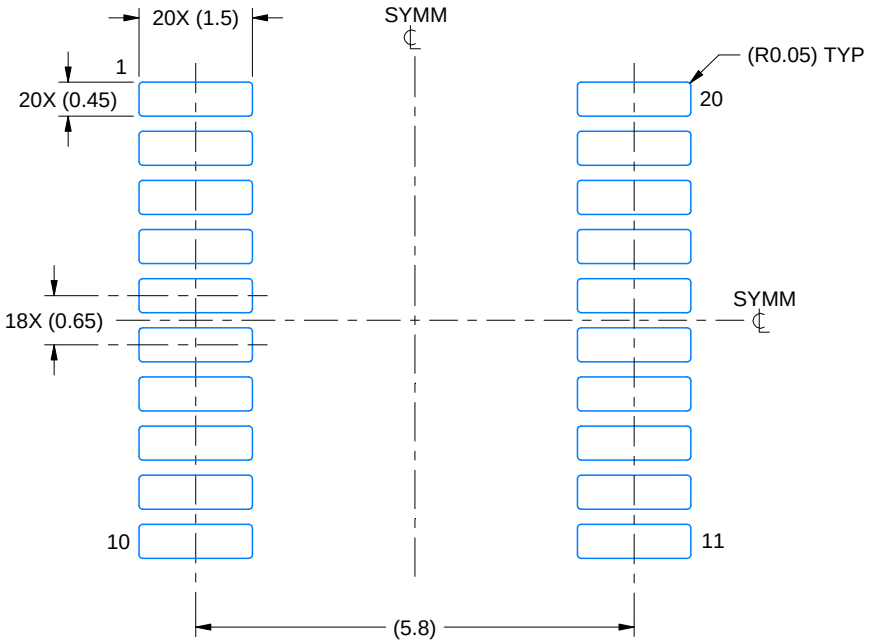
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



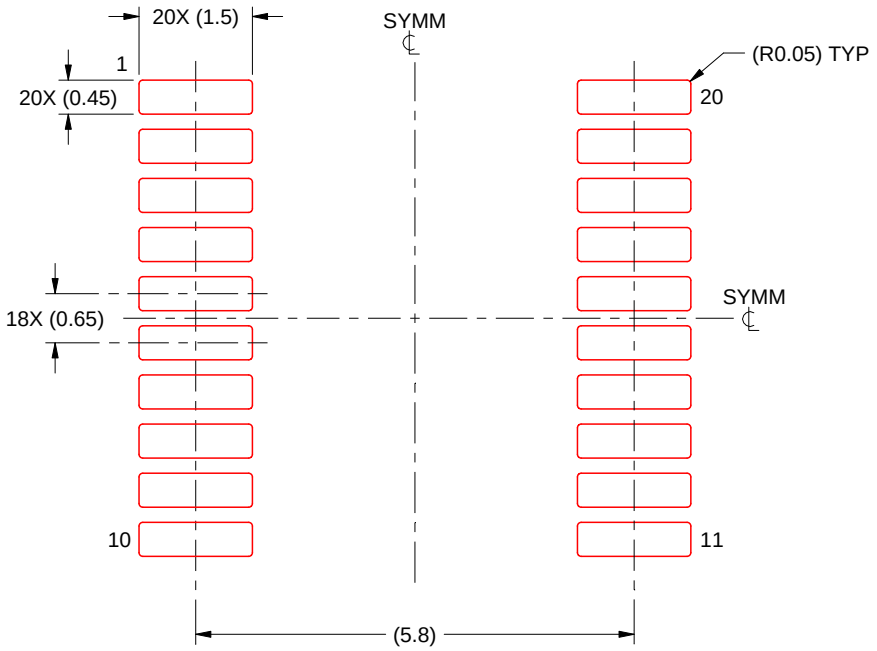
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



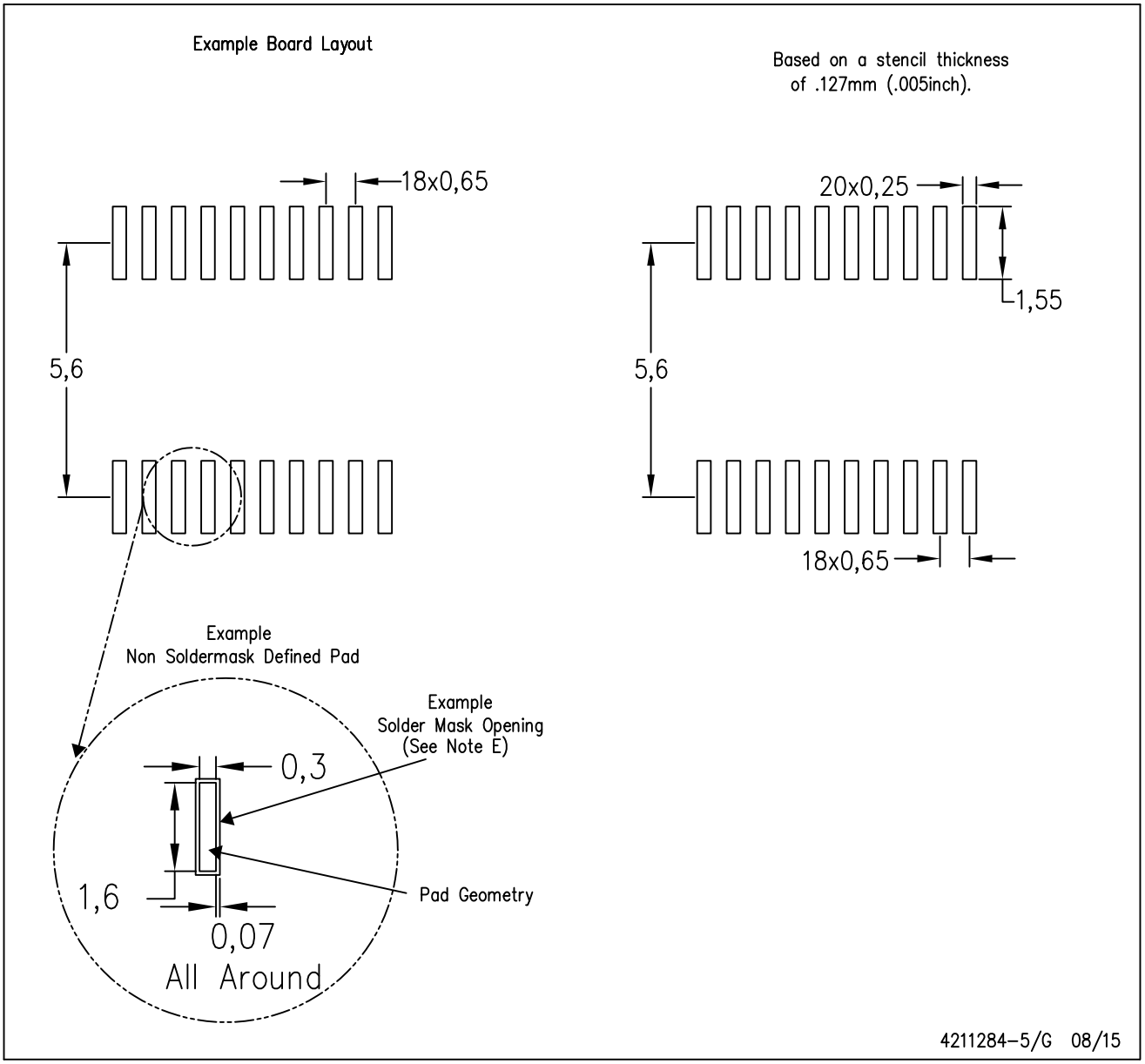
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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