适用于成本敏感型系统的 TLV936x 10MHz、40V、RRO 运算放大器

1 特性

- 低失调电压：±400μV
- 低失调电压漂移：±1.25μV/°C
- 低噪声：1kHz 时为 8.5nV/√Hz，6nV/√Hz 宽带
- 高共模抑制：110dB
- 低偏置电流：±10pA
- 轨到轨输出
- 高带宽：10.6MHz GBW，单位增益稳定
- 高压摆率：25 V/μs
- 低静态电流：每个放大器 2.6 mA
- 宽电源电压：±2.25V 至 ±20V，4.5V 至 40V
- 强大的 EMIRR 性能

2 应用

- 交流和电机驱动伺服控制模块
- 交流和电机驱动功率级模块
- 测试和测量设备
- 可编程逻辑控制器

3 说明

TLV936x 系列（TLV9361、TLV9362 和 TLV9364）是 40V 成本优化型运算放大器系列。

这些器件具有出色的直流和交流规格，包括轨至轨输出、低失调电压（典型值为 ±400μV）、低温漂（典型值为 ±1.25μV/°C）和 10.6MHz 带宽。

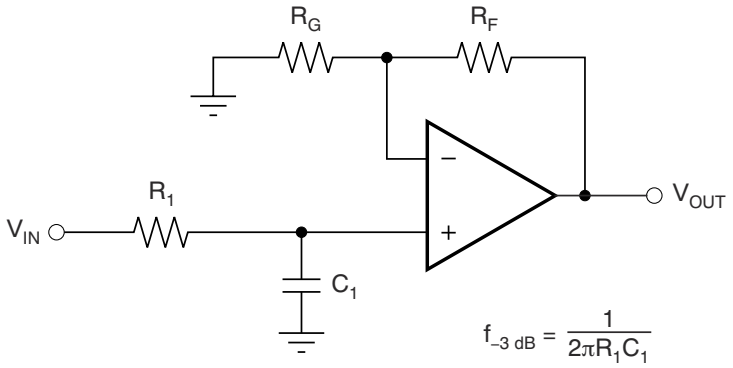
TLV936x 的特性（例如 EMIRR 滤波、高输出电流 (±60mA) 以及高压摆率 (25V/μs)）使其成为了一款可靠的运算放大器，适用于高电压成本敏感型应用。

TLV936x 系列运算放大器采用标准封装，额定工作温度范围为 –40°C 至 125°C。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TLV9361	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
TLV9362	SOIC (8)	4.90mm × 3.90mm
	SOT-23 (8)	2.90mm × 1.60mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
TLV9364	SOIC (14)(2)	8.65mm × 3.90mm
	TSSOP (14)(2)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 此封装为仅预发布状态。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

TLV936x 应用于单极低通滤波器

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SBOSA67

Table of Contents

1 特性.....1
2 应用.....1
3 说明.....1
4 Revision History.....2
5 Pin Configuration and Functions.....3
6 Specifications.....6
6.1 Absolute Maximum Ratings.....6
6.2 ESD Ratings.....6
6.3 Recommended Operating Conditions.....6
6.4 Thermal Information for Single Channel.....6
6.5 Thermal Information for Dual Channel.....7
6.6 Thermal Information for Quad Channel.....7
6.7 Electrical Characteristics.....8
6.8 Typical Characteristics.....10
7 Detailed Description.....17
7.1 Overview.....17
7.2 Functional Block Diagram.....17
7.3 Feature Description.....18
7.4 Device Functional Modes.....23
8 Application Information Disclaimer.....24
8.1 Application Information.....24
8.2 Typical Applications.....24
9 Power Supply Recommendations.....26
10 Layout.....26
10.1 Layout Guidelines.....26
10.2 Layout Example.....27
11 Device and Documentation Support.....28
11.1 Device Support.....28
11.2 Documentation Support.....28
11.3 接收文档更新通知.....28
11.4 支持资源.....28
11.5 Trademarks.....28
11.6 Electrostatic Discharge Caution.....29
11.7 术语表.....29
12 Mechanical, Packaging, and Orderable Information.....30

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
November 2021	*	Initial Release

Copyright © 2022 Texas Instruments Incorporated

5 Pin Configuration and Functions

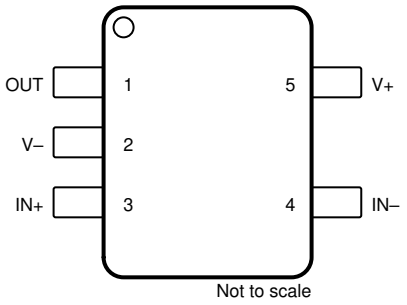


图 5-1. TLV9361 DBV Package 5-Pin SOT-23 (Top View)

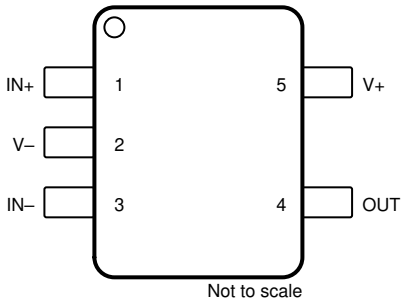


图 5-2. TLV9361 DCK Package 5-Pin SC70 (Top View)

表 5-1. Pin Functions: TLV9361

PIN			I/O	DESCRIPTION
NAME	SOT-23	SC70		
IN+	3	1	I	Noninverting input
IN –	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V –	2	2	—	Negative (lowest) power supply

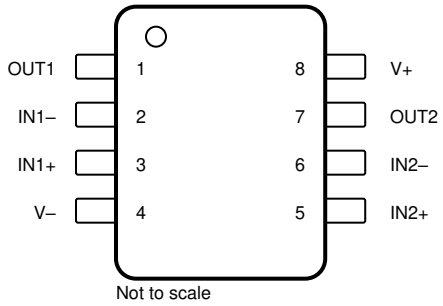
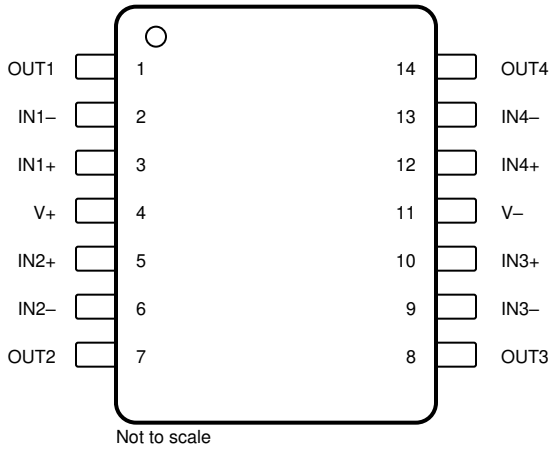


图 5-3. TLV9362 D, DDF, DGK, and PW Package 8-Pin SOIC, SOT-23, VSSOP, and TSSOP (Top View)

表 5-2. Pin Functions: TLV9362

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V –	4	—	Negative (lowest) power supply

Copyright © 2022 Texas Instruments Incorporated



A. 14-pin D and PW packages are preview only.

图 5-4. TLV9364 D and PW Package(A)
SOIC and TSSOP
(Top View)

表 5-3. Pin Functions: TLV9364

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

Copyright © 2022 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage[3]	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage[3]		V_S + 0.2	V
	Current[3]	–10	10	mA
Output short-circuit[2]		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	4.5	40	V
V_I	Common mode voltage range	(V–)	(V+) – 2	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV9361, TLV9361S		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.4	198.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.9	94.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	45.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.4	16.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.1	45.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2022 Texas Instruments Incorporated

6.5 Thermal Information for Dual Channel

THERMAL METRIC[1]		TLV9362				Unit
		D (SOIC)	DDF (SOT-23)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.0	149.6	174.2	183.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.0	85.3	65.9	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	68.6	95.9	114.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.0	7.9	11.0	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.8	68.4	94.4	112.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information for Quad Channel

THERMAL METRIC[1]		TLV9364		UNIT
		D[2] (SOIC)	PW[2] (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.0	118.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	47.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.4	61.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is in preview only for TLV9364.

Copyright © 2022 Texas Instruments Incorporated

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.4	±1.7	mV
			T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±1.25		μV/℃
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 5 V to 40 V(1)	T_A = –40°C to 125°C		±1.5	±7.5	μV/V
	DC channel separation				1		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			6		$μV_{PP}$
					1		$μV_{RMS}$
e_N	Input voltage noise density	f = 1 kHz			8.5		nV/√Hz
		f = 10 kHz			6		
i_N	Input current noise density	f = 1 kHz			100		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = 40 V, V– < V_{CM} < (V+) – 2 V	T_A = –40°C to 125°C	95	110		dB
		V_S = 5 V, V– < V_{CM} < (V+) – 2 V(1)		75	85		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V		115	130		dB
			T_A = –40°C to 125°C		130		
		V_S = 5 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V(1)		100	120		
			T_A = –40°C to 125°C		120		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				10.6		MHz
SR	Slew rate	V_S = 40 V, G = +1, V_{STEP} = 10 V, C_L = 20 pF(3)			25		V/μs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			0.65		μs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			0.3		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			0.86		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			0.44		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			64		°
	Overload recovery time	V_{IN} × gain > V_S			170		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ			0.0001%		
					120		dB
		V_S = 10 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 128 Ω			0.0056%		
					85		dB
		V_S = 10 V, V_O = 0.4 V_{RMS}, G = 1, f = 1 kHz, R_L = 32 Ω			0.00056%		
					105		dB

Copyright © 2022 Texas Instruments Incorporated

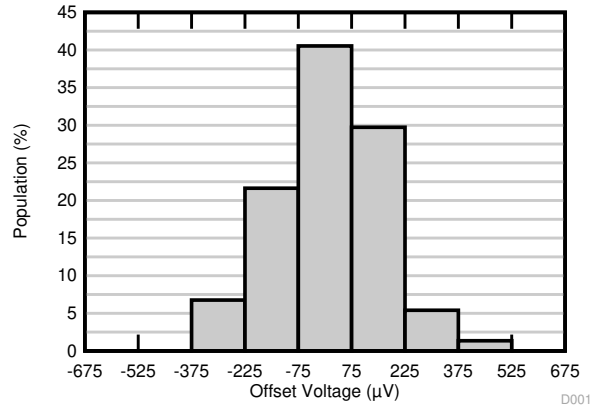
For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load		10		mV
			V_S = 40 V, R_L = 10 kΩ		60	100	
			V_S = 40 V, R_L = 2 kΩ		250	400	
I_{SC}	Short-circuit current				±60(2)		mA
C_{LOAD}	Capacitive Load Drive				See 图 6-28		pF
Z_O	Open-loop output impedance	I_O = 0 A			See 图 6-25		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			2.6	3	mA
			T_A = –40°C to 125°C			3.2	

(1) Specified by characterization only.
(2) At high supply voltage, placing the TLV936x in a sudden short to mid-supply or ground will lead to rapid thermal shutdown. Output current greater than I_{SC} can be achieved if rapid thermal shutdown is avoided as per 图 6-12.
(3) See 图 6-11 for more information.

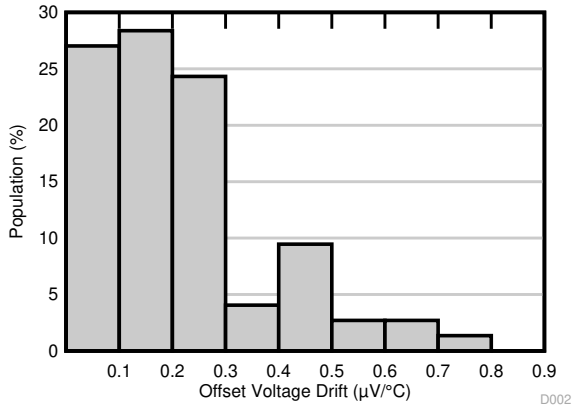
6.8 Typical Characteristics

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ (unless otherwise noted)



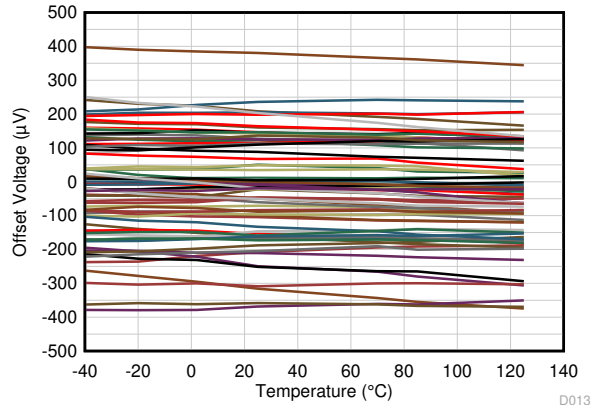
Distribution from 74 amplifiers, T_A = 25°C

图 6-1. Offset Voltage Production Distribution



Distribution from 74 amplifiers

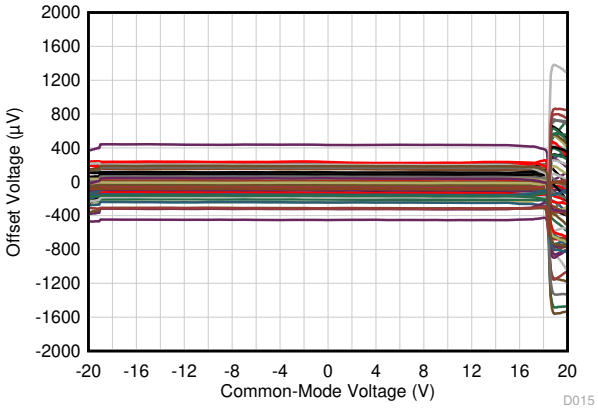
图 6-2. Offset Voltage Drift Distribution



V_{CM} = V-

Data from 74 amplifiers

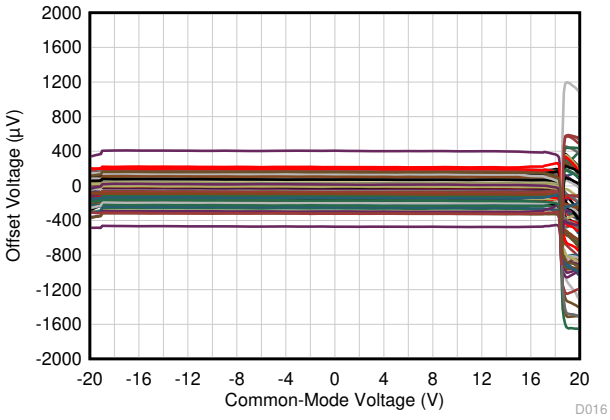
图 6-3. Offset Voltage vs Temperature



T_A = 25°C

Data from 74 amplifiers

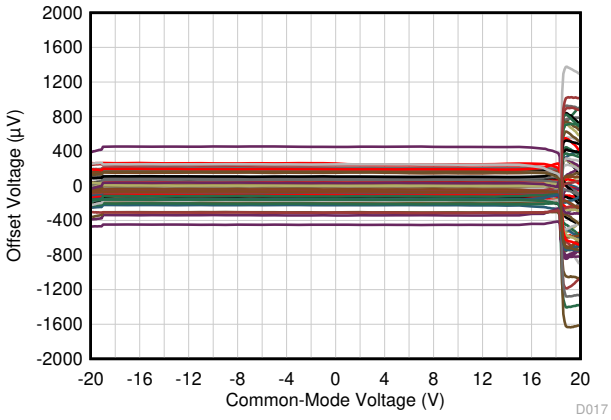
图 6-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

Data from 74 amplifiers

图 6-5. Offset Voltage vs Common-Mode Voltage

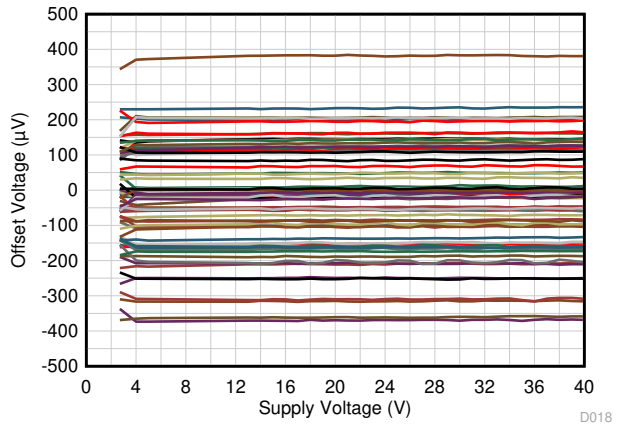


T_A = –40°C

Data from 74 amplifiers

图 6-6. Offset Voltage vs Common-Mode Voltage

Copyright © 2022 Texas Instruments Incorporated



V_{CM} = V –

Data from 74 amplifiers

图 6-7. Offset Voltage vs Power Supply

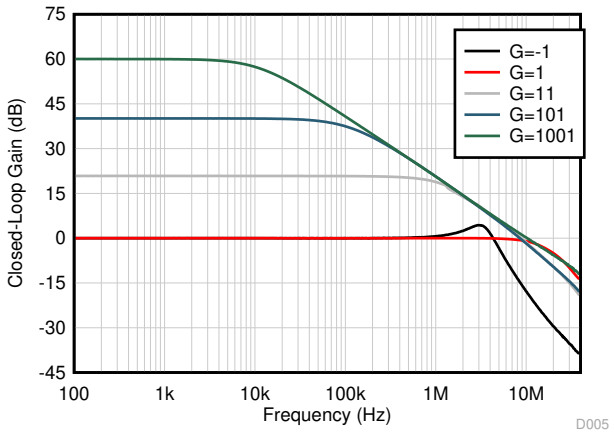


图 6-8. Closed-Loop Gain vs Frequency

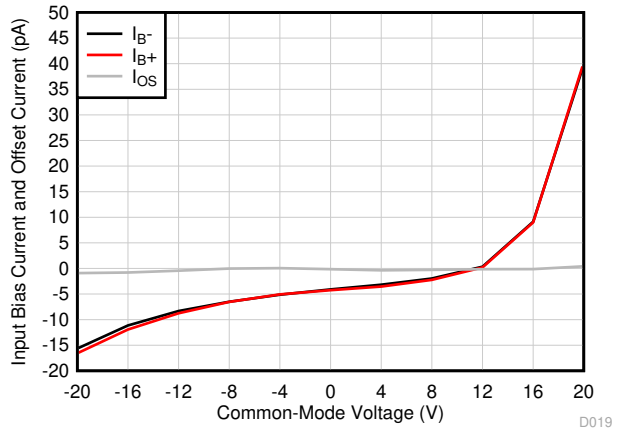


图 6-9. Input Bias Current and Offset Current vs Common-Mode Voltage

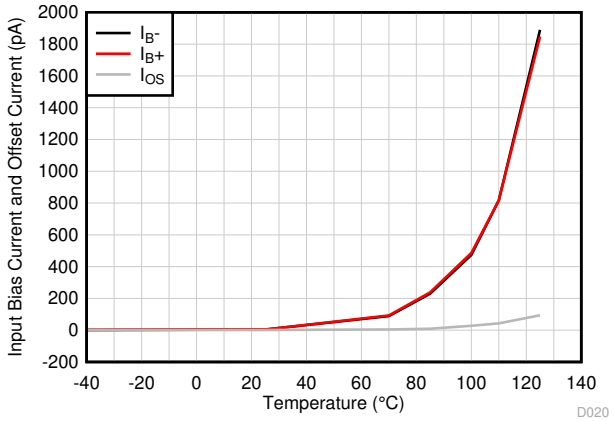
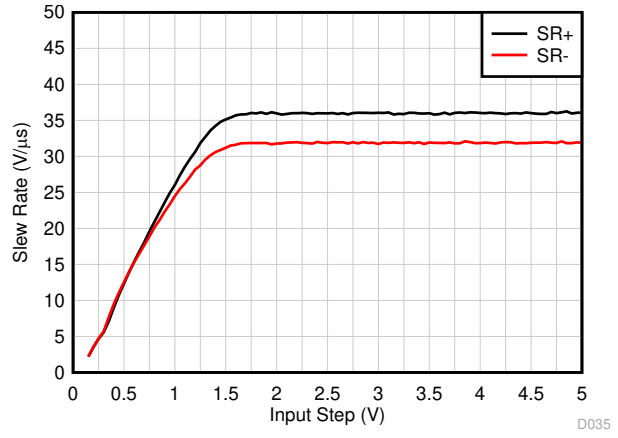
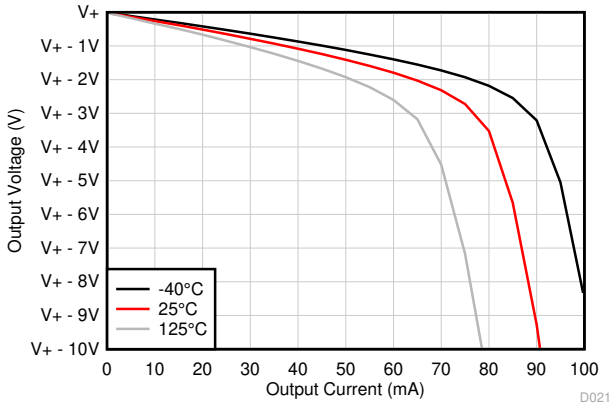


图 6-10. Input Bias Current and Offset Current vs Temperature



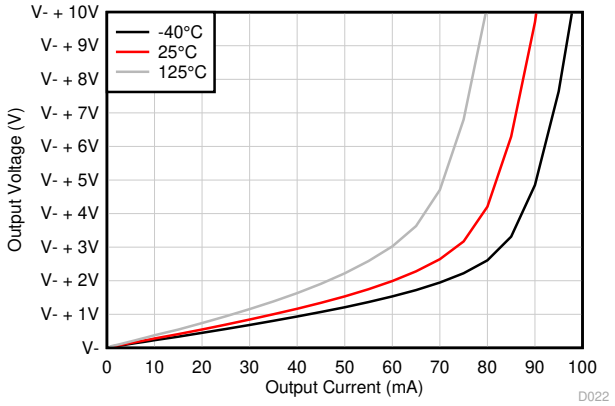
G = +1, C_L = 20 pF

图 6-11. Slew Rate vs Input Step Voltage



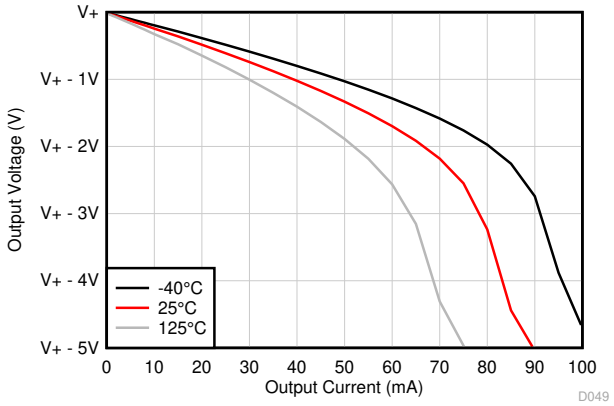
V_S = 40 V

图 6-12. Output Voltage Swing vs Output Current (Sourcing)



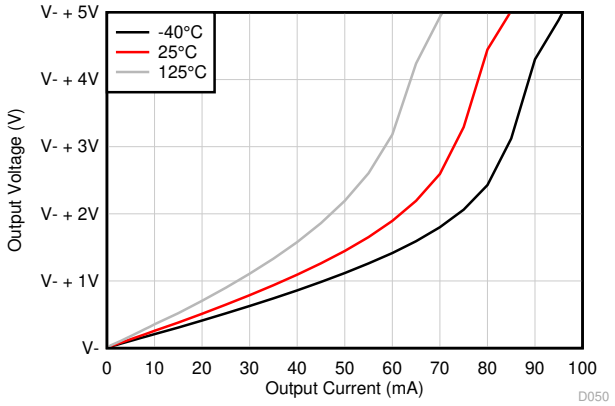
V_S = 40 V

图 6-13. Output Voltage Swing vs Output Current (Sinking)



V_S = 5 V

图 6-14. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5 V

图 6-15. Output Voltage Swing vs Output Current (Sinking)

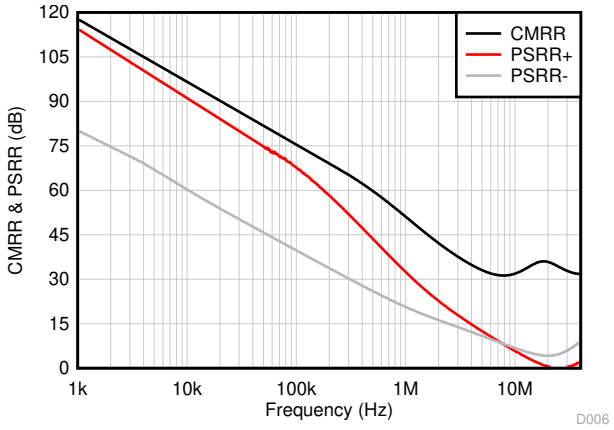
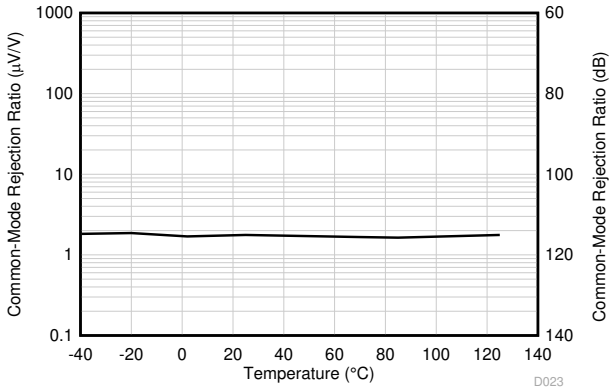
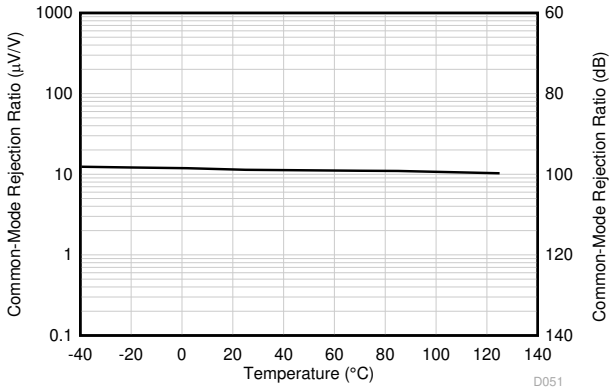


图 6-16. CMRR and PSRR vs Frequency



V_S = 40 V

图 6-17. CMRR vs Temperature



V_S = 5 V

图 6-18. CMRR vs Temperature

Copyright © 2022 Texas Instruments Incorporated

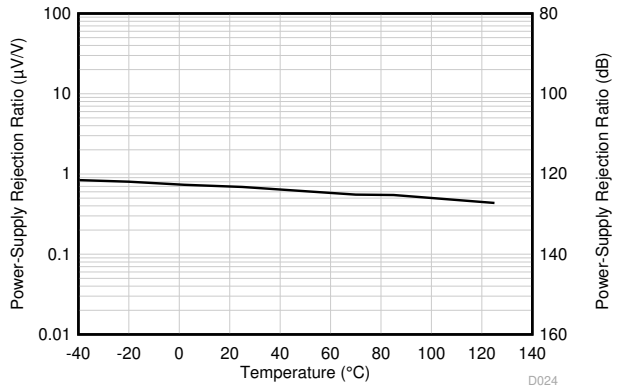


图 6-19. PSRR vs Temperature

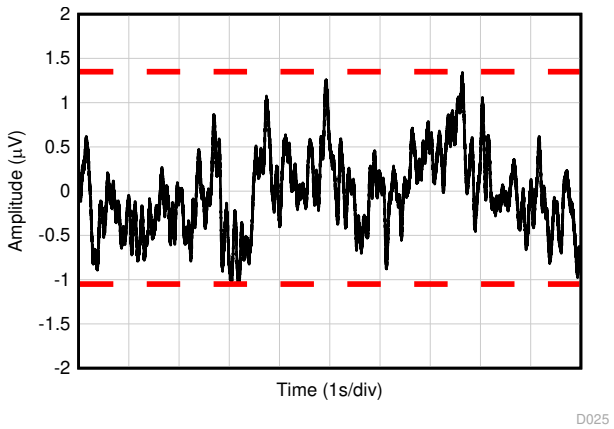


图 6-20. 0.1-Hz to 10-Hz Noise

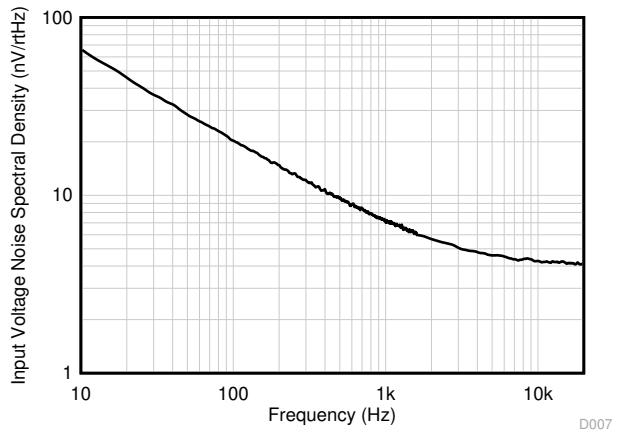
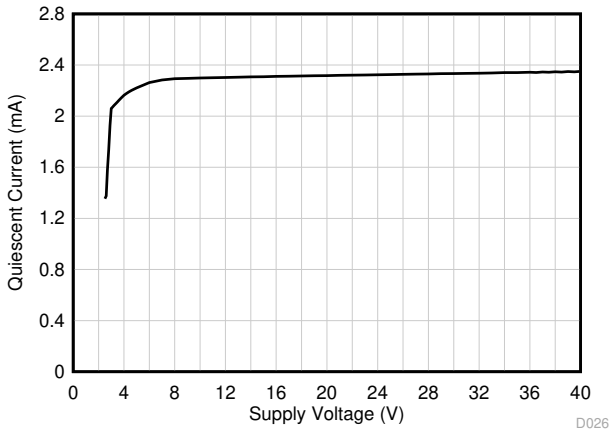
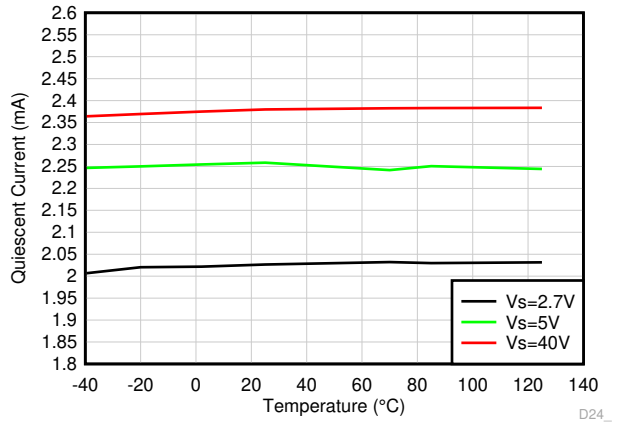


图 6-21. Input Voltage Noise Spectral Density vs Frequency



V_{CM} = V –

图 6-22. Quiescent Current vs Supply Voltage



V_{CM} = V –

图 6-23. Quiescent Current vs Temperature

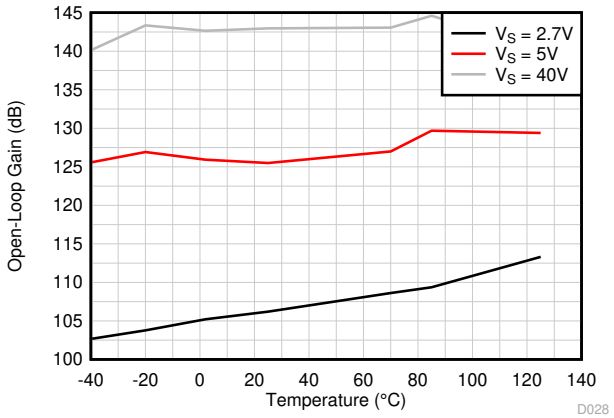


图 6-24. Open-Loop Voltage Gain vs Temperature (dB)

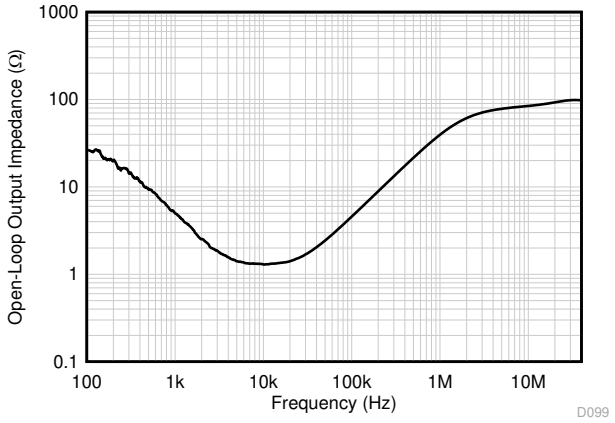
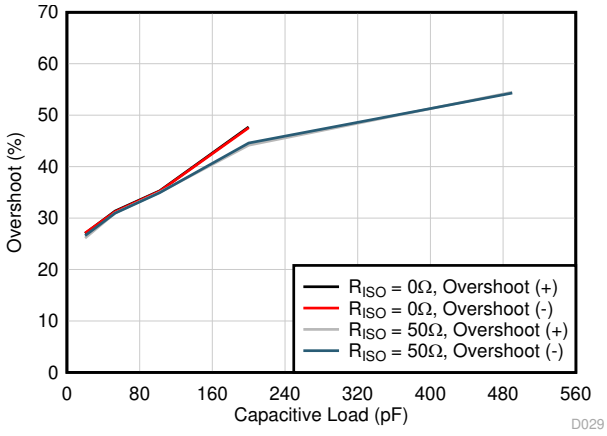
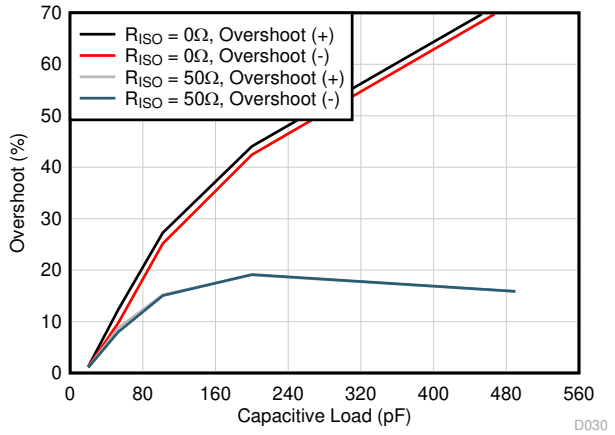


图 6-25. Open-Loop Output Impedance vs Frequency



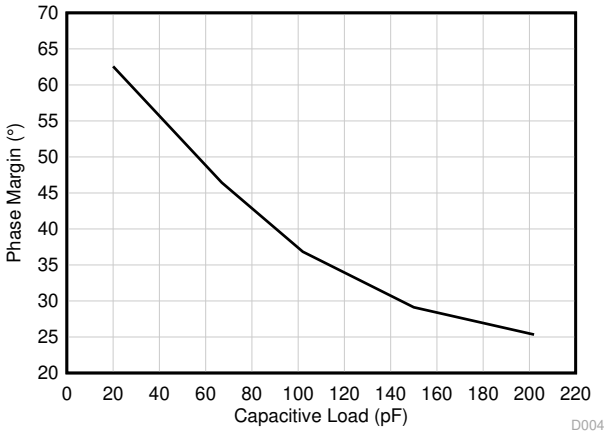
20-mV$_{pp}$ Output Step, G = -1

图 6-26. Small-Signal Overshoot vs Capacitive Load



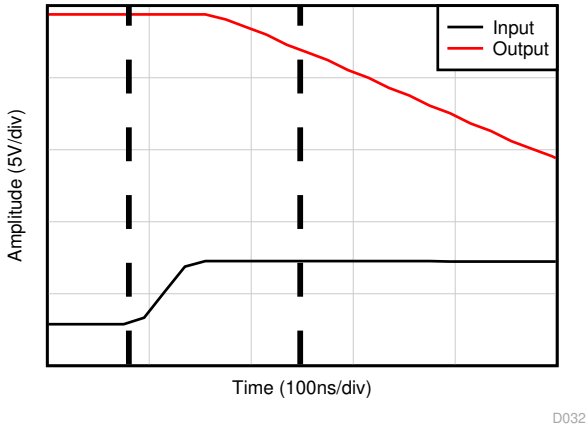
20-mV$_{pp}$ Output Step, G = +1

图 6-27. Small-Signal Overshoot vs Capacitive Load



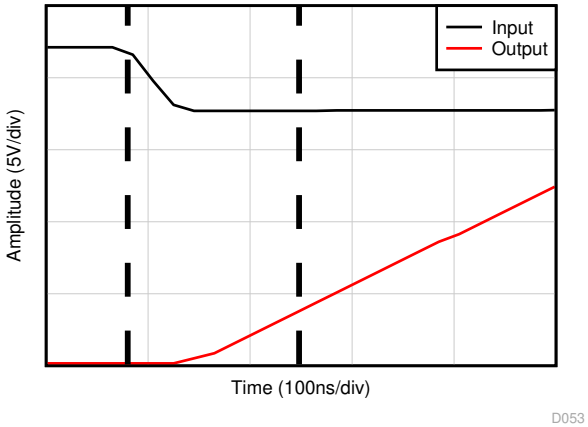
G = +1

图 6-28. Phase Margin vs Capacitive Load



G = –10

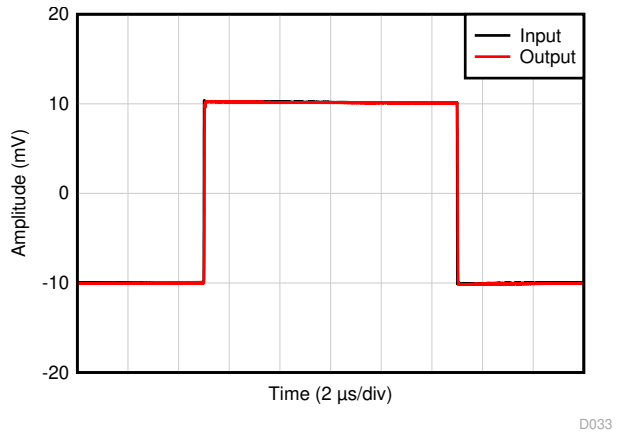
图 6-29. Positive Overload Recovery



G = –10

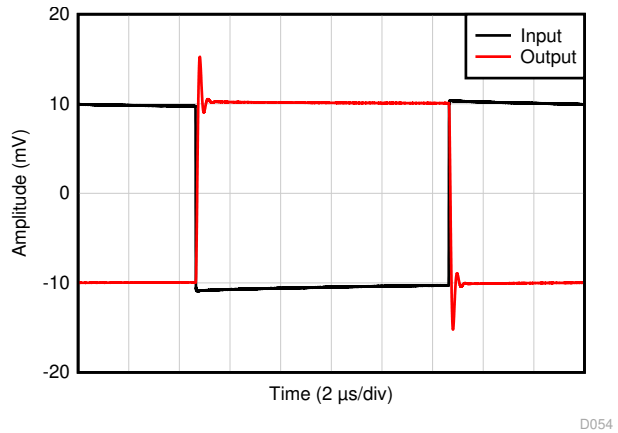
图 6-30. Negative Overload Recovery

Copyright © 2022 Texas Instruments Incorporated



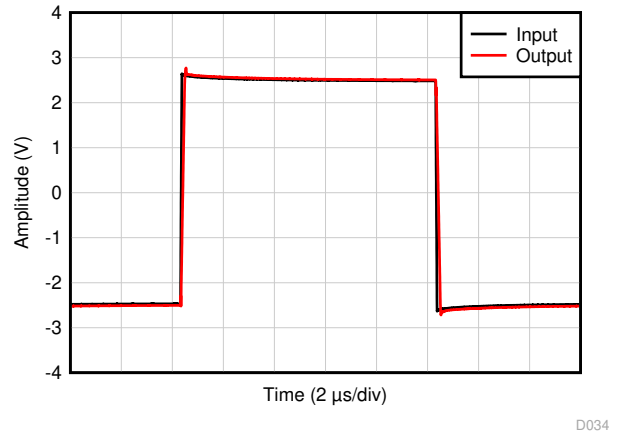
C_L = 20 pF, G = 1, 20-mV_{pp} step response

图 6-31. Small-Signal Step Response



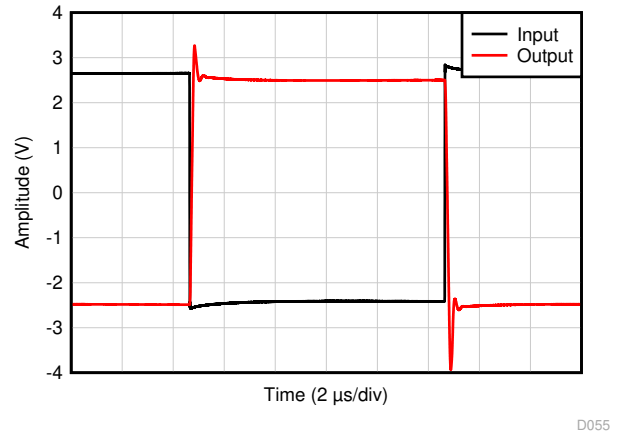
C_L = 20 pF, G = -1, 20-mV_{pp} step response

图 6-32. Small-Signal Step Response



C_L = 20 pF, G = 1, 5-V_{pp} step response

图 6-33. Large-Signal Step Response



C_L = 20 pF, G = -1, 5-V_{pp} step response

图 6-34. Large-Signal Step Response

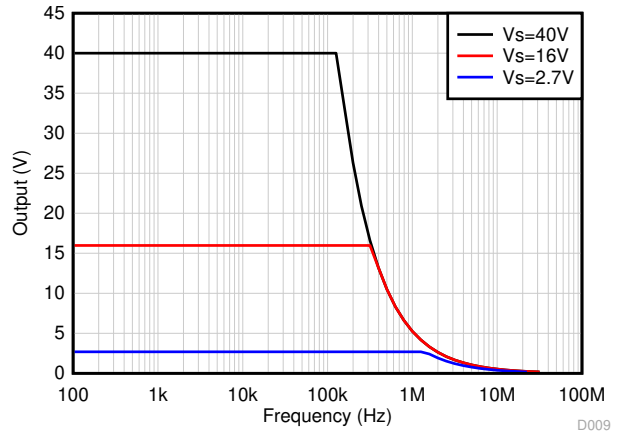


图 6-35. Maximum Output Voltage vs Frequency

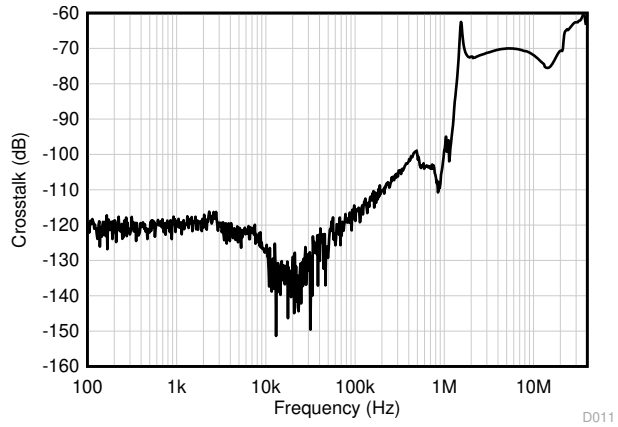


图 6-36. Channel Separation vs Frequency

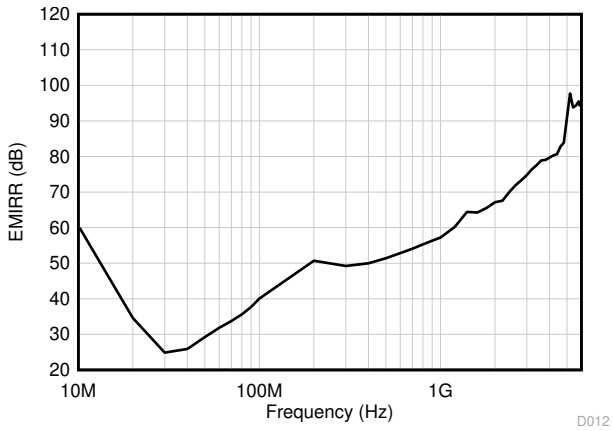


图 6-37. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

Copyright © 2022 Texas Instruments Incorporated

7 Detailed Description

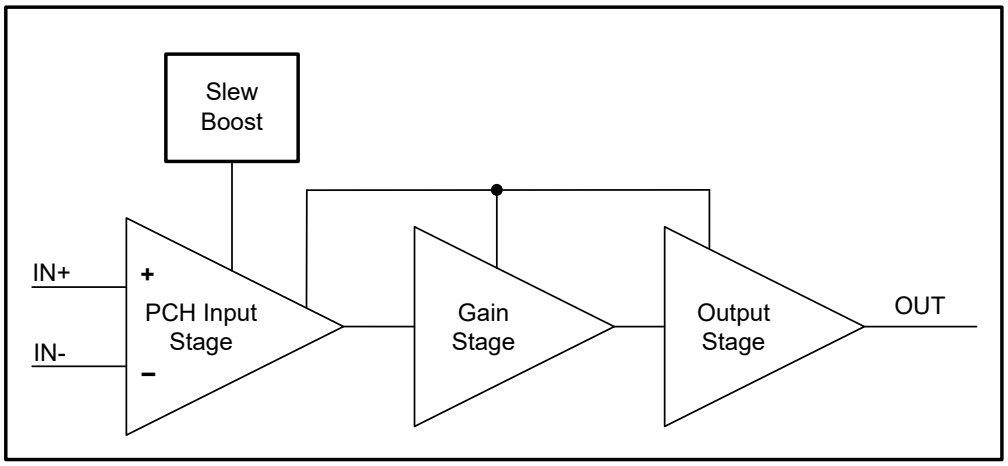
7.1 Overview

The TLV936x family (TLV9361, TLV9362, and TLV9364) is a family of 40-V, cost-optimized operational amplifiers. These devices offer strong general-purpose DC and AC specifications, including rail-to-rail output, low offset (±400 µV, typ), low offset drift (±1.25 µV/°C, typ), and 10.6-MHz bandwidth.

Convenient features such as wide differential input-voltage range, high output current (±60 mA), and high slew rate (25 V/µs) make the TLV936x a robust operational amplifier for high-voltage, cost-sensitive applications.

The TLV936x family of op amps is available in standard packages and is specified from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 EMI Rejection

The TLV936x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV936x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 7-1 shows the results of this testing on the TLV936x. 表 7-1 shows the EMIRR IN+ values for the TLV936x at particular frequencies commonly encountered in real-world applications. 表 7-1 lists applications that may be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

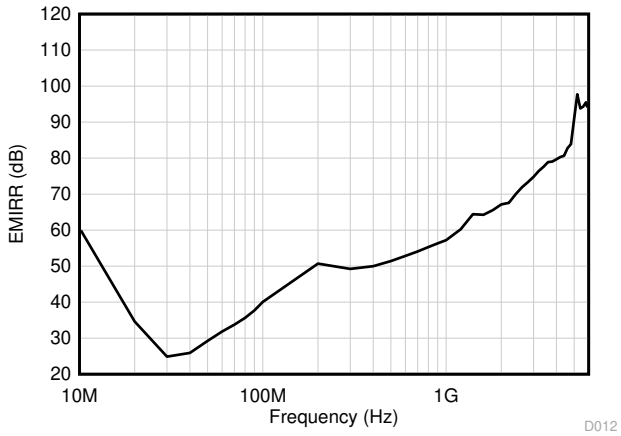


图 7-1. EMIRR Testing

表 7-1. TLV936x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	56.3 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	65.6 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	70.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	91.0 dB

7.3.2 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV936x is 150°C. Exceeding this temperature causes damage to the device. The TLV936x has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 7-2 shows an application example for the TLV9362 that has significant self heating because of its power dissipation (0.954 W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 55°C, the device junction temperature reaches 180°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 7-2 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V.

Copyright © 2022 Texas Instruments Incorporated

When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the SOIC (8) package.

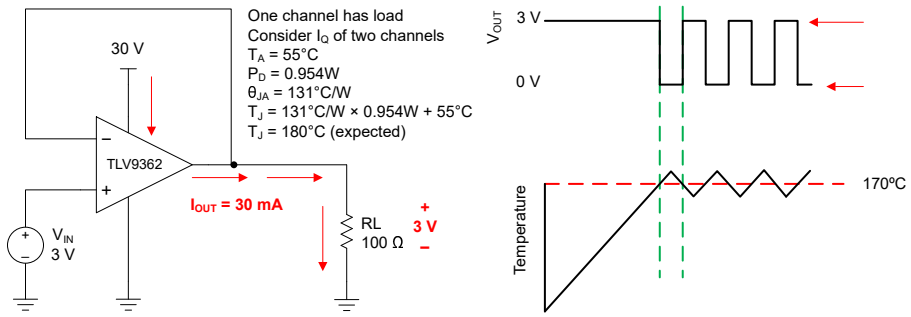


图 7-2. Thermal Protection

7.3.3 Capacitive Load and Stability

The TLV936x features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to driver large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 7-3 and 图 7-4. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

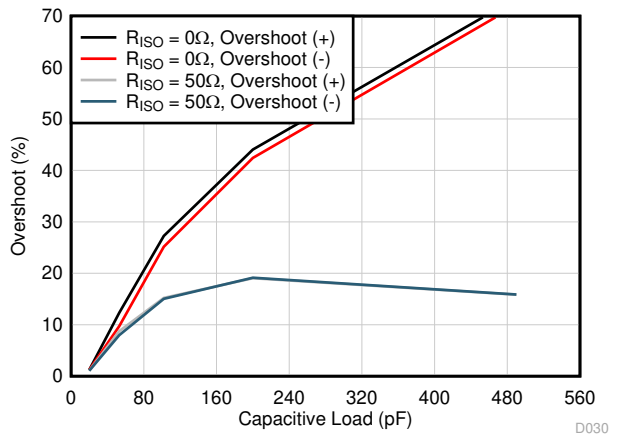


图 7-3. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = +1)

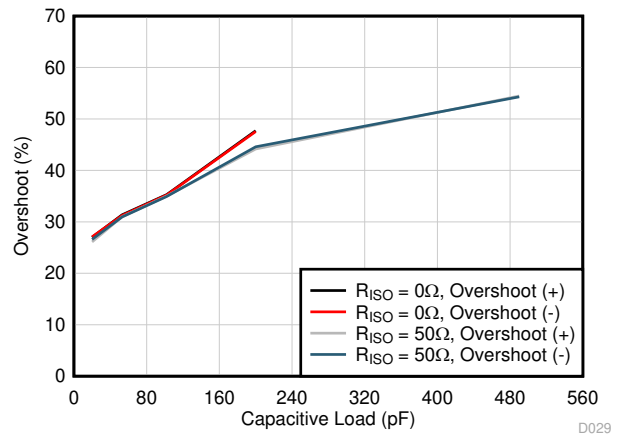


图 7-4. Small-Signal Overshoot vs Capacitive Load (20-mV_{pp} Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 图 7-5. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLV936x well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 7-5 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

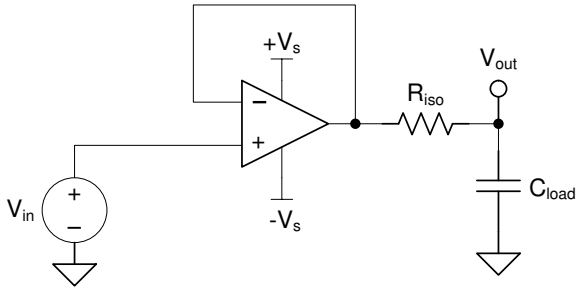


图 7-5. Extending Capacitive Load Drive With the TLV9361

Copyright © 2022 Texas Instruments Incorporated

7.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 7-6 shows an illustration of the ESD circuits contained in the TLV936x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

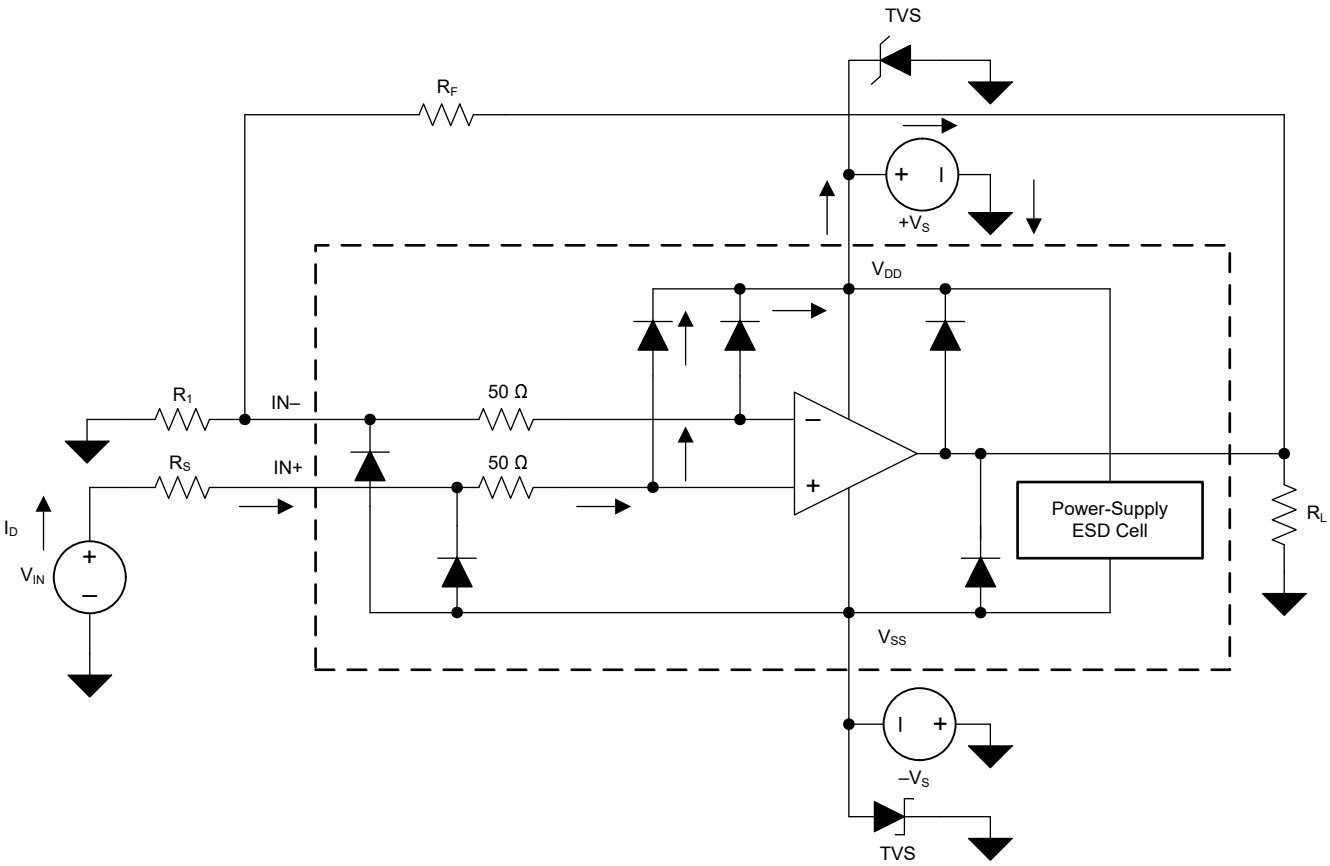


图 7-6. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.5 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV936x is approximately 170 ns.

7.3.6 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

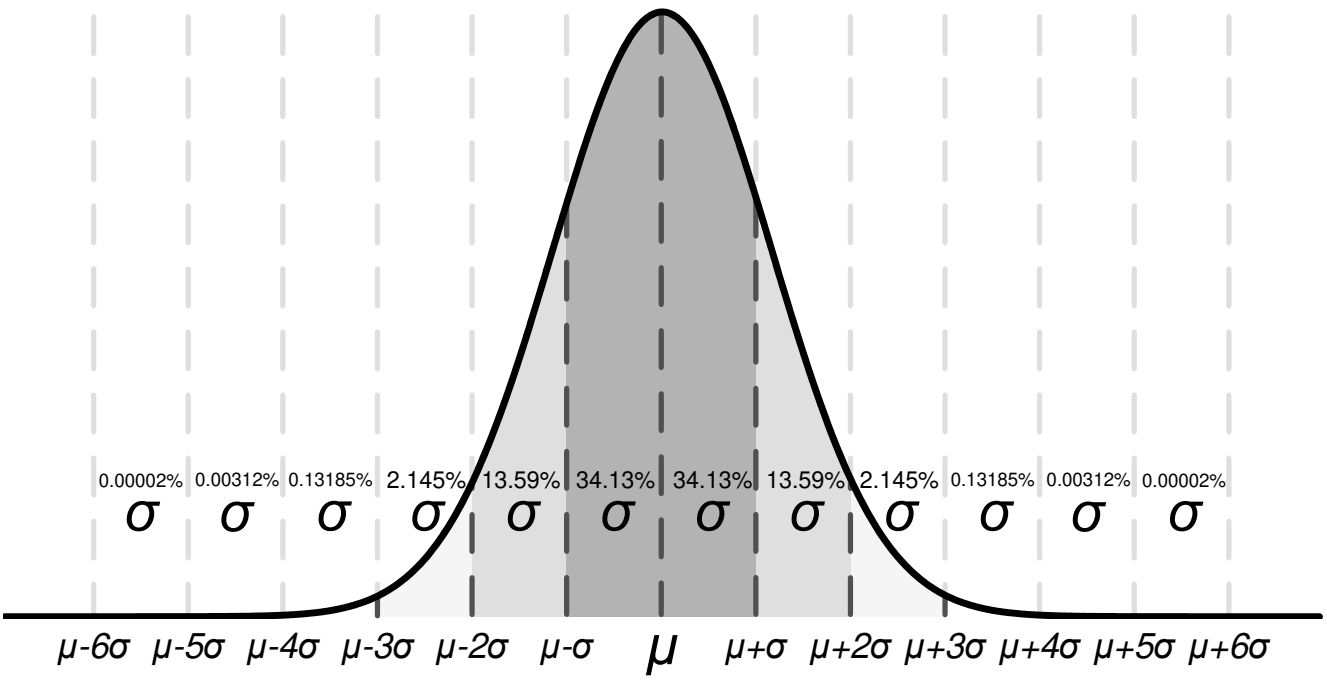


图 7-7. Ideal Gaussian Distribution

图 7-7 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ* – σ to *μ* + σ).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV936x, the typical input voltage offset is 400 μV, so 68.2% of all TLV936x devices are expected to have an offset from

Copyright © 2022 Texas Instruments Incorporated

–400 µV to 400 µV. At 4 σ (±1600 µV), 99.9937% of the distribution has an offset voltage less than ±1600 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV936x family has a maximum offset voltage of 1.7 mV at 125°C, and even though this corresponds to about 4.25 σ (≈2 in 100,000 units), which is unlikely, TI assures that any unit with larger offset than 1.7 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV936x family does not have a maximum or minimum for offset voltage drift, but based on the typical value of 1.25 µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 7.5 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.4 Device Functional Modes

The TLV936x has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the TLV936x is 40 V (±20 V).

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

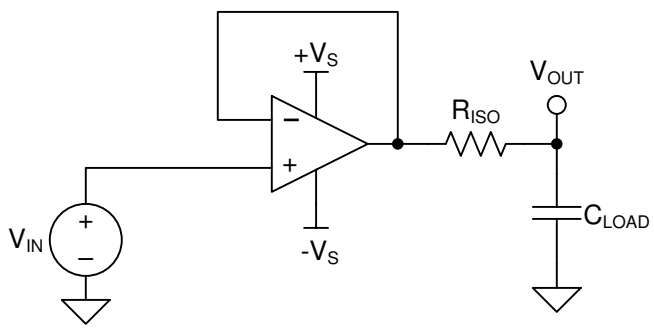
8.1 Application Information

The TLV936x family offers excellent DC precision and DC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail output, low offset voltage and offset voltage drift, as well as 10.6-MHz bandwidth and high output drive. These features make the TLV936x a robust, high-performance operational amplifier for high-voltage cost-sensitive applications.

8.2 Typical Applications

8.2.1 Unity-Gain Buffer With R_{ISO} Stability Compensation

This circuit can drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an operational amplifier. R_{ISO} modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin.



Copyright © 2017, Texas Instruments Incorporated

图 8-1. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 20 pF, 100 pF, 200 pF, and 500 pF
- Phase margin: 45°

8.2.1.2 Detailed Design Procedure

图 8-1 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in 图 8-1. 图 8-1 does not show the open-loop output resistance of the operational amplifier (R_o).

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. The R_{ISO} and C_{LOAD} components determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} so that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB per decade. 图 8-2 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Copyright © 2022 Texas Instruments Incorporated

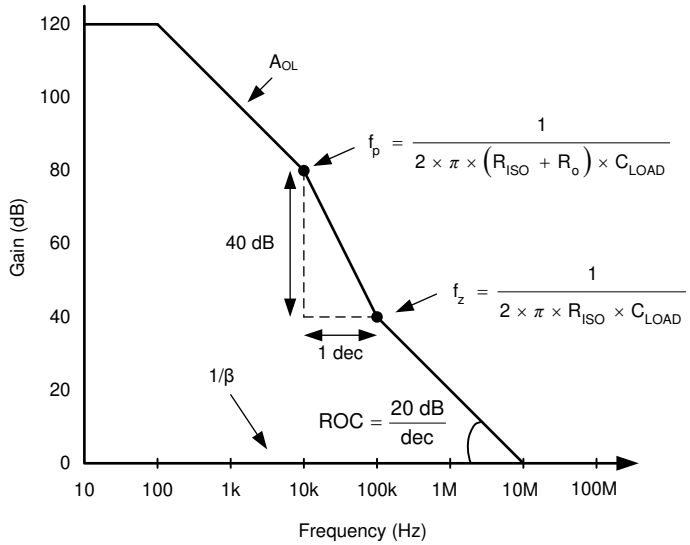


图 8-2. Unity-Gain Amplifier With R_{ISO} Compensation

Typically, ROC stability analysis is simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and/or AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 8-1 shows the overshoot percentage and AC gain peaking that correspond to a phase margin of 45°. For more details on this design and other alternative devices that can replace the TLV936x, see the *Capacitive Load Drive Solution Using an Isolation Resistor* precision design.

表 8-1. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB

8.2.1.3 Application Curve

The values of R_{ISO} that yield phase margins of 45°, or other typical design targets such as 60°, for various capacitive loads can be determined using the described methodology. 图 8-3 shows the results that can be achieved with no R_{ISO} compensation vs an R_{ISO} of 50 Ω .

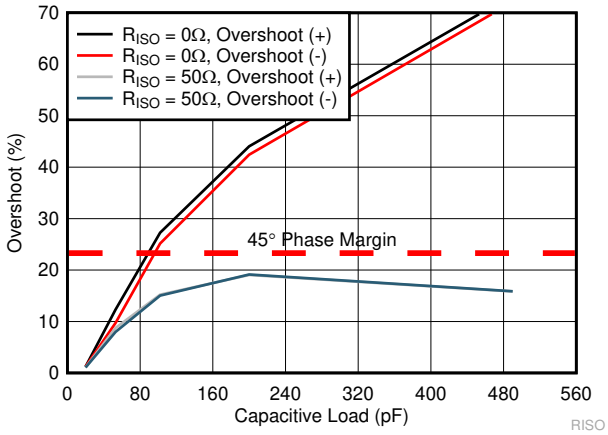


图 8-3. Small-Signal Overshoot vs Capacitive Load with R_{ISO}

9 Power Supply Recommendations

The TLV936x is specified for operation from 4.5 V to 40 V (±2.25 V to ±20 V); many specifications apply from –40°C to 125°C.

> **CAUTION**
>
> Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 10-2, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Copyright © 2022 Texas Instruments Incorporated

10.2 Layout Example

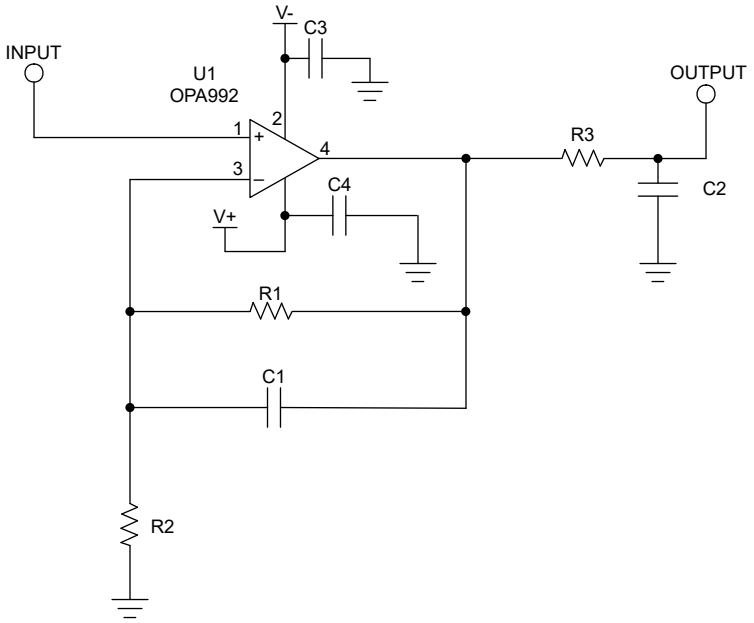


图 10-1. Schematic for Noninverting Configuration Layout Example

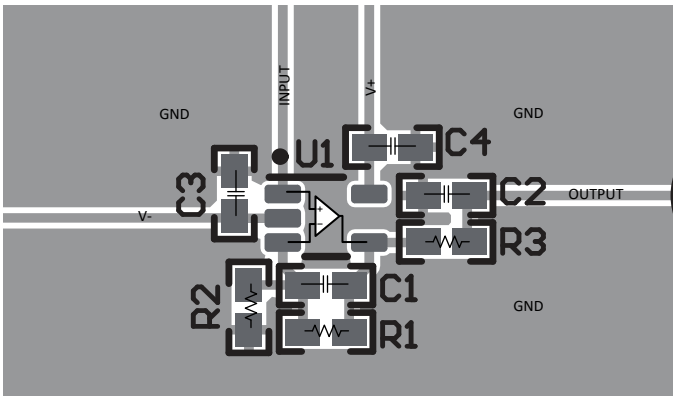


图 10-2. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

The TLV936x is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers*

Texas Instruments, *AN31 amplifier circuit collection* application report

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

Texas Instruments, *Capacitive Load Drive Solution using an Isolation Resistor* reference design

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

TINA-TI™ are trademarks of Texas Instruments, Inc and DesignSoft, Inc.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

Copyright © 2022 Texas Instruments Incorporated

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2022 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9361IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T93DB	Samples
TLV9361IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1JU	Samples
TLV9362IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2IDF	Samples
TLV9362IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2JWT	Samples
TLV9362IDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9362D	Samples
TLV9362IPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9362P	Samples
TLV9364IDR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9364D	Samples
TLV9364IPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9364PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

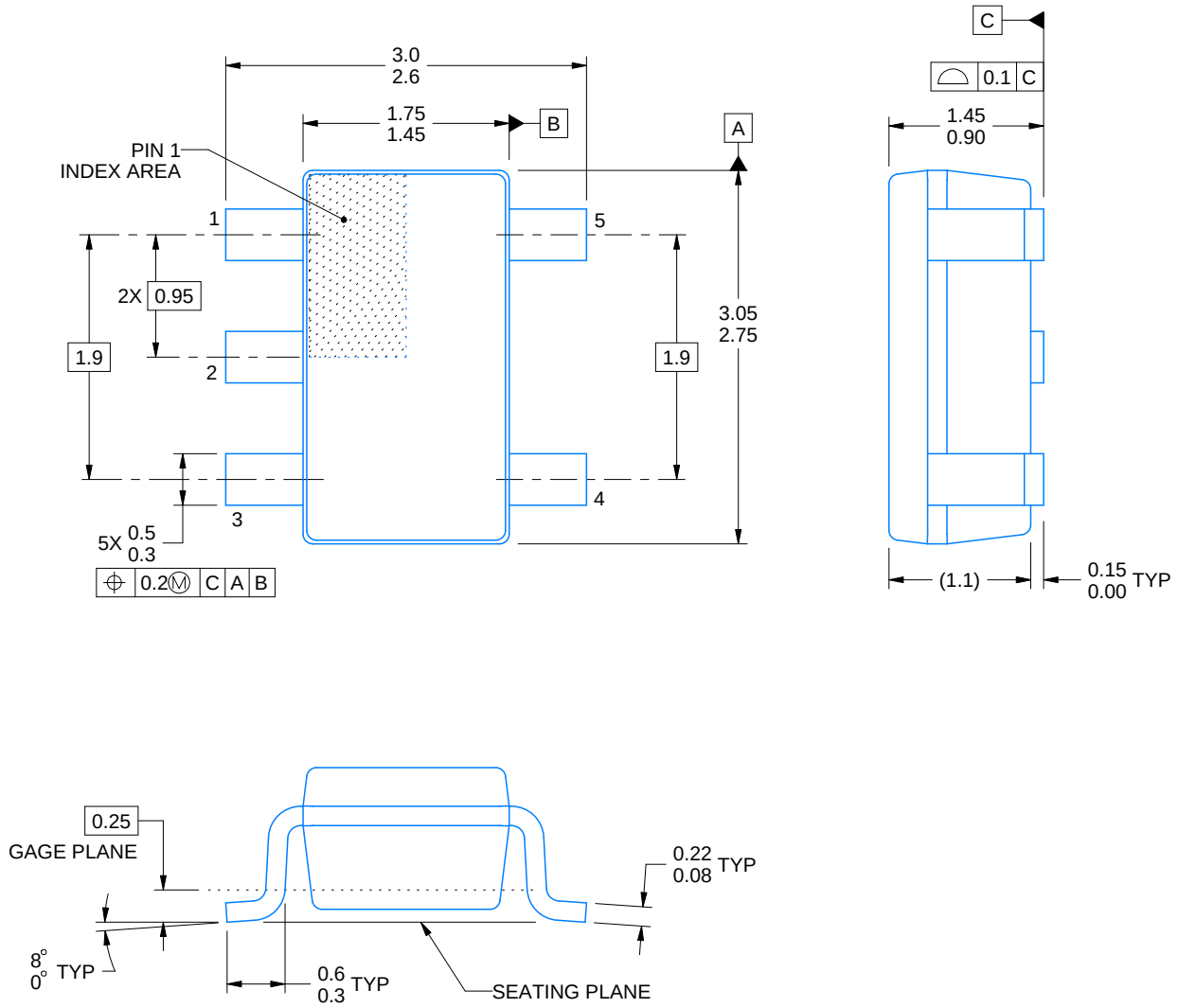
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

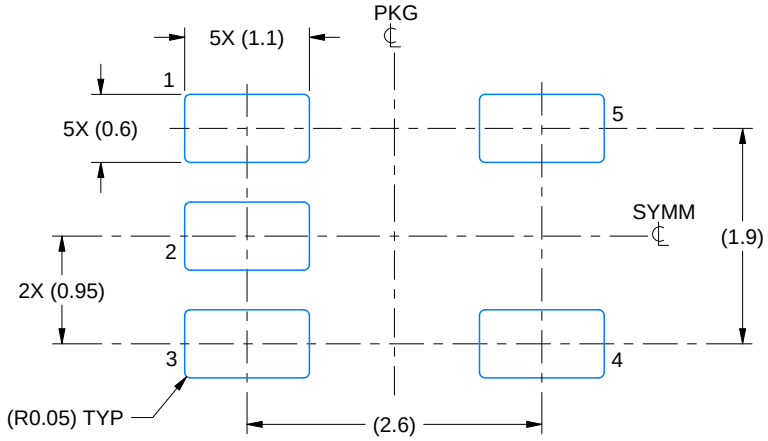
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



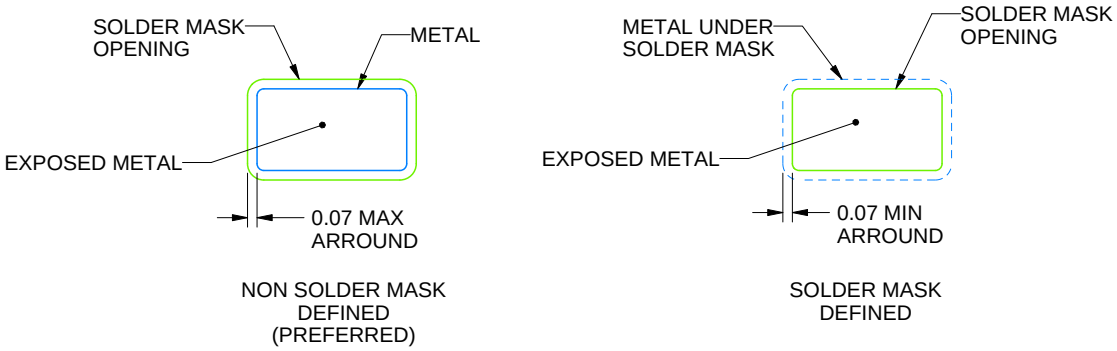
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

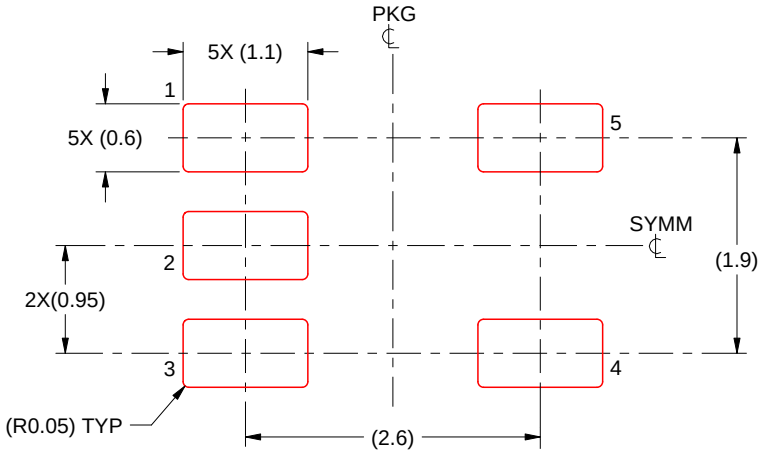


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



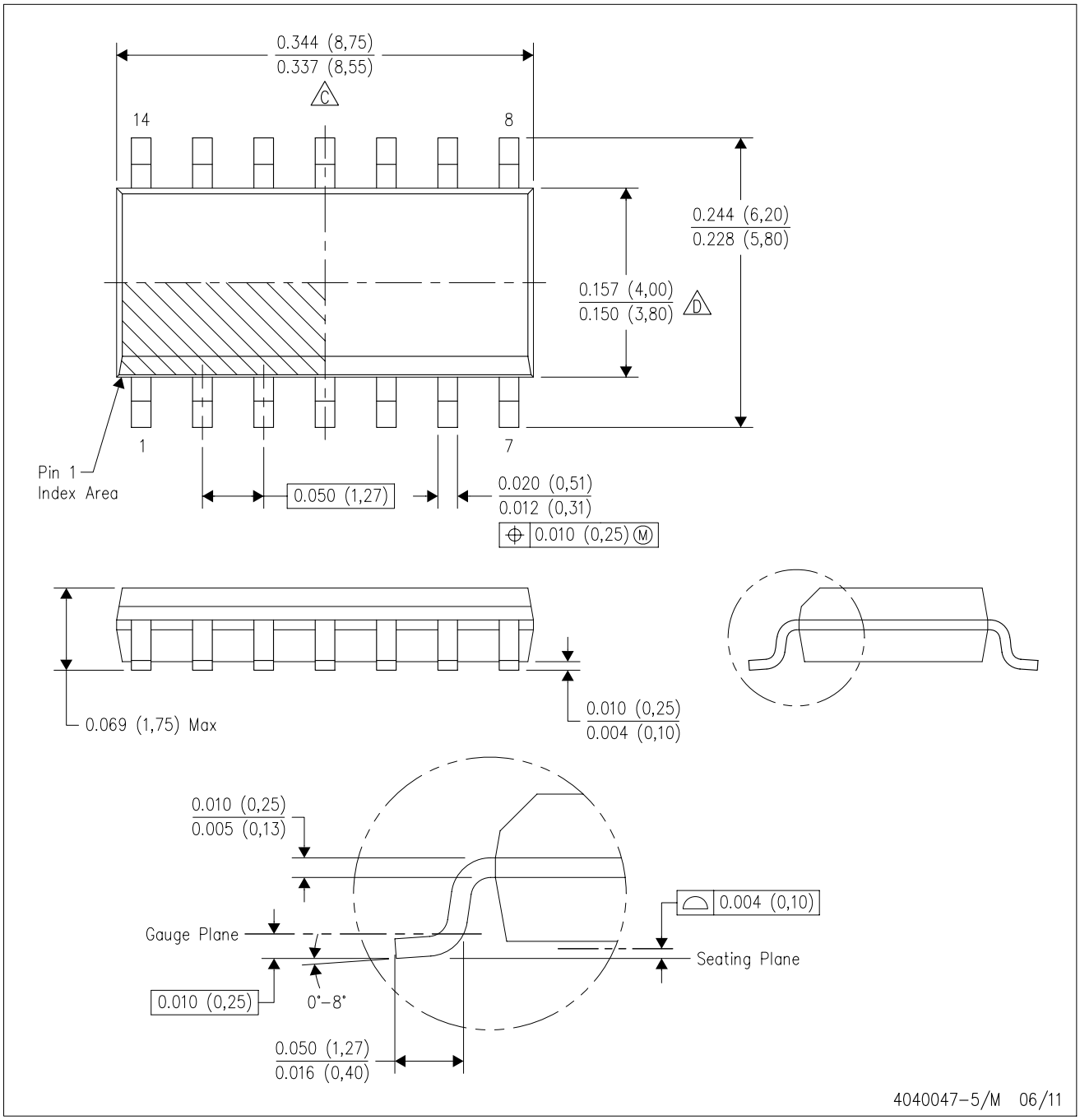
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

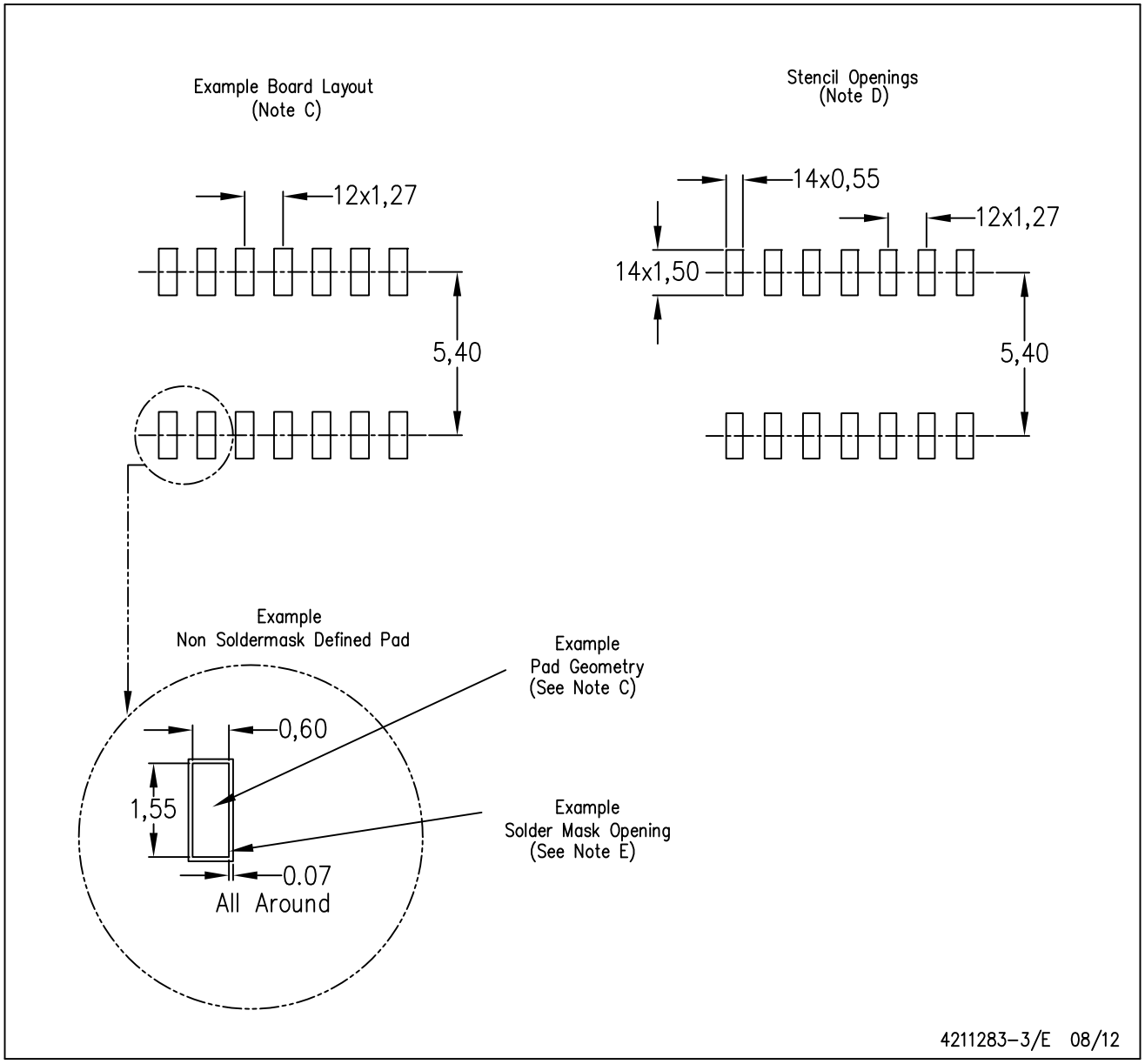
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



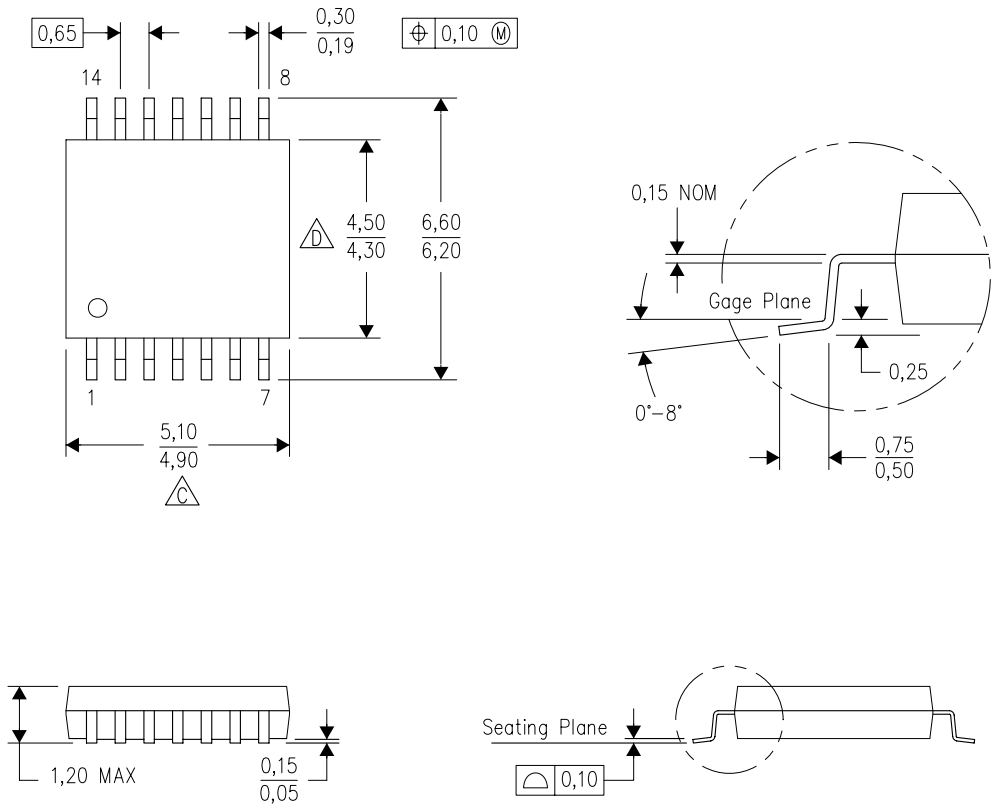
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



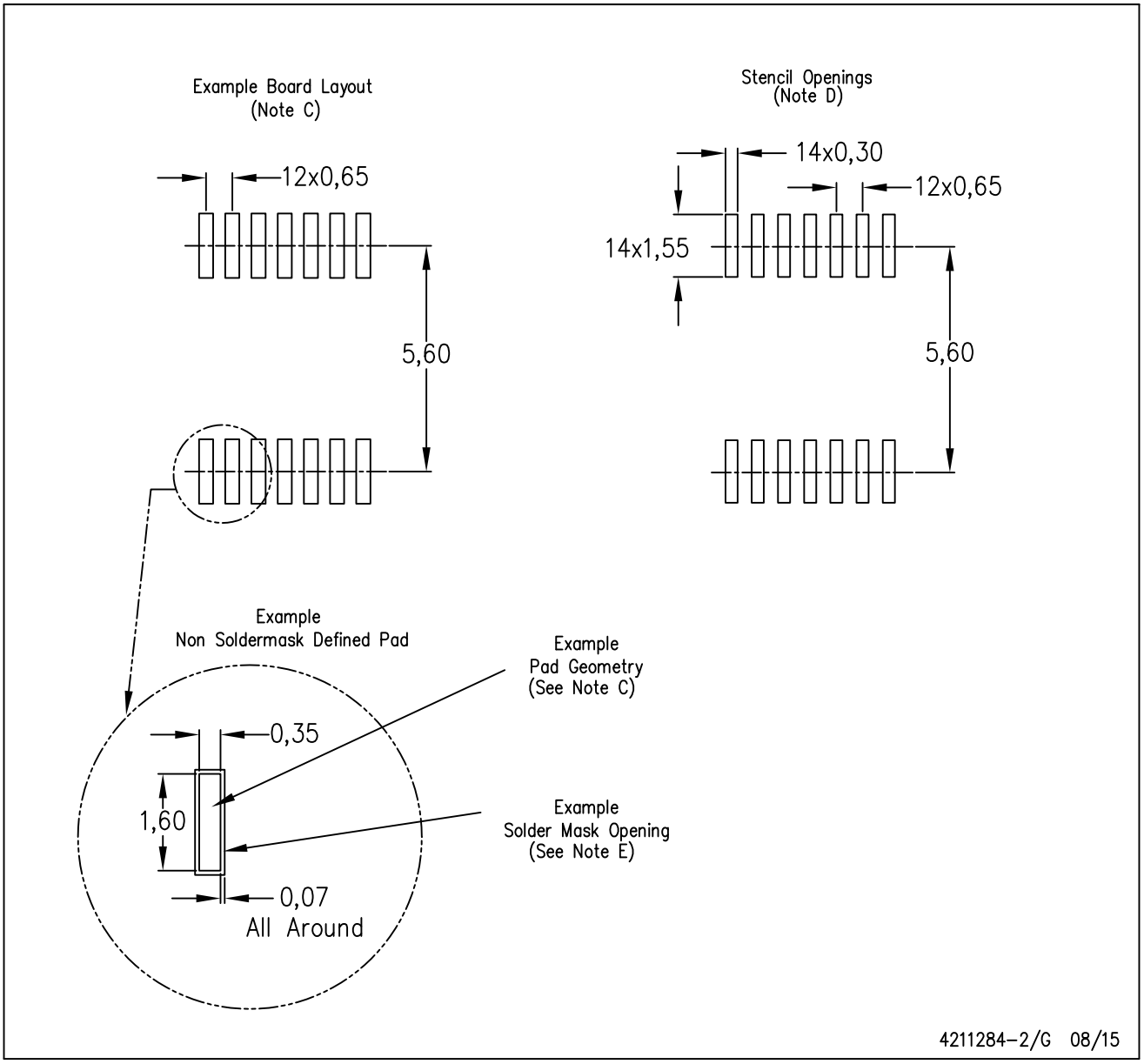
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

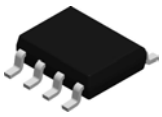


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

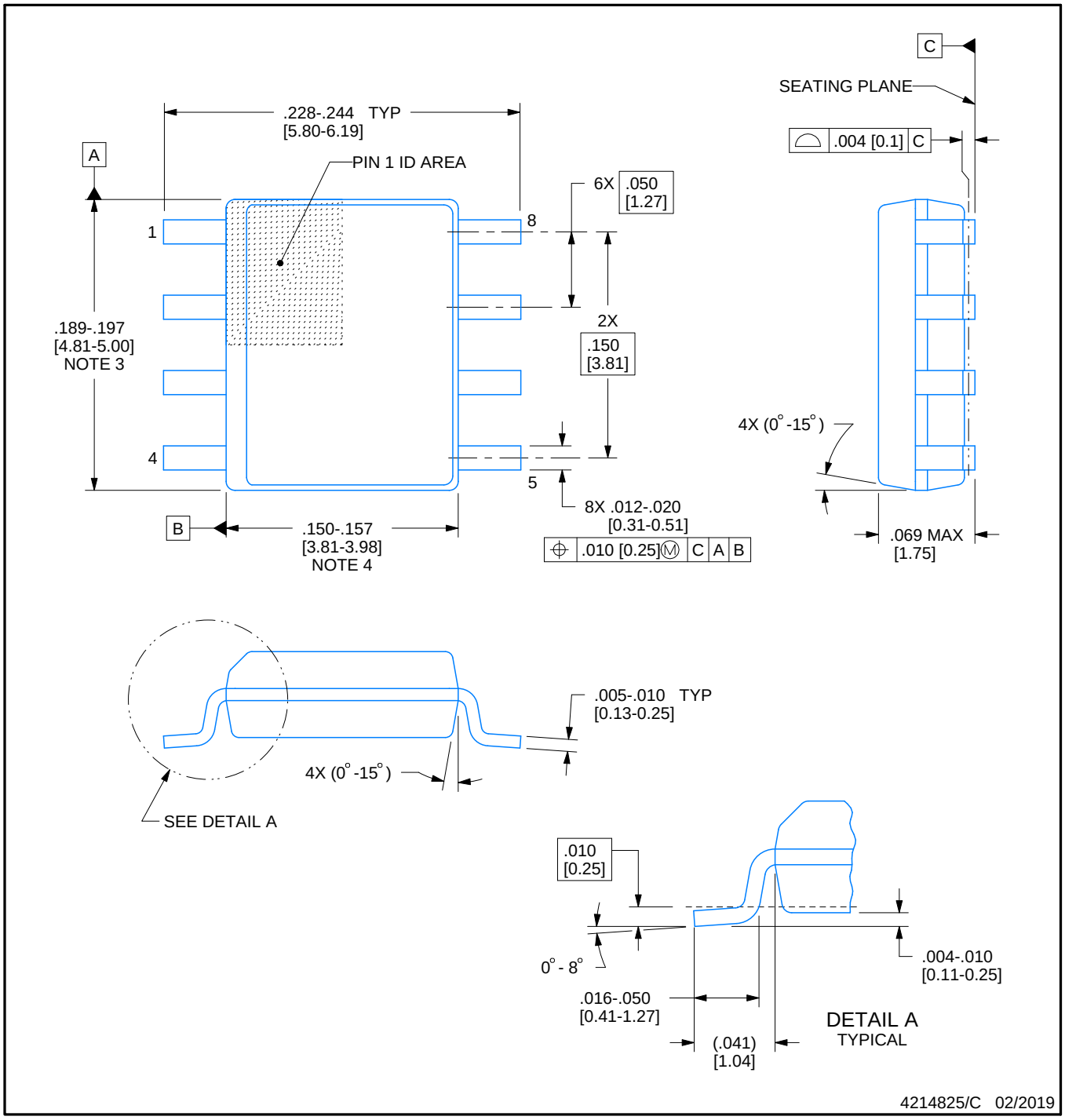


PACKAGE OUTLINE

D0008A

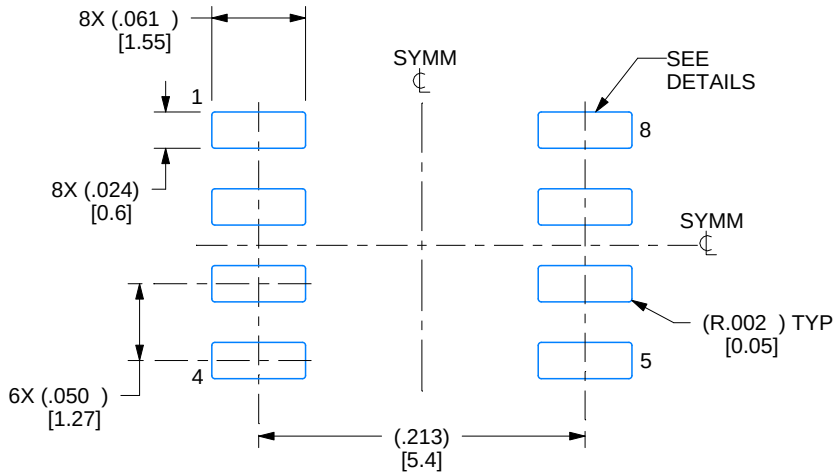
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

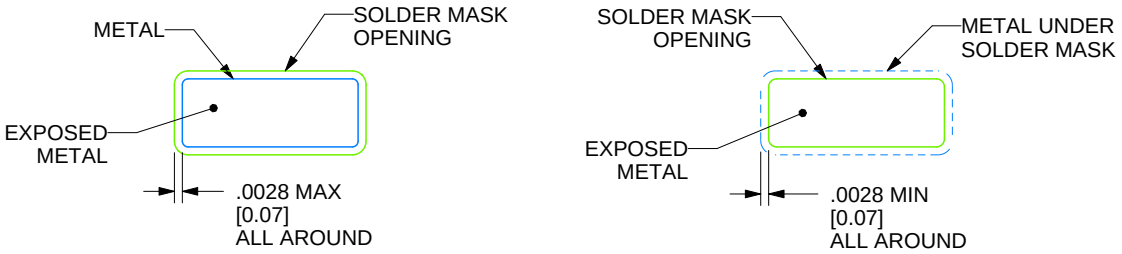


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

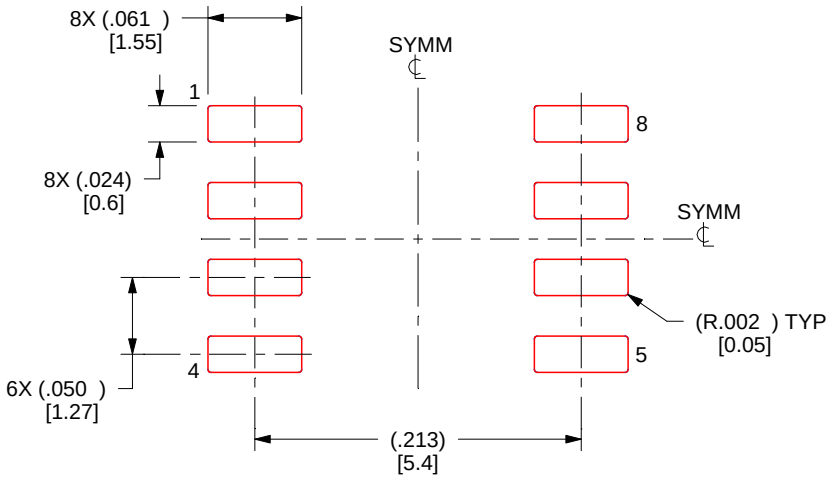


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



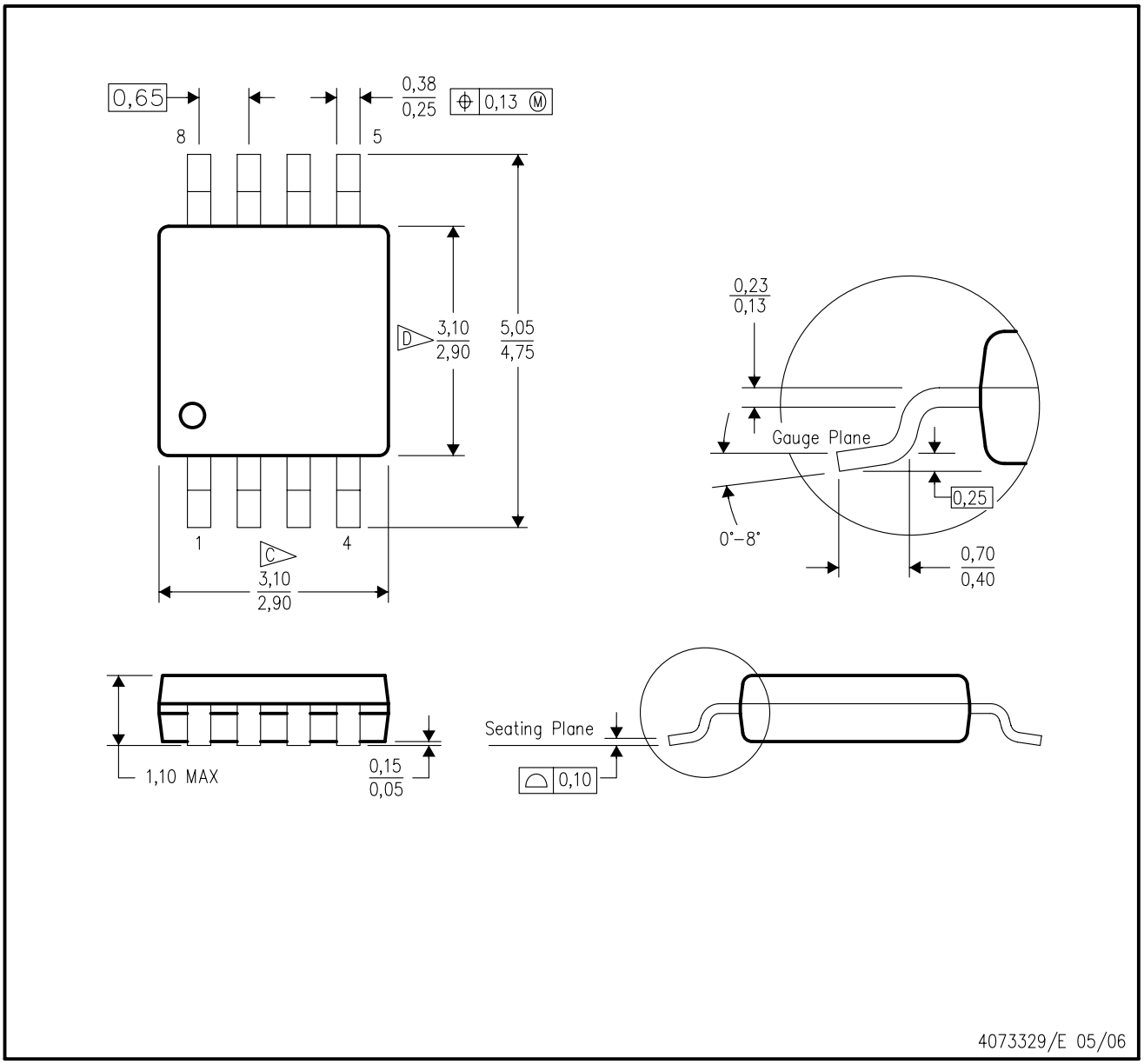
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

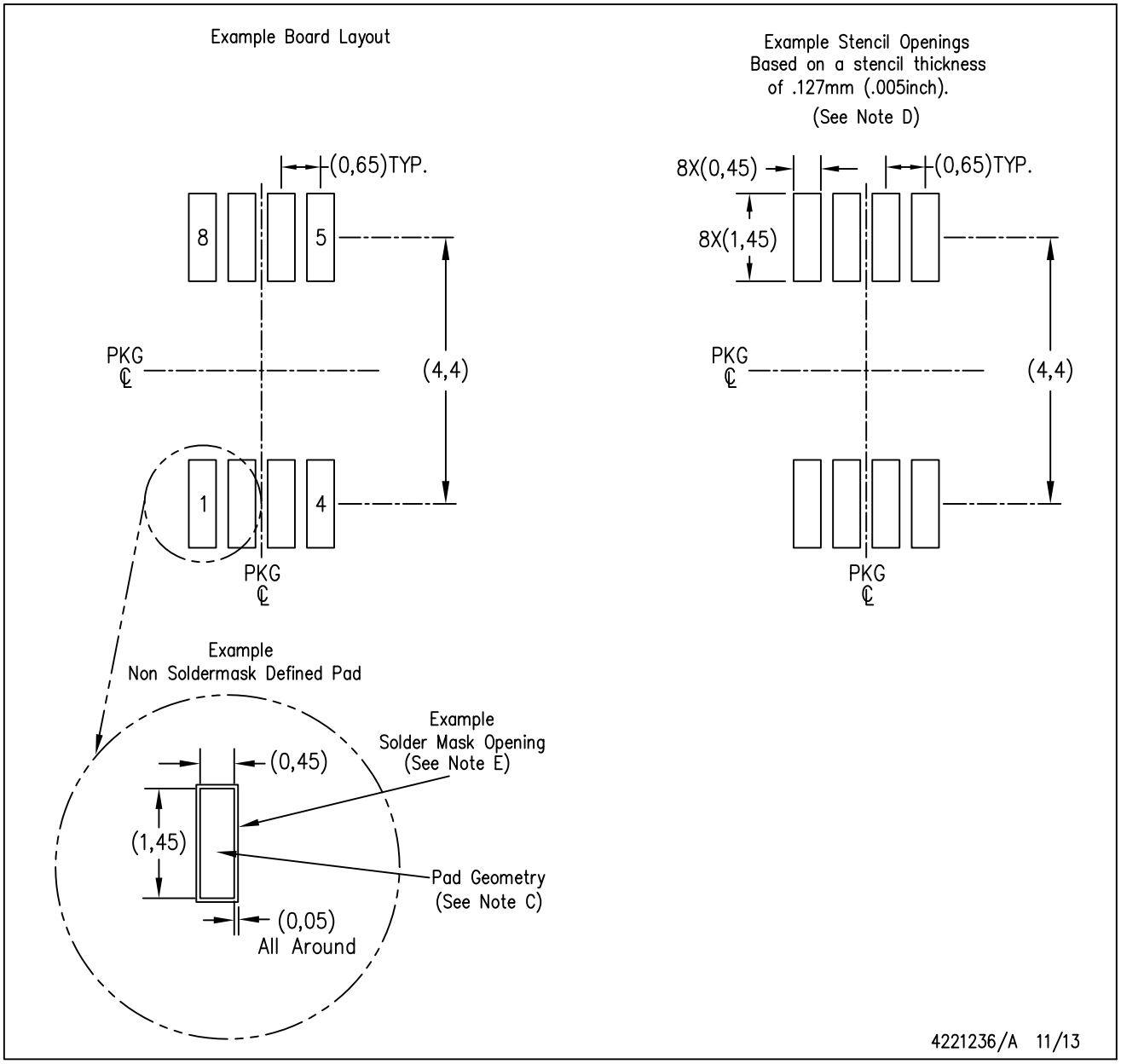
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

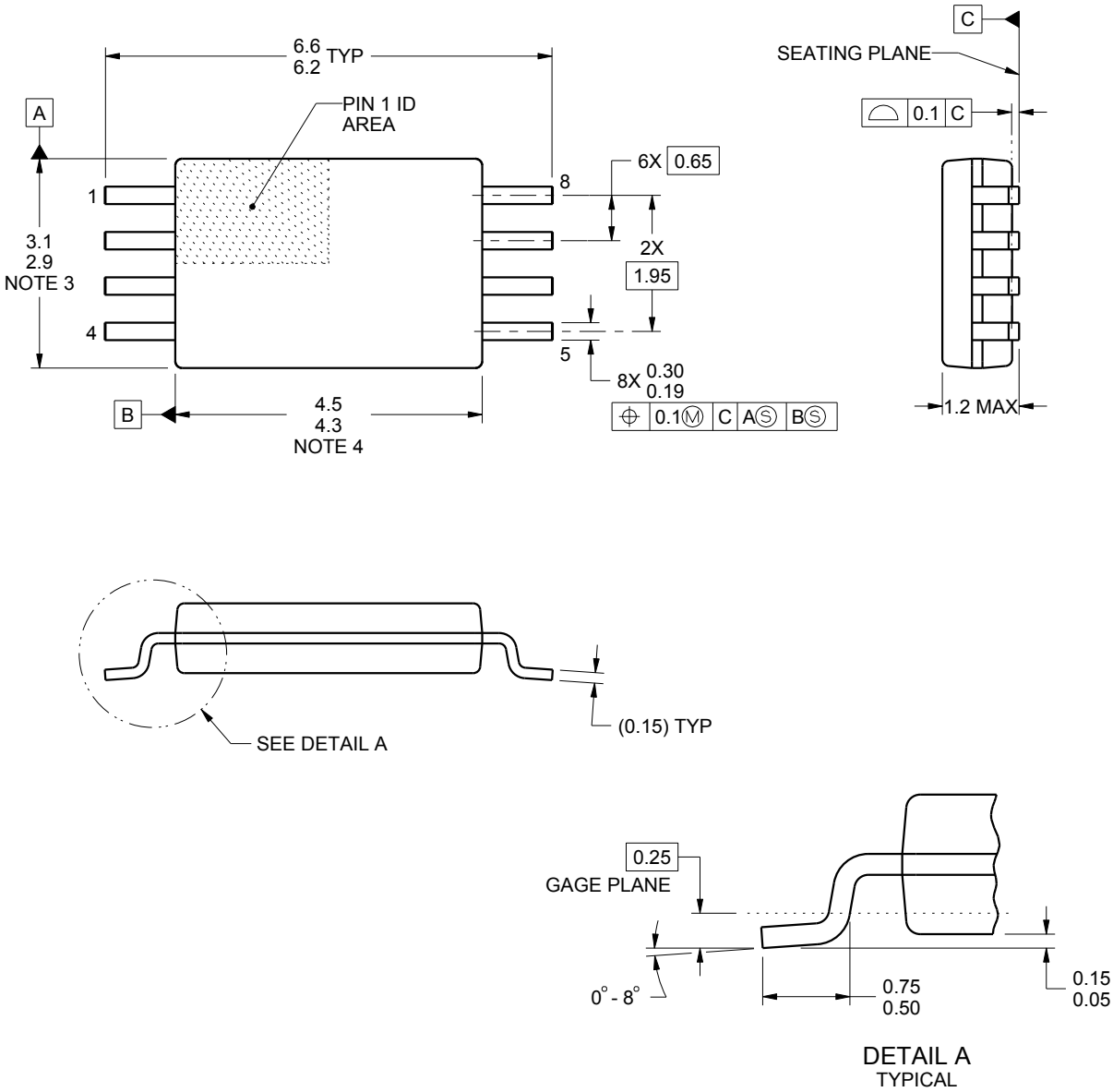


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE

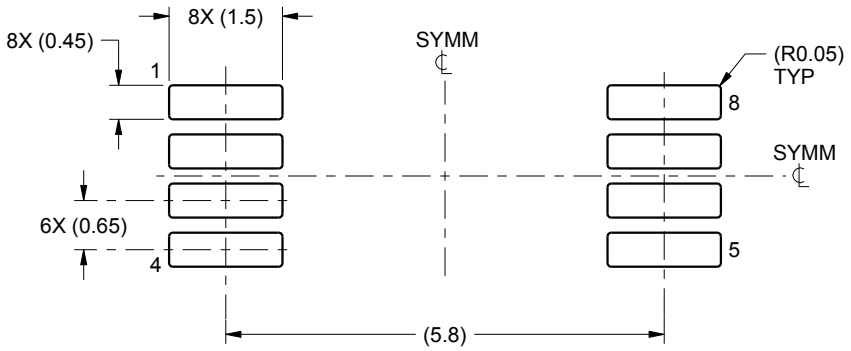


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

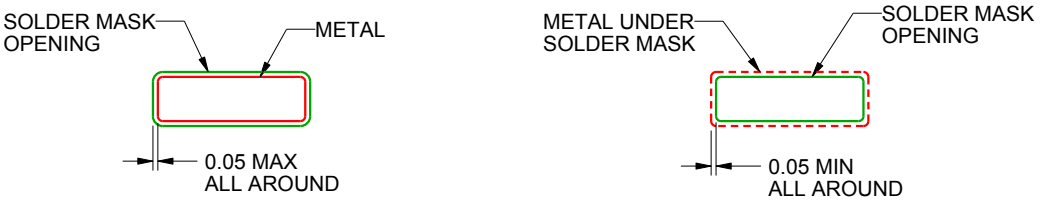


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

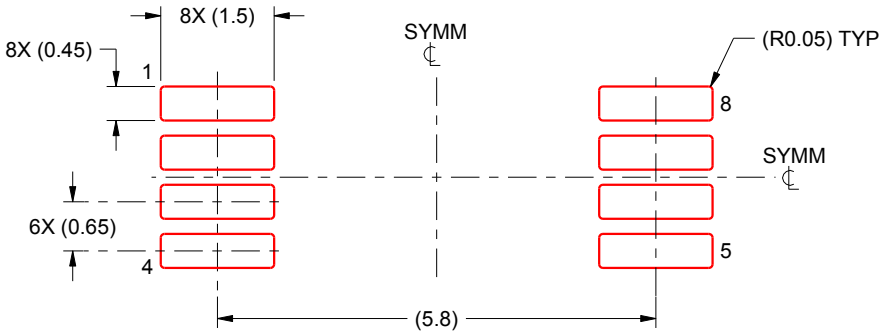
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



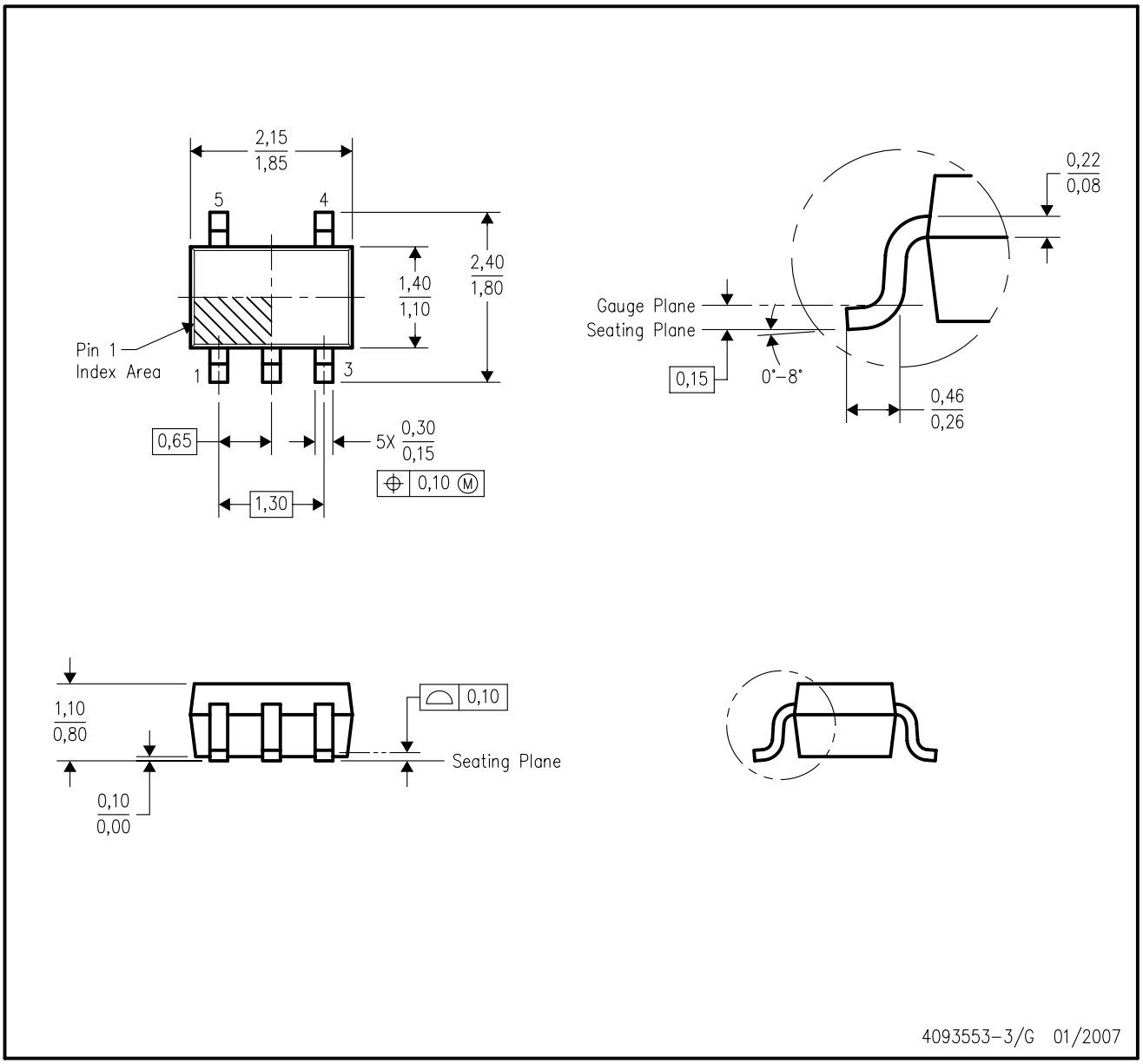
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

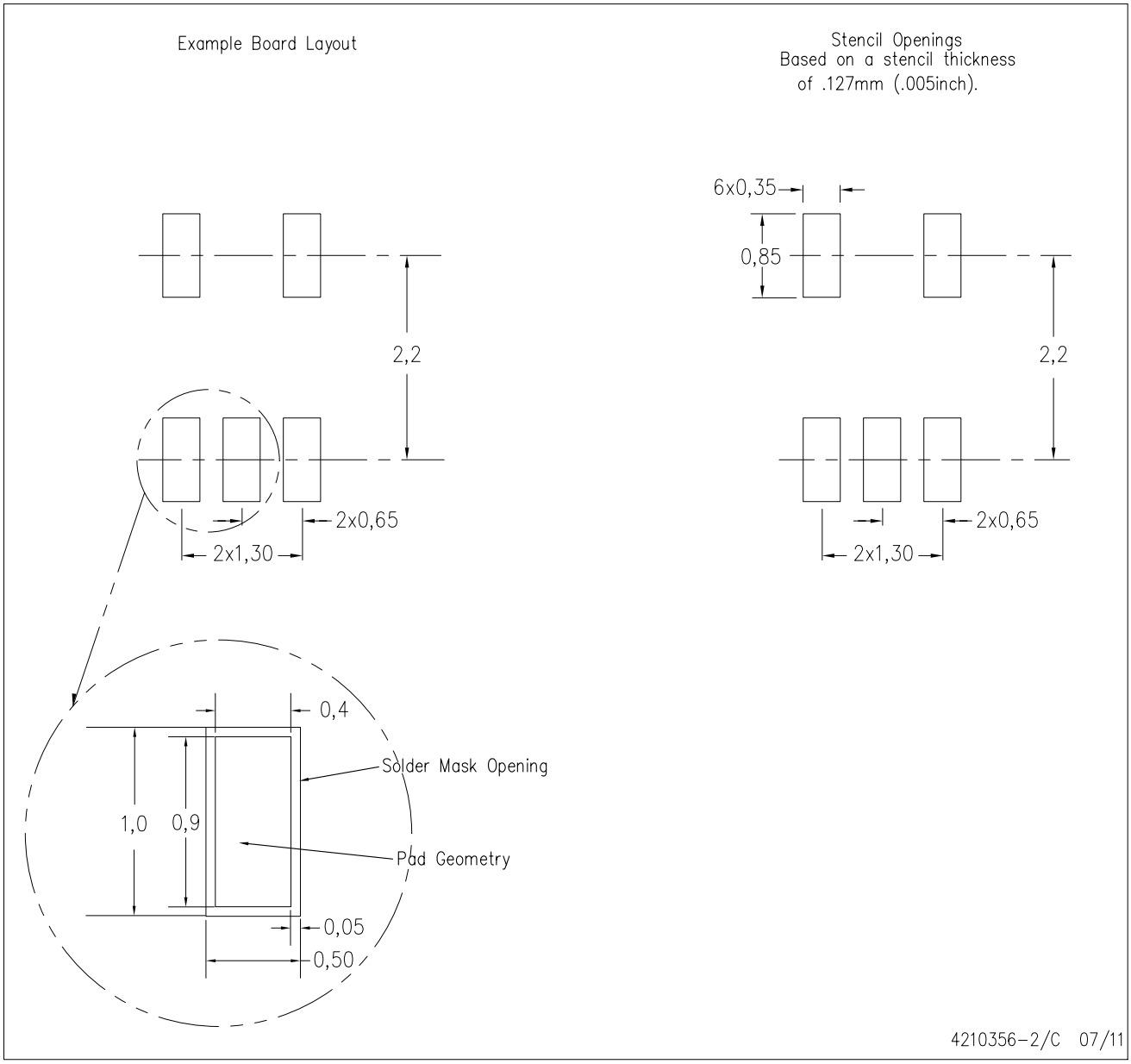
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

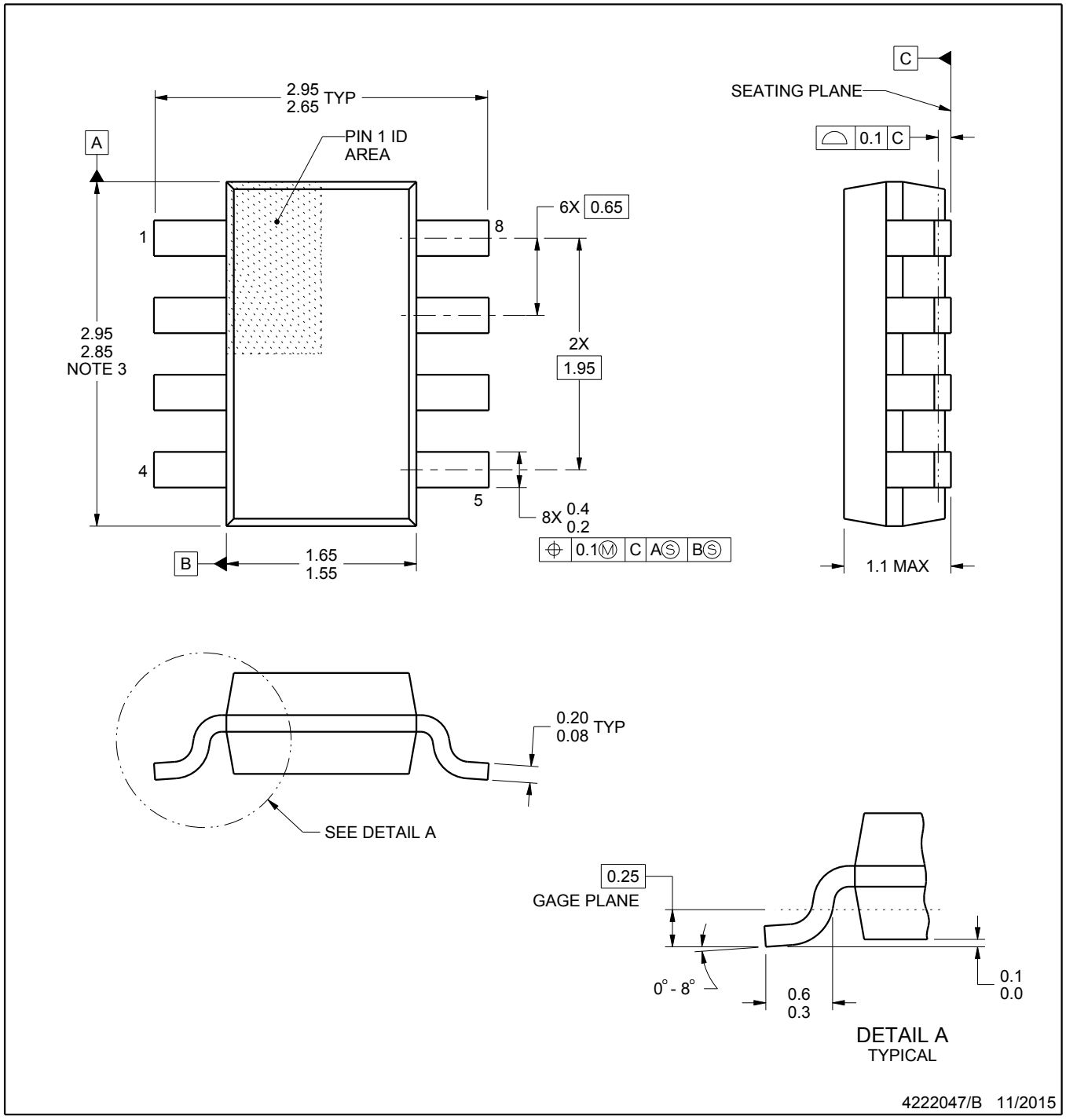


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE

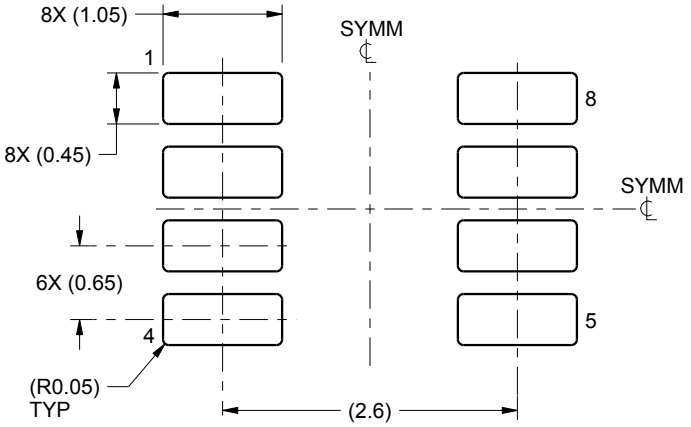


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

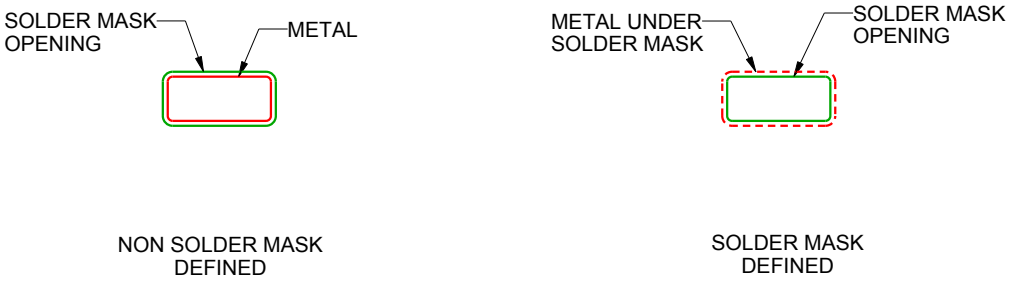


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

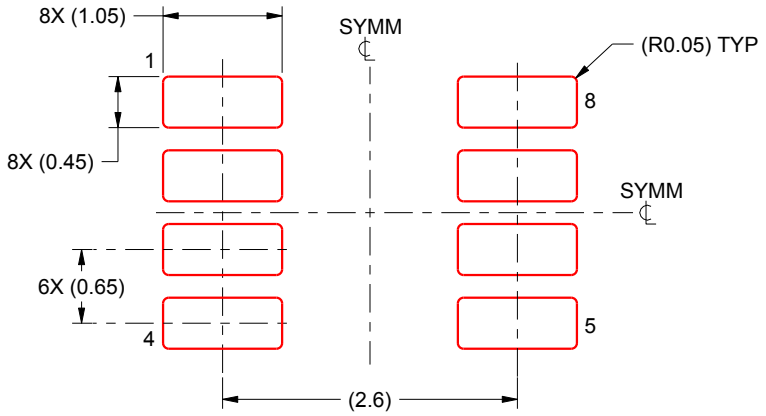


SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司