具有 SMBus 和双线制串行接口并采用 SOT563 封装的 TMP112x 高精度、低功耗数字温度传感器

1 特性

- TMP112A 不校准时的精度：
  - 0°C 至 +65°C 范围内为 0.5°C（最大值）(3.3V)
  - –40°C 至 +125°C 范围内为 1.0°C（最大值）
- TMP112B 不校准时的精度：
  - 0°C 至 +65°C 范围内为 0.5°C（最大值）(1.8V)
  - –40°C 至 +125°C 范围内为 1.0°C（最大值）
- TMP112N 不校准时的精度：
  - –40°C 至 +125°C 范围内为 1.0°C（最大值）
- SOT563 封装 (1.6mm × 1.6mm)
- 低静态电流：
  - 10μA 工作电流（最大值），1μA 关断电流（最大值）
- 电源范围：1.4V 至 3.6V
- 分辨率：12 位
- 数字输出： SMBus™、两线制和 I²C 接口兼容性
- NIST 可追溯

2 应用

- 便携式和电池供电类 应用
- 电源温度监控
- 计算机外设过热保护
- 笔记本电脑
- 电池管理
- 办公机器
- 恒温器控制
- 机电设备温度
- 通用温度测量：
  - 工业控制
  - 测试设备
  - 医疗仪器

3 说明

TMP112 系列器件是数字温度传感器，专为需要高精度的高精度低功耗 NTC/PTC 热敏电阻替代产品而设计。TMP112A 和 TMP112B 具有 0.5°C 的精度，经优化分别在 3.3V 和 1.8V 的工作电压下提供最佳 PSR 性能，而 TMP112N 则提供 1°C 的精度。这些温度传感器具有高线性度，无需复杂计算或查表即可得知温度。片载 12 位模数转换器提供的分辨率低至 0.0625°C。

1.6mm × 1.6mm SOT563 封装尺寸较 SOT23 封装减小 68%。TMP112 系列 具有 SMBus、两线制和 I²C 接口兼容性，并可在同一总线上支持多达四个器件。此外，该器件还 具备 SMBus 报警功能。器件的额定工作电压范围是 1.4V 至 3.6V，整个工作范围内最大静态电流为 10μA。

TMP112 系列专为进行扩展温度测量而设计，适用于通信、计算机、消费类产品、环境、工业和仪表 工作中运行。器件的额定工作温度范围为 –40°C 至 +125°C。

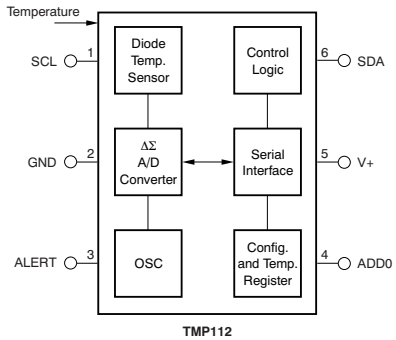
TMP112 系列生产单元已经过 100% 的传感器测试，具有 NIST 可追溯的特点，并已借助 NIST 可追溯的设备使用 ISO/IEC 17025 标准认可的校准要求进行验证。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMP112x	SOT563 (6)	1.60mm x 1.20mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

方框图



TMP112

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision H (October 2018) to Revision I — **Page**

- Changed input voltage maximum to voltage maximum for SCL, ADD0 and SDA pins ... 5
- Deleted *Absolute Maximum Ratings* for output voltage and replaced with pin level information ... 5
- Added voltage at ALERT pin *Absolute Maximum Ratings* ... 5

Changes from Revision G (May 2018) to Revision H — **Page**

- Added content to the ADD0 pin description in the *Pin Functions* table ... 3
- Changed the supply voltage maximum value in the *Absolute Maximum Ratings* table from: 5 V to: 4 V ... 5
- Changed input voltage maximum value for the SCL, ADD0, and SDA pins in the *Absolute Maximum Ratings* table from: 5 V to: 4 V ... 5
- Changed input voltage maximum value for the ALERT pin in the *Absolute Maximum Ratings* table from: (V+) + 0.5 V to: ((V+) + 0.5) and ≤ 4 V ... 5
- Changed Junction-to-ambient thermal resistance from 200 °C/W to 210.3 °C/W ... 5
- Changed Junction-to-case (top) thermal resistance from 73.7 °C/W to 105.0 °C/W ... 5
- Changed Junction-to-board thermal resistance from 34.4 °C/W to 87.5 °C/W ... 5
- Changed Junction-to-top characterization parameter from 3.1 °C/W to 6.1 °C/W ... 5
- Changed Junction-to-board characterization parameter from 34.2 °C/W to 87.0 °C/W ... 5

Changes from Revision F (February 2018) to Revision G — **Page**

- Changed long-term stability parameter to long-term drift ... 6
- Changed long-term drift test condition from: 3000 hours to: 3000 hours at 125°C ... 6
- Changed long-term drift typical value from: < 1 LSB to: ±0.0625°C ... 6

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Changes from Revision E (December 2015) to Revision F **Page**

- 在数据表中添加了 TMP112N 和 TMP112B 可订购产品 1
- Removed duplicate specified and operating temperature ranges from the *Electrical Characteristics* table 6
- Removed *Calibrating for Improved Accuracy* and *Using the Slope Specifications With a 1-Point Calibration* sections..... 23

Changes from Revision D (April 2015) to Revision E **Page**

- 添加 TI 设计 1
- 添加 NIST 特性 要点 1
- 已在*说明* 部分添加了 WQFN (RUN) 封装 1

Changes from Revision C (October 2014) to Revision D **Page**

- Changed MIN, TYP, and MAX values for the Temperature Accuracy (temperature error) parameter 6
- Changed the frequency from 2.85 to 3.4 MHz in the POWER SUPPLY section of the *Electrical Characteristics* table 6
- Changed the Temperature Error at 25°C graph in the *Typical Characteristics* section 8
- Changed the Temperature Error vs Temperature graph in the *Typical Characteristics* section 8

Changes from Revision B (June 2009) to Revision C **Page**

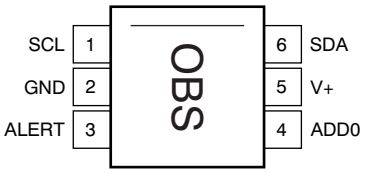
- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 5
- Changed parameters in *Timing Requirements* 7

Changes from Revision A (March 2009) to Revision B **Page**

- Changed footnote 1 of *Specifications for User-Calibrated Systems* table 23
- Clarified Example 1; extended worst-case accuracy to be from –15°C to +50°C 23
- Changed equation in *Using the Slope Specifications With a 1-Point Calibration* 23

5 Pin Configuration and Functions

DRL Package
6-Pin SOT563
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
2	GND	—	Ground
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	ADD0	I	Address Select. Connect to V+, GND, SDA or SCL

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
5	V+	I	Supply voltage, 1.4 V to 3.6 V
6	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V+		4	V
Voltage at SCL, ADD0, and SDA		–0.5	4	V
Voltage at ALERT		–0.5	((V+) + 0.3) and ≤ 4	V
Operating temperature		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.4	3.3	3.6	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP112 DRL (SOT563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	105.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

At T_A = +25°C and V_S = +1.4V to +3.6V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT							
	Temperature range			–40		+125	°C
	Accuracy (temperature error)	TMP112A	+25°C, V+ = 3.3 V		±0.1	±0.5	°C
			0°C to +65°C, V+ = 3.3 V		±0.25	±0.5	
			–40°C to +125°C		±0.5	±1	
		TMP112B	+25°C, V+ = 1.8 V		±0.1	±0.5	
			0°C to +65°C, V+ = 1.8 V		±0.25	±0.5	
			–40°C to +125°C		±0.5	±1	
		TMP112N	–40°C to +125°C			±1	
	DC power-supply sensitivity		–40°C to +125°C		0.0625	±0.25	°C/V
	Long-term drift (1)		3000 hours at 125°C		±0.0625		°C
	Resolution (LSB)				0.0625		°C
DIGITAL INPUT/OUTPUT							
	Input capacitance				3		pF
V_{IH}	Input logic level			0.7 (V+)		3.6	V
V_{IL}				–0.5		0.3 (V+)	
I_{IN}	Input current		0 < V_{IN} < 3.6 V			1	µA
V_{OL} SDA	Output logic level		V+ > 2 V, I_{OL} = 3 mA	0		0.4	V
			V+ < 2 V, I_{OL} = 3 mA	0		0.2 (V+)	
V_{OL} ALERT			V+ > 2 V, I_{OL} = 3 mA	0		0.4	V
			V+ < 2 V, I_{OL} = 3 mA	0		0.2 (V+)	
	Resolution				12		Bits
	Conversion time				26	35	ms
	Conversion modes		CR1 = 0, CR0 = 0		0.25		Conv/s
			CR1 = 0, CR0 = 1		1		
			CR1 = 1, CR0 = 0 (default)		4		
			CR1 = 1, CR0 = 1		8		
	Timeout time				30	40	ms
POWER SUPPLY							
	Operating supply range			+1.4		+3.6	V
I_Q	Average quiescent current		Serial bus inactive, CR1 = 1, CR0 = 0 (default)		7	10	µA
			Serial bus active, SCL frequency = 400 kHz		15		
			Serial bus active, SCL frequency = 3.4 MHz		85		
I_{SD}	Shutdown current		Serial bus inactive		0.5	1	µA
			Serial bus active, SCL frequency = 400 kHz		10		
			Serial bus active, SCL frequency = 3.4 MHz		80		

(1) Long-term drift is determined using accelerated operational life testing at a junction temperature of 150°C for 1000 hours.

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6.6 Timing Requirements

See the *Two-Wire Timing Diagrams* section for timing diagrams.

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.85	MHz
$t_{(BUF)}$	Bus-free time between STOP and START condition	See Figure 10	600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	repeated start condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time		100	900	25	105	ns
$t_{(SUDAT)}$	Data setup time		100		25		ns
$t_{(LOW)}$	SCL-clock low period	V+ , see Figure 10	1300		210		ns
$t_{(HIGH)}$	SCL-clock high period	See Figure 10	600		60		ns
t_{FD}	Data fall time	See Figure 10		300		80	ns
t_{RD}	Data rise time	See Figure 10		300			ns
		SCLK ≤ 100 kHz, see Figure 10		1000			ns
t_{FC}	Clock fall time	See Figure 10		300		40	ns
t_{RC}	Clock rise time	See Figure 10		300		40	ns

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6.7 Typical Characteristics

At T_A = +25°C and V+ = 3.3 V, unless otherwise noted.

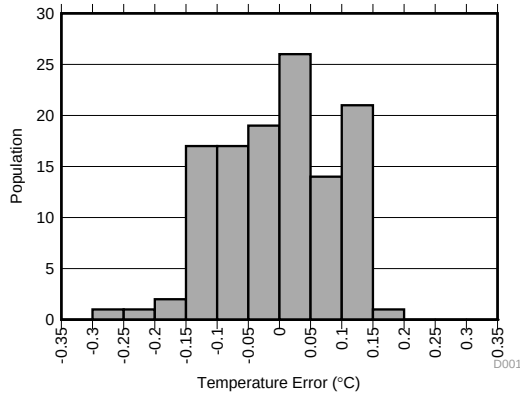


Figure 1. Temperature Error at 25°C

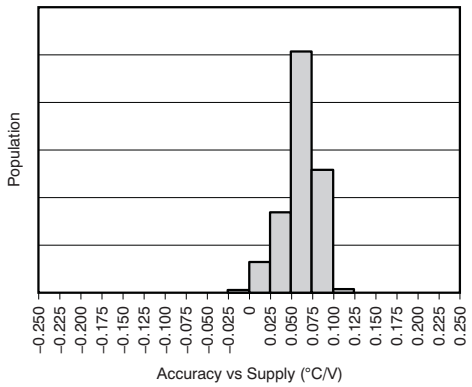


Figure 2. Accuracy vs Supply

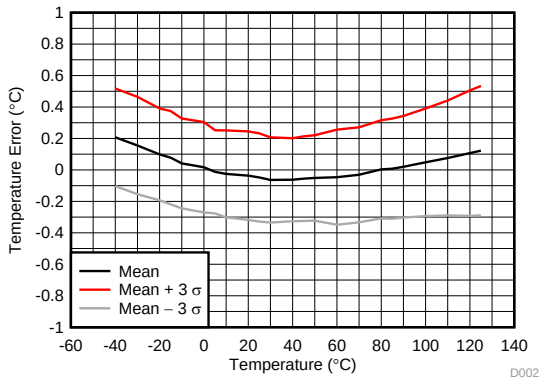


Figure 3. Temperature Error vs Temperature

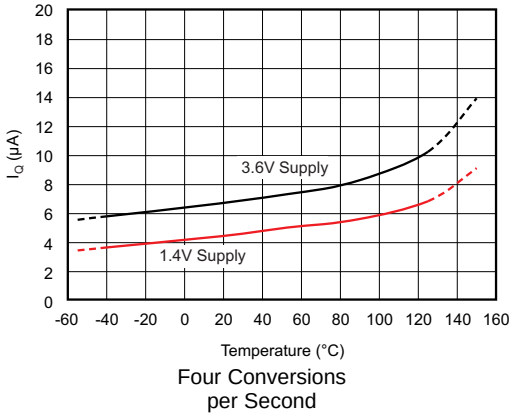


Figure 4. Average Quiescent Current vs Temperature

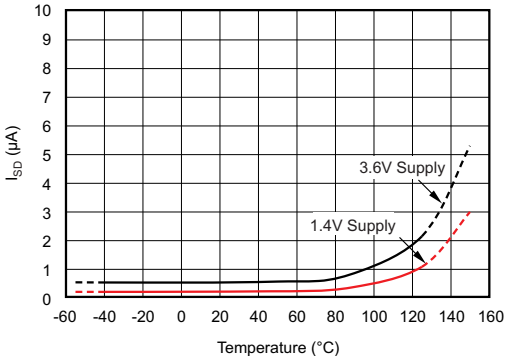


Figure 5. Shutdown Current vs Temperature

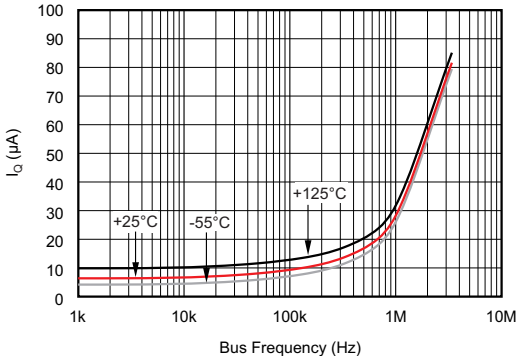


Figure 6. Quiescent Current vs Bus Frequency (Temperature at 3.3-V Supply)

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Typical Characteristics (continued)

At T_A = +25°C and V+ = 3.3 V, unless otherwise noted.

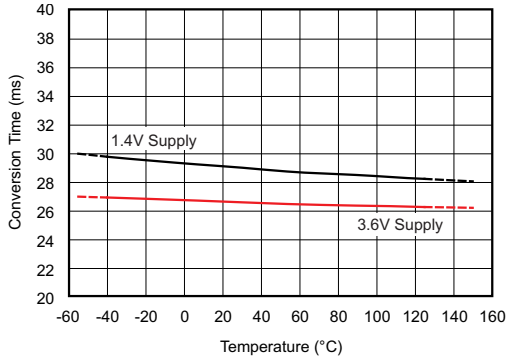


Figure 7. Conversion Time vs Temperature

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7 Detailed Description

7.1 Overview

The TMP112 family of devices are digital temperature sensors that are optimal for thermal-management and thermal-protection applications. The TMP112 family is two-wire, SMBus, and I^2C interface-compatible. The device is specified over an operating temperature range of –40°C to 125°C. Figure 8 shows a block diagram of the TMP112 family. Figure 9 shows the ESD protection circuitry contained in the TMP112 family.

The temperature sensor in the TMP112 family is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

An alternative version of the TMP112 family is available. The TMP102 device has reduced accuracy, the same micro-package, and is pin-to-pin compatible.

Table 1. Advantages of TMP112 family Versus TMP102

DEVICE	COMPATIBLE INTERFACES	PACKAGE	SUPPLY CURRENT	SUPPLY VOLTAGE (MIN)	SUPPLY VOLTAGE (MAX)	RESOLUTION	LOCAL SENSOR ACCURACY (MAX)	SPECIFIED CALIBRATION DRIFT SLOPE
TMP112 family	I^2C SMBus	SOT563 1.2 × 1.6 × 0.6	10 µA	1.4 V	3.6 V	12 Bit 0.0625°C	0.5°C: (0°C to 65°C) 1°C: (-40°C to 125°C)	Yes
TMP102	I^2C SMBus	SOT563 1.2 × 1.6 × 0.6	10 µA	1.4 V	3.6 V	12 Bit 0.0625°C	2°C: (25°C to 85°C) 3°C: (-40°C to 125°C)	No

7.2 Functional Block Diagrams

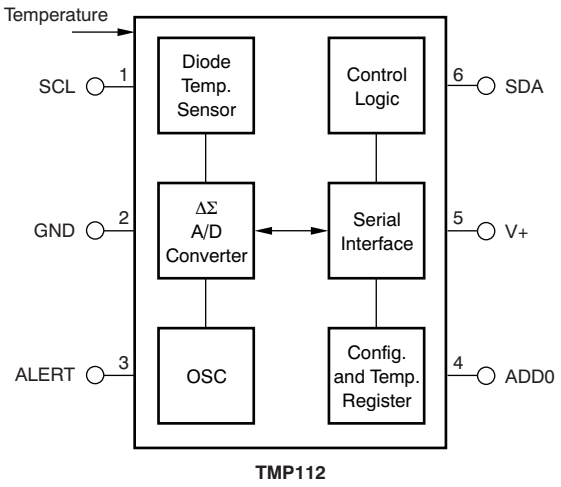


Figure 8. Internal Block Diagram

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Functional Block Diagrams (continued)

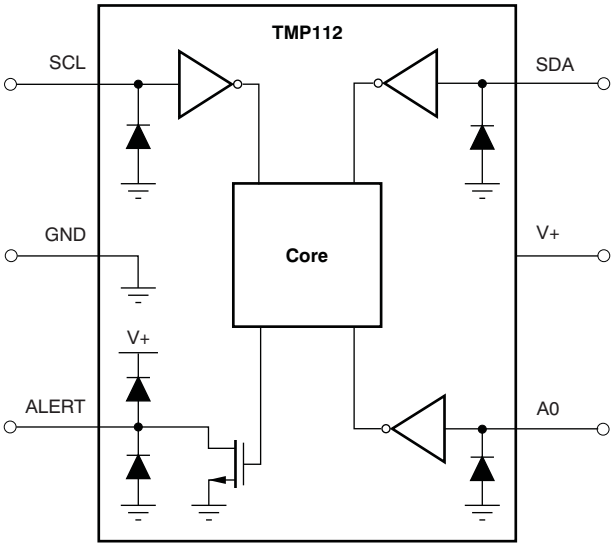


Figure 9. Equivalent Internal ESD Circuitry

7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only temperature register. The temperature register of the TMP112 family is configured as a 12-bit read-only register (setting the EM bit to 0 in the configuration register; see the *Extended Mode (EM)* section), or as a 13-bit read-only register (setting the EM bit to 1 in the configuration register) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 8 and Table 9. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is listed in Table 2 and Table 3. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format. Following power up or reset, the temperature register reads 0°C until the first conversion is complete. Bit D0 of byte 2 indicates normal mode (EM bit equals 0) or extended mode (EM bit equals 1), and can be used to distinguish between the two temperature register data formats. The unused bits in the temperature register always read 0.

Table 2. 12-Bit Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

(1) The resolution for the Temperature ADC in Internal Temperature mode is 0.0625°C/count.

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Table 2 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:

1. Divide the temperature by the resolution
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

   Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

   Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

   Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

   Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

1. Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

   Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

   Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

Table 3. 13-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
150	0 1001 0110 0000	0960
128	0 1000 0000 0000	0800
127.9375	0 0111 1111 1111	07FF
100	0 0110 0100 0000	0640
80	0 0101 0000 0000	0500
75	0 0100 1011 0000	04B0
50	0 0011 0010 0000	0320
25	0 0001 1001 0000	0190
0.25	0 0000 0000 0100	0004
0	0 0000 0000 0000	0000
–0.25	1 1111 1111 1100	1FFC
–25	1 1110 0111 0000	1E70
–55	1 1100 1001 0000	1C90

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7.3.2 Serial Interface

The TMP112 family operates as a slave device only on the SMBus, two-wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP112 family supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 2.85 MHz) modes. All data bytes are transmitted MSB first..

7.3.2.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a high- to low-logic level when the SCL pin is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and pulling the SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer the SDA pin must remain stable when the SCL pin is high, because any change in the SDA pin when the SCL pin is high is interpreted as a START or STOP signal.

When all data have been transferred, the master generates a STOP condition indicated by pulling the SDA pin from low to high when the SCL pin is high.

7.3.2.2 Serial Bus Address

To communicate with the device, the master must first address slave devices through a slave-address byte. The slave-address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP112 family features an address pin to allow up to four devices to be addressed on a single bus. Table 4 describes the pin logic levels used to properly connect up to four devices.

Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

7.3.2.3 Writing and Reading Operation

Accessing a particular register on the TMP112 family is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP112 family requires a value for the pointer register (see Figure 11).

When reading from the TMP112 family, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave-address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 12 for details of this sequence. If repeated reads from the same register are desired, continuously sending the pointer register bytes is not necessary because the TMP112 family retains the pointer register value until the value is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.

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7.3.2.4 Slave Mode Operations

The TMP112 family can operate as a slave receiver or slave transmitter. As a slave device, the TMP112 family never drives the SCL line.

7.3.2.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address with the R/$\overline{W}$ bit low. The TMP112 family then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP112 family then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP112 family acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

7.3.2.4.2 Slave Transmitter Mode

The first byte transmitted by the master is the slave address with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *not-acknowledge* on reception of any data byte or by generating a START or STOP condition.

7.3.2.5 SMBus Alert Function

The TMP112 family supports the SMBus alert function. When the TMP112 family operates in interrupt mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a master senses that an alert condition is present on the alert line, the master sends an SMBus ALERT command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus ALERT command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the alert condition is caused by the temperature exceeding $T_{(HIGH)}$ or falling below $T_{(LOW)}$. The LSB is high if the temperature is greater than $T_{(HIGH)}$, or low if the temperature is less than $T_{(LOW)}$. Refer to the Figure 13 section for details of this sequence.

If multiple devices on the bus respond to the SMBus ALERT command, arbitration during the slave address portion of the SMBus ALERT command determines which device clears the alert status of that device. The device with the lowest two-wire address wins the arbitration. If the TMP112 family wins the arbitration, the TMP112 family ALERT pin becomes inactive at the completion of the SMBus ALERT command. If the TMP112 family loses the arbitration, the TMP112 family ALERT pin remains active.

7.3.2.6 General Call

The TMP112 family responds to a two-wire general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP112 family internal registers are reset to power-up values. The TMP112 family does not support the general-address acquire command.

7.3.2.7 High-Speed (Hs) Mode

For the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP112 family does not acknowledge this byte, but switches the input filters on the SDA and SCL pins and the output filters on the SDA pin to operate in Hs-mode, thus allowing transfers at up to 2.85 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP112 family switches the input and output filters back to fast-mode operation.

7.3.2.8 Timeout Function

The TMP112 family resets the serial interface if the SCL pin is held low for 30 ms (typical) between a start and stop condition. The TMP112 family releases the SDA line if the SCL pin is pulled low and waits for a start condition from the host controller. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for SCL operating frequency.

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7.3.2.9 Timing Diagrams

The TMP112 family is two-wire, SMBus and I²C interface-compatible. Figure 10 to Figure 13 describe the various operations on the TMP112 family. Parameters for Figure 10 are defined in *Timing Requirements*. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, when the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The TMP112 family can also be used for single byte updates. To update only the MS byte, terminate the communication by issuing a START or STOP communication on the bus.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *Not-Acknowledge* ('1') on the last byte that has been transmitted by the slave.

7.3.2.9.1 Two-Wire Timing Diagrams

See the *Timing Requirements*.

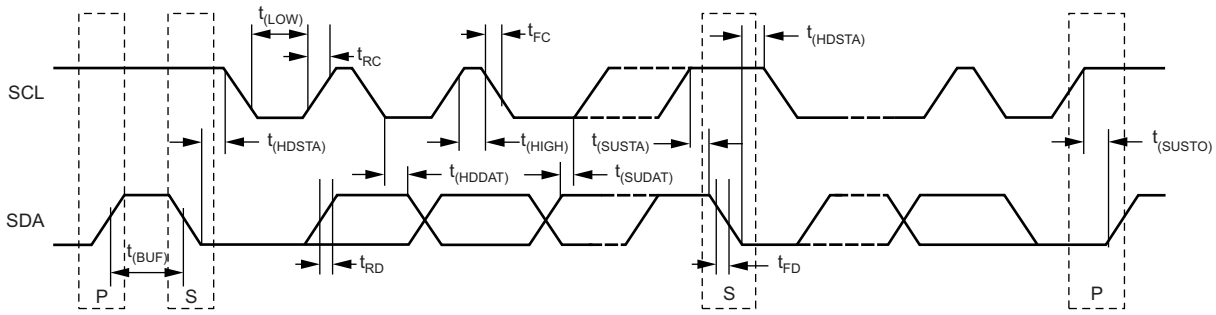
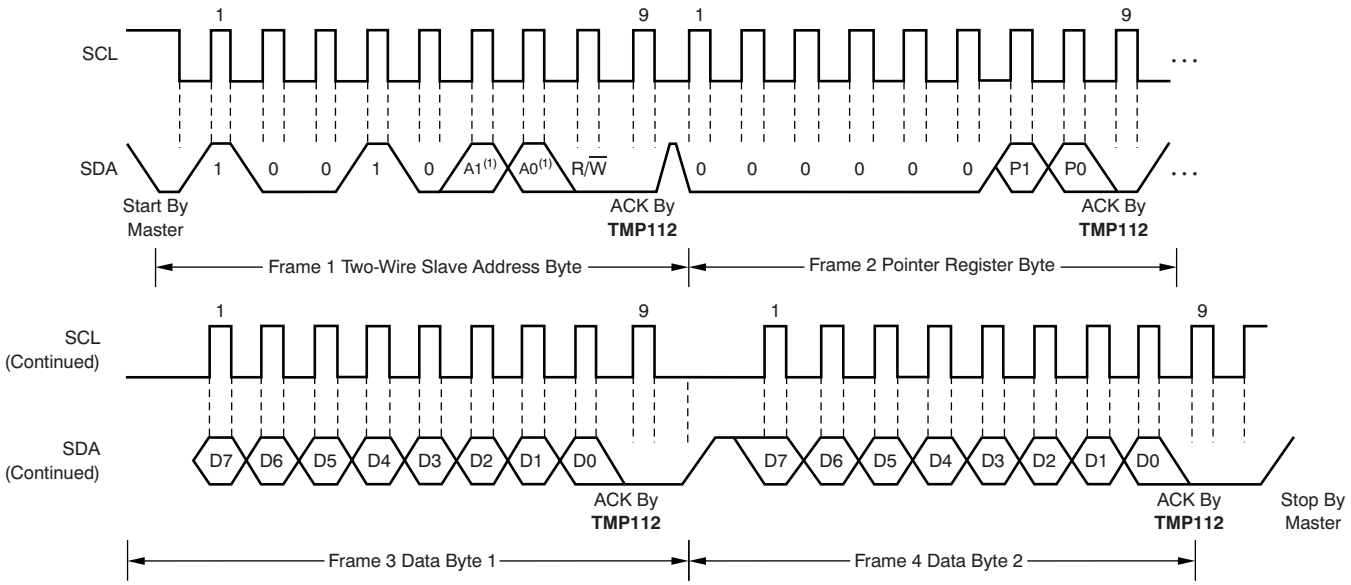


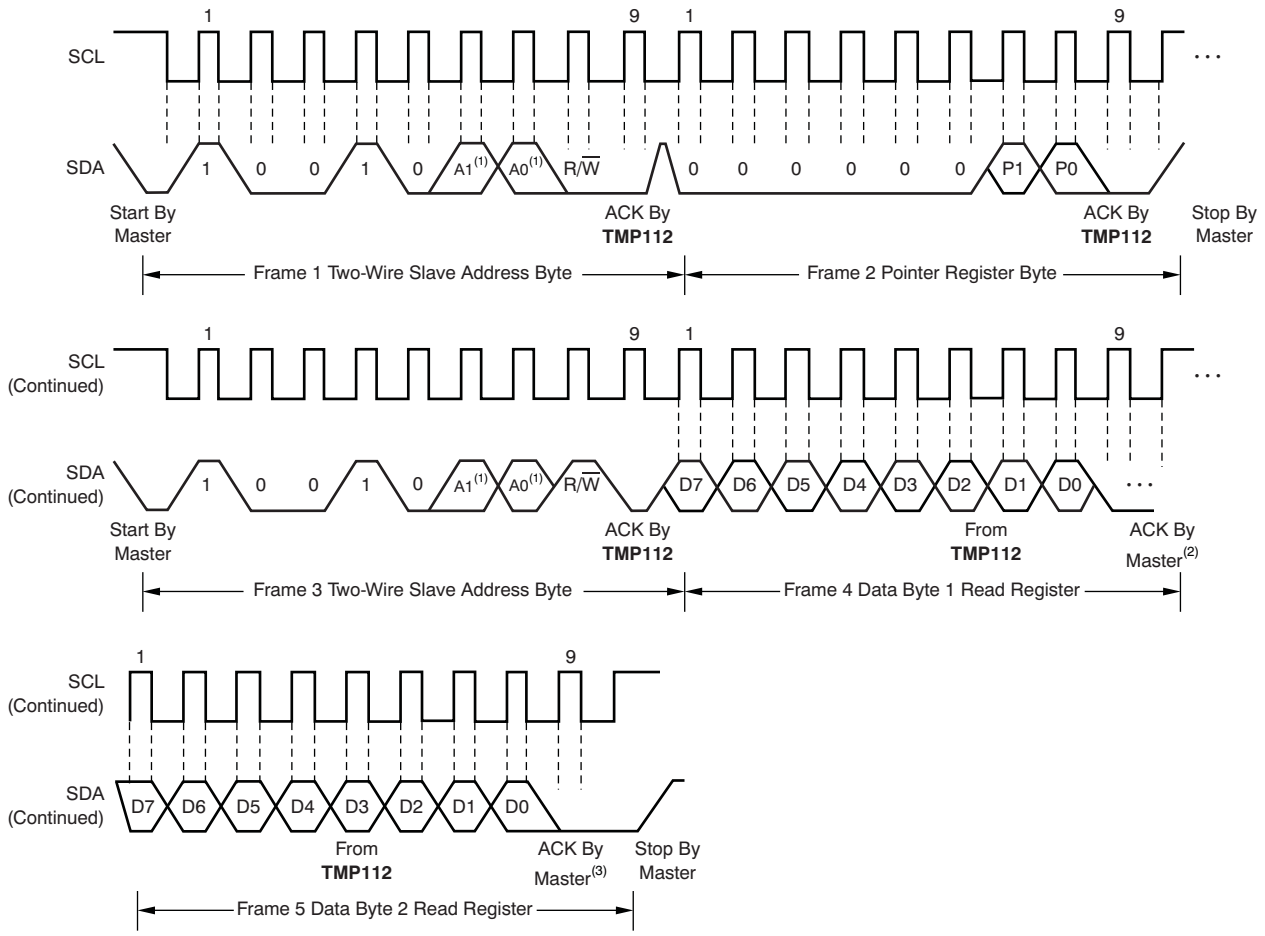
Figure 10. Two-Wire Timing Diagram



NOTE: (1) The values of A0 and A1 are determined by the ADD0 pin.

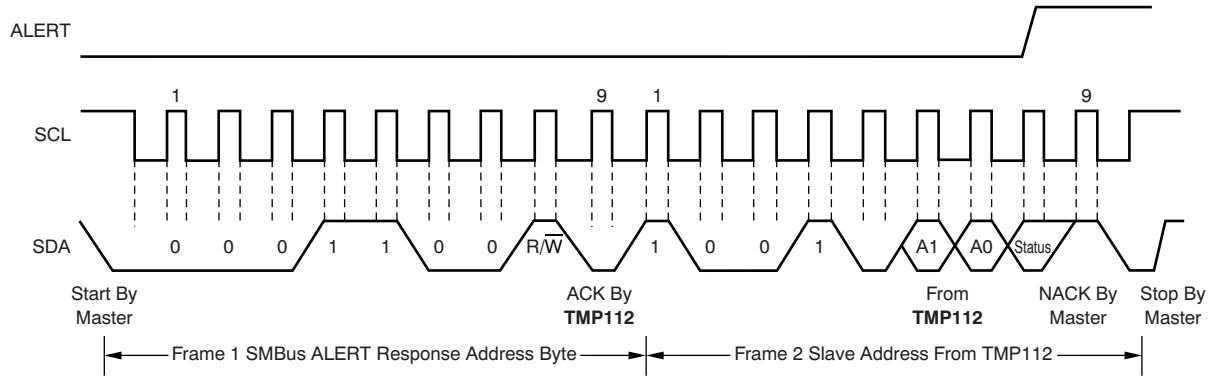
Figure 11. Two-Wire Timing Diagram for Write Word Format

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NOTE: (1) The values of A0 and A1 are determined by the ADD0 pin.
(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 12. Two-Wire Timing Diagram for Read Word Format



NOTE: (1) The values of A0 and A1 are determined by the ADD0 pin.

Figure 13. Timing Diagram for SMBus ALERT

7.4 Device Functional Modes

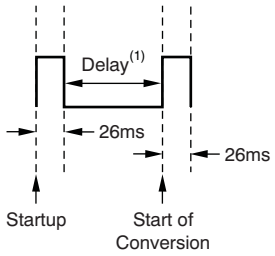
7.4.1 Continuos-Conversion Mode

The default mode of the TMP112 family is continuos conversion mode. During continuous-conversion mode, the ADC performs continuos temperature conversions and stores each results to the temperature register, overwriting the result from the previous conversion. The conversion rate bits, CR1 and CR0, configure the TMP112 family for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. The TMP112 family has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP112 family makes a conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 5 lists the settings for CR1 and CR0.

Table 5. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25 Hz
0	1	1 Hz
1	0	4 Hz (default)
1	1	8 Hz

After a power-up or general-call reset, the TMP112 family immediately begins a conversion as shown in Figure 14. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 μA (typical at +27°C). The quiescent current during delay is 2.2 μA (typical at +27°C).



(1) Delay is set by CR1 and CR0.

Figure 14. Conversion Start

7.4.2 Extended Mode (EM)

The extended mode bit configures the device for normal mode operation (EM = 0) or extended mode operation (EM = 1). In normal mode, the temperature register and the high and low limit registers use a 12-bit data format. Normal mode is used to make the TMP112 family compatible with the TMP75 device.

Extended mode (EM = 1) allows measurement of temperatures above 128°C by configuring the temperature register and the high and low limit registers for 13-bit data format.

7.4.3 One-Shot/Conversion Ready Mode (OS)

The TMP112 family features a one-shot temperature-measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit begins a single temperature conversion. During the conversion, the OS bit reads 0. The device returns to the SHUTDOWN state at the completion of the single conversion. After the conversion, the OS bit reads 1. This feature is useful for reducing power consumption in the TMP112 family when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP112 family can achieve a higher conversion rate. A single conversion typically occurs for 26 ms and a read can occur in less than 20 μs. When using one-shot mode, 30 or more conversions per second are possible.

7.4.4 Thermostat Mode (TM)

The thermostat mode bit indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1).

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7.4.4.1 Comparator Mode (TM = 0)

In Comparator mode (TM = 0), the Alert pin is activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and remains active until the temperature falls below the value in the $T_{(LOW)}$register. For more information on the comparator mode, see the *High- and Low-Limit Register* section.

7.4.4.2 Interrupt Mode (TM = 1)

In Interrupt mode (TM = 1), the Alert pin is activated when the temperature exceeds $T_{(HIGH)}$ or goes below $T_{(LOW)}$ registers. The Alert pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Register* section.

7.5 Programming

7.5.1 Pointer Register

Figure 15 shows the internal register structure of the TMP112 family. The 8-bit Pointer Register of the device is used to address a given data register. The Pointer Register uses the two LSBs (see Table 13) to identify which of the data registers must respond to a read or write command. The power-up reset value of P1/P0 is '00'. By default, the TMP112 family reads the temperature on power-up.

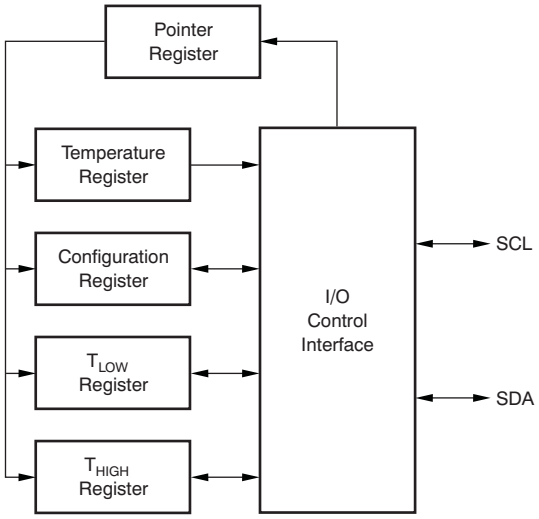


Figure 15. Internal Register Structure

Table 6 lists the pointer address of the registers available in the TMP112 family. Table 7 lists the bits of the Pointer Register byte. During a write command, bytes P2 through P7 must always be 0.

Table 6. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

Table 7. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

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7.5.2 Temperature Register

The Temperature Register of the TMP112 family is configured as a 12-bit read-only register (setting the EM bit to 0 in the configuration register; see the *Extended Mode* section), or as a 13-bit read-only register (setting the EM bit to 1 in the configuration register) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 8 and Table 9. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed.

Table 8. Byte 1 of Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	T11	T10	T9	T8	T7	T6	T5	T4
	(T12)	(T11)	(T10)	(T9)	(T8)	(T7)	(T6)	(T5)

Table 9. Byte 2 of Temperature Register(1)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	T3	T2	T1	T0	0	0	0	0
	(T4)	(T3)	(T2)	(T1)	(T0)	(0)	(0)	(1)

(1) Extended mode 13-bit configuration shown in parentheses.

7.5.3 Configuration Register

The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. Table 10 lists the format and power-up and reset values of the configuration register. For compatibility, the first byte corresponds to the Configuration Register in the TMP75 and TMP275 devices. All registers are updated byte by byte.

Table 10. Configuration and Power-Up/Reset Formats

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD
	0	1	1	0	0	0	0	0
2	CR1	CR0	AL	EM	0	0	0	0
	1	0	1	0	0	0	0	0

7.5.3.1 Shutdown Mode (SD)

The Shutdown mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 μA. Shutdown mode is enabled when the SD bit = 1; the device shuts down when current conversion is completed. When SD = 0, the device maintains a continuous conversion state.

7.5.3.2 Thermostat Mode (TM)

The Thermostat mode bit indicates to the device whether to operate in Comparator mode (TM = 0) or Interrupt mode (TM = 1). For more information on Comparator and Interrupt modes, see the *High- and Low-Limit Registers* section.

7.5.3.3 Polarity (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low . When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is illustrated in Figure 16.

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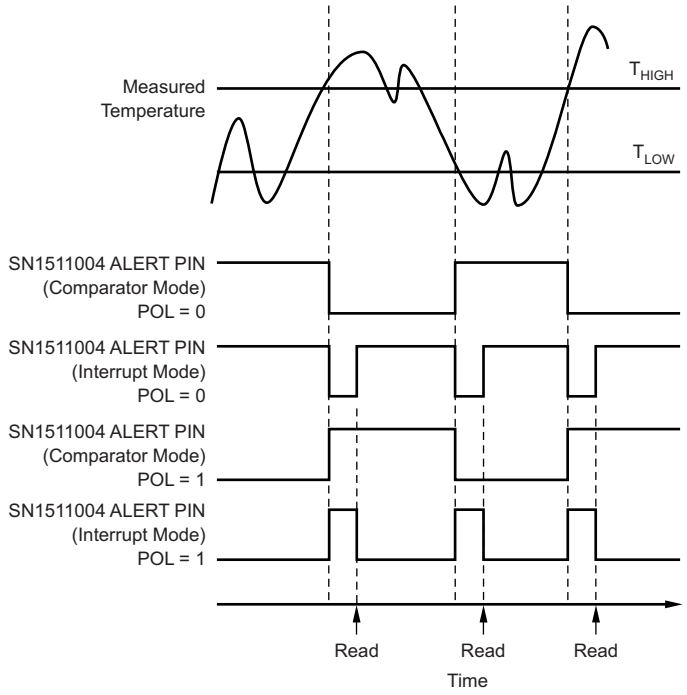


Figure 16. Output Transfer Function Diagrams

7.5.3.4 Fault Queue (F1/F0)

A fault condition exists when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 11 lists the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the *High- and Low-Limit Registers* section.

Table 11. TMP112 family Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

7.5.3.5 Converter Resolution (R1 and R0)

The converter resolution bits, R1 and R0, are read-only bits. The TMP112 family converter resolution is set on start up to 11 which sets the temperature register to a 12-bit resolution.

7.5.3.6 One-Shot (OS)

When the device is in shutdown mode, writing a 1 to the OS bit begins a single temperature conversion. During the conversion, the OS bit reads 0. The device returns to the SHUTDOWN state at the completion of the single conversion. For more information on the one-shot conversion mode, see the *One-Shot/Conversion Ready Mode (OS)* section.

7.5.3.7 Extended Mode (EM)

The extended mode bit configures the device for normal mode operation (EM = 0) or extended mode operation (EM = 1). In normal mode, the temperature register and the high and low limit registers use a 12-bit data format. For more information on the extended mode, see the *Extended Mode (EM)* section.

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7.5.3.8 Alert (AL)

The AL bit is a read-only function. Reading the AL bit provides information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. When the POL bit equals 0, the AL bit reads as 1 until the temperature equals or exceeds $T_{(HIGH)}$ for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below $T_{(LOW)}$ for the programmed number of consecutive faults, when it again reads as 1. The status of the TM bit does not affect the status of the AL bit.

7.5.4 High- and Low-Limit Register

The temperature limits are stored in the $T_{(LOW)}$ and $T_{(HIGH)}$ registers in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or an interrupt, and is set by the TM bit in the configuration register.

In Comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated $T_{(LOW)}$ value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in $T_{(HIGH)}$ for a consecutive number of fault conditions (as shown in Table 11). The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it becomes active again only when temperature falls below $T_{(LOW)}$, and remains active until cleared by a read operation of any register or a successful response to the SMBus alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds $T_{(HIGH)}$. The ALERT pin can also be cleared by resetting the device with the general-call Reset command. This action also clears the state of the internal registers in the device, returning the device to comparator mode (TM = 0).

Both operating modes are represented in Figure 16. Table 12 and Table 13 list the format for the T_{HIGH} and T_{LOW} registers. The most significant byte is sent first, followed by the least significant byte. The power-up reset values for $T_{(HIGH)}$ and $T_{(LOW)}$ are:

- T_{HIGH} = +80°C
- T_{LOW} = +75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 12. Bytes 1 and 2 of T_{HIGH} Register(1)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
	(H12)	(H11)	(H10)	(H9)	(H8)	(H7)	(H6)	(H5)
BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2	H3	H2	H1	H0	0	0	0	0
	(H4)	(H3)	(H2)	(H1)	(H0)	(0)	(0)	(0)

(1) Extended mode 13-bit configuration shown in parenthesis.

Table 13. Bytes 1 and 2 of T_{LOW} Register(1)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
	(L12)	(L11)	(L10)	(L9)	(L8)	(L7)	(L6)	(L5)
BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2	L3	L2	L1	L0	0	0	0	0
	(L4)	(L3)	(L2)	(L1)	(L0)	(0)	(0)	(0)

(1) Extended mode 13-bit configuration shown in parenthesis.

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8 Application and Implementation

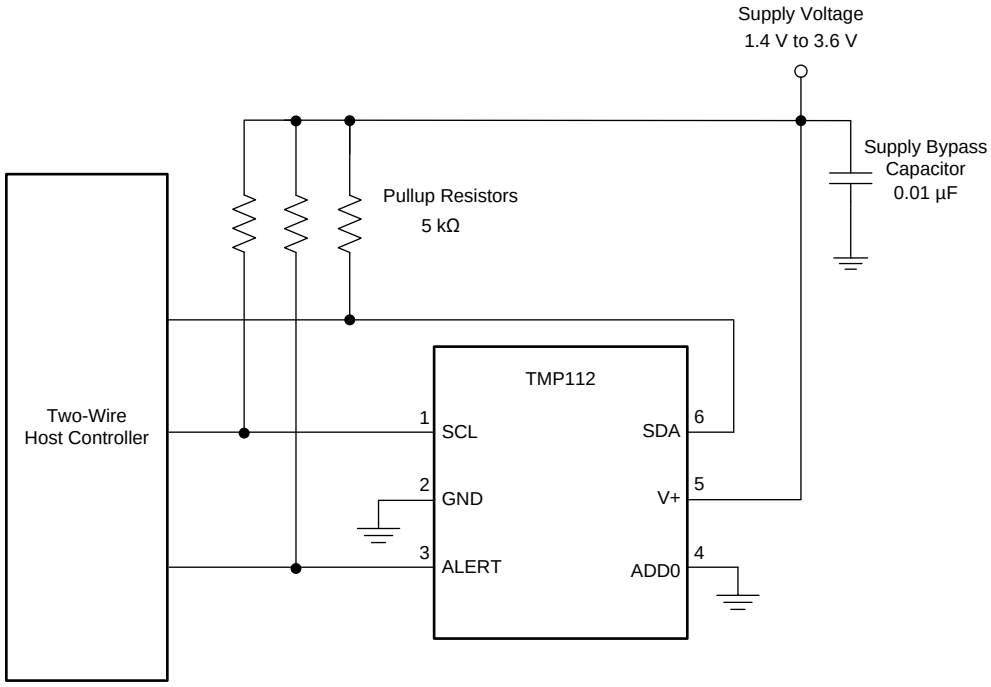
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP112 family is used to measure the PCB temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus.

8.2 Typical Application



NOTE: The SCL, SDA, and ALERT pins require pullup resistors.

Figure 17. Typical Connections

8.2.1 Design Requirements

The TMP112 family requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ but must not exceed 3 mA of current on any of those pins. A 0.01-µF bypass capacitor on the supply is recommended as shown in Figure 17. The SCL and SDA lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors. To configure one of four different addresses on the bus, connect the ADD0 pin to either the GND, V+, SDA, or SCL pin.

8.2.2 Detailed Design Procedure

Place the device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

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Typical Application (continued)

The TMP112 family is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V+ pin of the TMP112 family can further reduce any noise that the device might propagate to other components. $R_{(F)}$ in Figure 18 must be less than 5 kΩ and $C_{(F)}$ must be greater than 10 nF.

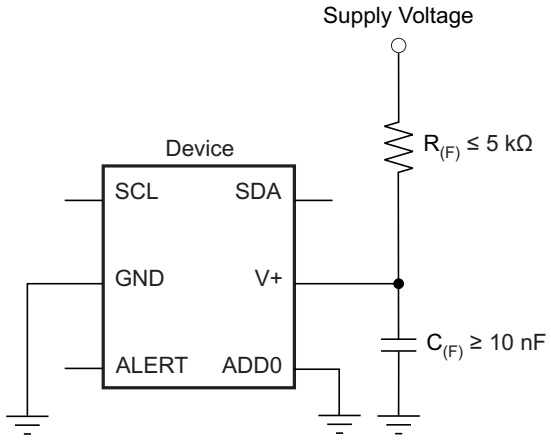


Figure 18. Noise Reduction Techniques

8.2.3 Application Curves

Figure 19 shows the step response of the TMP112 family to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 0.8 s. The time-constant result depends on the printed-circuit board (PCB) that the TMP112 family is mounted. For this test, the TMP112 family was soldered to a two-layer PCB that measured 0.375 inches × 0.437 inches.

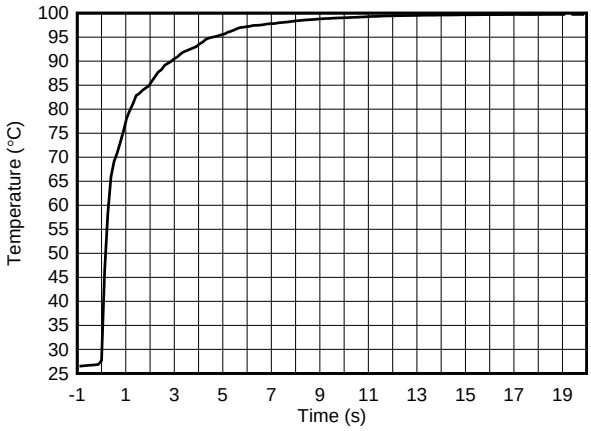


Figure 19. Temperature Step Response

9 Power Supply Recommendations

The TMP112 family operates with power supply in the range of 1.4 to 3.6 V. The device is optimized for operation at 3.3-V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

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10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins (SDA , SCL and ALERT) through 5-kΩ pullup resistors.

10.2 Layout Example

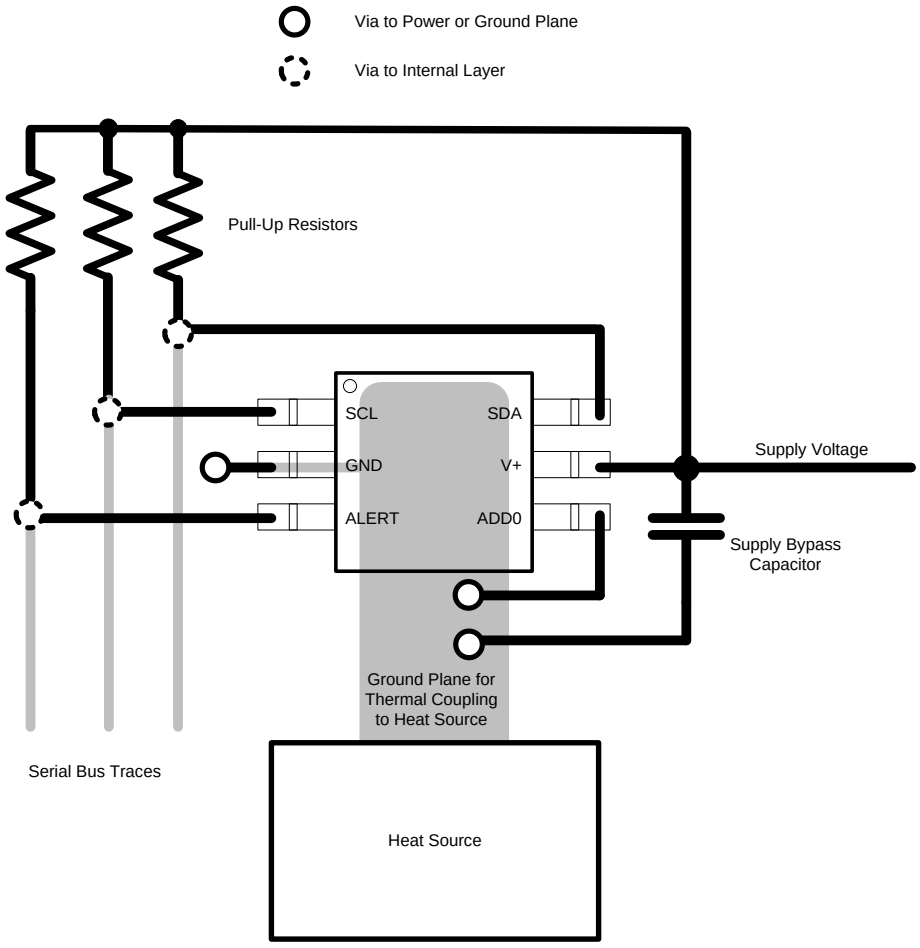


Figure 20. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《具有 SMBus 和双线制串行接口并采用 SOT563 封装的 TMP102 低功耗数字温度传感器》*(SBOS397)
- *《具有 I^2C 和 SMBus 接口并采用行业标准 LM75 外形尺寸和引脚的 TMPx75 温度传感器》*(SBOS288)
- *《具有 I^2C 和 SMBus 接口并采用行业标准 LM75 外形尺寸和引脚的 TMP275 ±0.5°C 温度传感器》*(SBOS363)
- *具有 NFC 接口的超低功耗多传感器数据记录器* 设计指南
- *适用于系统唤醒和中断的基于电容的人体接近检测* 设计指南

11.2 社区资源

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11.4 静电放电警告



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11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP112AIDRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBS	Samples
TMP112AIDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBS	Samples
TMP112BIDRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B8	Samples
TMP112BIDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B8	Samples
TMP112NAIDRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1AB	Samples
TMP112NAIDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1AB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

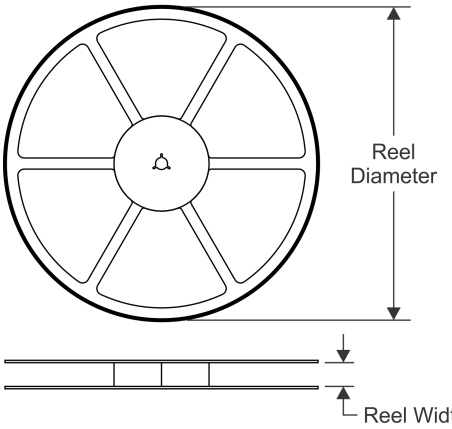
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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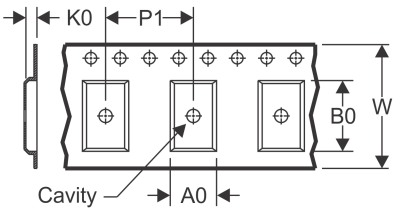
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

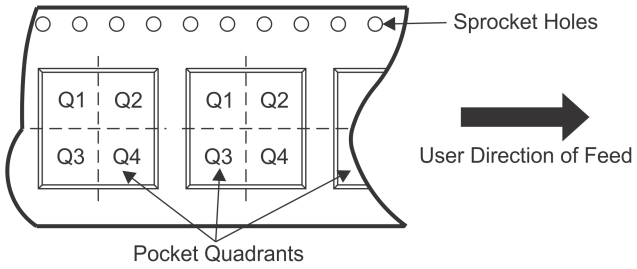


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

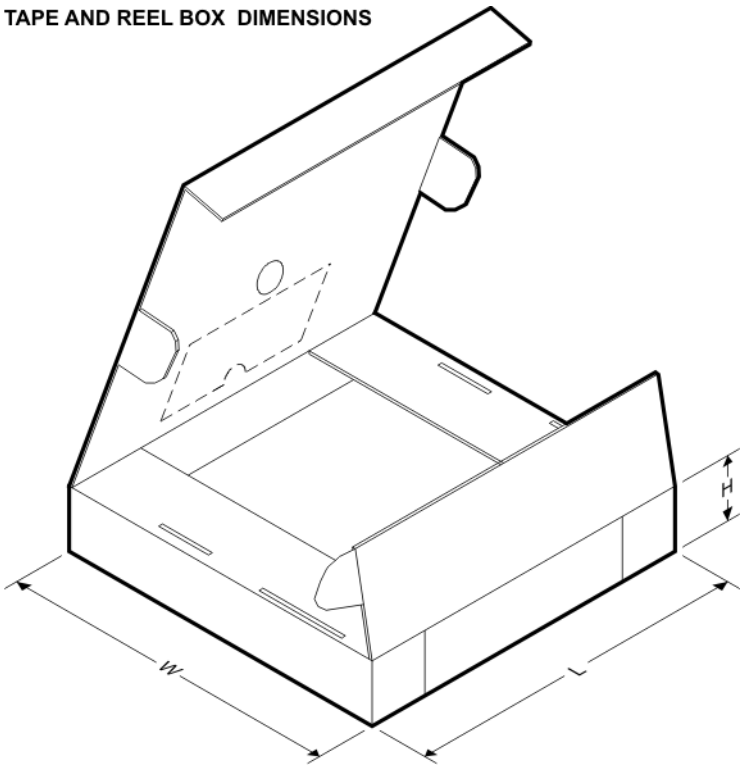
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP112AIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP112AIDRLR	SOT-5X3	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP112AIDRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP112BIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP112BIDRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP112NAIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP112NAIDRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

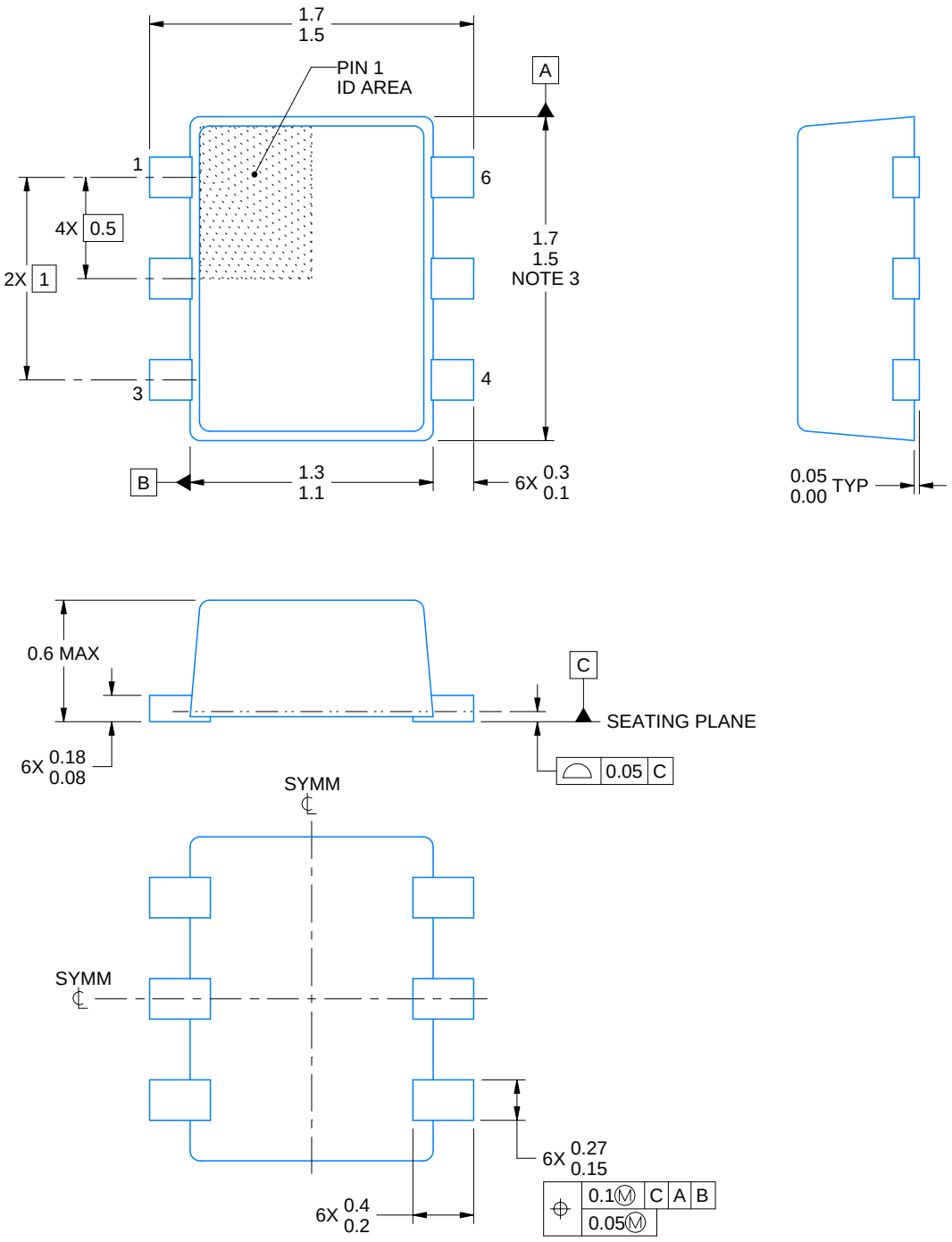
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP112AIDRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
TMP112AIDRLR	SOT-5X3	DRL	6	4000	184.0	184.0	19.0
TMP112AIDRLT	SOT-5X3	DRL	6	250	202.0	201.0	28.0
TMP112BIDRLR	SOT-5X3	DRL	6	4000	183.0	183.0	20.0
TMP112BIDRLT	SOT-5X3	DRL	6	250	183.0	183.0	20.0
TMP112NAIDRLR	SOT-5X3	DRL	6	4000	183.0	183.0	20.0
TMP112NAIDRLT	SOT-5X3	DRL	6	250	183.0	183.0	20.0

PACKAGE OUTLINE

DRL0006A

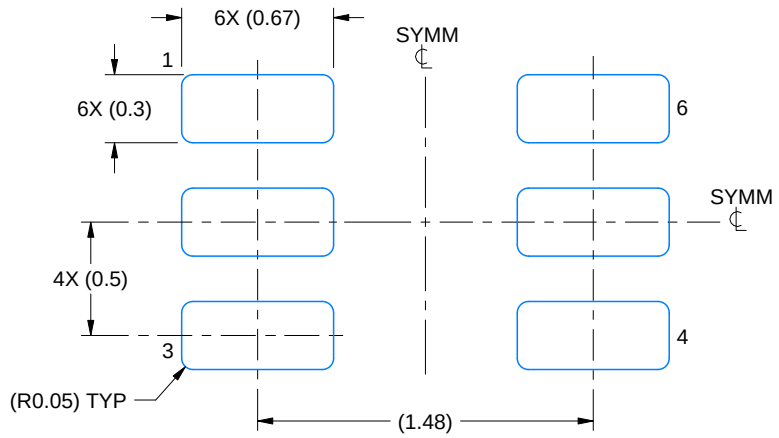
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

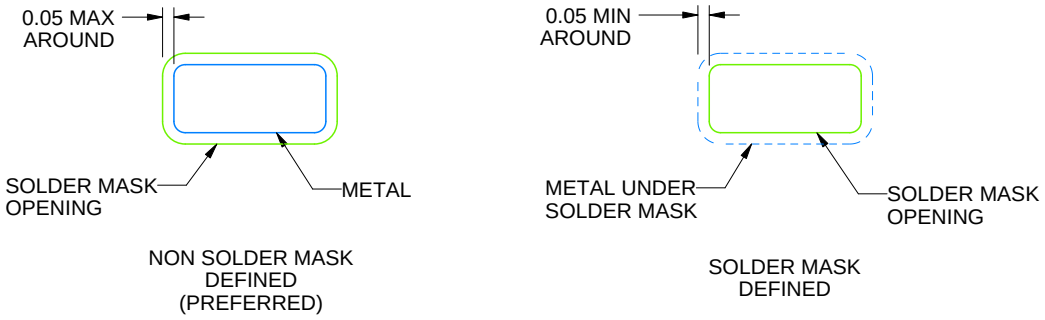


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

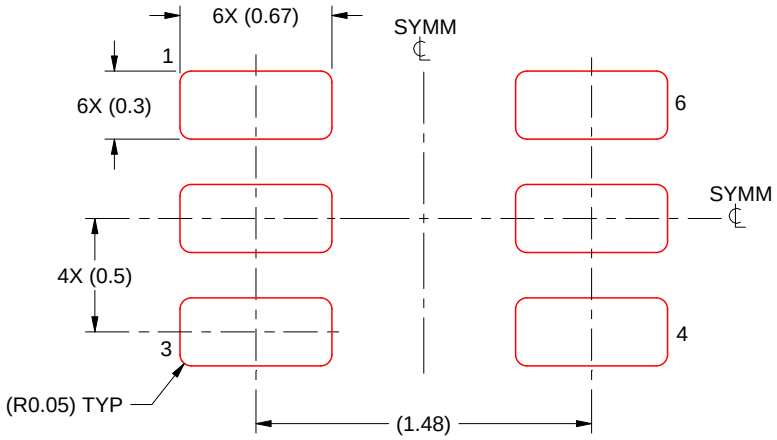
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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