TMS320F281x 数字信号处理器

1 器件概述

：更新了 Q 温度选项。

1.1 特性

- 高性能静态 CMOS 技术
  - 150MHz（6.67ns 周期时间）
  - 低功耗（135MHz 时为 1.8V 内核电压，150MHz 时为 1.9V 内核电压，3.3V I/O）设计
- 支持 JTAG 边界扫描
  - IEEE 标准 1149.1-1990 IEEE 标准测试访问端口和边界扫描架构
- 高性能 32 位 CPU (TMS320C28x)
  - 16 × 16 和 32 × 32 MAC 操作
  - 16 × 16 双 MAC
  - 哈佛 (Harvard) 总线架构
  - 连动运算
  - 快速中断响应和处理
  - 统一存储器编程模型
  - 4M 线性程序/数据地址范围
  - 高效代码（使用 C/C++ 和汇编语言）
  - TMS320F24x/LF240x 处理器源代码兼容
- 片上存储器
  - 高达 128K × 16 的闪存（四个 8K × 16 和六个 16K × 16 的扇区）
  - 1K × 16 OTP ROM
  - L0 和 L1：2 块 4K × 16 的单周期访问 RAM (SARAM)
  - H0：1 块 8K × 16 的 SARAM
  - M0 和 M1：2 块 1K × 16 的 SARAM
- 引导 ROM (4K × 16)
  - 具有软件引导模式
  - 标准数学表
- 外部接口 (F2812)
  - 总内存大于 1M × 16
  - 可编程等待状态
  - 可编程读取/写入选通计时
  - 三个独立芯片可选
- 字节序：小端字节序
- 时钟和系统控制
  - 片上振荡器
  - 看门狗计时器模块
- 三个外部中断
- 可支持 45 个外设中断的外设中断扩展 (PIE) 块
- 三个 32 位 CPU 计时器
- 128 位安全密钥/锁
  - 保护闪存/OTP 和 L0/L1 SARAM
  - 防止固件逆向工程
- 电机控制外设
  - 两个事件管理器（EVA，EVB）
  - 与 240xA 器件兼容
- 串行端口外设
  - 串行外设接口 (SPI)
  - 两个串行通信接口 (SCI)，标准 UART
  - 增强型控制器局域网络 (eCAN)
  - 多通道缓冲串行端口 (McBSP)
- 12 位 ADC、16 通道
  - 2 × 8 通道输入多路复用器
  - 两个采样保持
  - 单个/同步转换
  - 转换速率快：80ns/12.5MSPS
- 多达 56 个通用 I/O (GPIO) 引脚
- 高级仿真 特性
  - 分析和断点功能
  - 通过硬件的实时调试
- 开发工具包括
  - ANSI C/C++ 编译器/汇编器/连接器
  - Code Composer Studio™IDE
  - DSP/BIOS™
  - JTAG 扫描控制器
    - IEEE 标准 1149.1-1990 IEEE 标准测试访问端口和边界扫描架构
- 低功耗模式，节省能耗
  - 支持闲置、待机、停机模式
  - 禁用单独的外设时钟

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

- 封装选项
  - 具有外部存储器接口的 179 焊球 ™MicroStar BGA（GHH，ZHH）(F2812)
  - 具有外部存储器接口的 176 引脚薄型四方扁平封装 (LQFP) (PGF) (F2812)
  - 无外部存储器接口的 128 引脚 LQFP (PBK)（F2810，F2811）
- 温度选项
  - A：-40°C 至 85°C（GHH，ZHH，PGF，PBK）
  - S：-40°C 至 125°C（GHH，ZHH，PGF，PBK）
  - Q：–40°C 至 125°C（PGF，PBK）（通过针对汽车应用的 AEC-Q100 认证）

1.2 应用

- 高级驾驶辅助系统 (ADAS)
- 楼宇自动化
- 电子销售终端
- 电动汽车/混合动力电动汽车 (EV/HEV) 动力传动
- 工厂自动化
- 电网基础设施
- 工业运输
- 医疗、保健与健身
- 电机驱动器
- 电力输送
- 电信基础设施
- 测试和测量

1.3 说明

TMS320F2810、TMS320F2811 和 TMS320F2812 器件均属于 TMS320C28x DSP 系列器件，是适用于高要求控制应用的高度集成和高性能的 解决方案。

在本文档中，TMS320F2810、TMS320F2811 和 TMS320F2812 分别缩写为 F2810、F2811 和 F2812。F281x 表示上述三种器件。

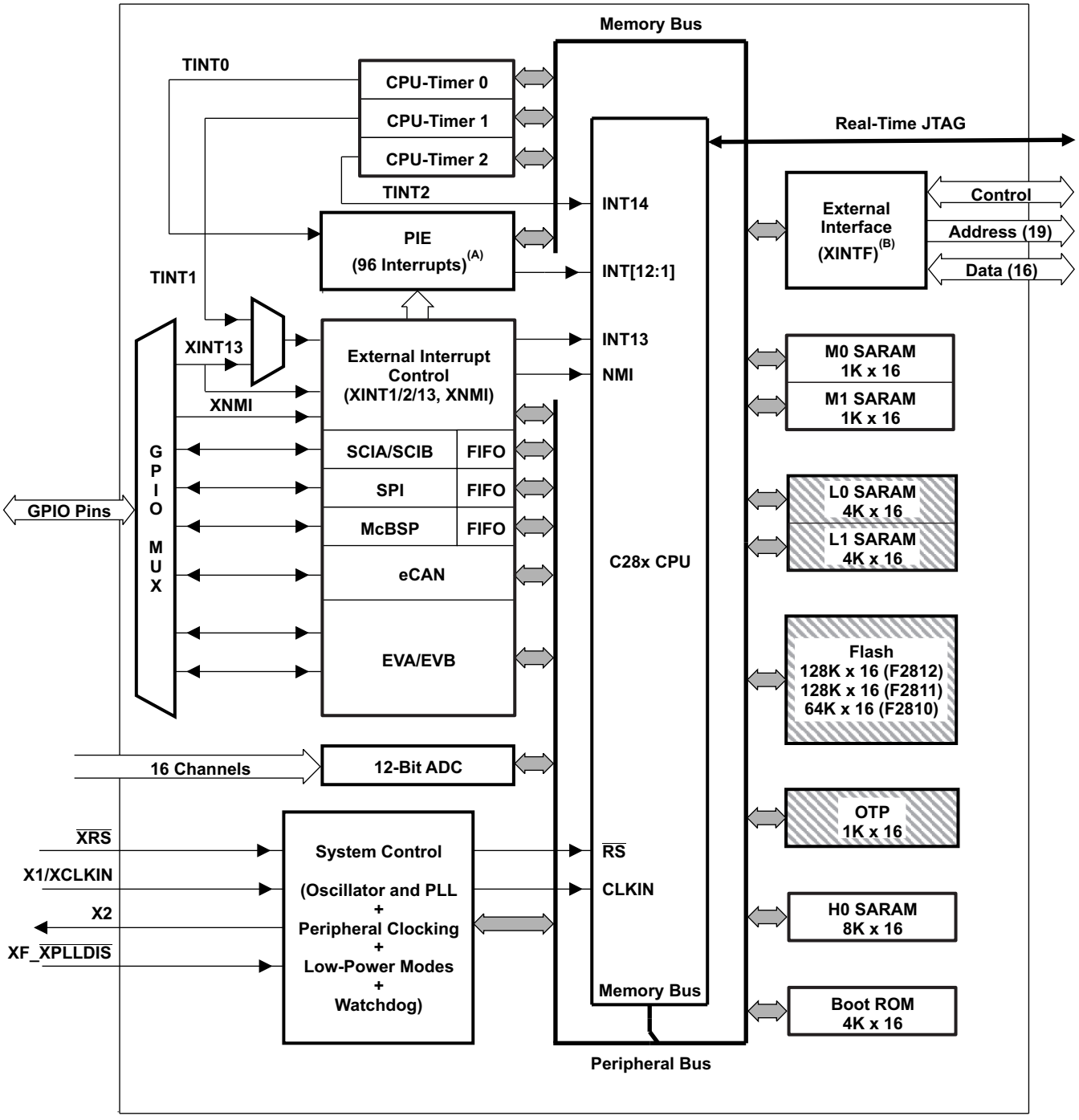
器件信息(1)

器件型号	封装	封装尺寸
TMS320F2812ZHH	MicroStar BGA (179)	12.0mm × 12.0mm
TMS320F2812GHH	MicroStar BGA (179)	12.0mm × 12.0mm
TMS320F2812PGF	LQFP (176)	24.0mm × 24.0mm
TMS320F2811PBK	LQFP (128)	14.0mm × 14.0mm
TMS320F2810PBK	LQFP (128)	14.0mm × 14.0mm

(1) 有关这些器件的更多信息，请参阅机械、封装和可订购信息。

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1.4 功能方框图



A. 96 个可能中断中有 45 个在器件上使用。
B. XINTF 只能在 F2812 器件上使用。

图 **1-1.** 功能方框图

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2 修订历史记录

Changes from May 31, 2012 to July 12, 2019 (from T Revision (May 2012) to U Revision) **Page**

- 全局：删除了 ROM 器件（TMS320C2810、TMS320C2811 和 TMS320C2812）删除了 C281x/ROM 数据。 1
- 全局：文档结构已经过重新编排 1
- 全局：将“Q100”更改为“AEC-Q100” 1
- 节 1.1 （特性）：更新了“时钟和系统控制”特性 1
- 节 1.1将“[通过 Q100 认证]”更改为“（通过针对汽车应用的 AEC-Q100 认证）” 1
- 节 1.2 （应用：添加了该部分。 2
- 节 1.3 （说明）：添加了器件信息表 2
- 节 1.4 （功能方框图）：添加了章节标题 3
- 图 1-1 （功能方框图）：删除了 ROM。更新了脚注 3
- Section 3 (Device Comparison): Changed section title from "Device Summary" to "Device Comparison". 7
- Table 3-1 (Device Comparison): Changed table title from "Hardware Features" to "Device Comparison". 7
- Table 3-1: Removed C2810, C2811, and C2812 data. 7
- Table 3-1: Removed "Product Status" row and its associated footnote. 7
- Section 3.1 (Related Products): Added section. 8
- Section 4 (Terminal Configuration and Functions): Changed section title from "Introduction" to "Terminal Configuration and Functions". 9
- Section 4.1 (Pin Diagrams): Changed section title from "Pin Assignments" to "Pin Diagrams". 9
- Table 4-1 (Signal Descriptions): Updated DESCRIPTION of $\overline{XRS}$. 12
- Table 4-1: Removed C281x/ROM data from DESCRIPTION of TEST1, TEST2, and V_{DD3VFL} 12
- Section 5 (Specifications): Changed section title from "Electrical Specifications" to "Specifications". 21
- Section 5.1 (Absolute Maximum Ratings): Updated "Long-term high-temperature storage ..." footnote. 21
- Section 5.2 (ESD Ratings – Commercial): Added section. 22
- Section 5.3 (ESD Ratings – Automotive): Added section. 22
- Section 5.5 (Power Consumption Summary): Changed section title from "Current Consumption" to "Power Consumption Summary". 24
- Table 5-2 (Typical Current Consumption by Various Peripherals (at 150 MHz)): Added footnote about achieving power savings. 26
- Section 5.6 (Electrical Characteristics): Removed I_{IL} for C281x devices. 27
- Section 5.7 (Thermal Resistance Characteristics for 179-Ball ZHH Package): Added section. 27
- Section 5.8 (Thermal Resistance Characteristics for 179-Ball GHH): Added section. 27
- Section 5.9 (Thermal Resistance Characteristics for 176-Pin PGF Package): Added section. 28
- Section 5.10 (Thermal Resistance Characteristics for 128-Pin PBK Package): Added section. 28
- Section 5.11 (Thermal Design Considerations): Added section. 28
- Section 5.12.2 (Power Supply Sequencing): Changed section title from "Power Sequencing Requirements" to "Power Supply Sequencing". Updated section. Removed "Recommended “Low-Dropout Regulators”" table. Removed C281x data. 31
- Section 5.12.4 (Clock Specifications): Added section title. 37
- Section 5.12.5 (Peripherals): Added section title. 40
- Figure 5-14 (General-Purpose Input Timing): Replaced "XCLKOUT" with "SYSCLK". 42
- Section 5.12.5.5 (Serial Peripheral Interface (SPI) Master Mode Timing): Updated section. 49
- Section 5.12.5.6 (Serial Peripheral Interface (SPI) Slave Mode Timing): Updated section. 51
- Section 5.12.5.7.2 (Synchronous Mode (USEREADY = 1, READYMODE = 0)): Updated "XTIMING register configuration restrictions" table by changing XRDACTIVE value from "≥ 1" to "≥ 2" and XWRACTIVE value from "≥ 1" to "≥ 2". 54
- Section 5.12.5.7.2 (Synchronous Mode (USEREADY = 1, READYMODE = 0)): Updated "Examples of valid and invalid timing" table by changing Valid XRDACTIVE value from "1" to "2" and Valid XWRACTIVE value from "1" to "2". 54
- Section 5.12.5.7.3 (Asynchronous Mode (USEREADY = 1, READYMODE = 1)): Updated second "XTIMING register configuration restrictions" table by changing XRDACTIVE value from "≥ 1" to "≥ 2" and XWRACTIVE value from "≥ 1" to "≥ 2". 55
- Section 5.12.5.7.3 (Asynchronous Mode (USEREADY = 1, READYMODE = 1)): Updated "Examples of valid and invalid timing" table by changing Valid XRDACTIVE value from "1" to "2" and Valid XWRACTIVE value from "1" to "2". 55
- Table 5-40 (ADC Absolute Maximum Ratings Over Recommended Operating Conditions (Unless Otherwise Noted)): Updated table. 70

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- Table 5-41 (ADC Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)—AC Specifications): Changed table title from "AC Specifications" to "ADC Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)—AC Specifications". 70
- Table 5-42 (ADC Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)—DC Specifications): Changed table title from "DC Specifications" to "ADC Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)—DC Specifications". 71
- Table 5-42: Removed C281x data. 71
- Table 5-49 (McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)): Updated footnotes. 80
- Table 5-50 (McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)): Updated footnote. 80
- Table 5-51 (McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)): Updated footnotes. 81
- Table 5-52 (McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)): Updated footnote. 81
- Table 5-53 (McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)): Updated footnotes. 82
- Table 5-54 (McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)): Updated footnote. 82
- Table 5-55 (McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)): Updated footnotes. 83
- Table 5-56 (McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)): Updated footnote. 83
- Table 5-61 (Flash Parameters at 150-MHz SYSCLKOUT): Updated "Typical parameters as seen at room temperature ..." footnote. 86
- Table 5-63 (Flash Data Retention Duration): Added table. 87
- Section 6 (Detailed Description): Changed section title from "Functional Overview" to "Detailed Description". 88
- Section 6.1.21 (Serial Port Peripherals): Updated description of eCAN. 94
- Section 6.2.3 (Enhanced Analog-to-Digital Converter (ADC) Module): Updated equations by which the digital value of the input analog voltage is derived. 103
- Section 6.2.4 (Enhanced Controller Area Network (eCAN) Module): Updated feature about CAN 2.0B. 108
- Section 6.2.7 (Serial Peripheral Interface (SPI) Module): Updated "Rising edge with phase delay" clocking scheme. 120
- Figure 6-22 (Watchdog Module): Updated figure. 145
- Section 7 (Applications, Implementation, and Layout): Added section. 147
- 节 8 （器件和文档支持）：将标题从“开发支持”更改为“器件和文档支持” 148
- 节 8.1（入门）：更新了该部分 148
- 图 8-1 （TMS320F281x 器件命名规则）：更新了 Q 温度范围的 说明 149
- 节 8.3 （工具和软件）：添加了此部分 149
- 节 8.4 （文档支持）：更新了该部分 150
- 节 8.5 （相关链接）：添加了该部分 152
- 节 9 （机械、封装和可订购信息）：将“机械数据”部分替换为“机械、封装和可订购信息”部分 153

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3 Device Comparison

Table 3-1 provides a summary of each device's features.

Table 3-1. Device Comparison(1)

FEATURE		TYPE(2)	F2810	F2811	F2812
Instruction Cycle (at 150 MHz)		–	6.67 ns	6.67 ns	6.67 ns
Single-Access RAM (SARAM) (16-bit word)		–	18K	18K	18K
3.3-V On-Chip Flash (16-bit word)		–	64K	128K	128K
Code Security for On-Chip Flash/SARAM/OTP		–	Yes	Yes	Yes
Boot ROM		–	Yes	Yes	Yes
OTP ROM (1K x 16)		–	Yes	Yes	Yes
External Memory Interface		0	–	–	Yes
Event Managers A and B (EVA and EVB)		–	EVA, EVB	EVA, EVB	EVA, EVB
• General-Purpose (GP) Timers		–	4	4	4
• Compare (CMP)/PWM		0	16	16	16
• Capture (CAP)/QEP Channels		0	6/2	6/2	6/2
Watchdog Timer		–	Yes	Yes	Yes
12-Bit ADC		0	Yes	Yes	Yes
• Channels			16	16	16
32-Bit CPU Timers		–	3	3	3
Serial Peripheral Interface (SPI)		0	Yes	Yes	Yes
Serial Communications Interfaces A and B (SCIA and SCIB)		0	SCIA, SCIB	SCIA, SCIB	SCIA, SCIB
Controller Area Network (CAN)		0	Yes	Yes	Yes
Multichannel Buffered Serial Port (McBSP)		0	Yes	Yes	Yes
Digital I/O Pins (Shared)		–	56	56	56
External Interrupts		–	3	3	3
Supply Voltage		–	1.8-V Core (135 MHz), 1.9-V Core (150 MHz), 3.3-V I/O		
Packaging	128-pin PBK	–	Yes	Yes	–
	176-pin PGF		–	–	Yes
	179-ball GHH		–	–	Yes
	179-ball ZHH		–	–	Yes
Temperature Options	A: –40°C to 85°C	–	Yes	Yes	Yes
	S: –40°C to 125°C	–	Yes	Yes	Yes
	Q: –40°C to 125°C (AEC-Q100 Qualification)	–	Yes	Yes	PGF only

(1) The *TMS320F281x DSPs Silicon Errata* has been posted on the Texas Instruments (TI) website. It will be updated as needed.
(2) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the *C2000 Real-Time Control Peripherals Reference Guide* and in the peripheral reference guides.

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3.1 Related Products

For information about other devices in this family of products, see the following links:

Original Delfino™ series:

TMS320F2833x Delfino™ Microcontrollers
The F2833x series is the original Delfino MCU. It is the first C2000™ MCU that is offered with a floating-point unit (FPU). It has the first-generation ePWM timers that are used throughout the rest of the Delfino and Piccolo™ families. The 12.5-MSPS, 12-bit ADC is still class-leading for an integrated analog-to-digital converter. The F2833x has a 150-MHz CPU and up to 512KB of on-chip Flash. It is available in a 176-pin QFP or 179-ball BGA package.

Newest Delfino™ series:

TMS320F2837xD Delfino™ Microcontrollers
The F2837xD series sets a new standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU accelerators. New capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

TMS320F2837xS Delfino™ Microcontrollers
The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the Piccolo™ TMS320F2807x series.

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4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the ball locations for the 179-ball GHH and ZHH ball grid array (BGA) packages. Figure 4-2 shows the pin assignments for the 176-pin PGF low-profile quad flatpack (LQFP) and Figure 4-3 shows the pin assignments for the 128-pin PBK LQFP. Table 4-1 describes the function(s) of each pin.

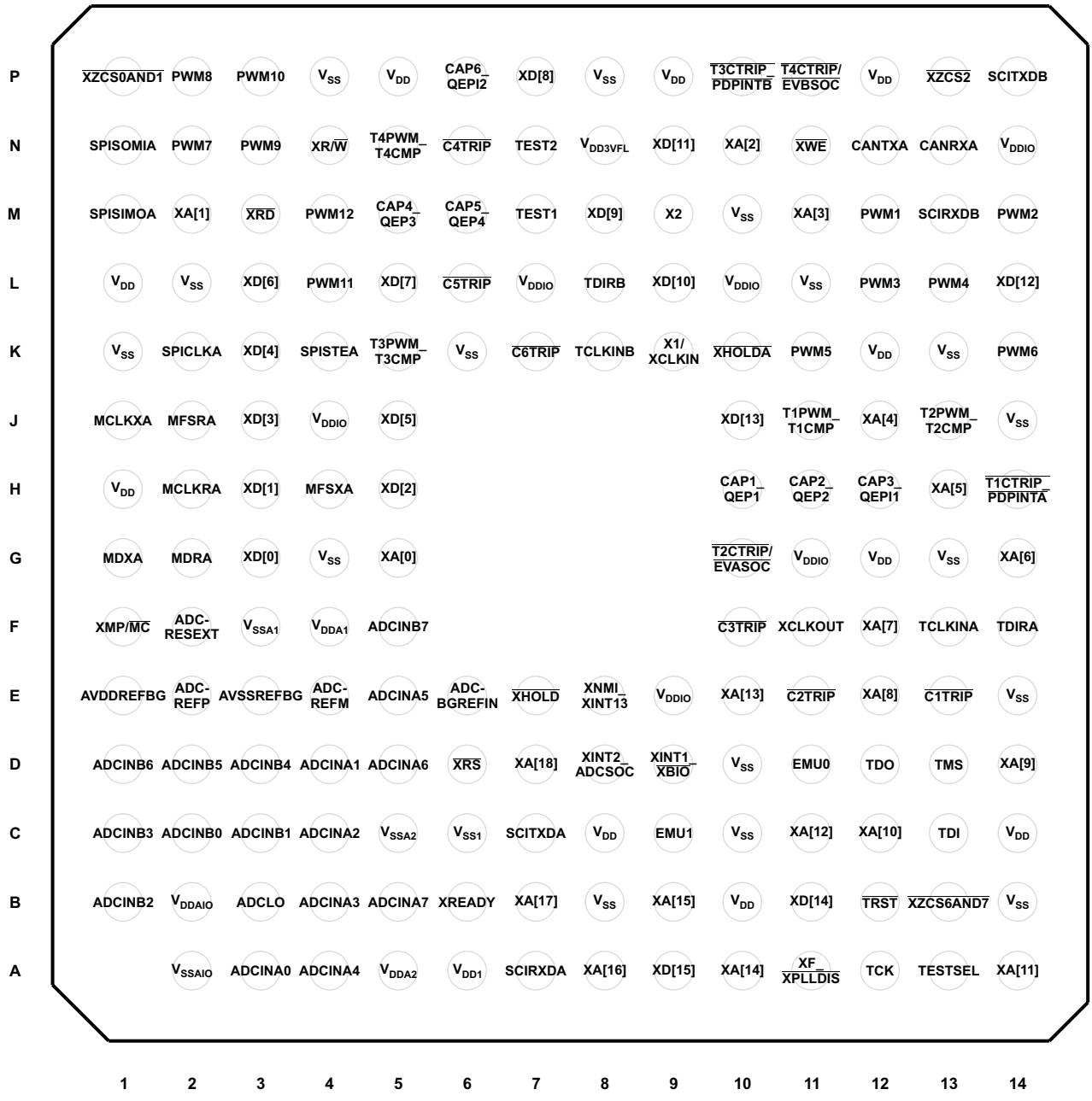


Figure 4-1. TMS320F2812 179-Ball GHH/ZHH MicroStar BGA™ (Bottom View)

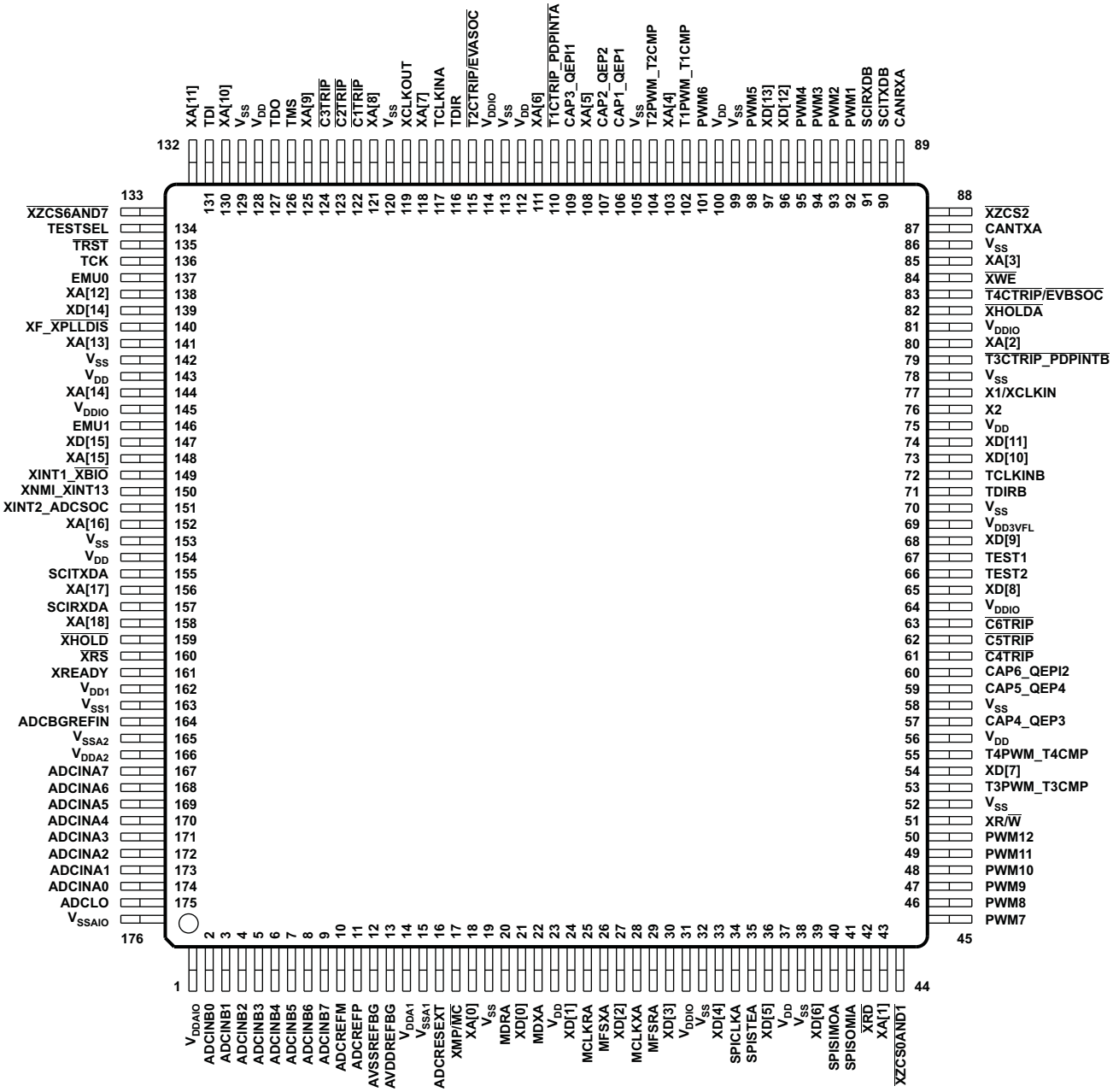


Figure 4-2. TMS320F2812 176-Pin PGF LQFP (Top View)

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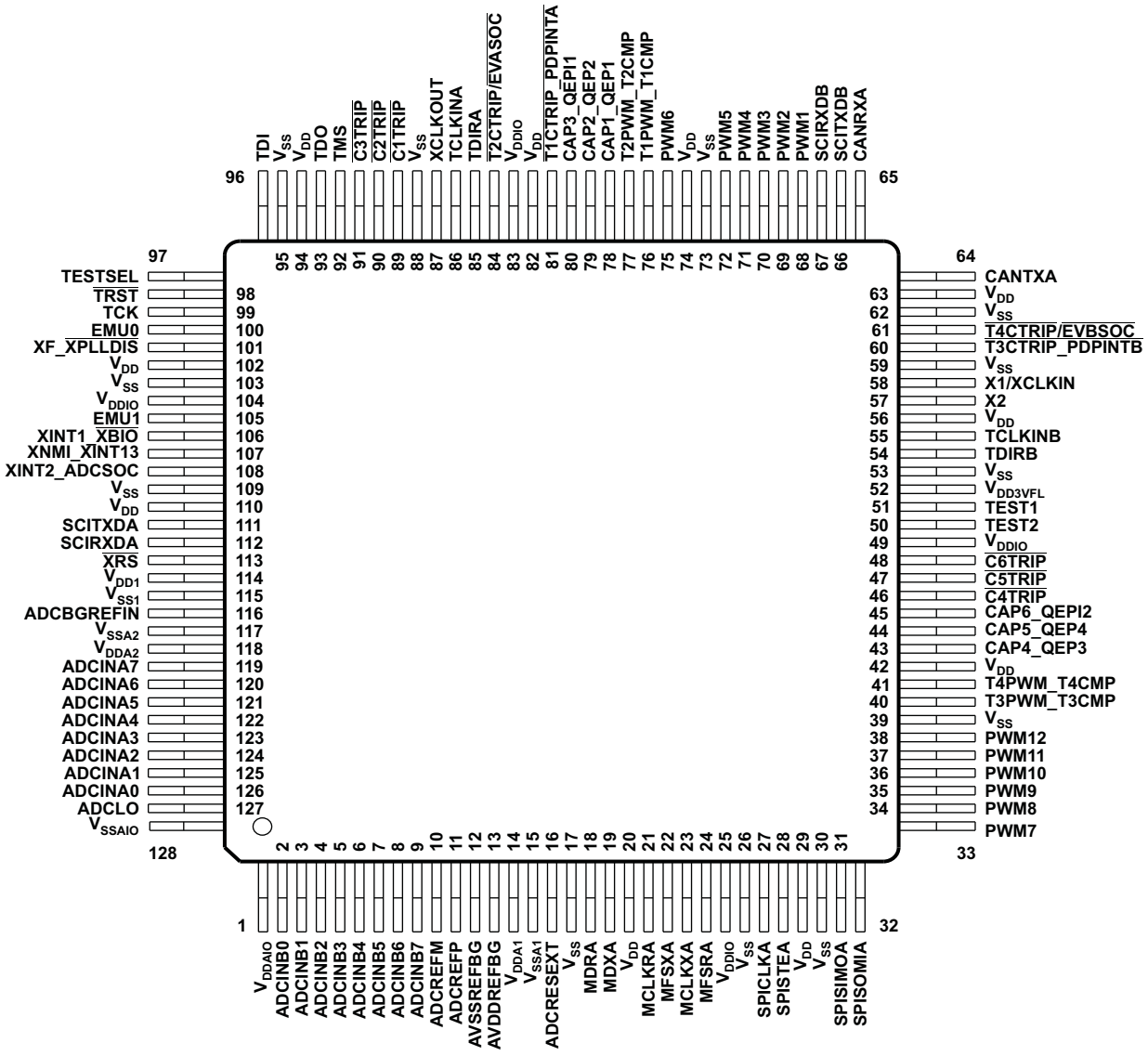


Figure 4-3. TMS320F2810 and TMS320F2811 128-Pin PBK LQFP (Top View)

4.2 Signal Descriptions

Table 4-1 specifies the signals on the F281x devices. All digital inputs are TTL-compatible. All outputs are 3.3 V with CMOS levels. Inputs are not 5-V tolerant. A 100-µA (or 20-µA) pullup/pulldown is used.

Table 4-1. Signal Descriptions(1)

NAME	PIN NO.			I/O/Z(2)	PU/PD(3)	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
XINTF SIGNALS (F2812 ONLY)						
XA[18]	D7	158	–	O/Z	–	19-bit XINTF Address Bus
XA[17]	B7	156	–	O/Z	–	
XA[16]	A8	152	–	O/Z	–	
XA[15]	B9	148	–	O/Z	–	
XA[14]	A10	144	–	O/Z	–	
XA[13]	E10	141	–	O/Z	–	
XA[12]	C11	138	–	O/Z	–	
XA[11]	A14	132	–	O/Z	–	
XA[10]	C12	130	–	O/Z	–	
XA[9]	D14	125	–	O/Z	–	
XA[8]	E12	121	–	O/Z	–	
XA[7]	F12	118	–	O/Z	–	
XA[6]	G14	111	–	O/Z	–	
XA[5]	H13	108	–	O/Z	–	
XA[4]	J12	103	–	O/Z	–	
XA[3]	M11	85	–	O/Z	–	
XA[2]	N10	80	–	O/Z	–	
XA[1]	M2	43	–	O/Z	–	
XA[0]	G5	18	–	O/Z	–	
XD[15]	A9	147	–	I/O/Z	PU	16-bit XINTF Data Bus
XD[14]	B11	139	–	I/O/Z	PU	
XD[13]	J10	97	–	I/O/Z	PU	
XD[12]	L14	96	–	I/O/Z	PU	
XD[11]	N9	74	–	I/O/Z	PU	
XD[10]	L9	73	–	I/O/Z	PU	
XD[9]	M8	68	–	I/O/Z	PU	
XD[8]	P7	65	–	I/O/Z	PU	
XD[7]	L5	54	–	I/O/Z	PU	
XD[6]	L3	39	–	I/O/Z	PU	
XD[5]	J5	36	–	I/O/Z	PU	
XD[4]	K3	33	–	I/O/Z	PU	
XD[3]	J3	30	–	I/O/Z	PU	
XD[2]	H5	27	–	I/O/Z	PU	
XD[1]	H3	24	–	I/O/Z	PU	
XD[0]	G3	21	–	I/O/Z	PU	

(1) Typical drive strength of the output buffer for all pins is 4 mA except for TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins, which are 8 mA.
(2) I = Input, O = Output, Z = High impedance
(3) PU = pin has internal pullup; PD = pin has internal pulldown. Pullup/pulldown strength is given in Section 5.6, Electrical Characteristics Over Recommended Operating Conditions. The pullups/pulldowns are enabled in boundary scan mode.

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
XMP/$\overline{MC}$	F1	17	–	I	PD	Microprocessor/Microcomputer Mode Select. Switches between microprocessor and microcomputer mode. When high, Zone 7 is enabled on the external interface. When low, Zone 7 is disabled from the external interface, and on-chip boot ROM may be accessed instead. This signal is latched into the XINTCNF2 register on a reset and the user can modify this bit in software. The state of the XMP/$\overline{MC}$ pin is ignored after reset.
$\overline{XHOLD}$	E7	159	–	I	PU	External Hold Request. $\overline{XHOLD}$, when active (low), requests the XINTF to release the external bus and place all buses and strobes into a high-impedance state. The XINTF will release the bus when any current access is complete and there are no pending accesses on the XINTF.
$\overline{XHOLDA}$	K10	82	–	O/Z	–	External Hold Acknowledge. $\overline{XHOLDA}$ is driven active (low) when the XINTF has granted a $\overline{XHOLD}$ request. All XINTF buses and strobe signals will be in a high-impedance state. $\overline{XHOLDA}$ is released when the $\overline{XHOLD}$ signal is released. External devices should only drive the external bus when $\overline{XHOLDA}$ is active (low).
$\overline{XZCS0AND1}$	P1	44	–	O/Z	–	XINTF Zone 0 and Zone 1 Chip Select. $\overline{XZCS0AND1}$ is active (low) when an access to the XINTF Zone 0 or Zone 1 is performed.
$\overline{XZCS2}$	P13	88	–	O/Z	–	XINTF Zone 2 Chip Select. $\overline{XZCS2}$ is active (low) when an access to the XINTF Zone 2 is performed.
$\overline{XZCS6AND7}$	B13	133	–	O/Z	–	XINTF Zone 6 and Zone 7 Chip Select. $\overline{XZCS6AND7}$ is active (low) when an access to the XINTF Zone 6 or Zone 7 is performed.
$\overline{XWE}$	N11	84	–	O/Z	–	Write Enable. Active-low write strobe. The write strobe waveform is specified, per zone basis, by the Lead, Active, and Trail periods in the XTIMINGx registers.
$\overline{XRD}$	M3	42	–	O/Z	–	Read Enable. Active-low read strobe. The read strobe waveform is specified, per zone basis, by the Lead, Active, and Trail periods in the XTIMINGx registers. **NOTE:** The $\overline{XRD}$ and $\overline{XWE}$ signals are mutually exclusive.
XR/$\overline{W}$	N4	51	–	O/Z	–	Read Not Write Strobe. Normally held high. When low, XR/$\overline{W}$ indicates write cycle is active; when high, XR/$\overline{W}$ indicates read cycle is active.
XREADY	B6	161	–	I	PU	Ready Signal. Indicates peripheral is ready to complete the access when asserted to 1. XREADY can be configured to be a synchronous or an asynchronous input. See the timing diagrams for more details.

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
JTAG AND MISCELLANEOUS SIGNALS						
X1/XCLKIN	K9	77	58	I	–	Oscillator Input – input to the internal oscillator. This pin is also used to feed an external clock. The 28x can be operated with an external clock source, provided that the proper voltage levels be driven on the X1/XCLKIN pin. It should be noted that the X1/XCLKIN pin is referenced to the 1.8-V (or 1.9-V) core digital power supply (V_{DD}), rather than the 3.3-V I/O supply (V_{DDIO}). A clamping diode may be used to clamp a buffered clock signal to ensure that the logic-high level does not exceed V_{DD} (1.8 V or 1.9 V) or a 1.8-V oscillator may be used.
X2	M9	76	57	O	–	Oscillator Output
XCLKOUT	F11	119	87	O	–	Output clock derived from SYSCLKOUT to be used for external wait-state generation and as a general-purpose clock source. XCLKOUT is either the same frequency, 1/2 the frequency, or 1/4 the frequency of SYSCLKOUT. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting bit 3 (CLKOFF) of the XINTCNF2 register to 1. Unlike other GPIO pins, the XCLKOUT pin is not placed in a high-impedance state during reset.
TESTSEL	A13	134	97	I	PD	Test Pin. Reserved for TI. Must be connected to ground.
$\overline{XRS}$	D6	160	113	I/O	PU	Device Reset (in) and Watchdog Reset (out). Device reset. $\overline{XRS}$ causes the device to terminate execution. The PC will point to the address contained at the location 0x3FFFC0. When $\overline{XRS}$ is brought to a high level, execution begins at the location pointed to by the PC. This pin is driven low by the DSP when a watchdog reset occurs. During watchdog reset, the $\overline{XRS}$ pin will be driven low for the watchdog reset duration of 512 XCLKIN cycles. The output buffer of this pin is an open-drain with an internal pullup (100 µA, typical). If this pin is driven by an external device, it should be done using an open-drain device.
TEST1	M7	67	51	I/O	–	Test Pin. Reserved for TI. On F281x devices, TEST1 must be left unconnected.
TEST2	N7	66	50	I/O	–	Test Pin. Reserved for TI. On F281x devices, TEST2 must be left unconnected.

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
JTAG						
$\overline{\text{TRST}}$	B12	135	98	I	PD	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. **NOTE:** Do not use pullup resistors on $\overline{\text{TRST}}$; it has an internal pulldown device. $\overline{\text{TRST}}$ is an active-high test pin and must be maintained low at all times during normal device operation. In a low-noise environment, $\overline{\text{TRST}}$ may be left floating. In other instances, an external pulldown resistor is highly recommended. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
TCK	A12	136	99	I	PU	JTAG test clock with internal pullup
TMS	D13	126	92	I	PU	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
TDI	C13	131	96	I	PU	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	D12	127	93	O/Z	–	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK.
EMU0	D11	137	100	I/O/Z	PU	Emulator pin 0. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
EMU1	C9	146	105	I/O/Z	PU	Emulator pin 1. When $\overline{TRST}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{TRST}$ pin would latch the device into boundary-scan mode. **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
ADC ANALOG INPUT SIGNALS						
ADCINA7	B5	167	119	I	–	8-channel analog inputs for Sample-and-Hold A. The ADC pins should not be driven before the V_{DDA1}, V_{DDA2}, and V_{DDAIO} pins have been fully powered up.
ADCINA6	D5	168	120	I	–	
ADCINA5	E5	169	121	I	–	
ADCINA4	A4	170	122	I	–	
ADCINA3	B4	171	123	I	–	
ADCINA2	C4	172	124	I	–	
ADCINA1	D4	173	125	I	–	
ADCINA0	A3	174	126	I	–	
ADCINB7	F5	9	9	I	–	8-channel analog inputs for Sample-and-Hold B. The ADC pins should not be driven before the V_{DDA1}, V_{DDA2}, and V_{DDAIO} pins have been fully powered up.
ADCINB6	D1	8	8	I	–	
ADCINB5	D2	7	7	I	–	
ADCINB4	D3	6	6	I	–	
ADCINB3	C1	5	5	I	–	
ADCINB2	B1	4	4	I	–	
ADCINB1	C3	3	3	I	–	
ADCINB0	C2	2	2	I	–	
ADCREFP	E2	11	11	I/O	–	ADC Voltage Reference Output (2 V). Requires a low ESR (under 1.5 Ω) ceramic bypass capacitor of 10 µF to analog ground. [Can accept external reference input (2 V) if the software bit is enabled for this mode. 1–10 µF low ESR capacitor can be used in the external reference mode.] **NOTE:** Use the ADC Clock rate to derive the ESR specification from the capacitor data sheet that is used in the system.
ADCREFM	E4	10	10	I/O	–	ADC Voltage Reference Output (1 V). Requires a low ESR (under 1.5 Ω) ceramic bypass capacitor of 10 µF to analog ground. [Can accept external reference input (1 V) if the software bit is enabled for this mode. 1–10 µF low ESR capacitor can be used in the external reference mode.] **NOTE:** Use the ADC Clock rate to derive the ESR specification from the capacitor data sheet that is used in the system.

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
ADCRESEXT	F2	16	16	O	–	ADC External Current Bias Resistor. Use 24.9 kΩ ± 5% for ADC clock range 1–18.75 MHz; use 20 kΩ ± 5% for ADC clock range 18.75 MHz–25 MHz.
ADCBGREFIN	E6	164	116	–	–	Test Pin. Reserved for TI. Must be left unconnected.
AVSSREFBG	E3	12	12	–	–	ADC Analog GND
AVDDREFBG	E1	13	13	–	–	ADC Analog Power (3.3-V)
ADCLO	B3	175	127	–	–	Common Low Side Analog Input. Connect to analog ground.
V_{SSA1}	F3	15	15	–	–	ADC Analog GND
V_{SSA2}	C5	165	117	–	–	ADC Analog GND
V_{DDA1}	F4	14	14	–	–	ADC Analog 3.3-V Supply
V_{DDA2}	A5	166	118	–	–	ADC Analog 3.3-V Supply
V_{SS1}	C6	163	115	–	–	ADC Digital GND
V_{DD1}	A6	162	114	–	–	ADC Digital 1.8-V (or 1.9-V) Supply
V_{DDAIO}	B2	1	1	–	–	3.3-V Analog I/O Power Pin
V_{SSAIO}	A2	176	128	–	–	Analog I/O Ground Pin
POWER SIGNALS						
V_{DD}	H1	23	20	–	–	1.8-V or 1.9-V Core Digital Power Pins. See Section 5.4, Recommended Operating Conditions, for voltage requirements.
V_{DD}	L1	37	29	–	–	
V_{DD}	P5	56	42	–	–	
V_{DD}	P9	75	56	–	–	
V_{DD}	P12	–	63	–	–	
V_{DD}	K12	100	74	–	–	
V_{DD}	G12	112	82	–	–	
V_{DD}	C14	128	94	–	–	
V_{DD}	B10	143	102	–	–	
V_{DD}	C8	154	110	–	–	
V_{SS}	G4	19	17	–	–	Core and Digital I/O Ground Pins
V_{SS}	K1	32	26	–	–	
V_{SS}	L2	38	30	–	–	
V_{SS}	P4	52	39	–	–	
V_{SS}	K6	58	–	–	–	
V_{SS}	P8	70	53	–	–	
V_{SS}	M10	78	59	–	–	
V_{SS}	L11	86	62	–	–	
V_{SS}	K13	99	73	–	–	
V_{SS}	J14	105	–	–	–	
V_{SS}	G13	113	–	–	–	
V_{SS}	E14	120	88	–	–	
V_{SS}	B14	129	95	–	–	
V_{SS}	D10	142	–	–	–	
V_{SS}	C10	–	103	–	–	
V_{SS}	B8	153	109	–	–	

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
V_{DDIO}	J4	31	25	–	–	3 3-V I/O Digital Power Pins
V_{DDIO}	L7	64	49	–	–	
V_{DDIO}	L10	81	–	–	–	
V_{DDIO}	N14	–	–	–	–	
V_{DDIO}	G11	114	83	–	–	
V_{DDIO}	E9	145	104	–	–	
V_{DD3VFL}	N8	69	52	–	–	3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times after power-up sequence requirements have been met.
GPIO OR PERIPHERAL SIGNALS						
GPIOA OR EVA SIGNALS						
GPIOA0 - PWM1 (O)	M12	92	68	I/O	PU	GPIO or PWM Output Pin #1
GPIOA1 - PWM2 (O)	M14	93	69	I/O	PU	GPIO or PWM Output Pin #2
GPIOA2 - PWM3 (O)	L12	94	70	I/O	PU	GPIO or PWM Output Pin #3
GPIOA3 - PWM4 (O)	L13	95	71	I/O	PU	GPIO or PWM Output Pin #4
GPIOA4 - PWM5 (O)	K11	98	72	I/O	PU	GPIO or PWM Output Pin #5
GPIOA5 - PWM6 (O)	K14	101	75	I/O	PU	GPIO or PWM Output Pin #6
GPIOA6 - T1PWM_T1CMP (I)	J11	102	76	I/O	PU	GPIO or Timer 1 Output
GPIOA7 - T2PWM_T2CMP (I)	J13	104	77	I/O	PU	GPIO or Timer 2 Output
GPIOA8 - CAP1_QEP1 (I)	H10	106	78	I/O	PU	GPIO or Capture Input #1
GPIOA9 - CAP2_QEP2 (I)	H11	107	79	I/O	PU	GPIO or Capture Input #2
GPIOA10 - CAP3_QEPI1 (I)	H12	109	80	I/O	PU	GPIO or Capture Input #3
GPIOA11 - TDIRA (I)	F14	116	85	I/O	PU	GPIO or Timer Direction
GPIOA12 - TCLKINA (I)	F13	117	86	I/O	PU	GPIO or Timer Clock Input
GPIOA13 - $\overline{\text{C1TRIP}}$ (I)	E13	122	89	I/O	PU	GPIO or Compare 1 Output Trip
GPIOA14 - $\overline{\text{C2TRIP}}$ (I)	E11	123	90	I/O	PU	GPIO or Compare 2 Output Trip
GPIOA15 - $\overline{\text{C3TRIP}}$ (I)	F10	124	91	I/O	PU	GPIO or Compare 3 Output Trip
GPIOB OR EVB SIGNALS						
GPIOB0 - PWM7 (O)	N2	45	33	I/O	PU	GPIO or PWM Output Pin #7
GPIOB1 - PWM8 (O)	P2	46	34	I/O	PU	GPIO or PWM Output Pin #8
GPIOB2 - PWM9 (O)	N3	47	35	I/O	PU	GPIO or PWM Output Pin #9
GPIOB3 - PWM10 (O)	P3	48	36	I/O	PU	GPIO or PWM Output Pin #10
GPIOB4 - PWM11 (O)	L4	49	37	I/O	PU	GPIO or PWM Output Pin #11
GPIOB5 - PWM12 (O)	M4	50	38	I/O	PU	GPIO or PWM Output Pin #12
GPIOB6 - T3PWM_T3CMP (I)	K5	53	40	I/O	PU	GPIO or Timer 3 Output
GPIOB7 - T4PWM_T4CMP (I)	N5	55	41	I/O	PU	GPIO or Timer 4 Output
GPIOB8 - CAP4_QEP3 (I)	M5	57	43	I/O	PU	GPIO or Capture Input #4
GPIOB9 - CAP5_QEP4 (I)	M6	59	44	I/O	PU	GPIO or Capture Input #5
GPIOB10 - CAP6_QEPI2 (I)	P6	60	45	I/O	PU	GPIO or Capture Input #6
GPIOB11 - TDIRB (I)	L8	71	54	I/O	PU	GPIO or Timer Direction
GPIOB12 - TCLKINB (I)	K8	72	55	I/O	PU	GPIO or Timer Clock Input
GPIOB13 - $\overline{\text{C4TRIP}}$ (I)	N6	61	46	I/O	PU	GPIO or Compare 4 Output Trip

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
GPIOB14 - C5TRIP (I)	L6	62	47	I/O	PU	GPIO or Compare 5 Output Trip
GPIOB15 - C6TRIP (I)	K7	63	48	I/O	PU	GPIO or Compare 6 Output Trip
GPIOD OR EVA SIGNALS						
GPIOD0 - T1CTRIP_PDPINTA (I)	H14	110	81	I/O	PU	GPIO or Timer 1 Compare Output Trip
GPIOD1 - T2CTRIP/EVASOC (I)	G10	115	84	I/O	PU	GPIO or Timer 2 Compare Output Trip or External ADC Start-of-Conversion EV-A
GPIOD OR EVB SIGNALS						
GPIOD5 - T3CTRIP_PDPINTB (I)	P10	79	60	I/O	PU	GPIO or Timer 3 Compare Output Trip
GPIOD6 - T4CTRIP/EVBSOC (I)	P11	83	61	I/O	PU	GPIO or Timer 4 Compare Output Trip or External ADC Start-of-Conversion EV-B
GPIOE OR INTERRUPT SIGNALS						
GPIOE0 - XINT1_XBIO (I)	D9	149	106	I/O/Z	–	GPIO or XINT1 or XBIO input
GPIOE1 - XINT2_ADCSOC (I)	D8	151	108	I/O/Z	–	GPIO or XINT2 or ADC start-of-conversion
GPIOE2 - XNMI_XINT13 (I)	E8	150	107	I/O	PU	GPIO or XNMI or XINT13
GPIOF OR SPI SIGNALS						
GPIOF0 - SPISIMOA (O)	M1	40	31	I/O/Z	–	GPIO or SPI slave in, master out
GPIOF1 - SPISOMIA (I)	N1	41	32	I/O/Z	–	GPIO or SPI slave out, master in
GPIOF2 - SPICLKA (I/O)	K2	34	27	I/O/Z	–	GPIO or SPI clock
GPIOF3 - SPISTEA (I/O)	K4	35	28	I/O/Z	–	GPIO or SPI slave transmit enable
GPIOF OR SCI-A SIGNALS						
GPIOF4 - SCITXDA (O)	C7	155	111	I/O	PU	GPIO or SCI asynchronous serial port TX data
GPIOF5 - SCIRXDA (I)	A7	157	112	I/O	PU	GPIO or SCI asynchronous serial port RX data
GPIOF OR CAN SIGNALS						
GPIOF6 - CANTXA (O)	N12	87	64	I/O	PU	GPIO or eCAN transmit data
GPIOF7 - CANRXA (I)	N13	89	65	I/O	PU	GPIO or eCAN receive data
GPIOF OR McBSP SIGNALS						
GPIOF8 - MCLKXA (I/O)	J1	28	23	I/O	PU	GPIO or McBSP transmit clock
GPIOF9 - MCLKRA (I/O)	H2	25	21	I/O	PU	GPIO or McBSP receive clock
GPIOF10 - MFSXA (I/O)	H4	26	22	I/O	PU	GPIO or McBSP transmit frame synch
GPIOF11 - MFSRA (I/O)	J2	29	24	I/O	PU	GPIO or McBSP receive frame synch
GPIOF12 - MDXA (O)	G1	22	19	I/O	–	GPIO or McBSP transmitted serial data
GPIOF13 - MDRA (I)	G2	20	18	I/O	PU	GPIO or McBSP received serial data

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Table 4-1. Signal Descriptions[1] (continued)

NAME	PIN NO.			I/O/Z[2]	PU/PD[3]	DESCRIPTION
	179-BALL GHH/ZHH	176-PIN PGF	128-PIN PBK			
GPIOF OR XF CPU OUTPUT SIGNAL						
GPIOF14 - XF_XPLLDIS (O)	A11	140	101	I/O	PU	This pin has three functions: 1. XF – General-purpose output pin. 2. XPLLDIS – This pin is sampled during reset to check whether the PLL must be disabled. The PLL will be disabled if this pin is sensed low. HALT and STANDBY modes cannot be used when the PLL is disabled. 3. GPIO – GPIO function
GPIOG OR SCI-B SIGNALS						
GPIOG4 - SCITXDB (O)	P14	90	66	I/O/Z	–	GPIO or SCI asynchronous serial port transmit data
GPIOG5 - SCIRXDB (I)	M13	91	67	I/O/Z	–	GPIO or SCI asynchronous serial port receive data

NOTE

Other than the power supply pins, no pin should be driven before the 3.3-V rail has reached recommended operating conditions. However, it is acceptable for an I/O pin to ramp along with the 3.3-V supply.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating temperature ranges (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{DDIO}	–0.3	4.6	V
	V_{DD3VFL}	–0.3	4.6	
	V_{DDA1}	–0.3	4.6	
	V_{DDA2}	–0.3	4.6	
	V_{DDAIO}	–0.3	4.6	
	AVDDREFBG	–0.3	4.6	
Supply voltage	V_{DD}	–0.5	2.5	V
	V_{DD1}	–0.5	2.5	
Input voltage	V_{IN}	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})(2)	–20	20	mA
Output clamp current	I_{OK} (V_O < 0 or V_O > V_{DDIO})	–20	20	mA
Operating ambient temperature, T_A	A version (GHH, ZHH, PGF, PBK)(3)	–40	85	°C
	S version (GHH, ZHH, PGF, PBK)(3)	–40	125	
	Q version (PGF, PBK)(3)	–40	125	
Junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}(3)	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V_{SS}.
(2) Continuous clamp current per pin is ±2 mA
(3) Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

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5.2 ESD Ratings – Commercial

			VALUE	UNIT
TMS320F2812 in 179-ball ZHH package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	
TMS320F2812 in 179-ball GHH package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings – Automotive

				VALUE	UNIT
TMS320F2812 in 176-pin PGF package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PGF: 1, 44, 45, 88, 89, 132, 133, 176	±750	
TMS320F2810 and TMS320F2811 in 128-pin PBK package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 128-pin PBK: 1, 32, 33, 64, 65, 96, 97, 128	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.4 Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		3.14	3.3	3.47	V
Device supply voltage, CPU, V_{DD}, V_{DD1}	1.8 V (135 MHz)	1.71	1.8	1.89	V
	1.9 V (150 MHz)	1.81	1.9	2	
Supply ground, V_{SS}			0		V
ADC supply voltage, V_{DDA1}, V_{DDA2}, AVDDREFBG, V_{DDAIO}		3.14	3.3	3.47	V
Flash programming supply voltage, V_{DD3VFL}		3.14	3.3	3.47	V
Device clock frequency (system clock), $f_{SYSCLKOUT}$	V_{DD} = 1.9 V ± 5%	2		150	MHz
	V_{DD} = 1.8 V ± 5%	2		135	
High-level input voltage, V_{IH}	All inputs except X1/XCLKIN	2		V_{DDIO}	V
	X1/XCLKIN (@ 50 µA max)	$0.7V_{DD}$		V_{DD}	
Low-level input voltage, V_{IL}	All inputs except X1/XCLKIN			0.8	V
	X1/XCLKIN (@ 50 µA max)			$0.3V_{DD}$	
High-level output source current, V_{OH} = 2.4 V, I_{OH}	All I/Os except Group 2			–4	mA
	Group 2(2)			–8	
Low-level output sink current, V_{OL} = V_{OL} MAX, I_{OL}	All I/Os except Group 2			4	mA
	Group 2(2)			8	
Ambient temperature, T_A	A version	–40		85	°C
	S version	–40		125	
	Q version	–40		125	

(1) See Section 5.12.2 for power sequencing of V_{DDIO}, V_{DDAIO}, V_{DD}, V_{DDA1}/V_{DDA2}/AVDDREFBG, and V_{DD3VFL}.
(2) Group 2 pins are as follows: XINTF pins, T1CTRIP_PDPINTA, TDO, XCLKOUT, XF, EMU0, and EMU1.

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5.5 Power Consumption Summary

Table 5-1. TMS320F281x Current Consumption by Power-Supply Pins Over Recommended Operating Conditions During Low-Power Modes at 150-MHz SYSCLKOUT

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DD3VFL}		I_{DDA} (2)	
		TYP	MAX (3)	TYP	MAX (3)	TYP	MAX (3)	TYP	MAX (3)
Operational	All peripheral clocks are enabled. All PWM pins are toggled at 100 kHz. Data is continuously transmitted out of the SCIA, SCIB, and CAN ports. The hardware multiplier is exercised. Code is running out of flash with 5 wait-states.	195 mA (4)	230 mA	15 mA	30 mA	40 mA	45 mA	40 mA	50 mA
IDLE	• Flash is powered down • XCLKOUT is turned off • All peripheral clocks are on, except ADC	125 mA	150 mA	5 mA	10 mA	2 µA	4 µA	1 µA	20 µA
STANDBY	• Flash is powered down • Peripheral clocks are turned off • Pins without an internal PU/PD are tied high/low	5 mA	10 mA	5 µA	20 µA	2 µA	4 µA	1 µA	20 µA
HALT	• Flash is powered down • Peripheral clocks are turned off • Pins without an internal PU/PD are tied high/low • Input clock is disabled	70 µA		5 µA	20 µA	2 µA	4 µA	1 µA	20 µA

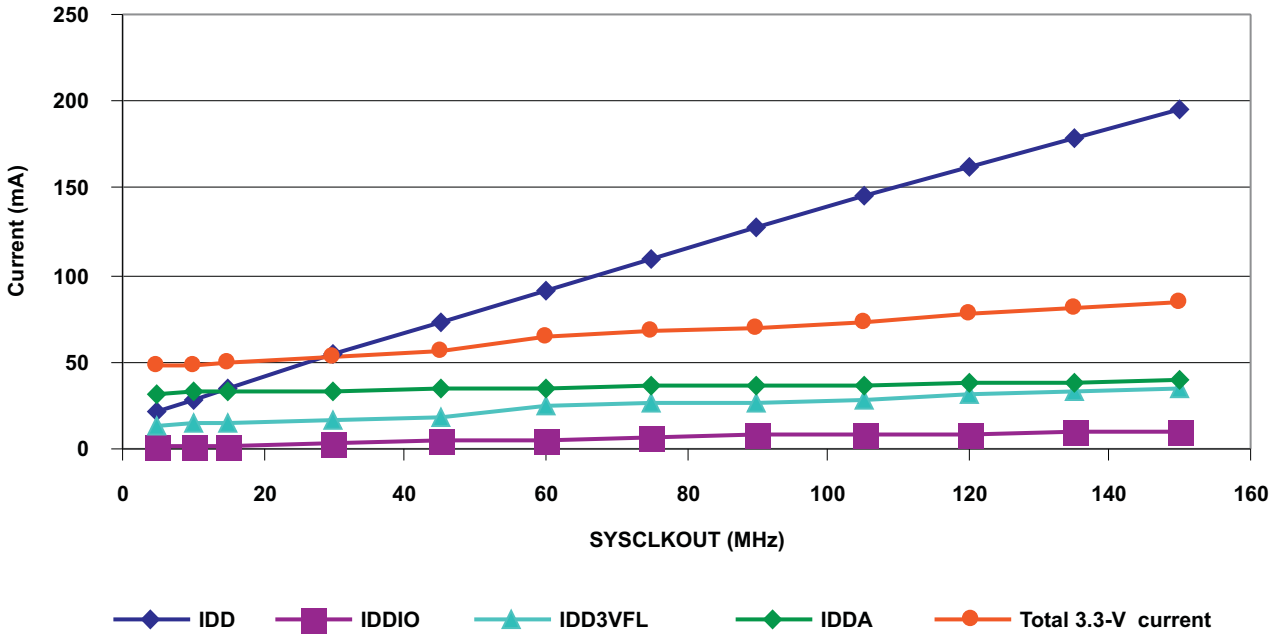
(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) I_{DDA} includes current into V_{DDA1}, V_{DDA2}, AVDDREFBG, and V_{DDAIO} pins.
(3) MAX numbers are at 125°C, and MAX voltage (V_{DD} = 1.89 V; V_{DDIO}, V_{DD3VFL}, V_{DDA} = 3.47 V).
(4) I_{DD} represents the total current drawn from the 1.8-V rail (V_{DD}). It includes a small amount of current (<1 mA) drawn by V_{DD1}.

NOTE

HALT and STANDBY modes cannot be used when the PLL is disabled.

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5.5.1 Current Consumption Graphs



A. Test conditions are as defined in Table 5-1 for operational currents.
B. I_{DD} represents the total current drawn from the 1.8-V rail (V_{DD}). It includes a small amount of current (<1 mA) drawn by V_{DD1}.
C. I_{DDA} represents the current drawn by V_{DDA1} and V_{DDA2} rails.
D. Total 3.3-V current is the sum of I_{DDIO}, I_{DD3VFL}, and I_{DDA}. It includes a small amount of current (<1 mA) drawn by V_{DDAIO}.

Figure 5-1. Typical Current Consumption Over Frequency

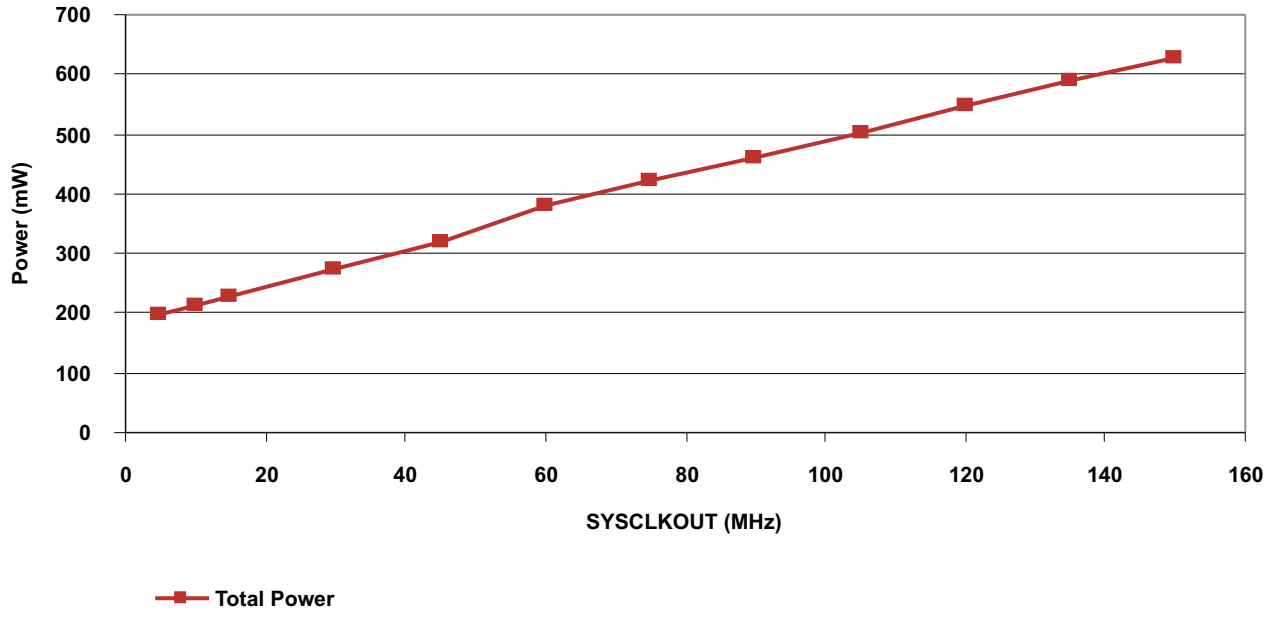


Figure 5-2. Typical Power Consumption Over Frequency

5.5.2 Reducing Current Consumption

28x DSPs incorporate a unique method to reduce the device current consumption. A reduction in current consumption can be achieved by turning off the clock to any peripheral module which is not used in a given application. Table 5-2 indicates the typical reduction in current consumption achieved by turning off the clocks to various peripherals.

Table 5-2. Typical Current Consumption by Various Peripherals (at 150 MHz)(1)(2)

PERIPHERAL MODULE	I_{DD} CURRENT REDUCTION (mA)
eCAN	12
EVA	6
EVB	6
ADC	8(3)
SCI	4
SPI	5
McBSP	13

(1) All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) Power savings can be achieved by powering down the flash. This must be done by code running off RAM (not flash).
(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.

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5.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}$ MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}$ MAX				0.4	V
I_{IL}	Input current (low level)	With pullup	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os[1] (including XRS) except EVB	–80	–140	–190	µA
				GPIOB/EVB	–13	–25	–35	
		With pulldown	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	With pullup	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$				±2	µA
		With pulldown[2]	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$		28	50	80	
I_{OZ}	Leakage current (for pins without internal PU/PD), high-impedance state (off-state)		$V_O = V_{DDIO}$ or 0 V				±2	µA
C_i	Input capacitance					2		pF
C_o	Output capacitance					3		pF

(1) The following pins have no internal PU/PD: GPIOE0, GPIOE1, GPIOF0, GPIOF1, GPIOF2, GPIOF3, GPIOF12, GPIOG4, and GPIOG5.
(2) The following pins have an internal pulldown: XMP/MC, TESTSEL, and TRST.

5.7 Thermal Resistance Characteristics for 179-Ball ZHH Package

		°C/W[1]
$R\Theta_{JC}$	Junction-to-case thermal resistance	16.08
$R\Theta_{JA}$	Junction-to-free air thermal resistance	42.57
Psi_{JT}	Junction-to-package top	0.658

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

5.8 Thermal Resistance Characteristics for 179-Ball GHH Package

		°C/W[1]
$R\Theta_{JC}$	Junction-to-case thermal resistance	16.08
$R\Theta_{JA}$	Junction-to-free air thermal resistance	42.57
Psi_{JT}	Junction-to-package top	0.658

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

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5.9 Thermal Resistance Characteristics for 176-Pin PGF Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance	9.73
$R\Theta_{JA}$	Junction-to-free air thermal resistance	41.88
Psi_{JT}	Junction-to-package top	0.247

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

5.10 Thermal Resistance Characteristics for 128-Pin PBK Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance	10.76
$R\Theta_{JA}$	Junction-to-free air thermal resistance	41.65
Psi_{JT}	Junction-to-package top	0.271

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

5.11 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

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5.12 Timing and Switching Characteristics

5.12.1 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

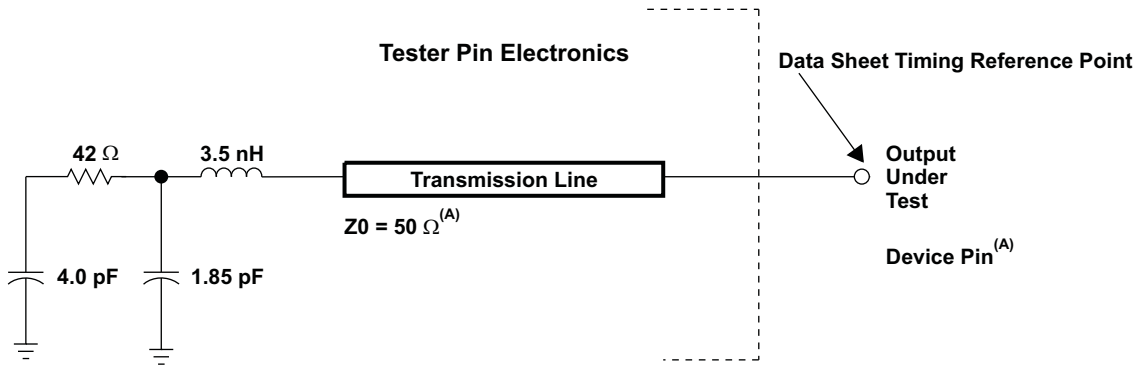
5.12.1.1 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

5.12.1.2 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-3. 3.3-V Test Load Circuit

5.12.1.3 Signal Transition Levels

Note that some of the signals use different reference voltages, see the recommended operating conditions table. Output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.4 V.

Figure 5-4 shows output levels.

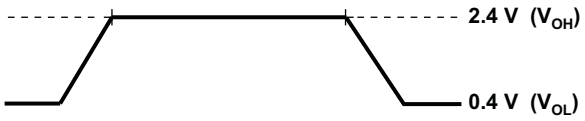


Figure 5-4. Output Levels

Output transition times are specified as follows:

- For a *high-to-low* transition, the level at which the output is said to be no longer high is below $V_{OH(MIN)}$ and the level at which the output is said to be low is $V_{OL(MAX)}$ and lower.
- For a *low-to-high* transition, the level at which the output is said to be no longer low is above $V_{OL(MAX)}$ and the level at which the output is said to be high is $V_{OH(MIN)}$ and higher.

Figure 5-5 shows the input levels.

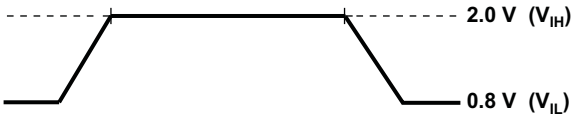


Figure 5-5. Input Levels

Input transition times are specified as follows:

- For a *high-to-low* transition on an input signal, the level at which the input is said to be no longer high is below $V_{IH(MIN)}$ and the level at which the input is said to be low is $V_{IL(MAX)}$ and lower.
- For a *low-to-high* transition on an input signal, the level at which the input is said to be no longer low is above $V_{IL(MAX)}$ and the level at which the input is said to be high is $V_{IH(MIN)}$ and higher.

NOTE

See the individual timing diagrams for levels used for testing timing parameters.

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5.12.2 Power Supply Sequencing

TMS320F2812/F2811/F2810 silicon requires dual voltages (1.8-V or 1.9-V and 3.3-V) to power up the CPU, Flash, ADC, and the I/Os. To ensure the correct reset state for all modules during power up, there are some requirements to be met while powering up/powering down the device.

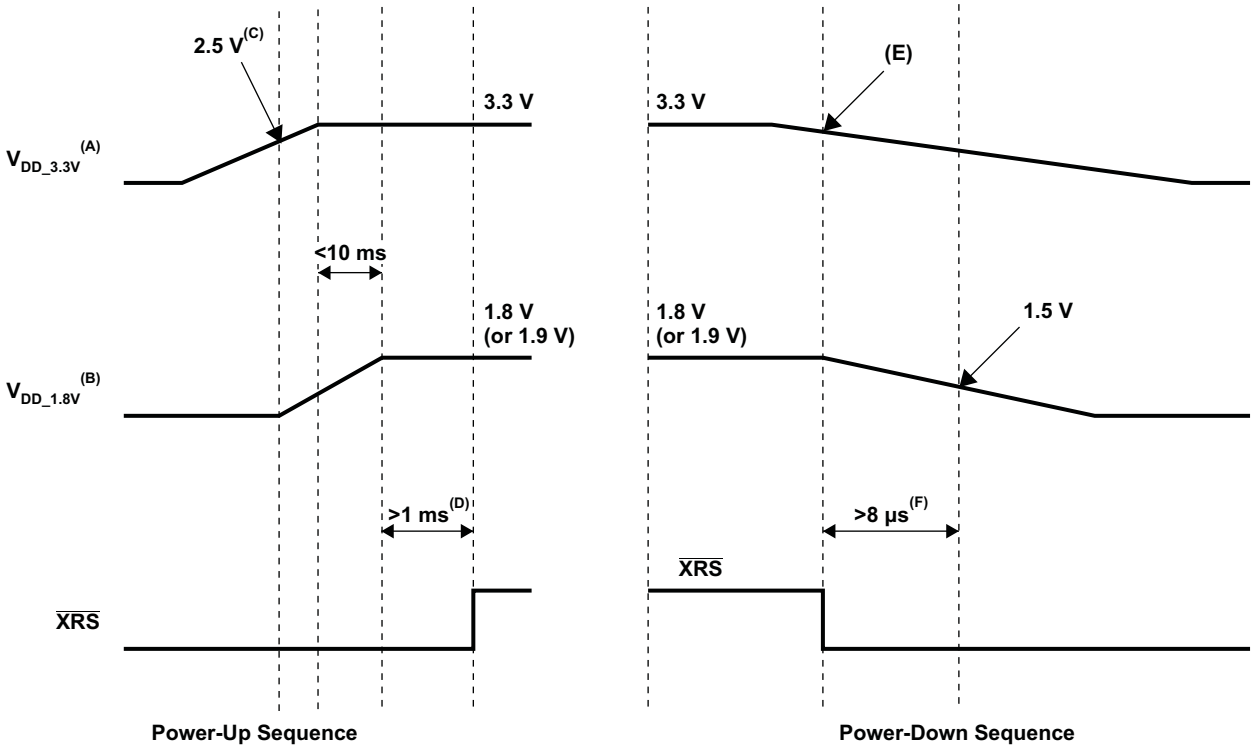
- Option 1:
  In this approach, an external power sequencing circuit enables V_{DDIO} first, then V_{DD} and V_{DD1} (1.8 V or 1.9 V). After 1.8 V (or 1.9 V) ramps, the 3.3 V for Flash (V_{DD3VFL}) and ADC (V_{DDA1}/V_{DDA2}/AVDDREFBG) modules are ramped up. While option 1 is still valid, TI has simplified the requirement. Option 2 is the recommended approach.
- Option 2:
  Enable power to all 3.3-V supply pins (V_{DDIO}, V_{DD3VFL}, V_{DDA1}/V_{DDA2}/V_{DDAIO}/AVDDREFBG) and then ramp 1.8 V (or 1.9 V) (V_{DD}/V_{DD1}) supply pins.

  1.8 V or 1.9 V (V_{DD}/V_{DD1}) should not reach 0.3 V until V_{DDIO} has reached 2.5 V. This ensures the reset signal from the I/O pin has propagated through the I/O buffer to provide power-on reset to all the modules inside the device. See Figure 5-7 for power-on reset timing.
- Power-Down Sequencing:
  During power-down, the device reset should be asserted low (8 µs, minimum) before the V_{DD} supply reaches 1.5 V. This will help to keep on-chip flash logic in reset prior to the V_{DDIO}/V_{DD} power supplies ramping down. It is recommended that the device reset control from “Low-Dropout (LDO)” regulators or voltage supervisors be used to meet this constraint. LDO regulators that facilitate power-sequencing (with the aid of additional external components) may be used to meet the power sequencing requirement. See www.spectrumdigital.com for F2812 eZdsp™ schematics and updates.

NOTE

The GPIO pins are undefined until V_{DD} = 1 V and V_{DDIO} = 2.5 V.

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A. $V_{DD_3.3V}$ – V_{DDIO}, V_{DD3VFL}, V_{DDAIO}, V_{DDA1}, V_{DDA2}, AVDDREFBG
B. $V_{DD_1.8V}$ – V_{DD}, V_{DD1}
C. 1.8-V (or 1.9-V) supply should ramp after the 3.3-V supply reaches at least 2.5 V.
D. Reset ($\overline{XRS}$) should remain low until supplies and clocks are stable. See Figure 5-7, Power-on Reset in Microcomputer Mode (XMP/$\overline{MC}$ = 0), for minimum requirements.
E. Voltage supervisor or LDO reset control will trip reset ($\overline{XRS}$) first when the 3.3-V supply is off regulation. Typically, this occurs a few milliseconds before the 1.8-V (or 1.9-V) supply reaches 1.5 V.
F. Keeping reset low ($\overline{XRS}$) at least 8 µs prior to the 1.8-V (or 1.9-V) supply reaching 1.5 V will keep the flash module in complete reset before the supplies ramp down.
G. Since the state of GPIO pins is undefined until the 1.8-V (or 1.9-V) supply reaches at least 1 V, this supply should be ramped as quickly as possible (after the 3.3-V supply reaches at least 2.5 V).
H. Other than the power supply pins, no pin should be driven before the 3.3-V rail has been fully powered up.

Figure 5-6. F2812/F2811/F2810 Typical Power-Up and Power-Down Sequence – Option 2

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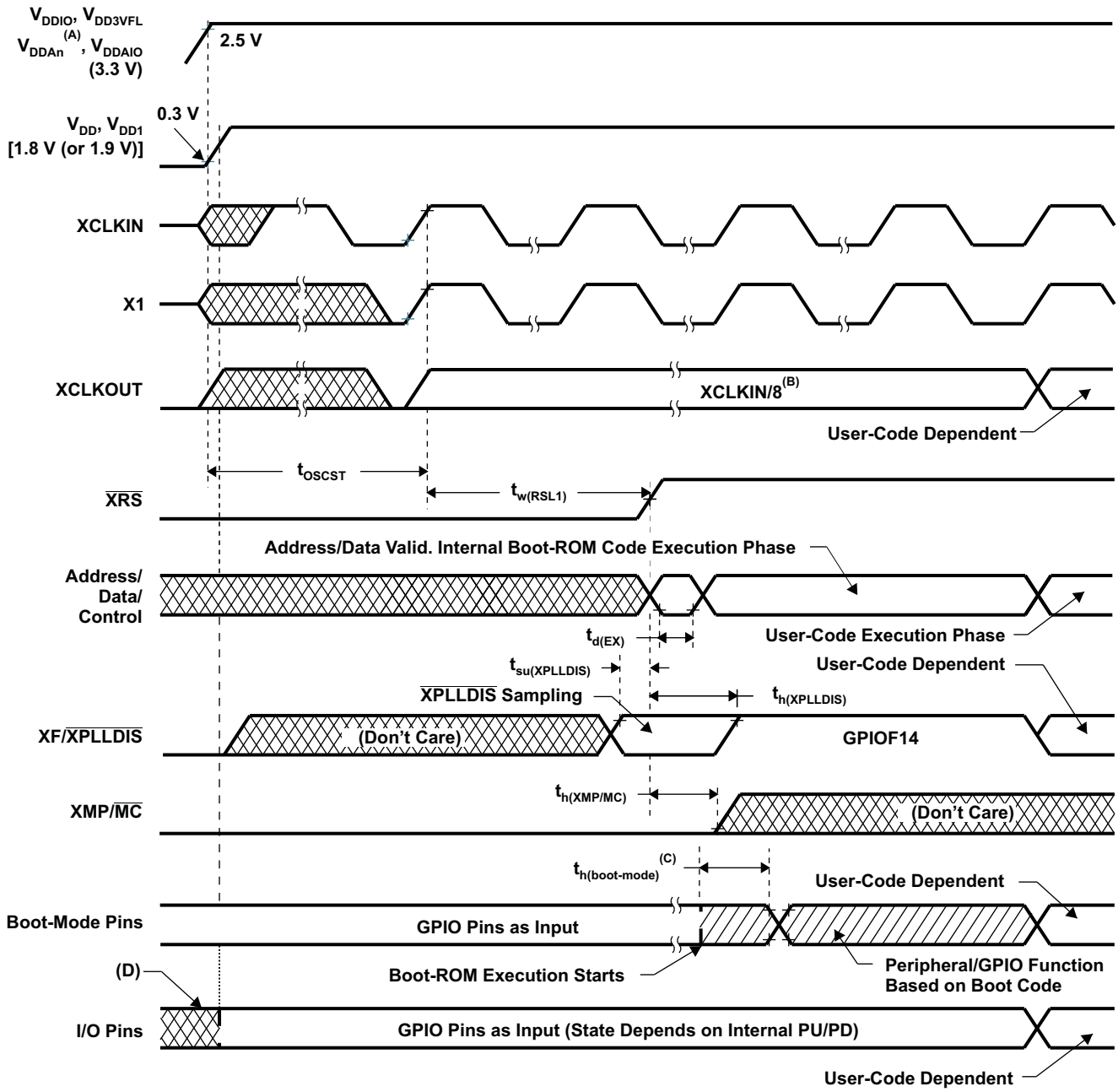
5.12.3 Reset Timing

Table 5-3. Reset ($\overline{XRS}$) Timing Requirements(1)

			MIN	NOM	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, stable XCLKIN to $\overline{XRS}$ high		$8t_{c(CI)}$			cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low	Warm reset	$8t_{c(CI)}$			cycles
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(CI)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(CI)}$		cycles
t_{OSCST}(2)	Oscillator start-up time		1	10		ms
$t_{su(XPLLDIS)}$	Setup time for $\overline{XPLLDIS}$ pin		$16t_{c(CI)}$			cycles
$t_{h(XPLLDIS)}$	Hold time for $\overline{XPLLDIS}$ pin		$16t_{c(CI)}$			cycles
$t_{h(XMP/MC)}$	Hold time for XMP/$\overline{MC}$ pin		$16t_{c(CI)}$			cycles
$t_{h(boot-mode)}$	Hold time for boot-mode pins		$2520t_{c(CI)}$(3)			cycles

(1) If external oscillator/clock source are used, reset time has to be low at least for 1 ms after V_{DD} reaches 1.5 V.
(2) Dependent on crystal/resonator and board design.
(3) The boot ROM reads the password locations. Therefore, this timing requirement includes the wakeup time for flash. See the *TMS320x281x DSP Boot ROM Reference Guide* and the *TMS320x281x DSP System Control and Interrupts Reference Guide* for further information.

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A. V_{DDAn} – V_{DDA1}/V_{DDA2} and AVDDREFBG

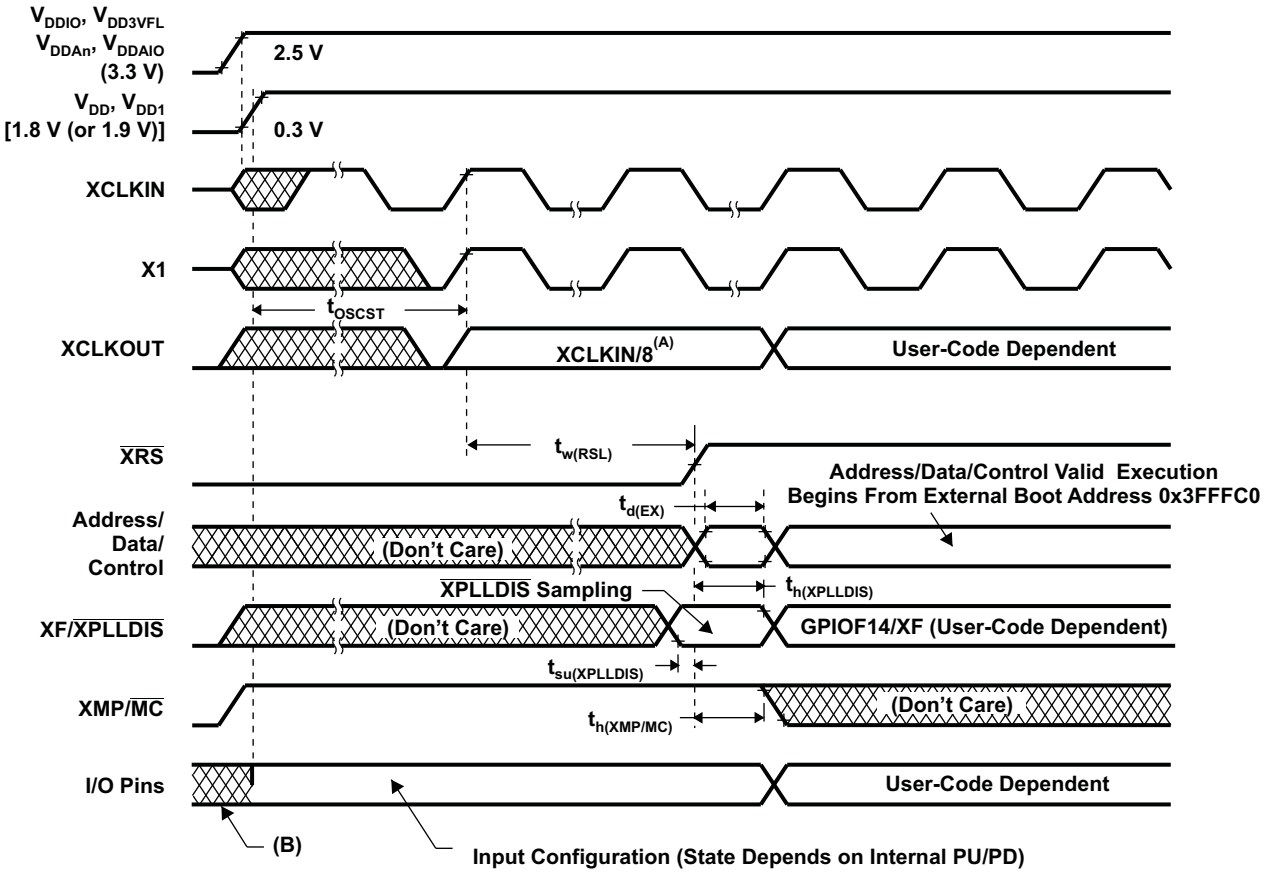
B. Upon power up, SYSCLKOUT is XCLKIN/2 if the PLL is enabled. Since both the XTIMCLK and CLKMODE bits in the XINTCNF2 register come up with a reset state of 1, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = XCLKIN/8 during this phase.

C. After reset, the Boot ROM code executes instructions for 1260 SYSCLKOUT cycles (SYSCLKOUT = XCLKIN/2) and then samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function in ROM. The BOOT Mode pins should be held high/low for at least 2520 XCLKIN cycles from boot ROM execution time for proper selection of Boot modes.
If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

D. The state of the GPIO pins is undefined (that is, they could be input or output) until the 1.8-V (or 1.9-V) supply reaches at least 1 V and 3.3-V supply reaches 2.5 V.

Figure 5-7. Power-on Reset in Microcomputer Mode (XMP/$\overline{MC}$ = 0) (See Note D)

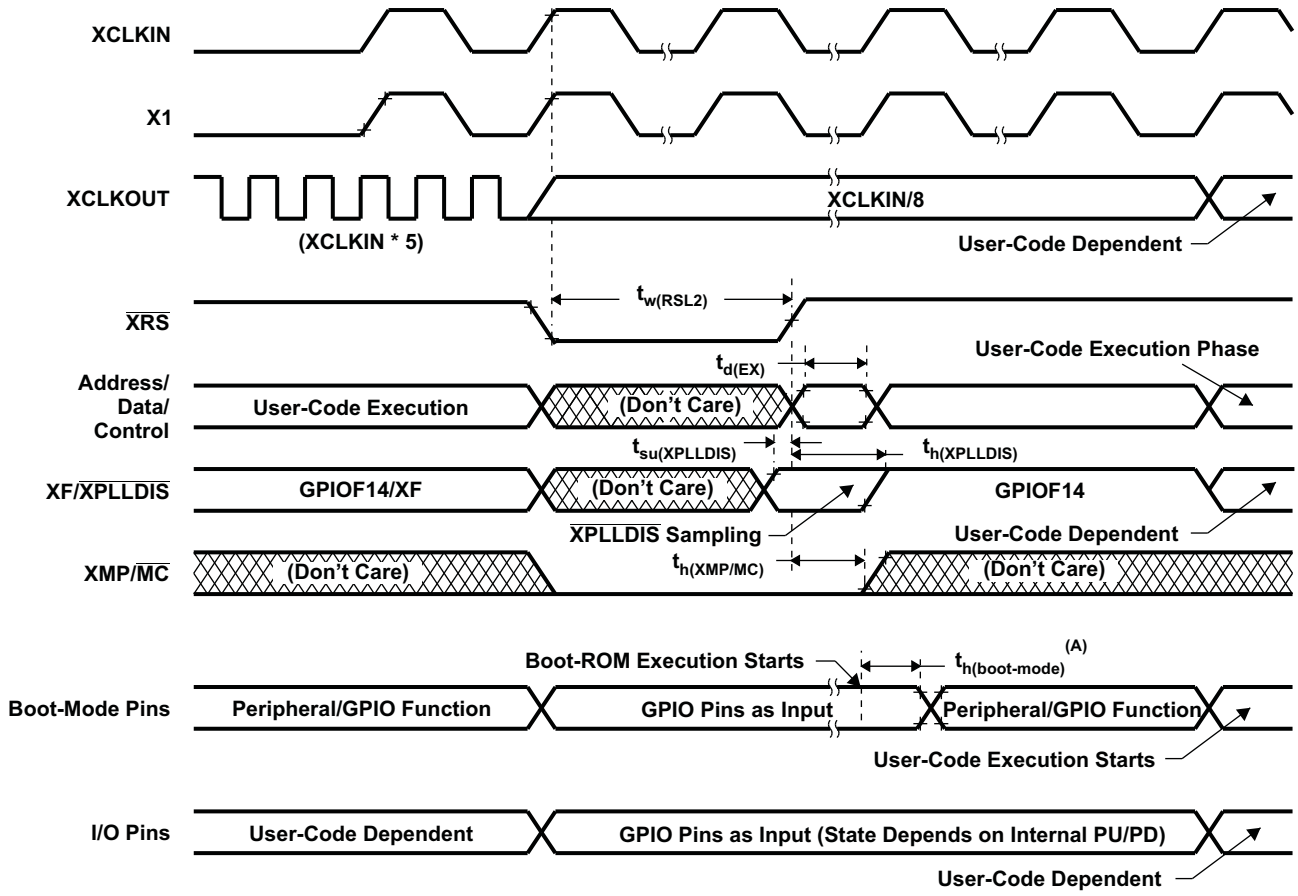
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A. Upon power up, SYSCLKOUT is XCLKIN/2 if the PLL is enabled. Since both the XTIMCLK and CLKMODE bits in the XINTCNF2 register come up with a reset state of 1, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = XCLKIN/8 during this phase.

B. The state of the GPIO pins is undefined (that is, they could be input or output) until the 1.8-V (or 1.9-V) supply reaches at least 1 V and 3.3-V supply reaches 2.5 V.

Figure 5-8. Power-on Reset in Microprocessor Mode (XMP/$\overline{MC}$ = 1)



A. After reset, the Boot ROM code executes instructions for 1260 SYSCLKOUT cycles (SYSCLKOUT = XCLKIN/2) and then samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function in ROM. The BOOT Mode pins should be held high/low for at least 2520 XCLKIN cycles from boot ROM execution time for proper selection of Boot modes.
If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 5-9. Warm Reset in Microcomputer Mode

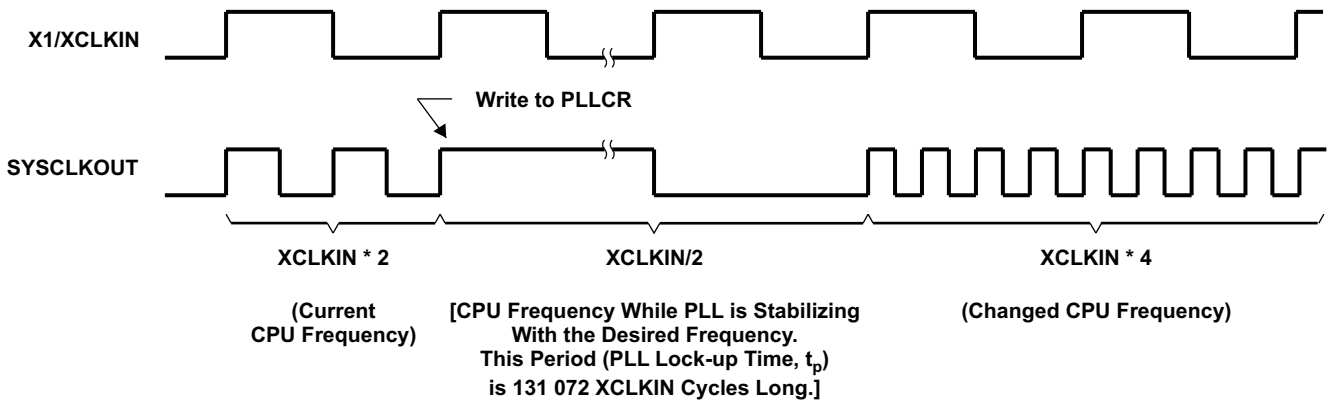


Figure 5-10. Effect of Writing Into PLLCR Register

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5.12.4 Clock Specifications

5.12.4.1 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the F281x DSPs. Table 5-4 lists the cycle times of various clocks.

Table 5-4. Clock Table and Nomenclature

		MIN	NOM	MAX	UNIT
On chip oscillator clock	$t_{c(OSC)}$, Cycle time	28.6		50	ns
	Frequency	20		35	MHz
XCLKIN	$t_{c(CI)}$, Cycle time	6.67		250	ns
	Frequency	4		150	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	6.67		500	ns
	Frequency	2		150	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	6.67		2000	ns
	Frequency	0.5		150	MHz
HSPCLK	$t_{c(HCO)}$, Cycle time	6.67	13.3(1)		ns
	Frequency		75(1)	150	MHz
LSPCLK	$t_{c(LCO)}$, Cycle time	13.3	26.6(1)		ns
	Frequency		37.5(1)	75	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time(2)	40			ns
	Frequency			25	MHz
SPI clock	$t_{c(SPC)}$, Cycle time	50			ns
	Frequency			20	MHz
McBSP	$t_{c(CKG)}$, Cycle time	50			ns
	Frequency			20	MHz
XTIMCLK	$t_{c(XTIM)}$, Cycle time	6.67			ns
	Frequency			150	MHz

(1) This is the default reset value if SYSCLKOUT = 150 MHz.
(2) The maximum value for ADCCLK frequency is 25 MHz. For SYSCLKOUT values of 25 MHz or lower, ADCCLK has to be SYSCLKOUT/2 or lower. ADCCLK = SYSCLKOUT is not a valid mode for any value of SYSCLKOUT.

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5.12.4.2 Clock Requirements and Characteristics

5.12.4.2.1 Input Clock Requirements

The clock provided at the XCLKIN pin generates the internal CPU clock cycle.

Table 5-5. Input Clock Frequency

PARAMETER				MIN	TYP	MAX	UNIT
f_x	Input clock frequency	Resonator		20		35	MHz
		Crystal		20		35	
		XCLKIN	Without PLL	4		150	
			With PLL	5		100	
f_l	Limp mode clock frequency				2		MHz

Table 5-6. XCLKIN Timing Requirements – PLL Bypassed or Enabled

NO.			MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN	6.67	250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, X1/XCLKIN low as a percentage of $t_{c(CI)}$	40	60	%
C12	$t_{w(CIH)}$	Pulse duration, X1/XCLKIN high as a percentage of $t_{c(CI)}$	40	60	%

Table 5-7. XCLKIN Timing Requirements – PLL Disabled

NO.				MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN		6.67	250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 30 MHz		6	ns
			30 MHz to 150 MHz		2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 30 MHz		6	ns
			30 MHz to 150 MHz		2	
C11	$t_{w(CIL)}$	Pulse duration, X1/XCLKIN low as a percentage of $t_{c(CI)}$	XCLKIN ≤ 120 MHz	40	60	%
			120 < XCLKIN ≤ 150 MHz	45	55	
C12	$t_{w(CIH)}$	Pulse duration, X1/XCLKIN high as a percentage of $t_{c(CI)}$	XCLKIN ≤ 120 MHz	40	60	%
			120 < XCLKIN ≤ 150 MHz	45	55	

Table 5-8. Possible PLL Configuration Modes

PLL MODE	REMARKS	SYSCLKOUT
PLL Disabled	Invoked by tying $\overline{\text{XPLLDIS}}$ pin low upon reset. PLL block is completely disabled. Clock input to the CPU (CLKIN) is directly derived from the clock signal present at the X1/XCLKIN pin.	XCLKIN
PLL Bypassed	Default PLL configuration upon power-up, if PLL is not disabled. The PLL itself is bypassed. However, the /2 module in the PLL block divides the clock input at the X1/XCLKIN pin by two before feeding it to the CPU.	XCLKIN/2
PLL Enabled	Achieved by writing a non-zero value “n” into PLLCR register. The /2 module in the PLL block now divides the output of the PLL by two before feeding it to the CPU.	(XCLKIN * n) / 2

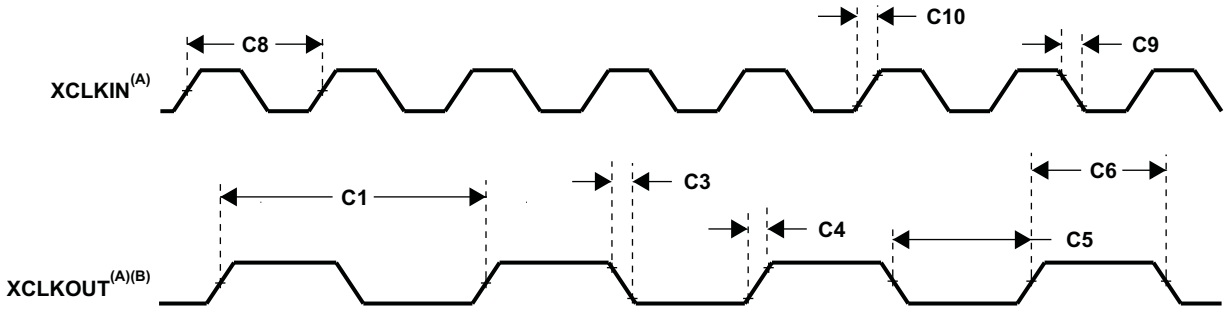
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5.12.4.2.2 Output Clock Characteristics

Table 5-9. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1)(2)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
C1	$t_{c(XCO)}$	Cycle time, XCLKOUT	6.67(3)			ns
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		2		ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		2		ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2		H + 2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2		H + 2	ns
C7	t_p	PLL lock time(4)			$131072t_{c(CI)}$	ns

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$
(3) The PLL must be used for maximum frequency operation.
(4) This parameter has changed from 4096 XCLKIN cycles in the earlier revisions of the silicon.



A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown in Figure 5-11 is intended to illustrate the timing parameters only and may differ based on configuration.
B. XCLKOUT configured to reflect SYSCLKOUT.

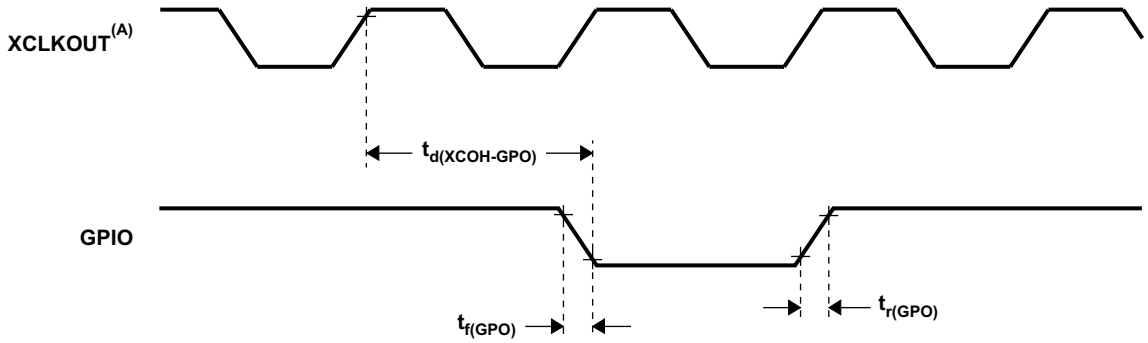
Figure 5-11. Clock Timing

5.12.5 Peripherals

5.12.5.1 General-Purpose Input/Output (GPIO) – Output Timing

Table 5-10. General-Purpose Output Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(XCOH-GPO)}$	Delay time, XCLKOUT high to GPIO low/high	All GPIOs		$1t_{c(SCO)}$	cycle
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		10	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		10	ns
f_{GPO}	Toggling frequency, GPO pins			20	MHz

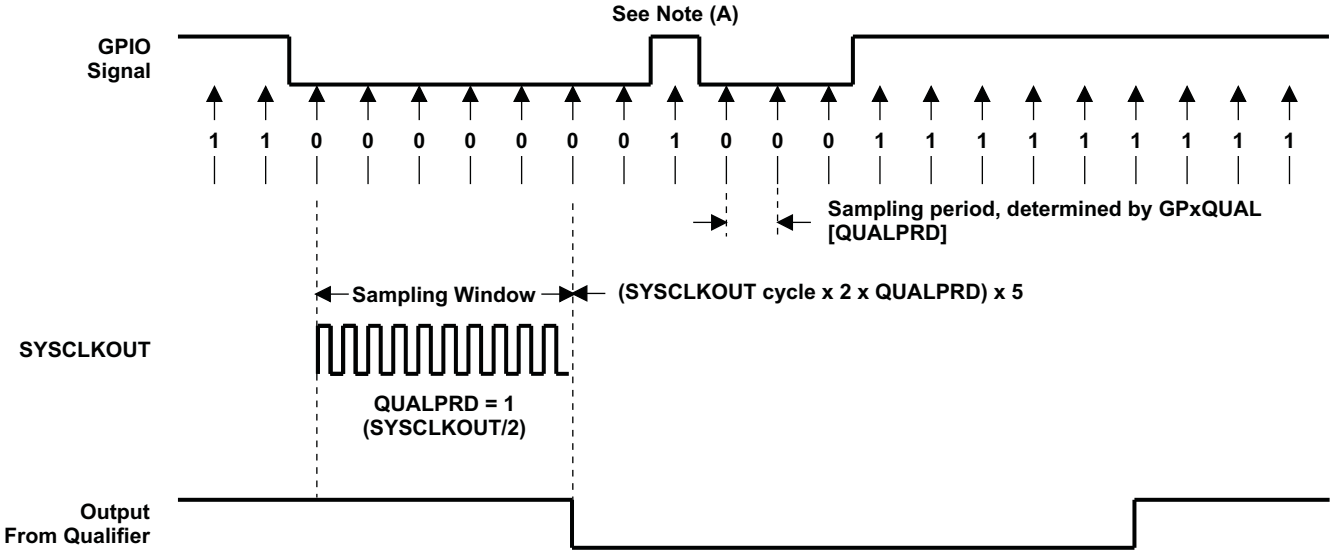


A. XCLKOUT = SYSCLKOUT

Figure 5-12. General-Purpose Output Timing

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5.12.5.2 General-Purpose Input/Output (GPIO) – Input Timing



A. This glitch is ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. Input qualification is not applicable when QUALPRD = 00. For any other value “n”, the qualification sampling period is 2n SYSCLKOUT cycles (that is, at every 2n SYSCLKOUT cycle, the GPIO pin will be sampled). Six consecutive samples must be of the same value for a given input to be recognized.

B. For the qualifier to detect the change, the input must be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLKOUT cycles. This would enable five sampling periods for detection to occur. Since external signals are driven asynchronously, a 13-SYSCLKOUT-wide pulse provides reliable recognition.

Figure 5-13. GPIO Input Qualifier – Example Diagram for QUALPRD = 1

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Table 5-11. General-Purpose Input Timing Requirements

				MIN	MAX	UNIT
$t_{w(GPI)}$	Pulse duration GPIO low/high	All GPIOs	With no qualifier	$2t_{c(SCO)}$		cycles
			With qualifier	$1t_{c(SCO)}$ + IQT(1)		

(1) Input Qualification Time (IQT) = [$t_{c(SCO)}$ × 2 × QUALPRD] × 5 + [$t_{c(SCO)}$ × 2 × QUALPRD].

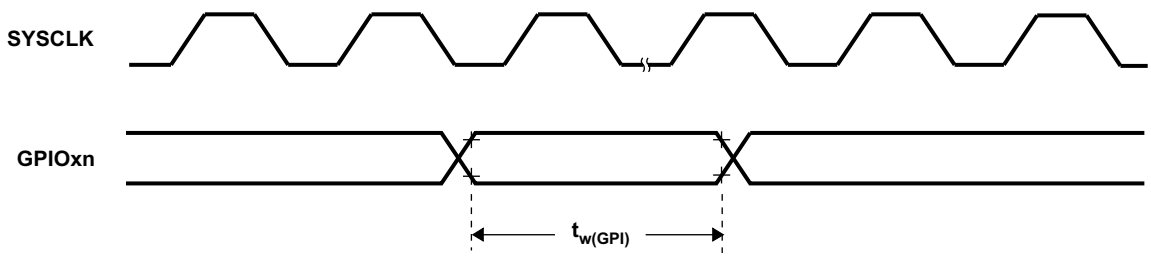


Figure 5-14. General-Purpose Input Timing

NOTE

The pulse width requirement for general-purpose input is applicable for the $\overline{\text{XBIO}}$ and ADCSOC pins as well.

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5.12.5.3 Event Manager Interface

5.12.5.3.1 PWM Timing

PWM refers to all PWM outputs on EVA and EVB.

Table 5-12. PWM Switching Characteristics(1)(2)

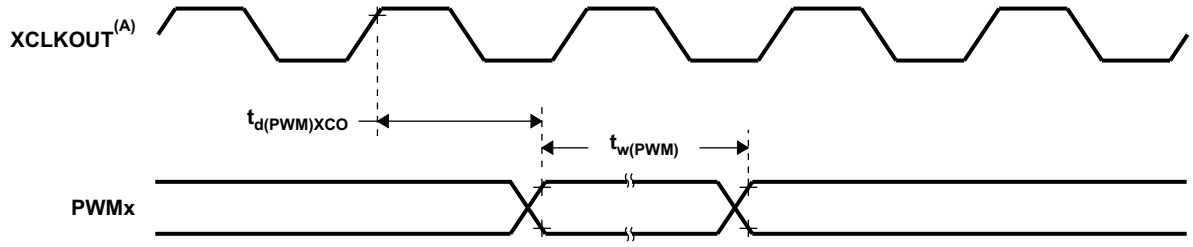
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$(3)	Pulse duration, PWMx output high/low		25		ns
$t_{d(PWM)XCO}$	Delay time, XCLKOUT high to PWMx output switching	XCLKOUT = SYSCLKOUT/4		10	ns

(1) See the GPIO output timing for fall/rise times for PWM pins.
(2) PWM pin toggling frequency is limited by the GPIO output buffer switching frequency (20 MHz).
(3) PWM outputs may be 100%, 0%, or increments of $t_{c(HCO)}$ with respect to the PWM period.

Table 5-13. Timer and Capture Unit Timing Requirements(1)(2)

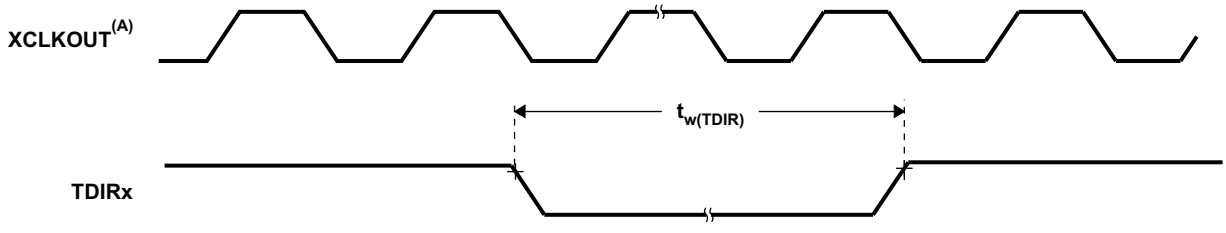
			MIN	MAX	UNIT
$t_{w(TDIR)}$	Pulse duration, TDIRx low/high	Without input qualifier	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)}$ + IQT(3)		
$t_{w(CAP)}$	Pulse duration, CAPx input low/high	Without input qualifier	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)}$ + IQT(3)		
$t_{w(TCLKINL)}$	Pulse duration, TCLKINx low as a percentage of TCLKINx cycle time		40	60	%
$t_{w(TCLKINH)}$	Pulse duration, TCLKINx high as a percentage of TCLKINx cycle time		40	60	%
$t_{c(TCLKIN)}$	Cycle time, TCLKINx		$4t_{c(HCO)}$		ns

(1) The QUALPRD bit field value can range from 0 (no qualification) through 0xFF (510 SYSCLKOUT cycles). The qualification sampling period is 2n SYSCLKOUT cycles, where "n" is the value stored in the QUALPRD bit field. As an example, when QUALPRD = 1, the qualification sampling period is 1 × 2 = 2 SYSCLKOUT cycles (that is, the input is sampled every 2 SYSCLKOUT cycles). Six such samples will be taken over five sampling windows, each window being 2n SYSCLKOUT cycles. For QUALPRD = 1, the minimum width that is needed is 5 × 2 = 10 SYSCLKOUT cycles. However, since the external signal is driven asynchronously, a 11-SYSCLKOUT-wide pulse ensures reliable recognition.
(2) Maximum input frequency to the QEP = min[HSPCLK/2, 20 MHz]
(3) Input Qualification Time (IQT) = [$t_{c(SCO)}$ × 2 × QUALPRD] × 5 + [$t_{c(SCO)}$ × 2 × QUALPRD].



A. XCLKOUT = SYSCLKOUT

Figure 5-15. PWM Output Timing



A. XCLKOUT = SYSCLKOUT

Figure 5-16. TDIRx Timing

Table 5-14. External ADC Start-of-Conversion – EVA – Switching Characteristics(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-EVASOCL)}$	Delay time, XCLKOUT high to $\overline{EVASOC}$ low		$1t_{c(SCO)}$	cycle
$t_{w(EVASOCL)}$	Pulse duration, $\overline{EVASOC}$ low	$32t_{c(HCO)}$		ns

(1) XCLKOUT = SYSCLKOUT

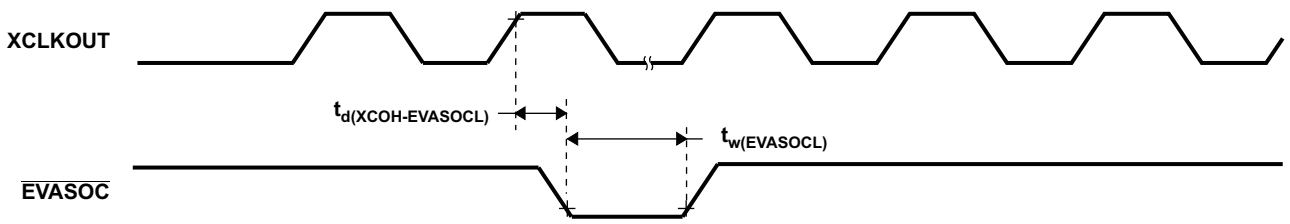


Figure 5-17. $\overline{EVASOC}$ Timing

Table 5-15. External ADC Start-of-Conversion – EVB – Switching Characteristics(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-EVBSOCL)}$	Delay time, XCLKOUT high to $\overline{EVBSOC}$ low		$1t_{c(SCO)}$	cycle
$t_{w(EVBSOCL)}$	Pulse duration, $\overline{EVBSOC}$ low	$32t_{c(HCO)}$		ns

(1) XCLKOUT = SYSCLKOUT

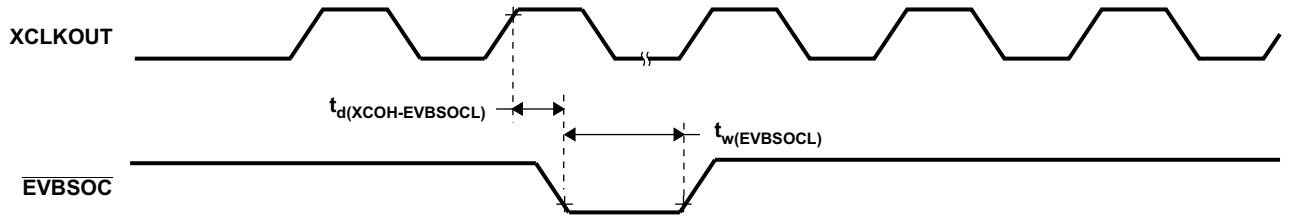


Figure 5-18. $\overline{EVBSOC}$ Timing

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5.12.5.4 Low-Power Mode Wakeup Timing

Table 5-16. IDLE Mode Timing Requirements

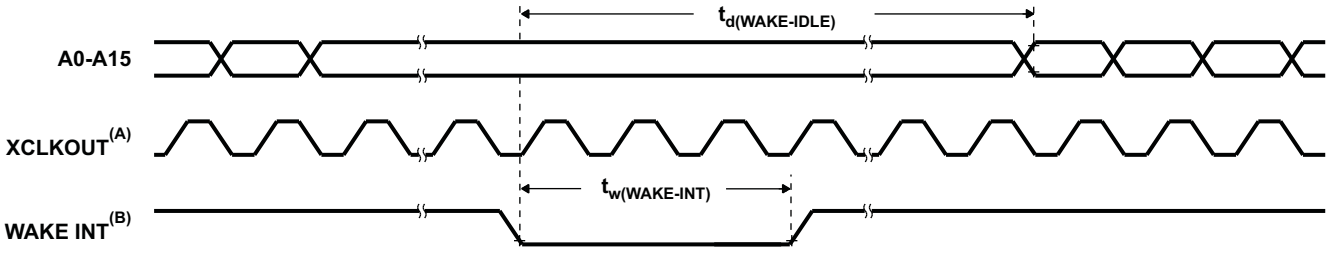
			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)}$ + IQT(1)		

(1) Input Qualification Time (IQT) = [$t_{c(SCO)}$ × 2 × QUALPRD] × 5 + [$t_{c(SCO)}$ × 2 × QUALPRD].

Table 5-17. IDLE Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume(1)				
	• Wake-up from Flash – Flash module in active state	Without input qualifier		$8t_{c(SCO)}$	cycles
		With input qualifier		$8t_{c(SCO)}$ + IQT(2)	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier		$1050t_{c(SCO)}$	cycles
		With input qualifier		$1050t_{c(SCO)}$ + IQT(2)	
	• Wake-up from SARAM	Without input qualifier		$8t_{c(SCO)}$	cycles
		With input qualifier		$8t_{c(SCO)}$ + IQT(2)	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up) signal involves additional latency.
(2) Input Qualification Time (IQT) = [$t_{c(SCO)}$ × 2 × QUALPRD] × 5 + [$t_{c(SCO)}$ × 2 × QUALPRD].



A. XCLKOUT = SYSCLKOUT
B. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$, XNMI, or $\overline{\text{XRS}}$.

Figure 5-19. IDLE Entry and Exit Timing

Table 5-18. STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$12t_{c(CI)}$		cycles
		With input qualifier	(2 + QUALSTDBY) * $t_{c(CI)}$ (1)		

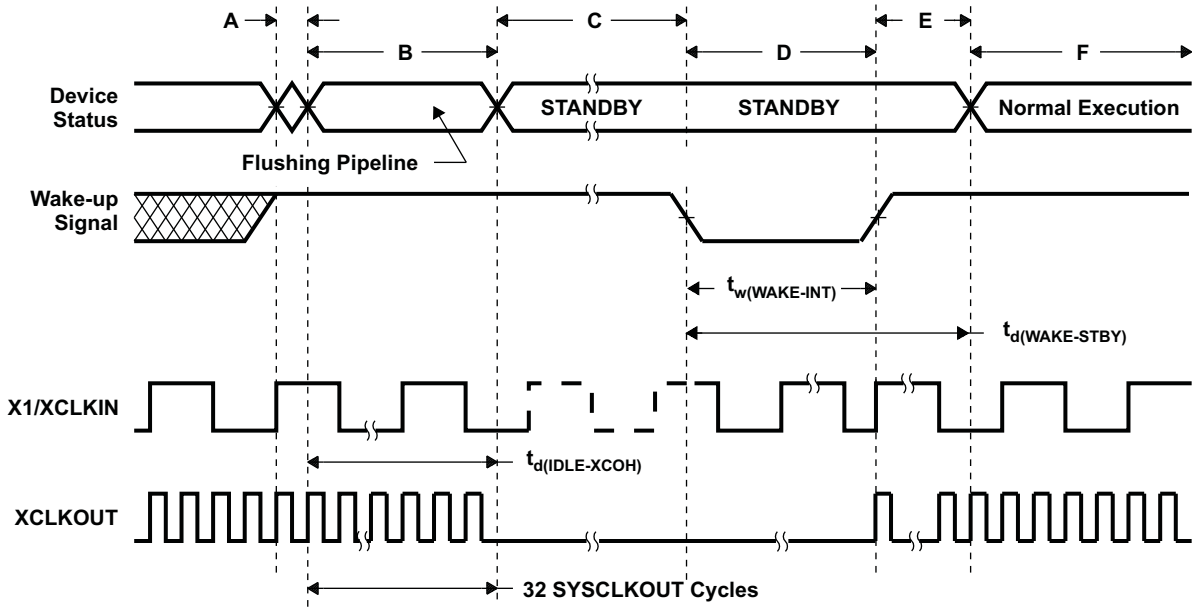
(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

Table 5-19. STANDBY Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOH)}$	Delay time, IDLE instruction executed to XCLKOUT high		$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume (1)				
	• Wake-up from Flash – Flash module in active state	Without input qualifier		$12t_{c(CI)}$	cycles
		With input qualifier		$12t_{c(CI)} + t_{w(WAKE-INT)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier		$1125t_{c(SCO)}$	cycles
		With input qualifier		$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake-up from SARAM	Without input qualifier		$12t_{c(CI)}$	cycles
		With input qualifier		$12t_{c(CI)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up) signal involves additional latency.

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A. IDLE instruction is executed to put the device into STANDBY mode.

B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for the number of cycles indicated below before being turned off:
   - 16 cycles, when DIVSEL = 00 or 01
   - 32 cycles, when DIVSEL = 10
   - 64 cycles, when DIVSEL = 11

   This delay enables the CPU pipeline and any other pending operations to flush properly. If an access to XINTF is in progress and its access time is longer than this number, then it will fail. It is recommended that STANDBY mode be entered from SARAM without an XINTF access in progress.

C. Clocks to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode.

D. The external wake-up signal is driven active.

E. After a latency period, the STANDBY mode is exited.

F. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 5-20. STANDBY Entry and Exit Timing

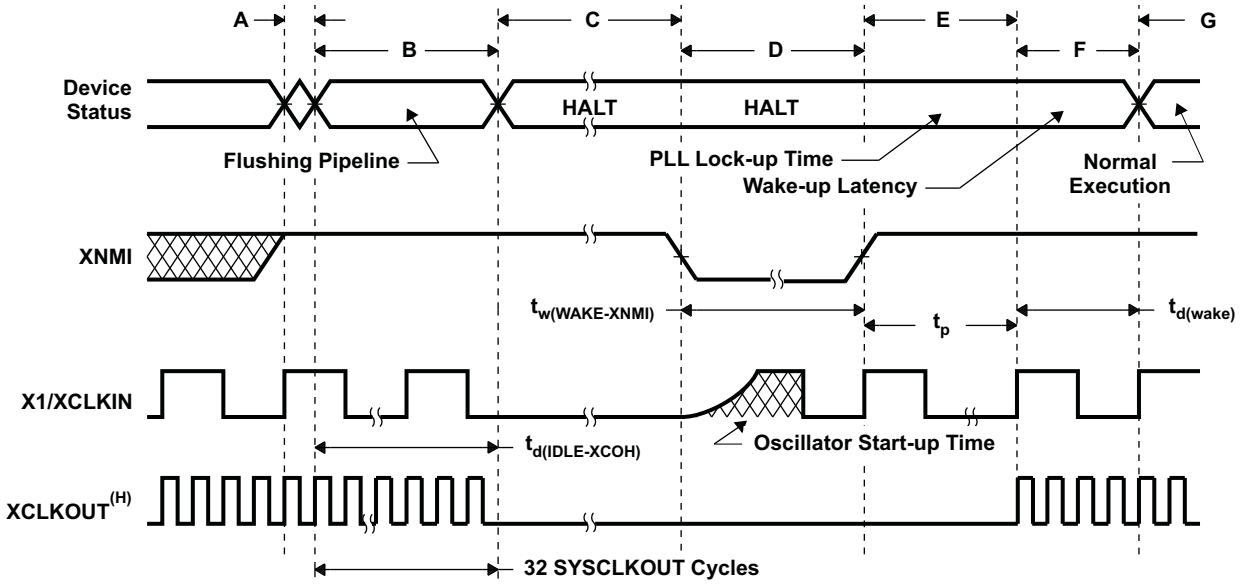
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Table 5-20. HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-XNMI)}$	Pulse duration, XNMI wakeup signal	$2t_{c(CI)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wakeup signal	$8t_{c(CI)}$		cycles

Table 5-21. HALT Mode Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOH)}$	Delay time, IDLE instruction executed to XCLKOUT high	$32t_{c(SCO)}$	$45t_{c(SCO)}$		cycles
t_p	PLL lock-up time			$131072t_{c(CI)}$	cycles
$t_{d(WAKE)}$	Delay time, PLL lock to program execution resume				
	• Wake up from flash – Flash module in sleep state			$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM			$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for another 32 cycles before the oscillator is turned off and the CLKIN to the core is stopped. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the internal oscillator and PLL are shut down. The device is now in HALT mode and consumes absolute minimum power.

D. When XNMI is driven active, the oscillator is turned on; but the PLL is not activated. The pulse duration of $2t_{c(CI)}$ is applicable when an external oscillator is used. If the internal oscillator is used, the oscillator wake-up time should be added to this parameter.

E. When XNMI is deactivated, it initiates the PLL lock sequence, which takes 131,072 X1/XCLKIN cycles.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.

G. Normal operation resumes.

H. XCLKOUT = SYSCLKOUT

Figure 5-21. HALT Wakeup Using XNMI

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5.12.5.5 Serial Peripheral Interface (SPI) Master Mode Timing

Table 5-22 lists the master mode timing (clock phase = 0) and Table 5-23 lists the master mode timing (clock phase = 1). Figure 5-22 and Figure 5-23 show the timing waveforms.

Table 5-22. SPI Master Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.	PARAMETER		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid		10		10	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
8	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	35		35		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MAX, slave mode receive 12.5-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).

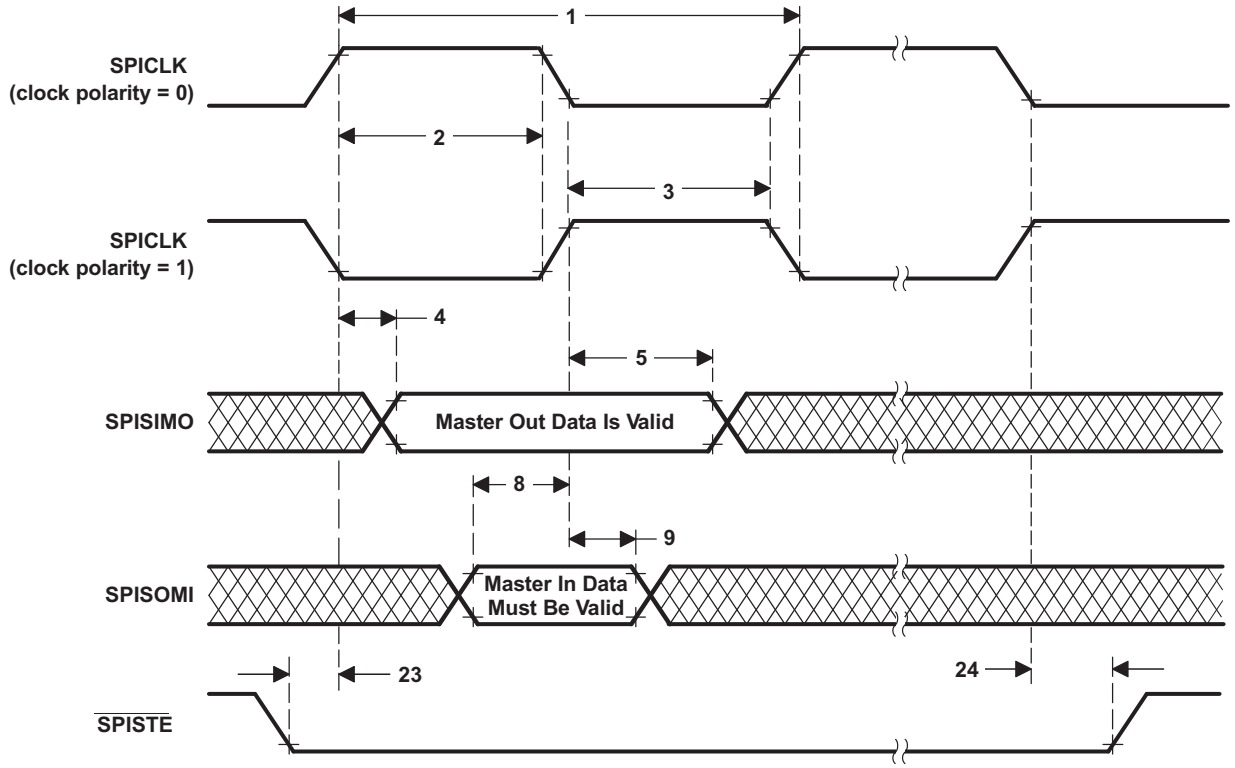


Figure 5-22. SPI Master Mode External Timing (Clock Phase = 0)

Table 5-23. SPI Master Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)(5)

NO.	PARAMETER		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
6	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$		ns
7	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
10	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	35		35		ns
11	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)} - 10$		$0.5t_{c(SPC)} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25 MHz MAX, master mode receive 12.5 MHz MAX
Slave mode transmit 12.5 MHz MAX, slave mode receive 12.5 MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

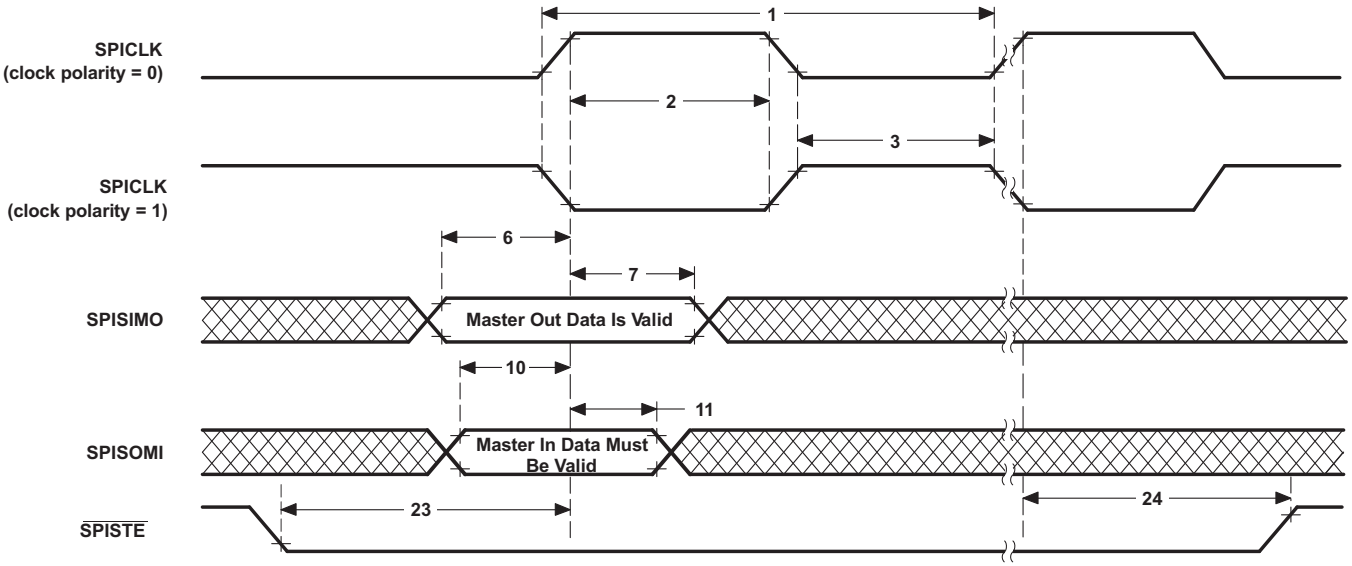


Figure 5-23. SPI Master Mode External Timing (Clock Phase = 1)

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5.12.5.6 Serial Peripheral Interface (SPI) Slave Mode Timing

Table 5-24 lists the slave mode timing (clock phase = 0) and Table 5-25 lists the slave mode timing (clock phase = 1). Figure 5-24 and Figure 5-25 show the timing waveforms.

Table 5-24. SPI Slave Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.	PARAMETER		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		35	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

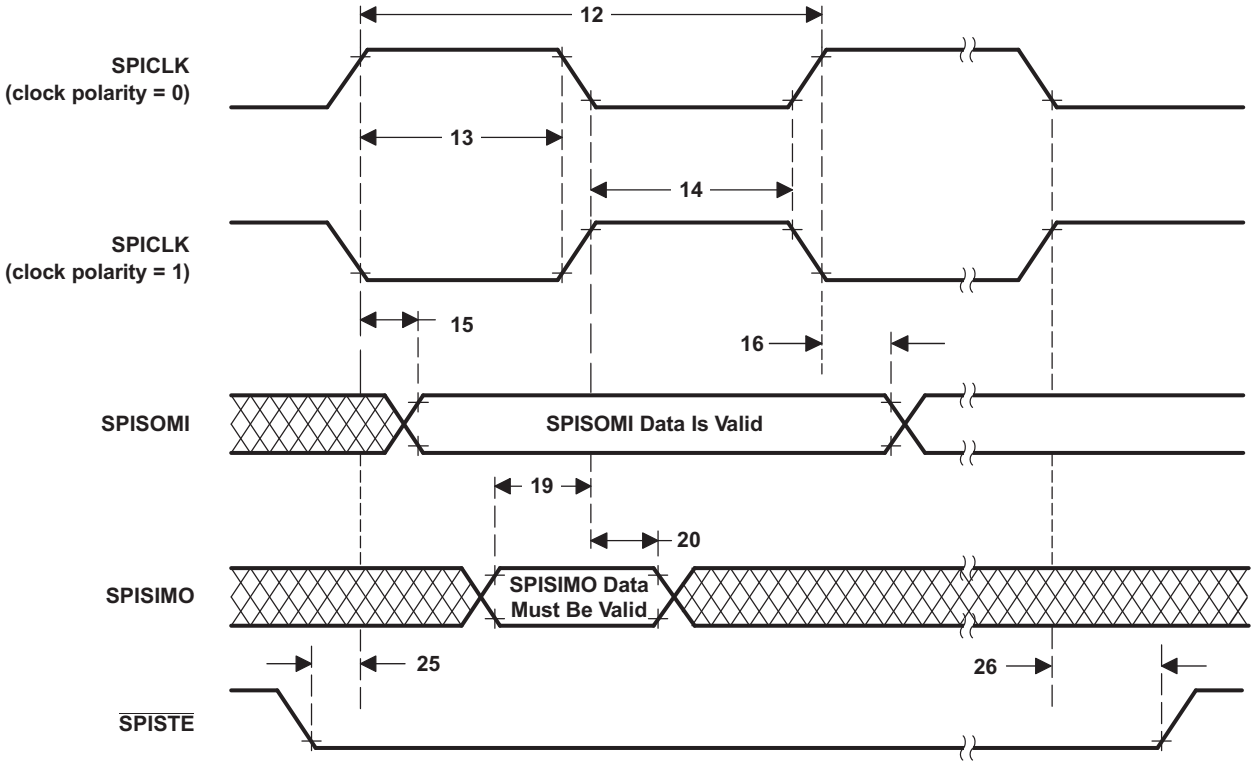


Figure 5-24. SPI Slave Mode External Timing (Clock Phase = 0)

Table 5-25. SPI Slave Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)

NO.	PARAMETER		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
17	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		35	ns
18	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
21	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
22	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

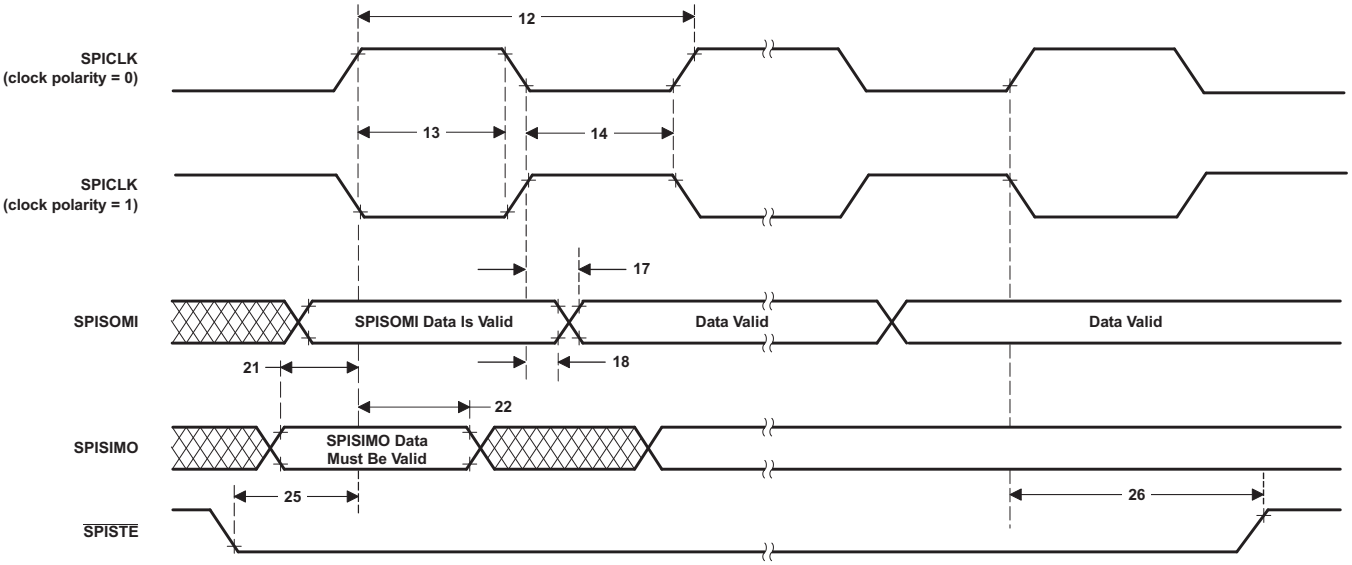


Figure 5-25. SPI Slave Mode External Timing (Clock Phase = 1)

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5.12.5.7 External Interface (XINTF) Timing

Each XINTF access consists of three parts: Lead, Active, and Trail. The user configures the Lead/Active/Trail wait states in the XTIMING registers. There is one XTIMING register for each XINTF zone. Table 5-26 shows the relationship between the parameters configured in the XTIMING register and the duration of the pulse in terms of XTIMCLK cycles.

Table 5-26. Relationship Between Parameters Configured in XTIMING and Duration of Pulse(1)(2)

DESCRIPTION		DURATION (ns)	
		X2TIMING = 0	X2TIMING = 1
LR	Lead period, read access	XRDLEAD × $t_{c(XTIM)}$	(XRDLEAD × 2) × $t_{c(XTIM)}$
AR	Active period, read access	(XRDACTIVE + WS + 1) × $t_{c(XTIM)}$	(XRDACTIVE × 2 + WS + 1) × $t_{c(XTIM)}$
TR	Trail period, read access	XRDTRAIL × $t_{c(XTIM)}$	(XRDTRAIL × 2) × $t_{c(XTIM)}$
LW	Lead period, write access	XWRLEAD × $t_{c(XTIM)}$	(XWRLEAD × 2) × $t_{c(XTIM)}$
AW	Active period, write access	(XWRACTIVE + WS + 1) × $t_{c(XTIM)}$	(XWRACTIVE × 2 + WS + 1) × $t_{c(XTIM)}$
TW	Trail period, write access	XWRTRAIL × $t_{c(XTIM)}$	(XWRTRAIL × 2) × $t_{c(XTIM)}$

(1) $t_{c(XTIM)}$ – Cycle time, XTIMCLK
(2) WS refers to the number of wait states inserted by hardware when using XREADY. If the zone is configured to ignore XREADY (USEREADY = 0), then WS = 0.

Minimum wait state requirements must be met when configuring each zone's XTIMING register. These requirements are in addition to any timing requirements as specified by that device's data sheet. No internal device hardware is included to detect illegal settings.

5.12.5.7.1 USEREADY = 0

If the XREADY signal is ignored (USEREADY = 0), then:

1. Lead: $LR \geq t_{c(XTIM)}$
   $LW \geq t_{c(XTIM)}$

These requirements result in the following XTIMING register configuration restrictions (no hardware to detect illegal XTIMING configurations):

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 0	≥ 0	≥ 1	≥ 0	≥ 0	0, 1

Examples of valid and invalid timing when not sampling XREADY (no hardware to detect illegal XTIMING configurations):

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Valid	1	0	0	1	0	0	0, 1

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5.12.5.7.2 Synchronous Mode (USEREADY = 1, READYMODE = 0)

If the XREADY signal is sampled in the synchronous mode (USEREADY = 1, READYMODE = 0), then:

1. Lead: $LR \geq t_{c(XTIM)}$
   $LW \geq t_{c(XTIM)}$
2. Active: $AR \geq 2 \times t_{c(XTIM)}$
   $AW \geq 2 \times t_{c(XTIM)}$

NOTE: Restriction does not include external hardware wait states.

These requirements result in the following XTIMING register configuration restrictions (no hardware to detect illegal XTIMING configurations):

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 2	≥ 0	≥ 1	≥ 2	≥ 0	0, 1

Examples of valid and invalid timing when using synchronous XREADY (no hardware to detect illegal XTIMING configurations):

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Invalid	1	0	0	1	0	0	0, 1
Valid	1	2	0	1	2	0	0, 1

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5.12.5.7.3 Asynchronous Mode (USEREADY = 1, READYMODE = 1)

If the XREADY signal is sampled in the asynchronous mode (USEREADY = 1, READYMODE = 1), then:

1. Lead: $LR \geq t_{c(XTIM)}$
   $LW \geq t_{c(XTIM)}$
2. Active: $AR \geq 2 \times t_{c(XTIM)}$
   $AW \geq 2 \times t_{c(XTIM)}$
   NOTE: Restriction does not include external hardware wait states
3. Lead + Active: $LR + AR \geq 4 \times t_{c(XTIM)}$
   $LW + AW \geq 4 \times t_{c(XTIM)}$
   NOTE: Restriction does not include external hardware wait states

These requirements result in the following XTIMING register configuration restrictions (no hardware to detect illegal XTIMING configurations):

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 2	0	≥ 1	≥ 2	0	0, 1

or (no hardware to detect illegal XTIMING configurations):

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 2	≥ 2	0	≥ 2	≥ 2	0	0, 1

Examples of valid and invalid timing when using asynchronous XREADY (no hardware to detect illegal XTIMING configurations):

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Invalid	1	0	0	1	0	0	0, 1
Invalid	1	1	0	1	1	0	0
Valid	1	2	0	1	2	0	1
Valid	1	2	0	1	2	0	0, 1
Valid	2	2	0	2	2	0	0, 1

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Unless otherwise specified, all XINTF timing is applicable for the clock configurations shown in Table 5-27.

Table 5-27. XINTF Clock Configurations

MODE	SYSCLKOUT	XTIMCLK	XCLKOUT
1 Example:	150 MHz	SYSCLKOUT 150 MHz	SYSCLKOUT 150 MHz
2 Example:	150 MHz	SYSCLKOUT 150 MHz	1/2 SYSCLKOUT 75 MHz
3 Example:	150 MHz	1/2 SYSCLKOUT 75 MHz	1/2 SYSCLKOUT 75 MHz
4 Example:	150 MHz	1/2 SYSCLKOUT 75 MHz	1/4 SYSCLKOUT 37.5 MHz

The relationship between SYSCLKOUT and XTIMCLK is shown in Figure 5-26.

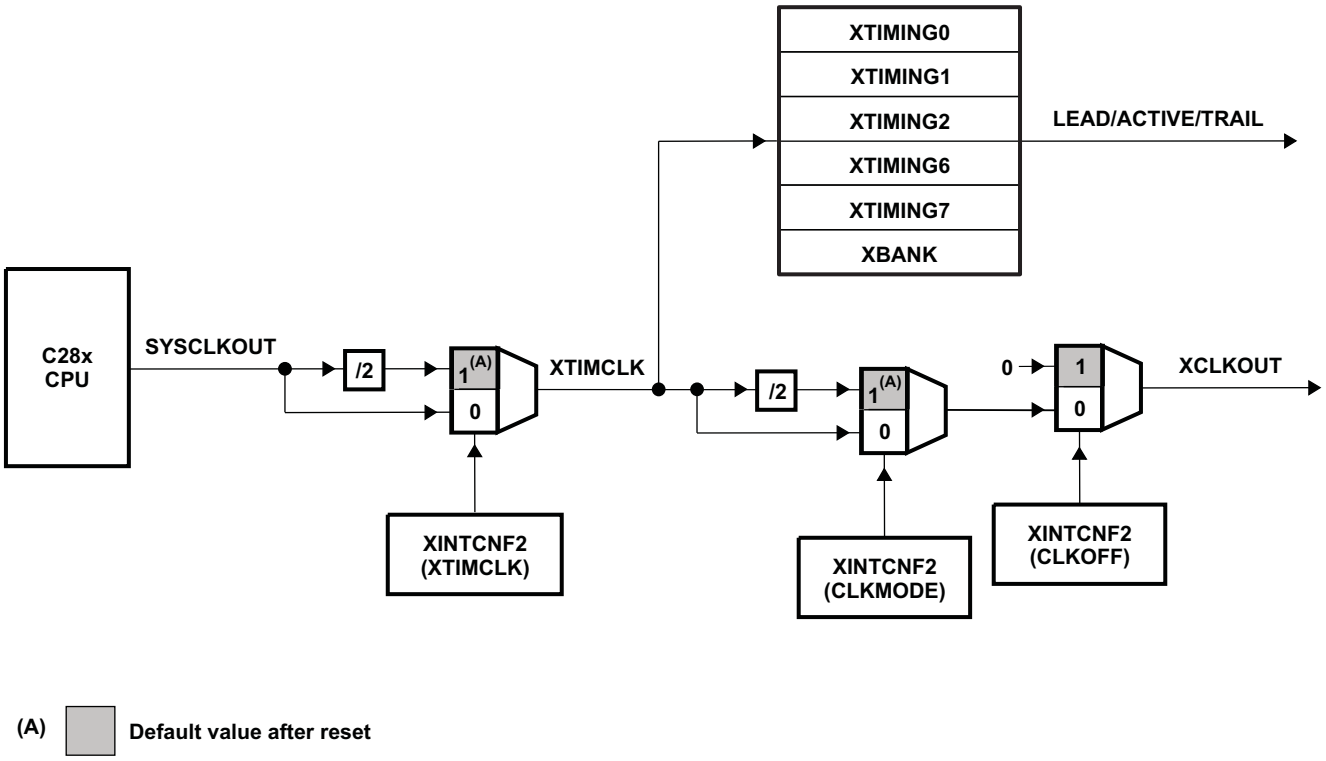


Figure 5-26. Relationship Between XTIMCLK and SYSCLKOUT

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5.12.5.8 XINTF Signal Alignment to XCLKOUT

For each XINTF access, the number of lead, active, and trail cycles is based on the internal clock XTIMCLK. Strobes such as $\overline{\text{XRD}}$, $\overline{\text{XWE}}$, and zone chip-select ($\overline{\text{XZCS}}$) change state in relationship to the rising edge of XTIMCLK. The external clock, XCLKOUT, can be configured to be either equal to or one-half the frequency of XTIMCLK.

For the case where XCLKOUT = XTIMCLK, all of the XINTF strobes will change state with respect to the rising edge of XCLKOUT. For the case where XCLKOUT = one-half XTIMCLK, some strobes will change state either on the rising edge of XCLKOUT or the falling edge of XCLKOUT. In the XINTF timing tables, the notation XCOHL is used to indicate that the parameter is with respect to either case; XCLKOUT rising edge (high) or XCLKOUT falling edge (low). If the parameter is always with respect to the rising edge of XCLKOUT, the notation XCOH is used.

For the case where XCLKOUT = one-half XTIMCLK, the XCLKOUT edge with which the change will be aligned can be determined based on the number of XTIMCLK cycles from the start of the access to the point at which the signal changes. If this number of XTIMCLK cycles is even, the alignment will be with respect to the rising edge of XCLKOUT. If this number is odd, then the signal will change with respect to the falling edge of XCLKOUT. Examples include the following:

- Strobes that change at the beginning of an access always align to the rising edge of XCLKOUT. This is because all XINTF accesses begin with respect to the rising edge of XCLKOUT.

Examples:	XZCSL	Zone chip-select active-low
	XRNWL	XR/$\overline{\text{W}}$ active-low

- Strobes that change at the beginning of the active period will align to the rising edge of XCLKOUT if the total number of lead XTIMCLK cycles for the access is even. If the number of lead XTIMCLK cycles is odd, then the alignment will be with respect to the falling edge of XCLKOUT.

Examples:	XRDL	$\overline{\text{XRD}}$ active-low
	XWEL	$\overline{\text{XWE}}$ active-low

- Strobes that change at the beginning of the trail period will align to the rising edge of XCLKOUT if the total number of lead + active XTIMCLK cycles (including hardware waitstates) for the access is even. If the number of lead + active XTIMCLK cycles (including hardware waitstates) is odd, then the alignment will be with respect to the falling edge of XCLKOUT.

Examples:	XRDH	$\overline{\text{XRD}}$ inactive-high
	XWEH	$\overline{\text{XWE}}$ inactive-high

- Strobes that change at the end of the access will align to the rising edge of XCLKOUT if the total number of lead + active + trail XTIMCLK cycles (including hardware waitstates) is even. If the number of lead + active + trail XTIMCLK cycles (including hardware waitstates) is odd, then the alignment will be with respect to the falling edge of XCLKOUT.

Examples:	XZCSH	Zone chip-select inactive-high
	XRNWH	XR/$\overline{\text{W}}$ inactive-high

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5.12.5.9 External Interface Read Timing

Table 5-28. External Memory Interface Read Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-XZCSL)}$	Delay time, XCLKOUT high to zone chip-select active-low		1	ns
$t_{d(XCOHL-XZCSH)}$	Delay time, XCLKOUT high/low to zone chip-select inactive-high	–2	3	ns
$t_{d(XCOH-XA)}$	Delay time, XCLKOUT high to address valid		2	ns
$t_{d(XCOHL-XRDL)}$	Delay time, XCLKOUT high/low to $\overline{XRD}$ active-low		1	ns
$t_{d(XCOHL-XRDH)}$	Delay time, XCLKOUT high/low to $\overline{XRD}$ inactive-high	–2	1	ns
$t_{h(XA)XZCSH}$	Hold time, address valid after zone chip-select inactive-high	(1)		ns
$t_{h(XA)XRD}$	Hold time, address valid after $\overline{XRD}$ inactive-high	(1)		ns

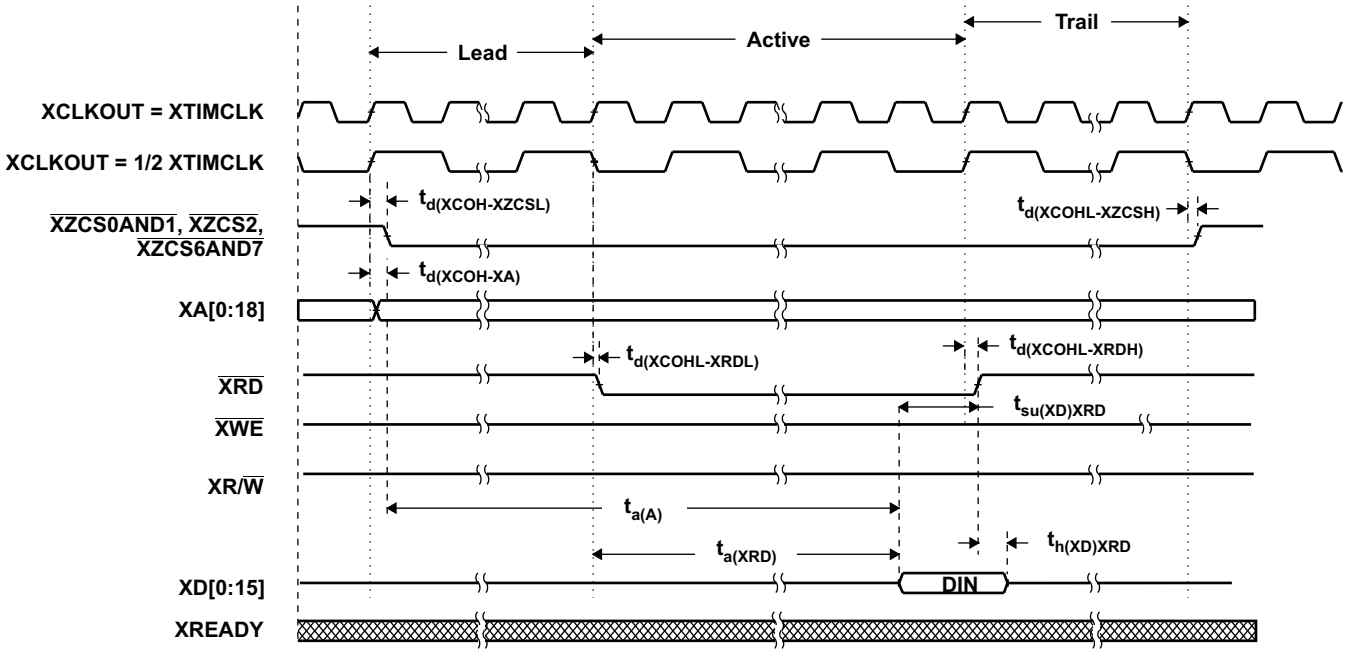
(1) During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.

Table 5-29. External Memory Interface Read Timing Requirements

		MIN	MAX	UNIT
$t_{a(A)}$	Access time, read data from address valid		(LR + AR) – 14 (1)	ns
$t_{a(XRD)}$	Access time, read data valid from $\overline{XRD}$ active-low		AR – 12 (1)	ns
$t_{su(XD)XRD}$	Setup time, read data valid before $\overline{XRD}$ strobe inactive-high	12		ns
$t_{h(XD)XRD}$	Hold time, read data valid after $\overline{XRD}$ inactive-high	0		ns

(1) LR = Lead period, read access. AR = Active period, read access. See Table 5-26.

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A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
B. During alignment cycles, all signals will transition to their inactive state.
C. For USEREADY = 0, the external XREADY input signal is ignored.
D. XA[0:18] will hold the last address put on the bus during inactive cycles, including alignment cycles.

Figure 5-27. Example Read Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
≥ 1	≥ 0	≥ 0	0	0	N/A(1)	N/A(1)	N/A(1)	N/A(1)

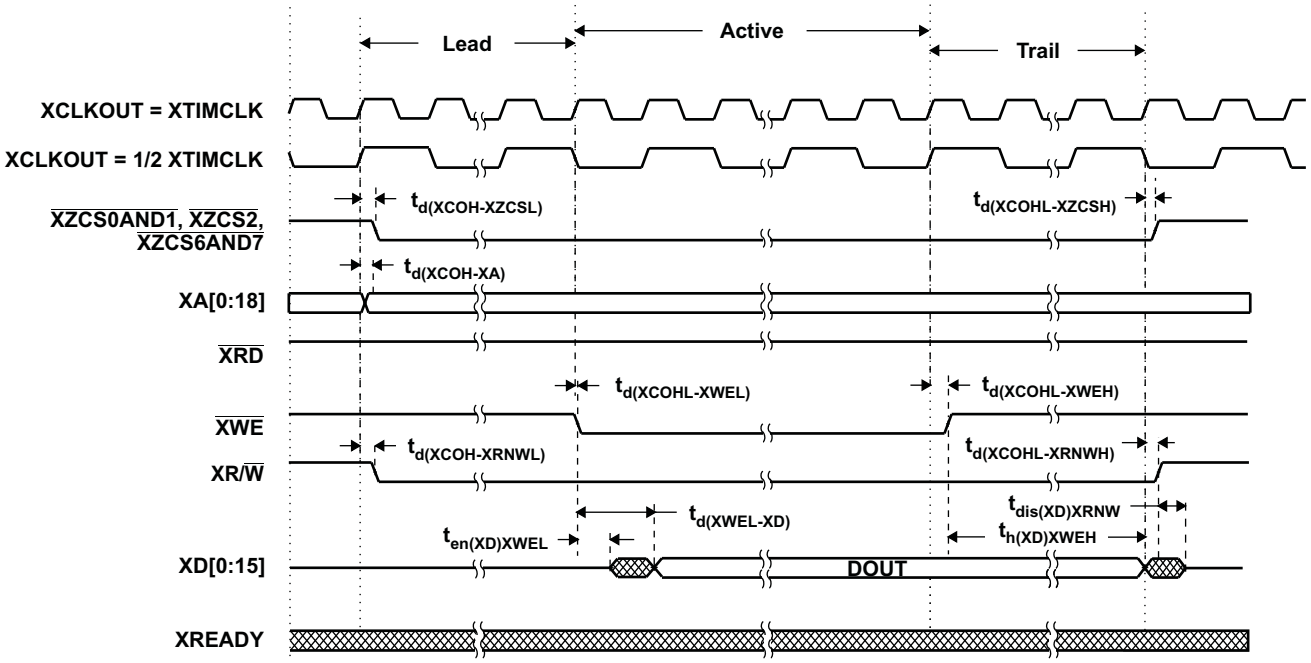
(1) N/A = “Don’t care” for this example

5.12.5.10 External Interface Write Timing

Table 5-30. External Memory Interface Write Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-XZCSL)}$	Delay time, XCLKOUT high to zone chip-select active-low		1	ns
$t_{d(XCOHL-XZCSH)}$	Delay time, XCLKOUT high or low to zone chip-select inactive-high	–2	3	ns
$t_{d(XCOH-XA)}$	Delay time, XCLKOUT high to address valid		2	ns
$t_{d(XCOHL-XWEL)}$	Delay time, XCLKOUT high/low to $\overline{XWE}$ low		2	ns
$t_{d(XCOHL-XWEH)}$	Delay time, XCLKOUT high/low to $\overline{XWE}$ high		2	ns
$t_{d(XCOH-XRNWL)}$	Delay time, XCLKOUT high to XR/$\overline{W}$ low		1	ns
$t_{d(XCOHL-XRNWH)}$	Delay time, XCLKOUT high/low to XR/$\overline{W}$ high	–2	1	ns
$t_{en(XD)XWEL}$	Enable time, data bus driven from $\overline{XWE}$ low	0		ns
$t_{d(XWEL-XD)}$	Delay time, data valid after $\overline{XWE}$ active-low		4	ns
$t_{h(XA)XZCSH}$	Hold time, address valid after zone chip-select inactive-high	(1)		ns
$t_{h(XD)XWE}$	Hold time, write data valid after $\overline{XWE}$ inactive-high	TW – 2 (2)		ns
$t_{dis(XD)XRNW}$	Maximum time for DSP to release the data bus after XR/$\overline{W}$ inactive-high		4	ns

(1) During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
(2) TW = Trail period, write access. See Table 5-26.



A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
B. During alignment cycles, all signals will transition to their inactive state.
C. For USEREADY = 0, the external XREADY input signal is ignored.
D. XA[0:18] will hold the last address put on the bus during inactive cycles, including alignment cycles.

Figure 5-28. Example Write Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
N/A (1)	N/A (1)	N/A (1)	0	0	≥ 1	≥ 0	≥ 0	N/A (1)

(1) N/A = “Don’t care” for this example

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5.12.5.11 External Interface Ready-on-Read Timing With One External Wait State

Table 5-31. External Memory Interface Read Switching Characteristics (Ready-on-Read, 1 Wait State)

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-XZCSL)}$	Delay time, XCLKOUT high to zone chip-select active-low		1	ns
$t_{d(XCOHL-XZCSH)}$	Delay time, XCLKOUT high/low to zone chip-select inactive-high	–2	3	ns
$t_{d(XCOH-XA)}$	Delay time, XCLKOUT high to address valid		2	ns
$t_{d(XCOHL-XRDL)}$	Delay time, XCLKOUT high/low to $\overline{XRD}$ active-low		1	ns
$t_{d(XCOHL-XRDH)}$	Delay time, XCLKOUT high/low to $\overline{XRD}$ inactive-high	–2	1	ns
$t_{h(XA)XZCSH}$	Hold time, address valid after zone chip-select inactive-high	(1)		ns
$t_{h(XA)XRD}$	Hold time, address valid after $\overline{XRD}$ inactive-high	(1)		ns

(1) During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.

Table 5-32. External Memory Interface Read Timing Requirements (Ready-on-Read, 1 Wait State)

		MIN	MAX	UNIT
$t_{a(A)}$	Access time, read data from address valid		(LR + AR) – 14 (1)	ns
$t_{a(XRD)}$	Access time, read data valid from $\overline{XRD}$ active-low		AR – 12 (1)	ns
$t_{su(XD)XRD}$	Setup time, read data valid before $\overline{XRD}$ strobe inactive-high	12		ns
$t_{h(XD)XRD}$	Hold time, read data valid after $\overline{XRD}$ inactive-high	0		ns

(1) LR = Lead period, read access. AR = Active period, read access. See Table 5-26.

Table 5-33. Synchronous XREADY Timing Requirements (Ready-on-Read, 1 Wait State) (1)

		MIN	MAX	UNIT
$t_{su(XRDYsynchL)XCOHL}$	Setup time, XREADY (synchronous) low before XCLKOUT high/low	15		ns
$t_{h(XRDYsynchL)}$	Hold time, XREADY (synchronous) low	12		ns
$t_{e(XRDYsynchH)}$	Earliest time XREADY (synchronous) can go high before the sampling XCLKOUT edge		3	ns
$t_{su(XRDYsynchH)XCOHL}$	Setup time, XREADY (synchronous) high before XCLKOUT high/low	15		ns
$t_{h(XRDYsynchH)XZCSH}$	Hold time, XREADY (synchronous) held high after zone chip-select high	0		ns

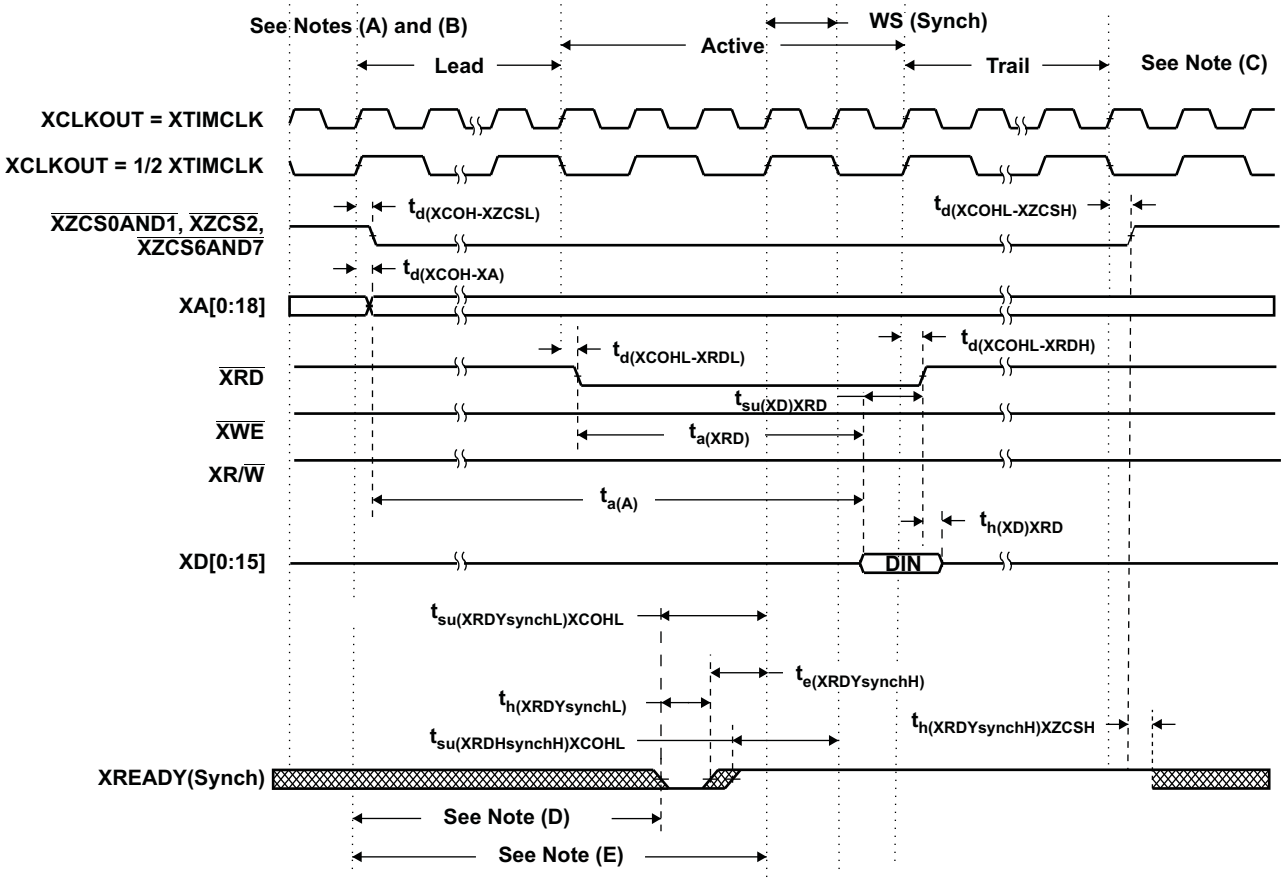
(1) The first XREADY (synchronous) sample occurs with respect to E in Figure 5-29:
E = (XRDLEAD + XRDACTIVE) $t_{c(XTIM)}$
When first sampled, if XREADY (synchronous) is found to be high, then the access will complete. If XREADY (synchronous) is found to be low, it will be sampled again each $t_{c(XTIM)}$ until it is found to be high.
For each sample (n), the setup time (D) with respect to the beginning of the access can be calculated as:
D = (XRDLEAD + XRDACTIVE + n – 1) $t_{c(XTIM)}$ – $t_{su(XRDYsynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3, and so forth).

Table 5-34. Asynchronous XREADY Timing Requirements (Ready-on-Read, 1 Wait State) (1)

		MIN	MAX	UNIT
$t_{su(XRDYAsynchL)XCOHL}$	Setup time, XREADY (asynchronous) low before XCLKOUT high/low	11		ns
$t_{h(XRDYAsynchL)}$	Hold time, XREADY (asynchronous) low	8		ns
$t_{e(XRDYAsynchH)}$	Earliest time XREADY (asynchronous) can go high before the sampling XCLKOUT edge		3	ns
$t_{su(XRDYAsynchH)XCOHL}$	Setup time, XREADY (asynchronous) high before XCLKOUT high/low	11		ns
$t_{h(XRDYAsynchH)XZCSH}$	Hold time, XREADY (asynchronous) held high after zone chip-select high	0		ns

(1) The first XREADY (asynchronous) sample occurs with respect to E in Figure 5-30:
E = (XRDLEAD + XRDACTIVE – 2) $t_{c(XTIM)}$
When first sampled, if XREADY (asynchronous) is found to be high, then the access will complete. If XREADY (asynchronous) is found to be low, it will be sampled again each $t_{c(XTIM)}$ until it is found to be high.
For each sample, setup time from the beginning of the access can be calculated as:
D = (XRDLEAD + XRDACTIVE – 3 + n) $t_{c(XTIM)}$ – $t_{su(XRDYAsynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3, and so forth).

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Legend:

▨ **= Don't care. Signal can be high or low during this time.**

A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.

B. During alignment cycles, all signals will transition to their inactive state.

C. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.

D. For each sample, setup time from the beginning of the access (D) can be calculated as:
D = (XRDLEAD + XRDACTIVE + n – 1) $t_{c(XTIM)}$ – $t_{su(XRDYsynchL)XCOHL}$

E. Reference for the first sample is with respect to this point
E = (XRDLEAD + XRDACTIVE) $t_{c(XTIM)}$
where n is the sample number (n = 1, 2, 3, and so forth).

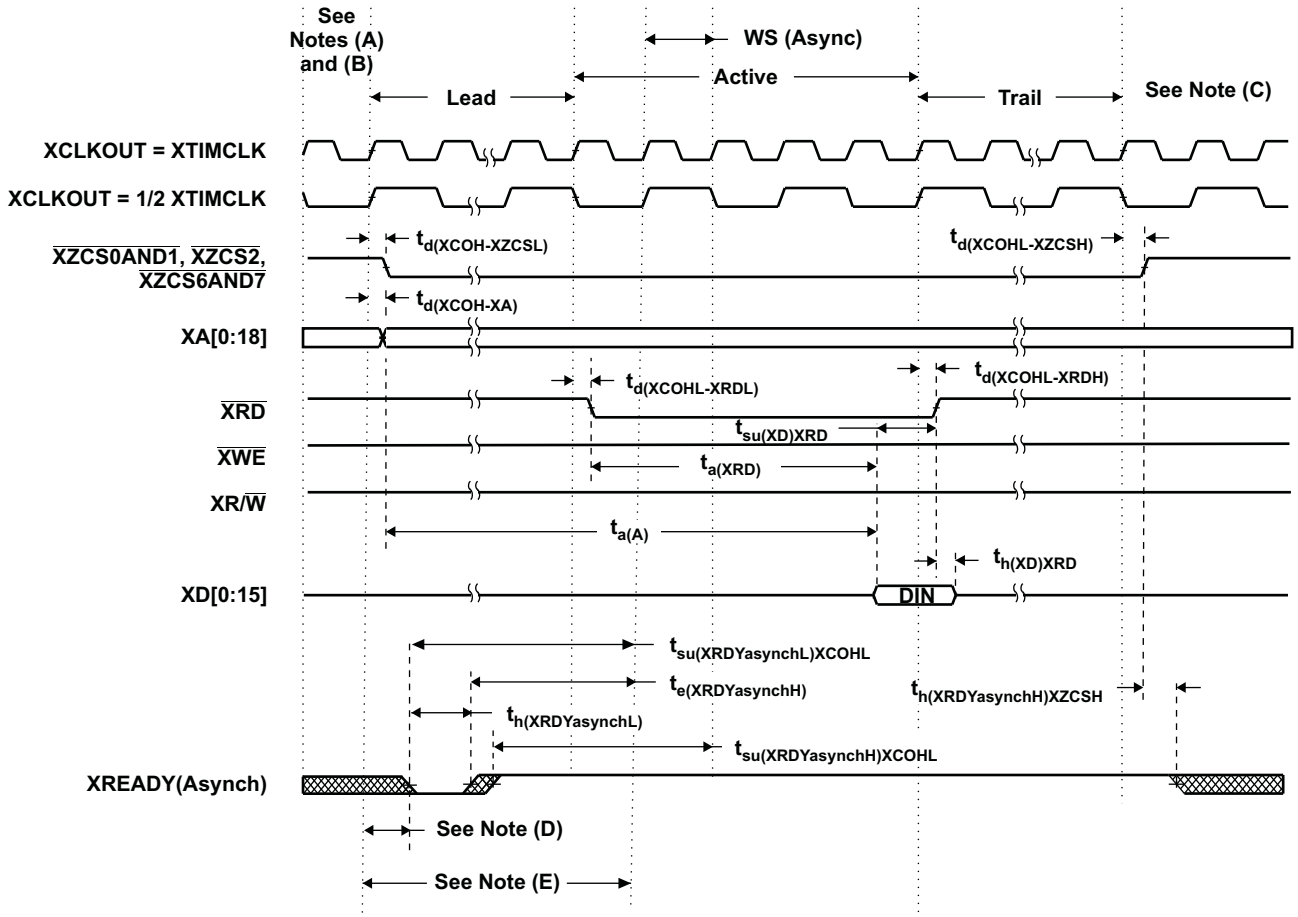
Figure 5-29. Example Read With Synchronous XREADY Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
≥ 1	3	≥ 1	1	0	N/A(1)	N/A(1)	N/A(1)	0 = XREADY (Synch)

(1) N/A = "Don't care" for this example

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Legend:

= Don't care. Signal can be high or low during this time.

A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.

B. During alignment cycles, all signals will transition to their inactive state.

C. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.

D. For each sample, setup time from the beginning of the access can be calculated as:
D = (XRDLEAD + XRDACTIVE – 3 + n) $t_{c(XTIM)}$ – $t_{su(XRDYAsynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3, and so forth).

E. Reference for the first sample is with respect to this point:
E = (XRDLEAD + XRDACTIVE – 2) $t_{c(XTIM)}$

Figure 5-30. Example Read With Asynchronous XREADY Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
≥ 1	3	≥ 1	1	0	N/A(1)	N/A(1)	N/A(1)	1 = XREADY (Async)

(1) N/A = "Don't care" for this example

5.12.5.12 External Interface Ready-on-Write Timing With One External Wait State

Table 5-35. External Memory Interface Write Switching Characteristics (Ready-on-Write, 1 Wait State)

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-XZCSL)}$	Delay time, XCLKOUT high to zone chip-select active-low		1	ns
$t_{d(XCOHL-XZCSH)}$	Delay time, XCLKOUT high or low to zone chip-select inactive-high	–2	3	ns
$t_{d(XCOH-XA)}$	Delay time, XCLKOUT high to address valid		2	ns
$t_{d(XCOHL-XWEL)}$	Delay time, XCLKOUT high/low to $\overline{XWE}$ low		2	ns
$t_{d(XCOHL-XWEH)}$	Delay time, XCLKOUT high/low to $\overline{XWE}$ high		2	ns
$t_{d(XCOH-XRNWL)}$	Delay time, XCLKOUT high to XR/$\overline{W}$ low		1	ns
$t_{d(XCOHL-XRNWH)}$	Delay time, XCLKOUT high/low to XR/$\overline{W}$ high	–2	1	ns
$t_{en(XD)XWEL}$	Enable time, data bus driven from $\overline{XWE}$ low	0		ns
$t_{d(XWEL-XD)}$	Delay time, data valid after $\overline{XWE}$ active-low		4	ns
$t_{h(XA)XZCSH}$	Hold time, address valid after zone chip-select inactive-high	(1)		ns
$t_{h(XD)XWE}$	Hold time, write data valid after $\overline{XWE}$ inactive-high	TW – 2 (2)		ns
$t_{dis(XD)XRNW}$	Maximum time for DSP to release the data bus after XR/$\overline{W}$ inactive-high		4	ns

(1) During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.
(2) TW = trail period, write access. See Table 5-26.

Table 5-36. Synchronous XREADY Timing Requirements (Ready-on-Write, 1 Wait State)(1)

		MIN	MAX	UNIT
$t_{su(XRDYsynchL)XCOHL}$	Setup time, XREADY (synchronous) low before XCLKOUT high/low	15		ns
$t_{h(XRDYsynchL)}$	Hold time, XREADY (synchronous) low	12		ns
$t_{e(XRDYsynchH)}$	Earliest time XREADY (synchronous) can go high before the sampling XCLKOUT edge		3	ns
$t_{su(XRDYsynchH)XCOHL}$	Setup time, XREADY (synchronous) high before XCLKOUT high/low	15		ns
$t_{h(XRDYsynchH)XZCSH}$	Hold time, XREADY (synchronous) held high after zone chip-select high	0		ns

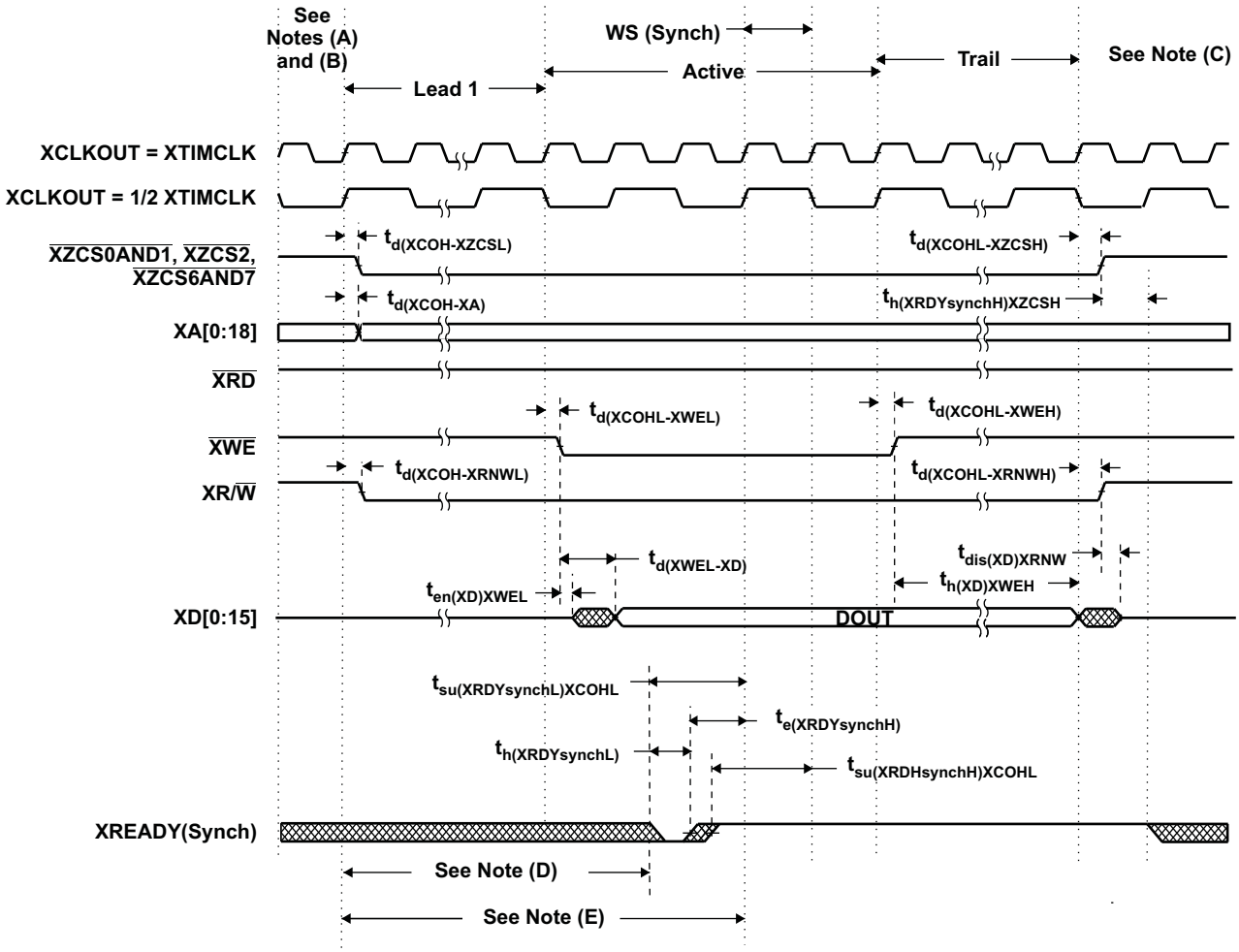
(1) The first XREADY (synchronous) sample occurs with respect to E in Figure 5-31:
E = (XWRLEAD + XWRACTIVE) $t_{c(XTIM)}$
When first sampled, if XREADY (synchronous) is found to be high, then the access will complete. If XREADY (synchronous) is found to be low, it will be sampled again each $t_{c(XTIM)}$ until it is found to be high.
For each sample, setup time from the beginning of the access can be calculated as:
D = (XWRLEAD + XWRACTIVE + n – 1) $t_{c(XTIM)}$ – $t_{su(XRDYsynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3, and so forth).

Table 5-37. Asynchronous XREADY Timing Requirements (Ready-on-Write, 1 Wait State)(1)

		MIN	MAX	UNIT
$t_{su(XRDYasynchL)XCOHL}$	Setup time, XREADY (asynchronous) low before XCLKOUT high/low	11		ns
$t_{h(XRDYasynchL)}$	Hold time, XREADY (asynchronous) low	8		ns
$t_{e(XRDYasynchH)}$	Earliest time XREADY (asynchronous) can go high before the sampling XCLKOUT edge		3	ns
$t_{su(XRDYasynchH)XCOHL}$	Setup time, XREADY (asynchronous) high before XCLKOUT high/low	11		ns
$t_{h(XRDYasynchH)XZCSH}$	Hold time, XREADY (asynchronous) held high after zone chip-select high	0		ns

(1) The first XREADY (synchronous) sample occurs with respect to E in Figure 5-32:
E = (XWRLEAD + XWRACTIVE – 2) $t_{c(XTIM)}$
When first sampled, if XREADY (asynchronous) is found to be high, then the access will complete. If XREADY (asynchronous) is found to be low, it will be sampled again each $t_{c(XTIM)}$ until it is found to be high.
For each sample, setup time from the beginning of the access can be calculated as:
D = (XWRLEAD + XWRACTIVE – 3 + n) $t_{c(XTIM)}$ – $t_{su(XRDYasynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3, and so forth).

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Legend:

= Don't care. Signal can be high or low during this time.

A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.

B. During alignment cycles, all signals will transition to their inactive state.

C. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.

D. For each sample, setup time from the beginning of the access can be calculated as:
D = (XWRLEAD + XWRACTIVE + n – 1) $t_{c(XTIM)}$ – $t_{su(XRDYsynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3 and so forth).

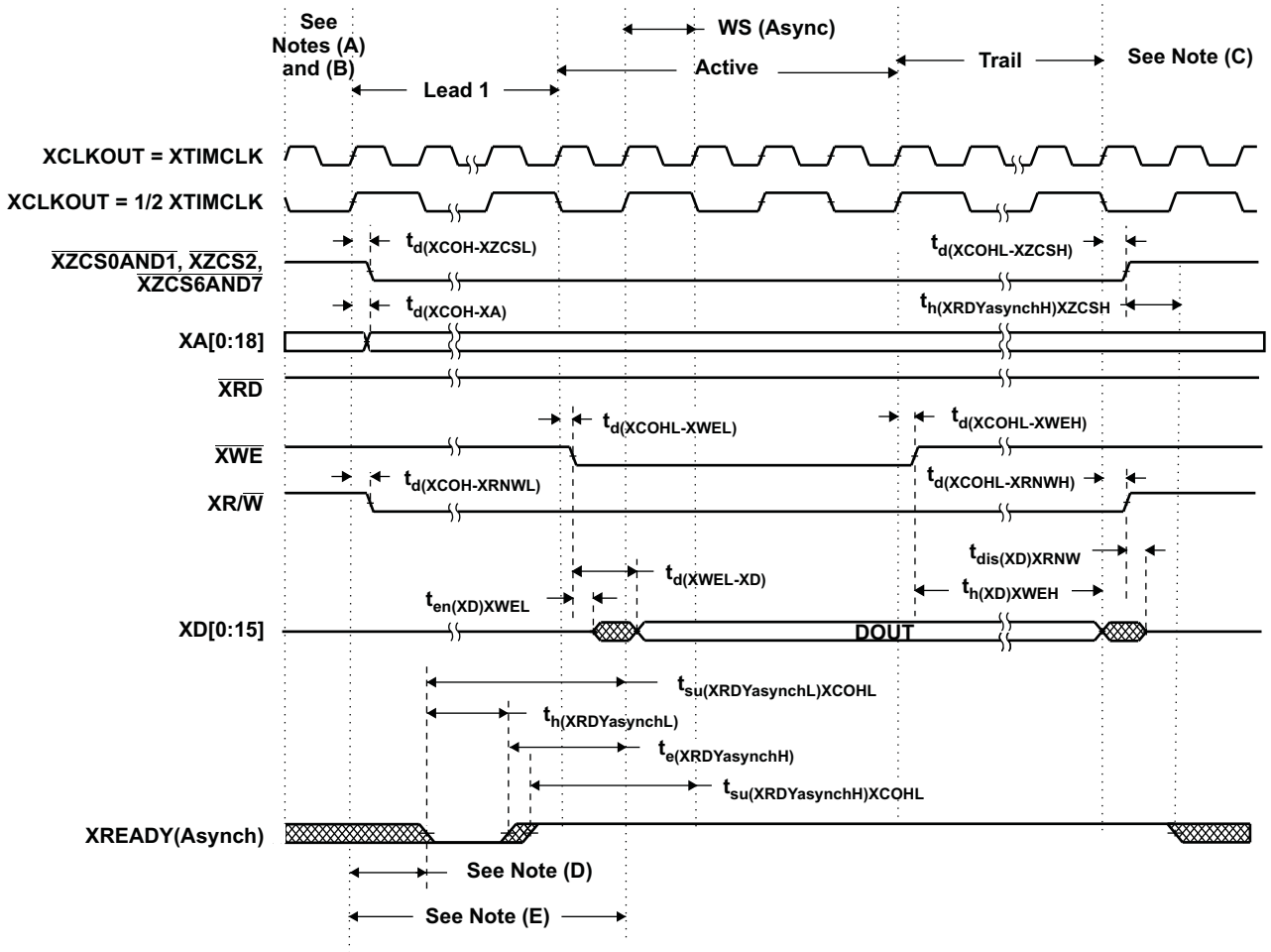
E. Reference for the first sample is with respect to this point
E = (XWRLEAD + XWRACTIVE) $t_{c(XTIM)}$

Figure 5-31. Write With Synchronous XREADY Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
N/A(1)	N/A(1)	N/A(1)	1	0	≥ 1	3	≥ 1	0 = XREADY (Synch)

(1) N/A = "Don't care" for this example



Legend:

= Don't care. Signal can be high or low during this time.

A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.

B. During alignment cycles, all signals will transition to their inactive state.

C. During inactive cycles, the XINTF address bus will always hold the last address put out on the bus. This includes alignment cycles.

D. For each sample, setup time from the beginning of the access can be calculated as:
$D = (XWRLEAD + XWRACTIVE - 3 + n)\ t_{c(XTIM)} - t_{su(XRDYasynchL)XCOHL}$
where n is the sample number (n = 1, 2, 3 and so forth).

E. Reference for the first sample is with respect to this point
$E = (XWRLEAD + XWRACTIVE - 2)\ t_{c(XTIM)}$

Figure 5-32. Write With Asynchronous XREADY Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
N/A(1)	N/A(1)	N/A(1)	1	0	≥ 1	3	≥ 1	1 = XREADY (Async)

(1) N/A = "Don't care" for this example

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5.12.5.13 $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$

If the HOLD mode bit is set while $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$ are both low (external bus accesses granted), the $\overline{\text{XHOLDA}}$ signal is forced high (at the end of the current cycle) and the external interface is taken out of high-impedance mode.

On a reset ($\overline{\text{XRS}}$), the HOLD mode bit is set to 0. If the $\overline{\text{XHOLD}}$ signal is active low on a system reset, the bus and all signal strobes must be in high-impedance mode, and the $\overline{\text{XHOLDA}}$ signal is also driven active low.

When HOLD mode is enabled and $\overline{\text{XHOLDA}}$ is active-low (external bus grant active), the CPU can still execute code from internal memory. If an access is made to the external interface, the CPU is stalled until the $\overline{\text{XHOLD}}$ signal is removed.

An external DMA request, when granted, places the following signals in a high-impedance mode:

XA[18:0]	$\overline{\text{XZCS0AND1}}$
XD[15:0]	$\overline{\text{XZCS2}}$
$\overline{\text{XWE}}$, $\overline{\text{XRD}}$	$\overline{\text{XZCS6AND7}}$
XR/$\overline{\text{W}}$	

All other signals not listed in this group remain in their default or functional operational modes during these signal events.

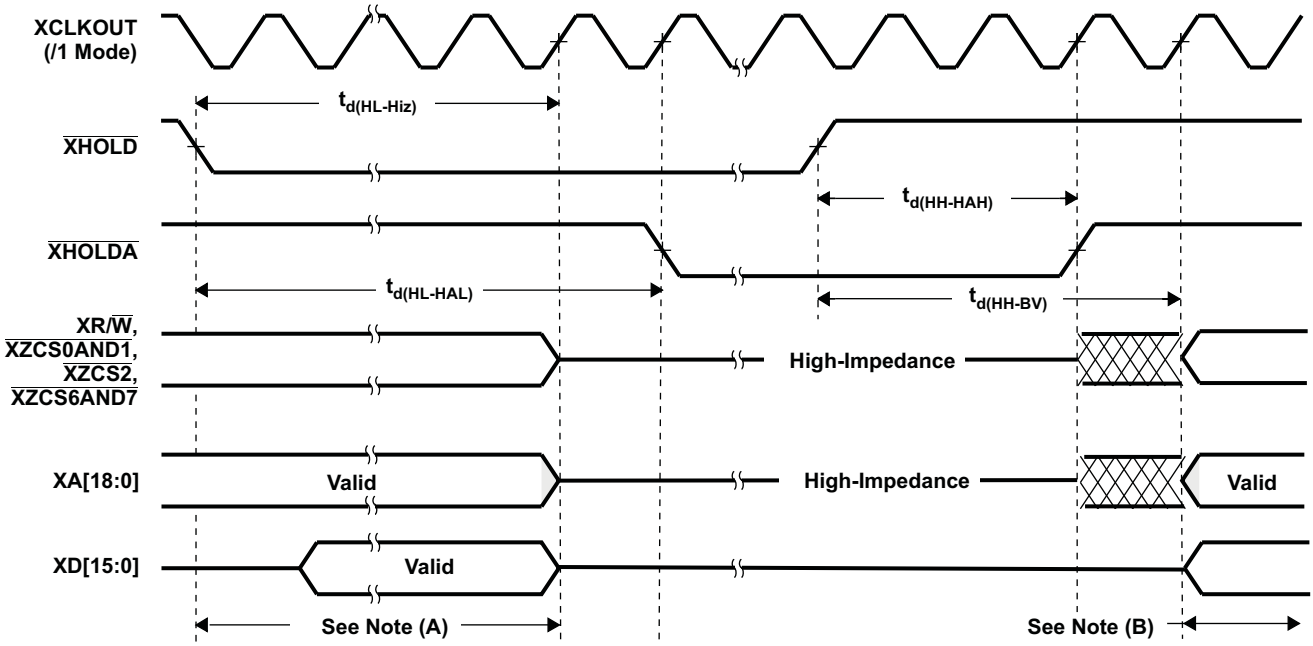
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5.12.5.14 XHOLD/XHOLDA Timing

Table 5-38. XHOLD/XHOLDA Timing Requirements (XCLKOUT = XTIMCLK)(1)(2)

		MIN	MAX	UNIT
$t_{d(HL-HiZ)}$	Delay time, XHOLD low to Hi-Z on all Address, Data, and Control		$4t_{c(XTIM)}$	ns
$t_{d(HL-HAL)}$	Delay time, XHOLD low to XHOLDA low		$5t_{c(XTIM)}$	ns
$t_{d(HH-HAH)}$	Delay time, XHOLD high to XHOLDA high		$3t_{c(XTIM)}$	ns
$t_{d(HH-BV)}$	Delay time, XHOLD high to Bus valid		$4t_{c(XTIM)}$	ns

(1) When a low signal is detected on XHOLD, all pending XINTF accesses will be completed before the bus is placed in a high-impedance state.
(2) The state of XHOLD is latched on the rising edge of XTIMCLK.



A. All pending XINTF accesses are completed.
B. Normal XINTF operation resumes.

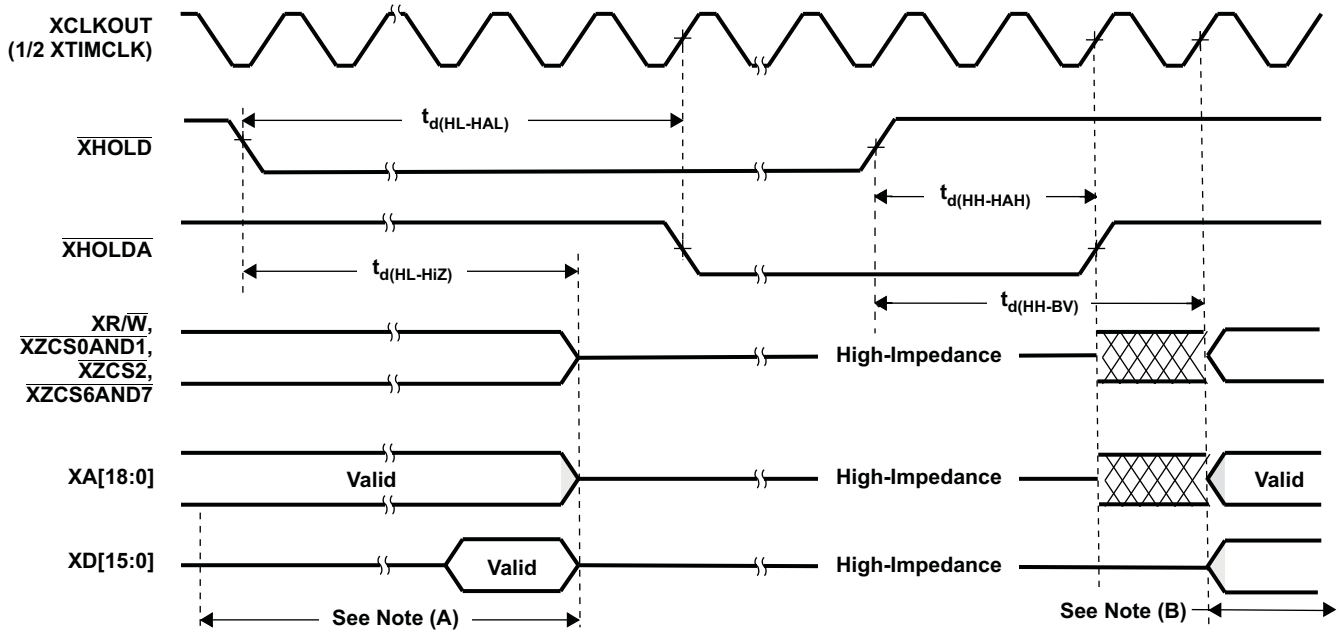
Figure 5-33. External Interface Hold Waveform

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Table 5-39. $\overline{\text{XHOLD}}$/$\overline{\text{XHOLDA}}$ Timing Requirements (XCLKOUT = 1/2 XTIMCLK)(1)(2)(3)

		MIN	MAX	UNIT
$t_{d(HL-HiZ)}$	Delay time, $\overline{\text{XHOLD}}$ low to Hi-Z on all Address, Data, and Control		$4t_{c(XTIM)} + t_{c(XCO)}$	ns
$t_{d(HL-HAL)}$	Delay time, $\overline{\text{XHOLD}}$ low to $\overline{\text{XHOLDA}}$ low		$4t_{c(XTIM)} + 2t_{c(XCO)}$	ns
$t_{d(HH-HAH)}$	Delay time, $\overline{\text{XHOLD}}$ high to $\overline{\text{XHOLDA}}$ high		$4t_{c(XTIM)}$	ns
$t_{d(HH-BV)}$	Delay time, $\overline{\text{XHOLD}}$ high to Bus valid		$6t_{c(XTIM)}$	ns

(1) When a low signal is detected on $\overline{\text{XHOLD}}$, all pending XINTF accesses will be completed before the bus is placed in a high-impedance state.
(2) The state of $\overline{\text{XHOLD}}$ is latched on the rising edge of XTIMCLK.
(3) After the $\overline{\text{XHOLD}}$ is detected low or high, all bus transitions and $\overline{\text{XHOLDA}}$ transitions will occur with respect to the rising edge of XCLKOUT. Thus, for this mode where XCLKOUT = 1/2 XTIMCLK, the transitions can occur up to 1 XTIMCLK cycle earlier than the maximum value specified.



A. All pending XINTF accesses are completed.
B. Normal XINTF operation resumes.

Figure 5-34. $\overline{\text{XHOLD}}$/$\overline{\text{XHOLDA}}$ Timing Requirements (XCLKOUT = 1/2 XTIMCLK)

5.12.5.15 On-Chip Analog-to-Digital Converter

Table 5-40. ADC Absolute Maximum Ratings Over Recommended Operating Conditions (Unless Otherwise Noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{SSA1}/V_{SSA2} to V_{DDA1}/V_{DDA2}/AVDDREFBG	–0.3	4.6	V
Supply voltage range	V_{SS1} to V_{DD1}	–0.3	2.5	V
Analog Input (ADCIN) Clamp Current, total (max)		–20(2)	20(2)	mA

(1) Unless otherwise noted, the list of absolute maximum ratings are specified over recommended operating conditions. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The analog inputs have an internal clamping circuit that clamps the voltage to a diode drop above V_{DDA} or below V_{SS}. The continuous clamp current per pin is ±2 mA.

Table 5-41. ADC Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)—AC Specifications

PARAMETER		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion		62		dB
SNR	Signal-to-noise ratio		62		dB
THD (100 kHz)	Total harmonic distortion		–68		dB
ENOB (SNR)	Effective number of bits		10.1		Bits
SFDR	Spurious free dynamic range		69		dB

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Table 5-42. ADC Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)—DC Specifications(1)

PARAMETER		MIN	TYP	MAX	UNIT
Resolution		12			Bits
ADC clock(2)		1			kHz
				25	MHz
ACCURACY					
INL (Integral nonlinearity)(3)	1–18.75 MHz ADC clock			±1.5	LSB
DNL (Differential nonlinearity)(3)	1–18.75 MHz ADC clock			±1	LSB
Offset error(4)		–80		80	LSB
Overall gain error with internal reference(5)		–200		200	LSB
Overall gain error with external reference(6)	If ADCREFP – ADCREFM = 1 V ± 0.1%	–50		50	LSB
Channel-to-channel offset variation			±8		LSB
Channel-to-channel Gain variation			±8		LSB
ANALOG INPUT					
Analog input voltage (ADCINx to ADCLO)(7)		0		3	V
ADCLO		–5	0	5	mV
Input capacitance			10		pF
Input leakage current			3	±5	µA
INTERNAL VOLTAGE REFERENCE(5)					
Accuracy, $ADCV_{REFP}$		1.9	2	2.1	V
Accuracy, $ADCV_{REFM}$		0.95	1	1.05	V
Voltage difference, ADCREFP – ADCREFM			1		V
Temperature coefficient			50		PPM/°C
Reference noise			100		µV
EXTERNAL VOLTAGE REFERENCE(6)					
Accuracy, $ADCV_{REFP}$		1.9	2	2.1	V
Accuracy, $ADCV_{REFM}$		0.95	1	1.05	V
Input voltage difference, ADCREFP – ADCREFM		0.99	1	1.01	V

(1) Tested at 12.5-MHz ADCCLK.
(2) If SYSCLKOUT ≤ 25 MHz, ADC clock ≤ SYSCLKOUT/2.
(3) The INL degrades for frequencies beyond 18.75 MHz–25 MHz. Applications that require these sampling rates should use a 20K resistor as bias resistor on the ADCRESEXT pin. This improves overall linearity and typical current drawn by the ADC will be a few mA more than 24.9-kΩ bias.
(4) 1 LSB has the weighted value of 3.0/4096 = 0.732 mV.
(5) A single internal band gap reference (±5% accuracy) sources both ADCREFP and ADCREFM signals, and hence, these voltages track together. The ADC converter uses the difference between these two as its reference. The total gain error will be the combination of the gain error shown here and the voltage reference accuracy (ADCREFP – ADCREFM). A software-based calibration procedure is recommended for better accuracy. See the *F2810, F2811, and F2812 ADC Calibration Application Report* and 节 8.4 for relevant documents.
(6) In this mode, the accuracy of external reference is critical for overall gain. The voltage difference (ADCREFP – ADCREFM) will determine the overall accuracy.
(7) Voltages above V_{DDA} + 0.3 V or below V_{SS} – 0.3 V applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.

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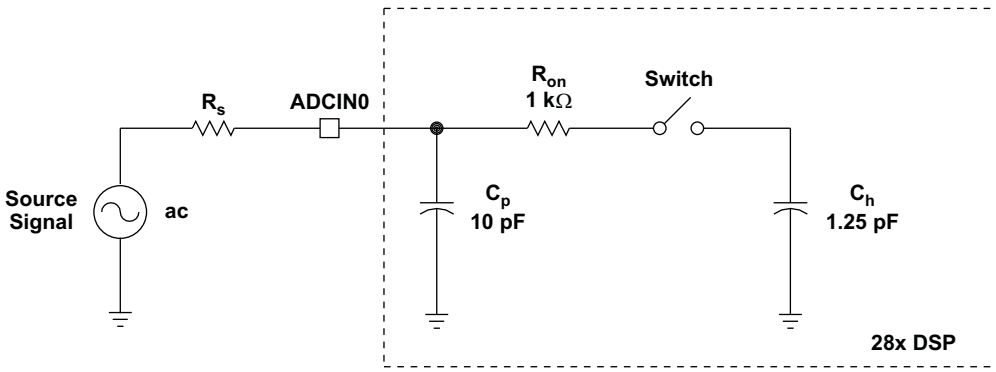
5.12.5.15.1 Current Consumption for Different ADC Configurations

Table 5-43. Current Consumption for Different ADC Configurations (at 25-MHz ADCCLK)(1)

I_{DDA} (TYP)(2)	I_{DDAIO} (TYP)	I_{DD1} (TYP)	ADC OPERATING MODE/CONDITIONS
40 mA	1 µA	0.5 mA	Mode A (Operational Mode): • BG and REF enabled • PWD disabled
7 mA	0	5 µA	Mode B: • ADC clock enabled • BG and REF enabled • PWD enabled
1 µA	0	5 µA	Mode C: • ADC clock enabled • BG and REF disabled • PWD enabled
1 µA	0	0	Mode D: • ADC clock disabled • BG and REF disabled • PWD enabled

(1) Test Conditions:
- SYSCLKOUT = 150 MHz
- ADC module clock = 25 MHz
- ADC performing a continuous conversion of all 16 channels in Mode A

(2) I_{DDA} – includes current into V_{DDA1}/V_{DDA2} and AVDDREFBG



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}): 1 kΩ
Sampling Capacitor (C_h): 1.25 pF
Parasitic Capacitance (C_p): 10 pF
Source Resistance (R_s): 50 Ω

Figure 5-35. ADC Analog Input Impedance Model

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5.12.5.15.2 ADC Power-Up Control Bit Timing

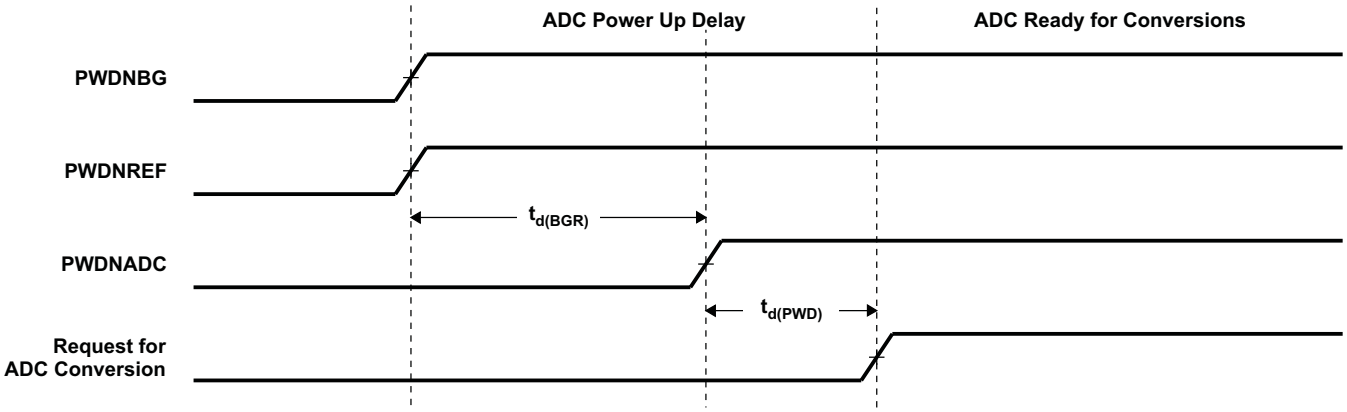


Figure 5-36. ADC Power-Up Control Bit Timing

Table 5-44. ADC Power-Up Delays(1)

		MIN	TYP	MAX	UNIT
$t_{d(BGR)}$	Delay time for band gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) are to be set to 1 before the ADCPWDN bit is enabled.	7	8	10	ms
$t_{d(PWD)}$	Delay time for power-down control to be stable. Bit 5 of the ADCTRL3 register (ADCPWDN) is to be set to 1 before any ADC conversions are initiated.	20	50		µs
				1	ms

(1) These delays are necessary and recommended to make the ADC analog reference circuit stable before conversions are initiated. If conversions are started without these delays, the ADC results will show a higher gain. For power down, all three bits can be cleared at the same time.

5.12.5.15.3 Detailed Description

5.12.5.15.3.1 Reference Voltage

The on-chip ADC has a built-in reference, which provides the reference voltages for the ADC. ADCVREFP is set to 2.0 V and ADCVREFM is set to 1.0 V.

5.12.5.15.3.2 Analog Inputs

The on-chip ADC consists of 16 analog inputs, which are sampled either one at a time or two channels at a time. These inputs are software-selectable.

5.12.5.15.3.3 Converter

The on-chip ADC uses a 12-bit four-stage pipeline architecture, which achieves a high sample rate with low power consumption.

5.12.5.15.3.4 Conversion Modes

The conversion can be performed in two different conversion modes:

- Sequential sampling mode (SMODE = 0)
- Simultaneous sampling mode (SMODE = 1)

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5.12.5.15.4 Sequential Sampling Mode (Single-Channel) (SMODE = 0)

In sequential sampling mode, the ADC can continuously convert input signals on any of the channels (Ax to Bx). The ADC can start conversions on event triggers from the Event Managers (EVA/EVB), software trigger, or from an external ADCSOC signal. If the SMODE bit is 0, the ADC will do conversions on the selected channel on every Sample/Hold pulse. The conversion time and latency of the Result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled at every falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

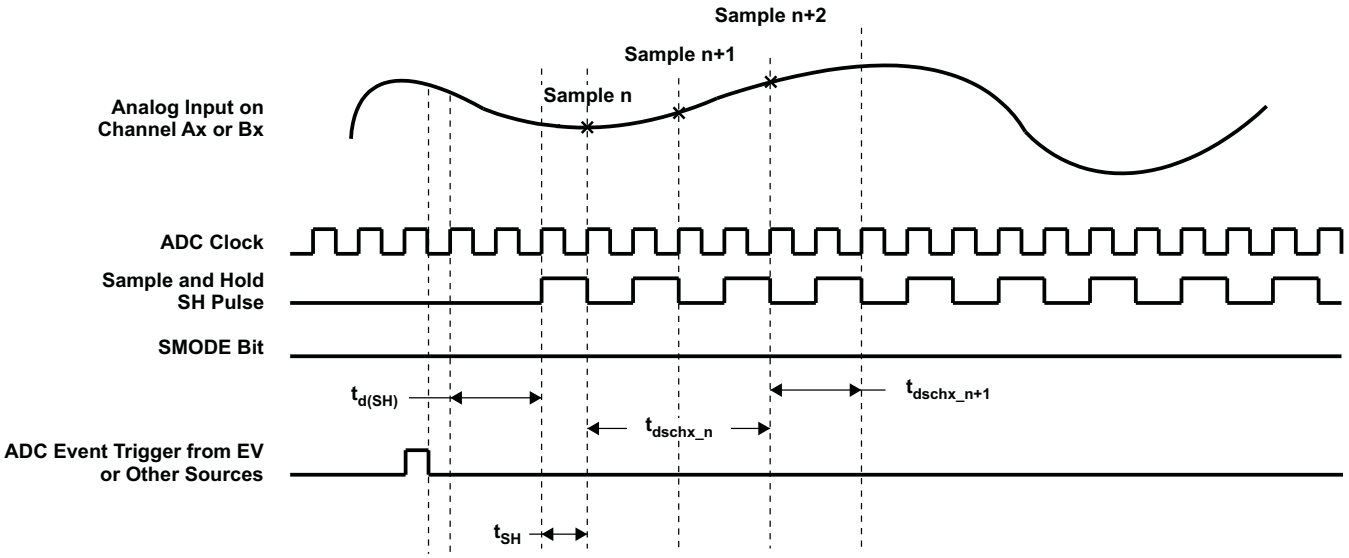


Figure 5-37. Sequential Sampling Mode (Single-Channel) Timing

Table 5-45. Sequential Sampling Mode Timing

		SAMPLE n	SAMPLE n + 1	AT 25-MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 40 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/ Hold width/ Acquisition width	(1 + Acqps) * $t_{c(ADCCLK)}$		40 ns with Acqps = 0	Acqps value = 0–15 ADCTRL1[8:11]
$t_{d(schx_n)}$	Delay time for first result to appear in the Result register	$4t_{c(ADCCLK)}$		160 ns	
$t_{d(schx_n+1)}$	Delay time for successive results to appear in the Result register		(2 + Acqps) * $t_{c(ADCCLK)}$	80 ns	

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5.12.5.15.5 Simultaneous Sampling Mode (Dual-Channel) (SMODE = 1)

In simultaneous mode, the ADC can continuously convert input signals on any one pair of channels (A0/B0 to A7/B7). The ADC can start conversions on event triggers from the Event Managers (EVA/EVB), software trigger, or from an external ADCSOC signal. If the SMODE bit is 1, the ADC will do conversions on two selected channels on every Sample/Hold pulse. The conversion time and latency of the Result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled simultaneously at the falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

NOTE

In Simultaneous Mode, the ADCIN channel pair select has to be A0/B0, A1/B1, ..., A7/B7, and *not* in other combinations (such as A1/B3, and so forth).

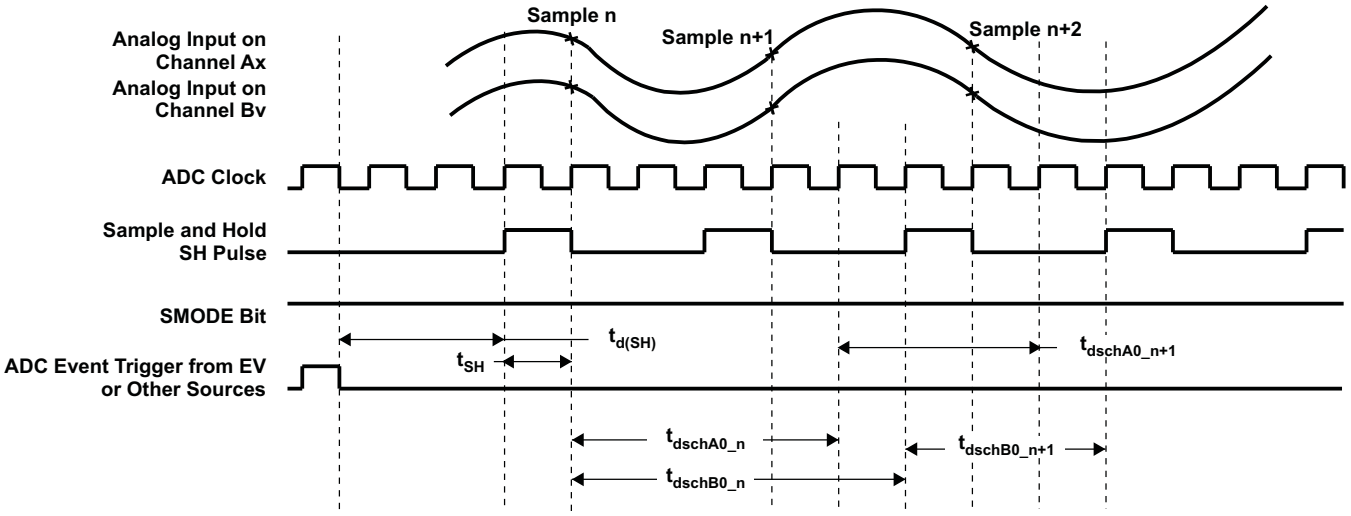


Figure 5-38. Simultaneous Sampling Mode Timing

Table 5-46. Simultaneous Sampling Mode Timing

		SAMPLE n	SAMPLE n + 1	AT 25-MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 40 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/ Acquisition Width	(1 + Acqps) * $t_{c(ADCCLK)}$		40 ns with Acqps = 0	Acqps value = 0–15 ADCTRL1[8:11]
$t_{d(schA0_n)}$	Delay time for first result to appear in Result register	$4t_{c(ADCCLK)}$		160 ns	
$t_{d(schB0_n)}$	Delay time for first result to appear in Result register	$5t_{c(ADCCLK)}$		200 ns	
$t_{d(schA0_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) * $t_{c(ADCCLK)}$	120 ns	
$t_{d(schB0_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) * $t_{c(ADCCLK)}$	120 ns	

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5.12.5.15.6 Definitions of Specifications and Terminology

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volt. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = \frac{(SINAD - 1.76)}{6.02}$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

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5.12.5.16 Multichannel Buffered Serial Port (McBSP) Timing

5.12.5.16.1 McBSP Transmit and Receive Timing

Table 5-47. McBSP Timing Requirements(1)(2)

NO.				MIN	MAX	UNIT
	McBSP module clock (CLKG, CLKX, CLKR) range			1		kHz
					20(3)	MHz
	McBSP module cycle time (CLKG, CLKX, CLKR) range			50		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P – 7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	18		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = CLKSRG/(1 + CLKGDV). CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLKOUT/2). McBSP performance is limited by I/O buffer switching speed.
(3) Internal clock prescalers must be adjusted such that the McBSP clock (CLKG, CLKX, CLKR) speeds are not greater than the I/O buffer speed limit (20 MHz).

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Table 5-48. McBSP Switching Characteristics(1)(2)

NO.	PARAMETER				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D – 5(3)	D + 5(3)	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C – 5(3)	C + 5(3)	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	0	4	ns
				CLKR ext	3	27	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	0	4	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int		8	ns
				CLKX ext		14	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int		9	ns
				CLKX ext		28	
		Delay time, CLKX high to DX valid. Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes.	DXENA = 0	CLKX int		8	
				CLKX ext		14	
			DXENA = 1	CLKX int		P + 8	
				CLKX ext		P + 14	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven. Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes.	DXENA = 0	CLKX int	0		ns
				CLKX ext	6		
			DXENA = 1	CLKX int	P		
				CLKX ext	P + 6		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid. Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode.	DXENA = 0	FSX int		8	ns
				FSX ext		14	
			DXENA = 1	FSX int		P + 8	
				FSX ext		P + 14	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven. Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode.	DXENA = 0	FSX int	0		ns
				FSX ext	6		
			DXENA = 1	FSX int	P		
				FSX ext	P + 6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns.
(3) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

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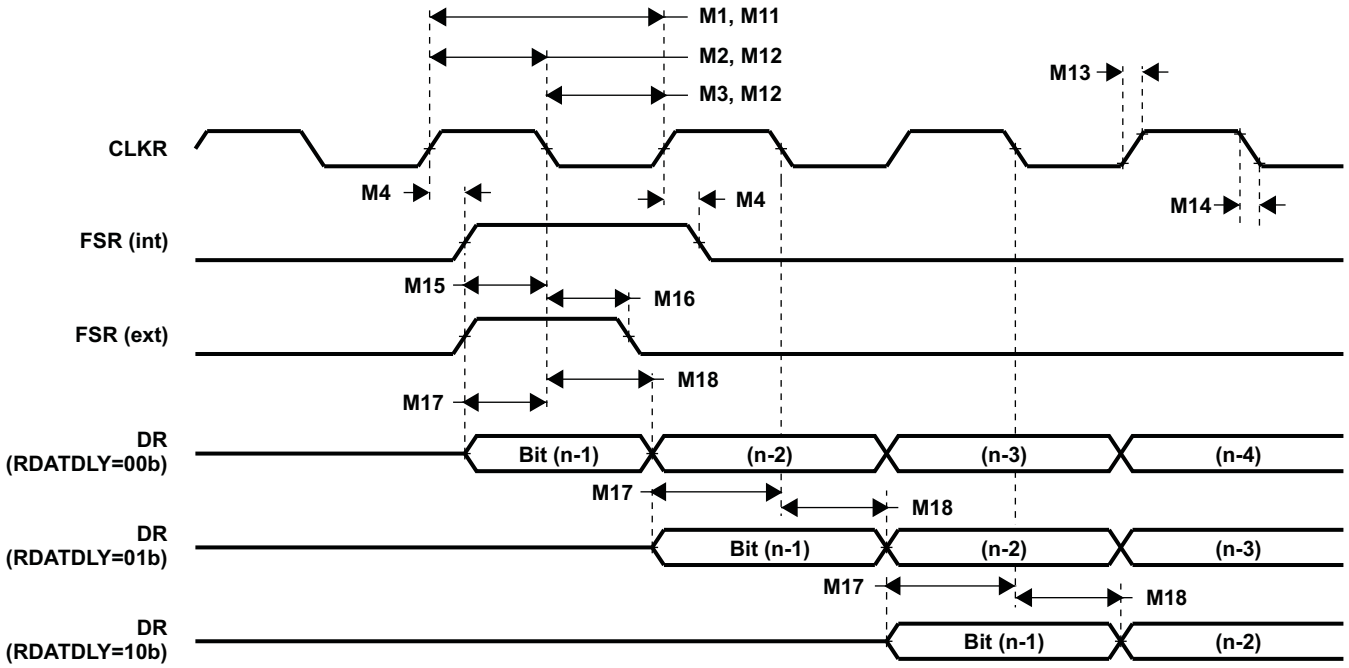


Figure 5-39. McBSP Receive Timing

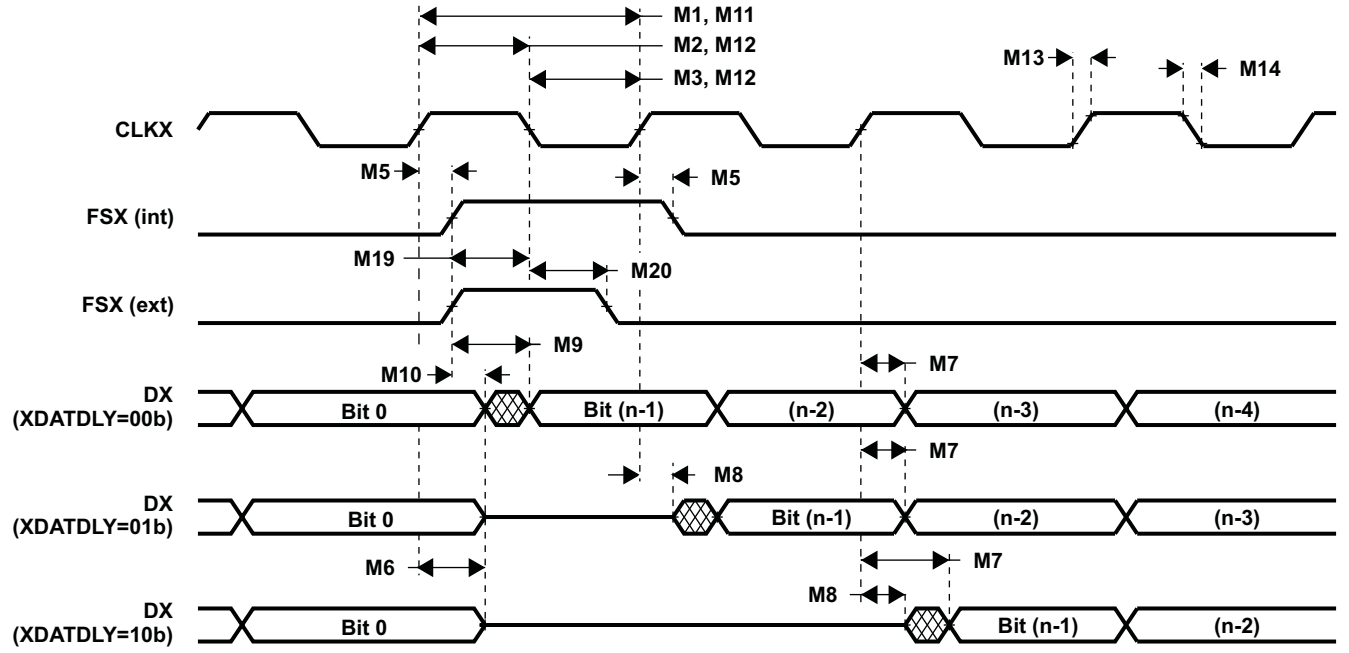


Figure 5-40. McBSP Transmit Timing

5.12.5.16.2 McBSP as SPI Master or Slave Timing

Table 5-49. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)(1)(2)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high			8P + 10		ns
M33	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 5-50. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)(1)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M24	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	2P				ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P				ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

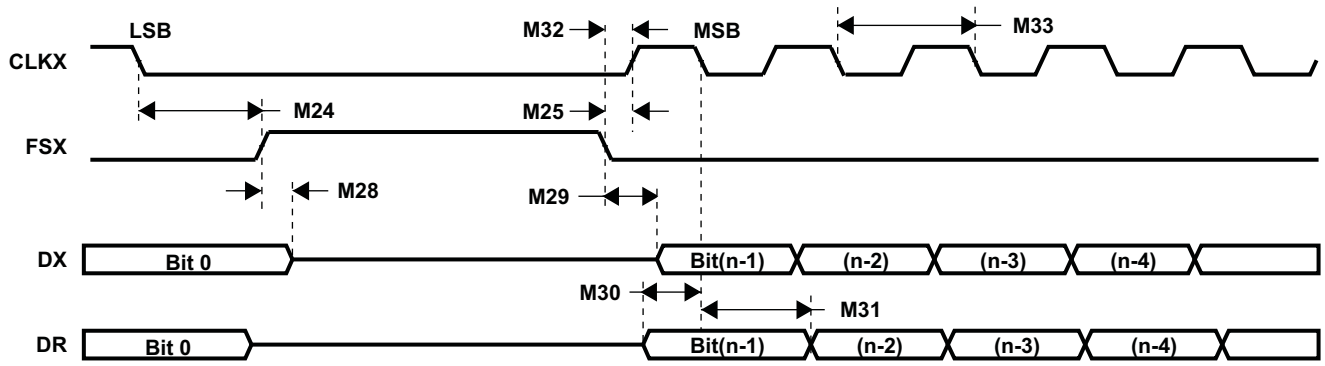


Figure 5-41. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

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Table 5-51. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)(1)(2)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high			16P + 10		ns
M42	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 5-52. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)(1)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M34	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	P				ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	2P				ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P + 6		7P + 6		ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

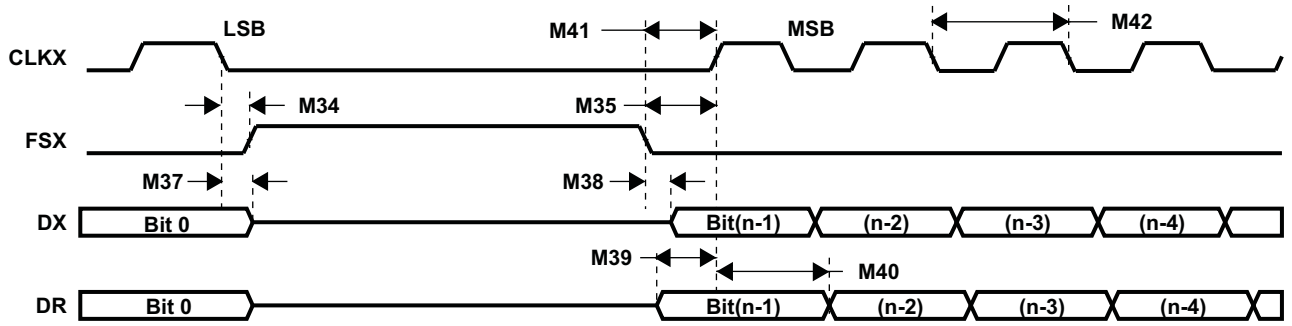


Figure 5-42. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

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Table 5-53. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)(1)(2)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			8P + 10		ns
M52	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 5-54. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)(1)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M43	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	2P				ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	P				ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

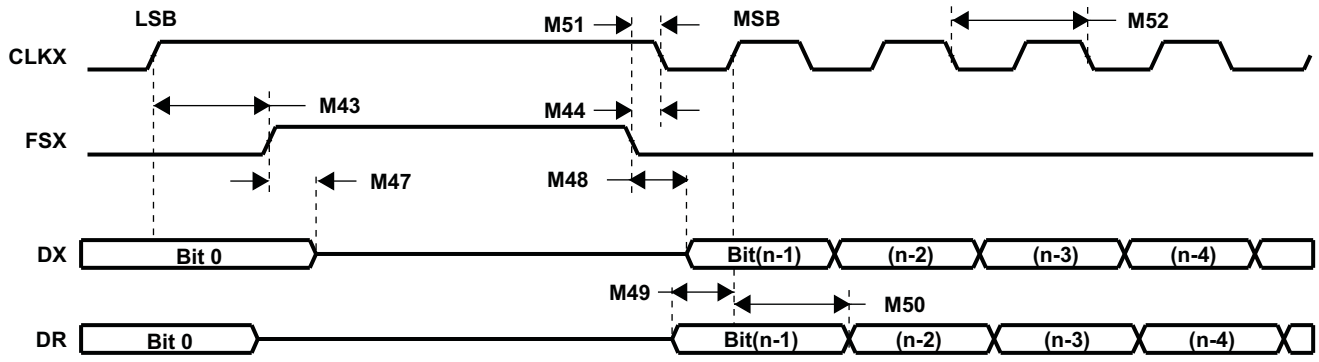


Figure 5-43. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

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Table 5-55. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)(1)(2)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			16P + 10		ns
M61	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 5-56. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)(1)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M53	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	P				ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	2P				ns
M55	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	0	3P + 6	5P + 20	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P + 6		7P + 6		ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

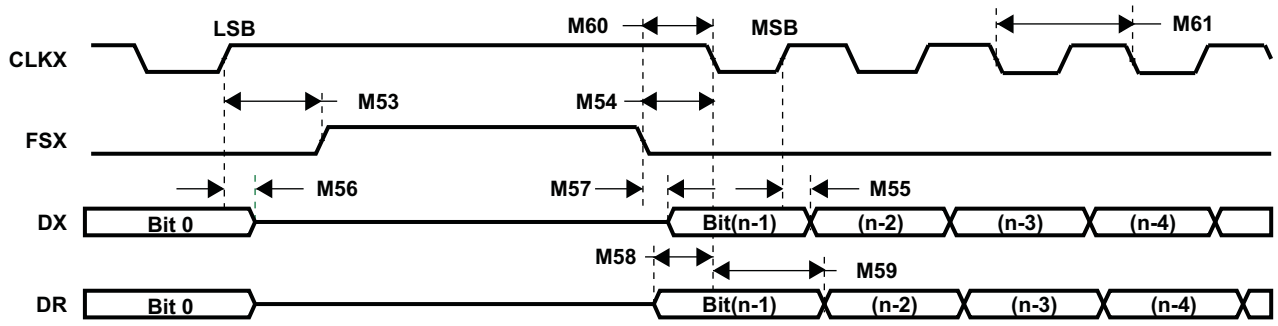


Figure 5-44. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.12.6 Emulator Connection Without Signal Buffering for the DSP

Figure 5-45 shows the connection between the DSP and JTAG header for a single-processor configuration. If the distance between the JTAG header and the DSP is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 5-45 shows the simpler, no-buffering situation. For the pullup/pulldown resistor values, see the pin description section.

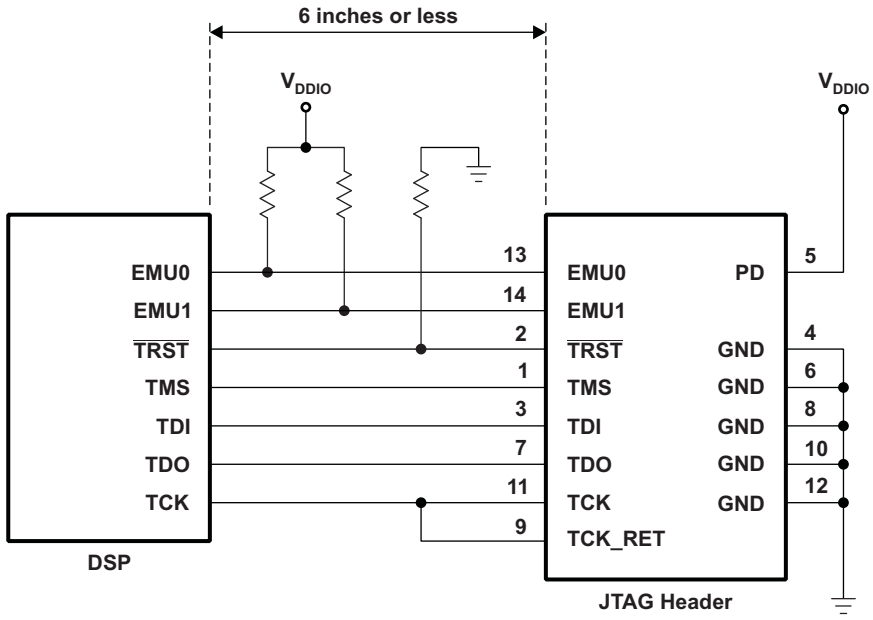


Figure 5-45. Emulator Connection Without Signal Buffering for the DSP

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5.12.7 Interrupt Timing

Table 5-57. Interrupt Switching Characteristics

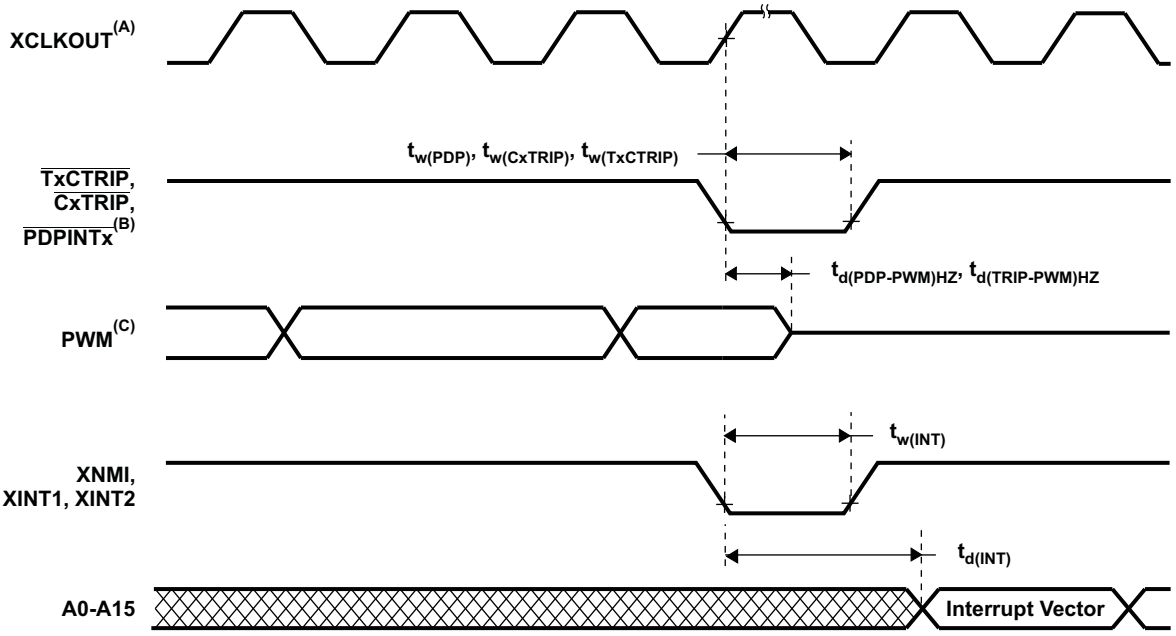
PARAMETER			MIN	MAX	UNIT
$t_{d(PDP-PWM)HZ}$	Delay time, $\overline{PDPINTx}$ low to PWM high-impedance state	Without input qualifier		12	ns
		With input qualifier		$1t_{c(SCO)}$ + IQT + 12 (1)	
$t_{d(TRIP-PWM)HZ}$	Delay time, $\overline{CxTRIP}$/$\overline{TxCTRIP}$ signals low to PWM high-impedance state	Without input qualifier		3 * $t_{c(SCO)}$	ns
		With input qualifier		$2t_{c(SCO)}$ + IQT (1)	
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch			IQT + $12t_{c(SCO)}$ (1)	ns

(1) Input Qualification Time (IQT) = [$t_{c(SCO)}$ × 2 × QUALPRD] × 5 + [$t_{c(SCO)}$ × 2 × QUALPRD].

Table 5-58. Interrupt Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	With no qualifier	$2t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)}$ + IQT (1)		
$t_{w(PDP)}$	Pulse duration, $\overline{PDPINTx}$ input low	With no qualifier	$2t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)}$ + IQT (1)		
$t_{w(CxTRIP)}$	Pulse duration, $\overline{CxTRIP}$ input low	With no qualifier	$2t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)}$ + IQT (1)		
$t_{w(TxCTRIP)}$	Pulse duration, $\overline{TxCTRIP}$ input low	With no qualifier	$2t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)}$ + IQT (1)		

(1) Input Qualification Time (IQT) = [$t_{c(SCO)}$ × 2 × QUALPRD] × 5 + [$t_{c(SCO)}$ × 2 × QUALPRD].



A. XCLKOUT = SYSCLKOUT

B. $\overline{TxCTRIP}$ – $\overline{T1CTRIP}$, $\overline{T2CTRIP}$, $\overline{T3CTRIP}$, $\overline{T4CTRIP}$
$\overline{CxTRIP}$ – $\overline{C1TRIP}$, $\overline{C2TRIP}$, $\overline{C3TRIP}$, $\overline{C4TRIP}$, $\overline{C5TRIP}$, or $\overline{C6TRIP}$
$\overline{PDPINTx}$ – $\overline{PDPINTA}$ or $\overline{PDPINTB}$

C. $\overline{PWM}$ refers to **all** the PWM pins in the device (that is, PWMn and TnPWM pins or PWM pin pair relevant to each $\overline{CxTRIP}$ pin). The state of the PWM pins after $\overline{PDPINTx}$ is taken high depends on the state of the FCOMPOE bit.

Figure 5-46. External Interrupt Timing

5.12.8 Flash Timing

Table 5-59. Flash Endurance for A and S Temperature Material(1)

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (Write/Erase cycles)	0°C to 85°C (ambient)	20000(2)	50000(2)		cycles
N_{OTP}	OTP endurance for the array (Write cycles)	0°C to 85°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.
(2) The Write/Erase cycle numbers of 20000 (MIN) and 50000 (TYP) are applicable ***only*** for silicon revision G. For older silicon revisions, the Write/Erase cycle numbers of 100 (MIN) and 1000 (TYP) are applicable.

Table 5-60. Flash Endurance for Q Temperature Material(1)

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (Write/Erase cycles)	–40°C to 125°C (ambient)	20000(2)	50000(2)		cycles
N_{OTP}	OTP endurance for the array (Write cycles)	–40°C to 125°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.
(2) The Write/Erase cycle numbers of 20000 (MIN) and 50000 (TYP) are applicable ***only*** for silicon revision G. For older silicon revisions, the Write/Erase cycle numbers of 100 (MIN) and 1000 (TYP) are applicable.

Table 5-61. Flash Parameters at 150-MHz SYSCLKOUT(1)

PARAMETER				MIN	TYP	MAX	UNIT
Program Time	16-Bit Word	Using Flash API v1(2)			35		µs
		Using Flash API v2.10			50		
	8K Sector	Using Flash API v1(2)			170		ms
		Using Flash API v2.10			250		
	16K Sector	Using Flash API v1(2)			320		ms
		Using Flash API v2.10			500		
Erase Time(3)	8K Sector				10		s
	16K Sector				11		
$I_{DD3VFLP}$	V_{DD3VFL} current consumption during the Erase/Program cycle		Erase		75		mA
			Program		35		
I_{DDP}	V_{DD} current consumption during Erase/Program cycle				140		mA
I_{DDIOP}	V_{DDIO} current consumption during Erase/Program cycle				20		mA

(1) Typical parameters as seen at room temperature including function call overhead, with all peripherals off. It is important to maintain a stable power supply during the entire flash programming process. It is conceivable that device current consumption during flash programming could be higher than normal operating conditions. The power supply used should ensure V_{MIN} on the supply rails at all times, as specified in the Recommended Operating Conditions of the data sheet. Any brown-out or interruption to power during erasing/programming could potentially corrupt the password locations and lock the device permanently. Powering a target board (during flash programming) through the USB port is not recommended, as the port may be unable to respond to the power demands placed during the programming process.
(2) Flash API v1.00 is useable on rev. C silicon only.
(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

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Table 5-62. Flash/OTP Access Timing

PARAMETER		MIN	MAX	UNIT
$t_{a(fp)}$	Paged Flash access time	36		ns
$t_{a(fr)}$	Random Flash access time	36		ns
$t_{a(OTP)}$	OTP access time	60		ns

Table 5-63. Flash Data Retention Duration

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{retention}$	Data retention duration	T_J = 55°C	15		years

Table 5-64. Minimum Required Flash Wait States at Different Frequencies

SYSCLKOUT (MHz)	SYSCLKOUT (ns)	PAGE WAIT STATE(1)	RANDOM WAIT STATE(1) (2)	OTP
150	6.67	5	5	8
120	8.33	4	4	7
100	10	3	3	5
75	13.33	2	2	4
50	20	1	1	2
30	33.33	1	1	1
25	40	0	1	1
15	66.67	0	1	1
4	250	0	1	1

(1) Formulas to compute page wait state and random wait state:

$$\text{Flash Page Wait State} = \left[\left(\frac{t_{a(fp)}}{t_{c(SCO)}}\right) - 1\right] \quad \text{(round up to the next highest integer, or 0, whichever is larger)}$$

$$\text{Flash Random Wait State} = \left[\left(\frac{t_{a(fr)}}{t_{c(SCO)}}\right) - 1\right] \quad \text{(round up to the next highest integer, or 1, whichever is larger)}$$

$$\text{OTP Wait State} = \left[\left(\frac{t_{a(OTP)}}{t_{c(SCO)}}\right) - 1\right] \quad \text{(round up to the next highest integer, or 1, whichever is larger)}$$

(2) Random wait state must be greater than or equal to 1.

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6 Detailed Description

6.1 Brief Descriptions

6.1.1 C28x CPU

The C28x DSP generation is the newest member of the TMS320C2000™ DSP platform. The C28x is source code compatible to the 24x/240x DSP devices, hence existing 240x users can leverage their significant software investment. Additionally, the C28x is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

6.1.2 Memory Bus (Harvard Bus Architecture)

As with many DSP type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed “Harvard Bus”, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus will prioritize memory accesses. Generally, the priority of Memory Bus accesses can be summarized as follows:

Highest: Data Writes (Simultaneous data and program writes cannot occur on the memory bus.)

Program Writes (Simultaneous data and program writes cannot occur on the memory bus.)

Data Reads

Program Reads (Simultaneous program reads and fetches cannot occur on the memory bus.)

Lowest: Fetches (Simultaneous program reads and fetches cannot occur on the memory bus.)

6.1.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) DSP family of devices, the F281x adopts a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor “Memory Bus” into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Two versions of the peripheral bus are supported on the F281x. One version only supports 16-bit accesses (called peripheral frame 2). The other version supports both 16- and 32-bit accesses (called peripheral frame 1).

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6.1.4 Real-Time JTAG and Analysis

The F281x implements the standard IEEE 1149.1 JTAG interface. Additionally, the F281x supports real-time mode of operation whereby the contents of memory, peripheral, and register locations can be modified while the processor is running and executing code and servicing interrupts. The user can also single step through non-time critical code while enabling time-critical interrupts to be serviced without interference. The F281x implements the real-time mode in hardware within the CPU. This is a unique feature to the F281x, no software monitor is required. Additionally, special analysis hardware is provided that allows the user to set hardware breakpoint or data/address watch-points and generate various user selectable break events when a match occurs.

6.1.5 External Interface (XINTF) (F2812 Only)

This asynchronous interface consists of 19 address lines, 16 data lines, and three chip-select lines. The chip-select lines are mapped to five external zones, Zones 0, 1, 2, 6, and 7. Zones 0 and 1 share a single chip-select; Zones 6 and 7 also share a single chip-select. Each of the five zones can be programmed with a different number of wait states, strobe signal setup and hold timing and each zone can be programmed for extending wait states externally or not. The programmable wait-state, chip-select and programmable strobe timing enables glueless interface to external memories and peripherals.

6.1.6 Flash

The F2812 and F2811 contain 128K x 16 of embedded flash memory, segregated into four 8K x 16 sectors, and six 16K x 16 sectors. The F2810 has 64K x 16 of embedded flash, segregated into two 8K x 16 sectors, and three 16K x 16 sectors. All three devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800–0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information.

NOTE

The F2810/F2811/F2812 Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x281x DSP System Control and Interrupts Reference Guide*.

6.1.7 M0, M1 SARAMs

All C28x devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 block overlaps the 240x device B0, B1, B2 RAM blocks and hence the mapping of data variables on the 240x devices can remain at the same physical address on C28x devices. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

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6.1.8 L0, L1, H0 SARAMs

The F281x contains an additional 16K x 16 of single-access RAM, divided into three blocks (4K + 4K + 8K). Each block can be independently accessed hence minimizing pipeline stalls. Each block is mapped to both program and data space.

6.1.9 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. The Boot ROM program executes after device reset and checks several GPIO pins to determine which boot mode to enter. For example, the user can select to execute code already present in the internal Flash or download new software to internal RAM through one of several serial ports. Other boot modes exist as well. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms. Table 6-1 shows the details of how various boot modes may be invoked. See the *TMS320x281x DSP Boot ROM Reference Guide*, for more information.

Table 6-1. Boot Mode Selection(1)(2)

BOOT MODE SELECTED	GPIOF4 (SCITXDA)	GPIOF12 (MDXA)	GPIOF3 (SPISTEA)	GPIOF2 (SPICLK)
GPIO PU status(3)	PU	No PU	No PU	No PU
Jump to Flash address 0x3F 7FF6. A branch instruction must have been programmed here prior to reset to re-direct code execution as desired.	1	x	x	x
Call SPI_Boot to load from an external serial SPI EEPROM	0	1	x	x
Call SCI_Boot to load from SCI-A	0	0	1	1
Jump to H0 SARAM address 0x3F 8000	0	0	1	0
Jump to OTP address 0x3D 7800	0	0	0	1
Call Parallel_Boot to load from GPIO Port B	0	0	0	0

(1) Extra care must be taken due to any effect toggling SPICLK to select a boot mode may have on external logic.
(2) If the boot mode selected is Flash, H0, or OTP, then no external code is loaded by the bootloader.
(3) PU = pin has an internal pullup. No PU = pin does not have an internal pullup.

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6.1.10 Security

The F281x supports high levels of security to protect the user firmware from being reverse-engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit ”KEY” value, which matches the value stored in the password locations within the Flash.

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F 7F80 and 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F 7F80 through 0x3F 7FEF may be used for code or data.
- The 128-bit password (at 0x3F 7FF8–0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

Table 6-2. Impact of Using the Code Security Module

ADDRESS	CODE SECURITY STATUS	
	Code Security Enabled	Code Security Disabled
0x3F 7F80 – 0x3F 7FEF	Fill with 0x0000	Application code and data(1)
0x3F 7FF0 – 0x3F 7FF5		
0x3D 7BFC – 0x3D 7BFF	Application code and data	

(1) See the *TMS320F281x DSPs Silicon Errata* for some restrictions.

Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANT ABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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6.1.11 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F281x, 45 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

6.1.12 External Interrupts (XINT1, XINT2, XINT13, XNMI)

The F281x supports three masked external interrupts (XINT1, 2, 13). XINT13 is combined with one non-masked external interrupt (XNMI). The combined signal name is XNMI_XINT13. Each of the interrupts can be selected for negative or positive edge triggering and can also be enabled/disabled (including the XNMI). The masked interrupts also contain a 16-bit free-running up-counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time-stamp the interrupt.

6.1.13 Oscillator and PLL

The F281x can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10-input clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to Section 5 for timing details. The PLL block can be set in bypass mode.

6.1.14 Watchdog

The F281x supports a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary.

6.1.15 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except eCAN) and the event managers, CAP and QEP blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

6.1.16 Low-Power Modes

The F281x devices are fully static CMOS devices. Three low-power modes are provided:

IDLE: Place CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that must function during IDLE are left operating. An enabled interrupt from an active peripheral will wake the processor from IDLE mode.

STANDBY: Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event.

HALT: Turns off the internal oscillator. This mode basically shuts down the device and places it in the lowest possible power consumption mode. Only a reset or XNMI can wake the device from this mode.

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6.1.17 Peripheral Frames 0, 1, 2 (PFn)

The F281x segregates peripherals into three sections. The mapping of peripherals is as follows:

PF0:	XINTF:	External Interface Configuration Registers (F2812 only)
	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Control, Programming, Erase, Verify Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
PF1:	eCAN:	eCAN Mailbox and Control Registers
PF2:	SYS:	System Control Registers
	GPIO:	GPIO Mux Configuration and Control Registers
	EV:	Event Manager (EVA/EVB) Control Registers
	McBSP:	McBSP Control and TX/RX Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Peripheral Interface (SPI) Control and RX/TX Registers
	ADC:	12-Bit ADC Registers

6.1.18 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose I/O (GPIO) signals. This multiplexing enables use of a pin as GPIO if the peripheral signal or function is not used. On reset, all GPIO pins are configured as inputs. The user can then individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

6.1.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is reserved for the DSP/BIOS Real-Time OS, and is connected to INT14 of the CPU. If DSP/BIOS is not being used, CPU-Timer 2 is available for general use. CPU-Timer 1 is for general use and can be connected to INT13 of the CPU. CPU-Timer 0 is also for general use and is connected to the PIE block.

6.1.20 Control Peripherals

The F281x supports the following peripherals that are used for embedded control and communication:

EV: The event manager module includes general-purpose timers, full-compare/PWM units, capture inputs (CAP) and quadrature-encoder pulse (QEP) circuits. Two such event managers are provided which enable two three-phase motors to be driven or four two-phase motors. The event managers on the F281x are compatible to the event managers on the 240x devices (with some minor enhancements).

ADC: The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

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6.1.21 Serial Port Peripherals

The F281x supports the following serial communication peripherals:

eCAN: This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is compliant with ISO 11898-1 (CAN 2.0B).

McBSP: The multichannel buffered serial port (McBSP) connects to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo audio DAC devices. The McBSP receive and transmit registers are supported by a 16-level FIFO that significantly reduces the overhead for servicing this peripheral.

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the F281x, the port supports a 16-level, receive-and-transmit FIFO for reducing servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the F281x, the port supports a 16-level, receive-and-transmit FIFO for reducing servicing overhead.

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6.2 Peripherals

The integrated peripherals of the F281x are described in the following subsections:

- Three 32-bit CPU-Timers
- Two event-manager modules (EVA, EVB)
- Enhanced analog-to-digital converter (ADC) module
- Enhanced controller area network (eCAN) module
- Multichannel buffered serial port (McBSP) module
- Serial communications interface modules (SCI-A, SCI-B)
- Serial peripheral interface (SPI) module
- Digital I/O and shared pin functions

6.2.1 32-Bit CPU-Timers 0/1/2

There are three 32-bit CPU-timers on the F281x devices (CPU-TIMER0/1/2).

Timer 2 is reserved for DSP/BIOS. CPU-Timer 0 and CPU-Timer 1 can be used in user applications. These timers are different from the general-purpose (GP) timers that are present in the Event Manager modules (EVA, EVB).

NOTE

If the application is not using DSP/BIOS, then CPU-Timer 2 can be used in the application.

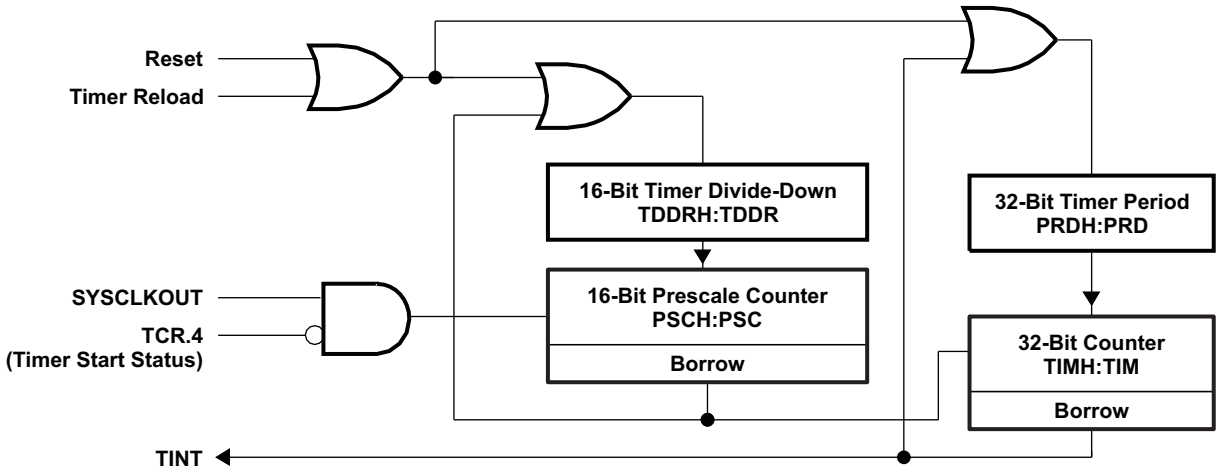
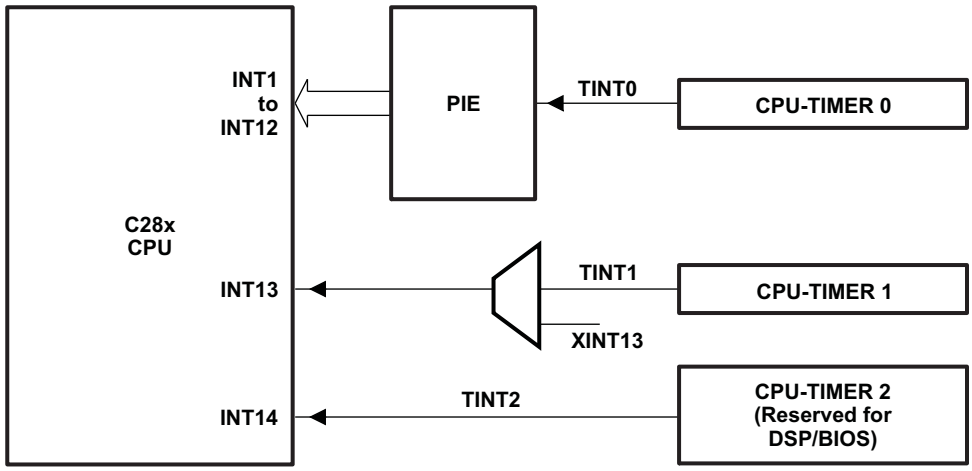


Figure 6-1. CPU-Timers

In the F281x devices, the timer interrupt signals (TINT0, TINT1, TINT2) are connected as shown in Figure 6-2.



A. The timer registers are connected to the memory bus of the C28x processor.
B. The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

Figure 6-2. CPU-Timer Interrupts Signals and Output Signal

The general operation of the timer is as follows: The 32-bit counter register “TIMH:TIM” is loaded with the value in the period register “PRDH:PRD”. The counter register decrements at the SYSCLKOUT rate of the C28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 6-3 are used to configure the timers. For more information, see the *TMS320x281x DSP System Control and Interrupts Reference Guide*.

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Table 6-3. CPU-Timers 0, 1, 2 Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER0TIM	0x00 0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x00 0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x00 0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x00 0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x00 0C04	1	CPU-Timer 0, Control Register
Reserved	0x00 0C05	1	
TIMER0TPR	0x00 0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x00 0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x00 0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x00 0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x00 0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x00 0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x00 0C0C	1	CPU-Timer 1, Control Register
Reserved	0x00 0C0D	1	
TIMER1TPR	0x00 0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x00 0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x00 0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x00 0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x00 0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x00 0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x00 0C14	1	CPU-Timer 2, Control Register
Reserved	0x00 0C15	1	
TIMER2TPR	0x00 0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x00 0C17	1	CPU-Timer 2, Prescale Register High
Reserved	0x00 0C18 – 0x00 0C3F	40	

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6.2.2 Event Manager Modules (EVA, EVB)

The event-manager modules include general-purpose (GP) timers, full-compare/PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. EVA and EVB timers, compare units, and capture units function identically. However, timer/unit names differ for EVA and EVB. Table 6-4 shows the module and signal names used. Table 6-4 shows the features and functionality available for the event-manager modules and highlights EVA nomenclature.

Event managers A and B have identical peripheral register sets with EVA starting at 7400h and EVB starting at 7500h. The paragraphs in this section describe the function of GP timers, compare units, capture units, and QEPs using EVA nomenclature. These paragraphs are applicable to EVB with regard to function—however, module/signal names would differ. Table 6-5 lists the EVA registers. For more information, see the *TMS320x281x DSP Event Manager (EV) Reference Guide*.

Table 6-4. Module and Signal Names for EVA and EVB

EVENT MANAGER MODULES	EVA		EVB	
	MODULE	SIGNAL	MODULE	SIGNAL
GP Timers	GP Timer 1 GP Timer 2	T1PWM/T1CMP T2PWM/T2CMP	GP Timer 3 GP Timer 4	T3PWM/T3CMP T4PWM/T4CMP
Compare Units	Compare 1 Compare 2 Compare 3	PWM1/2 PWM3/4 PWM5/6	Compare 4 Compare 5 Compare 6	PWM7/8 PWM9/10 PWM11/12
Capture Units	Capture 1 Capture 2 Capture 3	CAP1 CAP2 CAP3	Capture 4 Capture 5 Capture 6	CAP4 CAP5 CAP6
QEP Channels	QEP1 QEP2 QEPI1	QEP1 QEP2	QEP3 QEP4 QEPI2	QEP3 QEP4
External Clock Inputs	Direction External Clock	TDIRA TCLKINA	Direction External Clock	TDIRB TCLKINB
External Trip Inputs	Compare	$\overline{\text{C1TRIP}}$ $\overline{\text{C2TRIP}}$ $\overline{\text{C3TRIP}}$	Compare	$\overline{\text{C4TRIP}}$ $\overline{\text{C5TRIP}}$ $\overline{\text{C6TRIP}}$
External Trip Inputs		$\overline{\text{T1CTRIP_PDPINTA}}$(1) $\overline{\text{T2CTRIP}}$/EVASOC		$\overline{\text{T3CTRIP_PDPINTB}}$(1) $\overline{\text{T4CTRIP}}$/EVBSOC

(1) In the 24x/240x-compatible mode, the $\overline{\text{T1CTRIP_PDPINTA}}$ pin functions as $\overline{\text{PDPINTA}}$ and the $\overline{\text{T3CTRIP_PDPINTB}}$ pin functions as $\overline{\text{PDPINTB}}$.

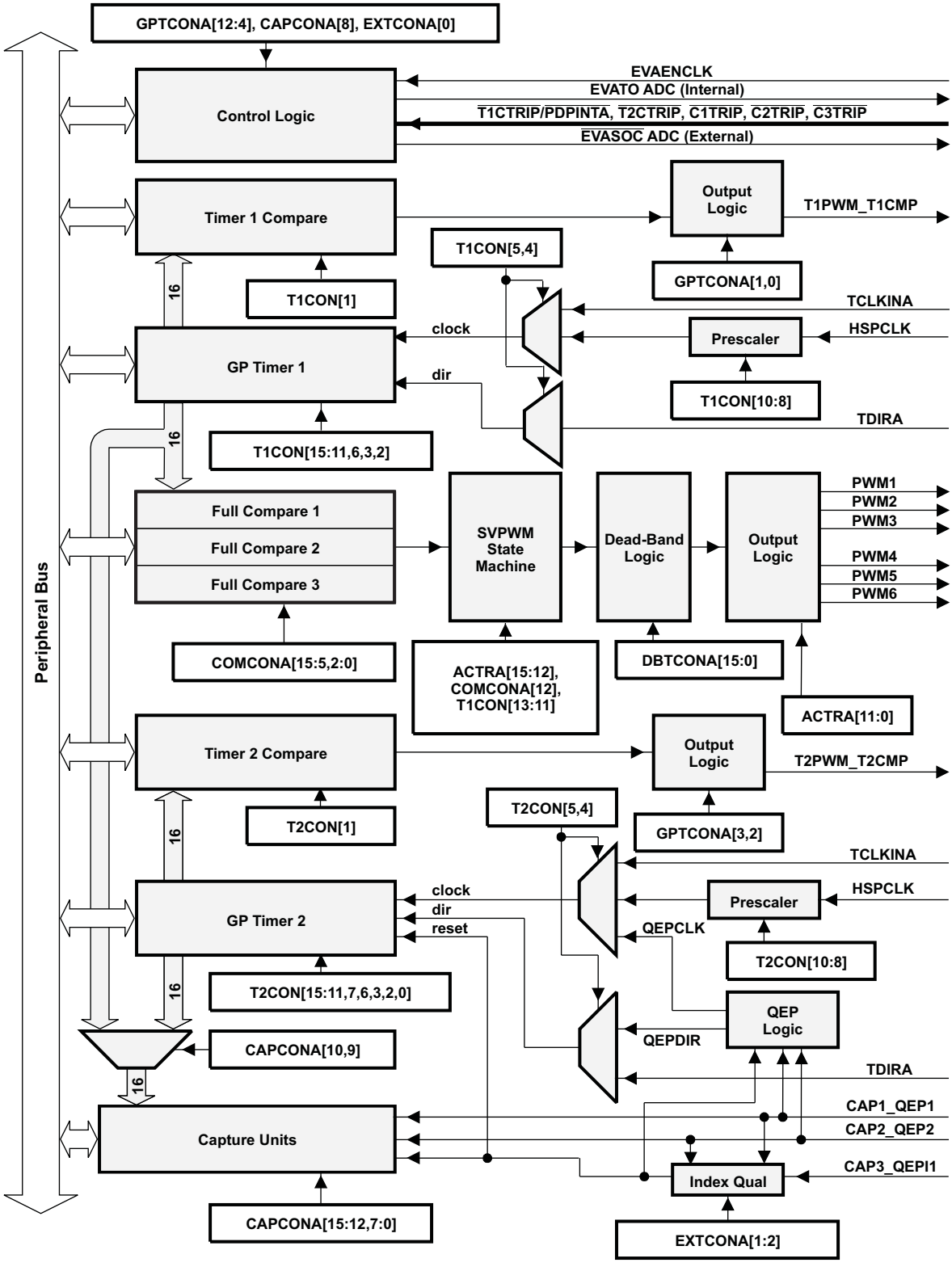
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Table 6-5. EVA Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPTCONA	0x00 7400	1	GP Timer Control Register A
T1CNT	0x00 7401	1	GP Timer 1 Counter Register
T1CMPR	0x00 7402	1	GP Timer 1 Compare Register
T1PR	0x00 7403	1	GP Timer 1 Period Register
T1CON	0x00 7404	1	GP Timer 1 Control Register
T2CNT	0x00 7405	1	GP Timer 2 Counter Register
T2CMPR	0x00 7406	1	GP Timer 2 Compare Register
T2PR	0x00 7407	1	GP Timer 2 Period Register
T2CON	0x00 7408	1	GP Timer 2 Control Register
EXTCONA(2)	0x00 7409	1	GP Extension Control Register A
COMCONA	0x00 7411	1	Compare Control Register A
ACTRA	0x00 7413	1	Compare Action Control Register A
DBTCONA	0x00 7415	1	Dead-Band Timer Control Register A
CMPR1	0x00 7417	1	Compare Register 1
CMPR2	0x00 7418	1	Compare Register 2
CMPR3	0x00 7419	1	Compare Register 3
CAPCONA	0x00 7420	1	Capture Control Register A
CAPFIFOA	0x00 7422	1	Capture FIFO Status Register A
CAP1FIFO	0x00 7423	1	Two-Level-Deep Capture FIFO Stack 1
CAP2FIFO	0x00 7424	1	Two-Level-Deep Capture FIFO Stack 2
CAP3FIFO	0x00 7425	1	Two-Level-Deep Capture FIFO Stack 3
CAP1FBOT	0x00 7427	1	Bottom Register of Capture FIFO Stack 1
CAP2FBOT	0x00 7428	1	Bottom Register of Capture FIFO Stack 2
CAP3FBOT	0x00 7429	1	Bottom Register of Capture FIFO Stack 3
EVAIMRA	0x00 742C	1	Interrupt Mask Register A
EVAIMRB	0x00 742D	1	Interrupt Mask Register B
EVAIMRC	0x00 742E	1	Interrupt Mask Register C
EVAIFRA	0x00 742F	1	Interrupt Flag Register A
EVAIFRB	0x00 7430	1	Interrupt Flag Register B
EVAIFRC	0x00 7431	1	Interrupt Flag Register C

(1) The EV-B register set is identical except the address range is from 0x00 7500 to 0x00 753F. The above registers are mapped to Zone 2. This space allows only 16-bit accesses. 32-bit accesses produce undefined results.
(2) New register compared to 24x/240x

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A. The EVB module is similar to the EVA module.

Figure 6-3. Event Manager A Functional Block Diagram

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6.2.2.1 General-Purpose (GP) Timers

There are two GP timers. The GP timer x (x = 1 or 2 for EVA; x = 3 or 4 for EVB) includes:

- A 16-bit timer, up-/down-counter, TxCNT, for reads or writes
- A 16-bit timer-compare register, TxCMPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-period register, TxPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-control register, TxCON, for reads or writes
- Selectable internal or external input clocks
- A programmable prescaler for internal or external clock inputs
- Control and interrupt logic, for four maskable interrupts: *underflow*, *overflow*, *timer compare*, and *period interrupts*
- A selectable direction input pin (TDIRx) (to count up or down when directional up-/down-count mode is selected)

The GP timers can be operated independently or synchronized with each other. The compare register associated with each GP timer can be used for compare function and PWM-waveform generation. There are three continuous modes of operations for each GP timer in up- or up/down-counting operations. Internal or external input clocks with programmable prescaler are used for each GP timer. GP timers also provide the time base for the other event-manager submodules: GP timer 1 for all the compares and PWM circuits, GP timer 2/1 for the capture units and the quadrature-pulse counting operations. Double-buffering of the period and compare registers allows programmable change of the timer (PWM) period and the compare/PWM pulse width as needed.

6.2.2.2 Full-Compare Units

There are three full-compare units on each event manager. These compare units use GP timer1 as the time base and generate six outputs for compare and PWM-waveform generation using programmable deadband circuit. The state of each of the six outputs is configured independently. The compare registers of the compare units are double-buffered, allowing programmable change of the compare/PWM pulse widths as needed.

6.2.2.3 Programmable Deadband Generator

Deadband generation can be enabled/disabled for each compare unit output individually. The deadband-generator circuit produces two outputs (with or without deadband zone) for each compare unit output signal. The output states of the deadband generator are configurable and changeable as needed by way of the double-buffered ACTRx register.

6.2.2.4 PWM Waveform Generation

Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) by the three full-compare units with *programmable deadbands*, and two independent PWMs by the GP-timer compares.

6.2.2.5 Double Update PWM Mode

The F281x Event Manager supports “Double Update PWM Mode.” This mode refers to a PWM operation mode in which the position of the leading edge and the position of the trailing edge of a PWM pulse are independently modifiable in each PWM period. To support this mode, the compare register that determines the position of the edges of a PWM pulse must allow (buffered) compare value update once at the beginning of a PWM period and another time in the middle of a PWM period. The compare registers in F281x Event Managers are all buffered and support three compare value reload/update (value in buffer becoming active) modes. These modes have earlier been documented as compare value reload conditions. The reload condition that supports double update PWM mode is reloaded on Underflow (beginning of PWM period) OR Period (middle of PWM period). Double update PWM mode can be achieved by using this condition for compare value reload.

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6.2.2.6 PWM Characteristics

Characteristics of the PWMs are as follows:

- 16-bit registers
- Wide range of programmable deadband for the PWM output pairs
- Change of the PWM carrier frequency for PWM frequency wobbling as needed
- Change of the PWM pulse widths within and after each PWM period as needed
- External-maskable power and drive-protection interrupts
- Pulse-pattern-generator circuit, for programmable generation of asymmetric, symmetric, and four-space vector PWM waveforms
- Minimized CPU overhead using auto-reload of the compare and period registers
- The PWM pins are driven to a high-impedance state when the $\overline{\text{PDPINTx}}$ pin is driven low and **after** $\overline{\text{PDPINTx}}$ signal qualification. The $\overline{\text{PDPINTx}}$ pin (after qualification) is reflected in bit 8 of the COMCONx register.
  - $\overline{\text{PDPINTA}}$ pin status is reflected in bit 8 of COMCONA register.
  - $\overline{\text{PDPINTB}}$ pin status is reflected in bit 8 of COMCONB register.
- EXTCON register bits provide options to individually trip control for each PWM pair of signals

6.2.2.7 Capture Unit

The capture unit provides a logging function for different events or transitions. The values of the selected GP timer counter is captured and stored in the two-level-deep FIFO stacks when selected transitions are detected on capture input pins, CAPx (x = 1, 2, or 3 for EVA; and x = 4, 5, or 6 for EVB). The capture unit consists of three capture circuits.

Capture units include the following features:

- One 16-bit capture control register, CAPCONx (R/W)
- One 16-bit capture FIFO status register, CAPFIFOx
- Selection of GP timer 1/2 (for EVA) or 3/4 (for EVB) as the time base
- Three 16-bit 2-level-deep FIFO stacks, one for each capture unit
- Three capture input pins (CAP1/2/3 for EVA, CAP4/5/6 for EVB)—one input pin per capture unit. [All inputs are synchronized with the device (CPU) clock. In order for a transition to be captured, the input must hold at its current level to meet the input qualification circuitry requirements. The input pins CAP1/2 and CAP4/5 can also be used as QEP inputs to the QEP circuit.]
- User-specified transition (rising edge, falling edge, or both edges) detection
- Three maskable interrupt flags, one for each capture unit
- The capture pins can also be used as general-purpose interrupt pins, if they are not used for the capture function.

6.2.2.8 Quadrature-Encoder Pulse (QEP) Circuit

Two capture inputs (CAP1 and CAP2 for EVA; CAP4 and CAP5 for EVB) can be used to interface the on-chip QEP circuit with a quadrature encoder pulse. Full synchronization of these inputs is performed on-chip. Direction or leading-quadrature pulse sequence is detected, and GP timer 2/4 is incremented or decremented by the rising and falling edges of the two input signals (four times the frequency of either input pulse).

With EXTCONA register bits, the EVA QEP circuit can use CAP3 as a capture index pin as well. Similarly, with EXTCONB register bits, the EVB QEP circuit can use CAP6 as a capture index pin.

6.2.2.9 External ADC Start-of-Conversion

EVA/EVB start-of-conversion (SOC) can be sent to an external pin ($\overline{\text{EVASOC}}$/$\overline{\text{EVBSOC}}$) for external ADC interface. $\overline{\text{EVASOC}}$ and $\overline{\text{EVBSOC}}$ are MUXed with $\overline{\text{T2CTRIP}}$ and $\overline{\text{T4CTRIP}}$, respectively.

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6.2.3 Enhanced Analog-to-Digital Converter (ADC) Module

A simplified functional block diagram of the ADC module is shown in Figure 6-4. The ADC module consists of a 12-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 12-bit ADC core with built-in S/H
- Analog input: 0.0 V to 3.0 V (voltages above 3.0 V produce full-scale conversion results)
- Fast conversion rate: 80 ns at 25-MHz ADC clock, 12.5 MSPS
- 16-channel, MUXed inputs
- Autosequencing capability provides up to 16 “autoconversions” in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (that is, two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 0 \quad \text{, when ADCIN} \leq \text{ADCLO}$$

$$\text{Digital Value} = \text{floor}\left(4096 \times \frac{\text{ADCIN} - \text{ADCLO}}{3}\right) \quad \text{, when ADCLO} < \text{ADCIN} < 3\ \text{V}$$

$$\text{Digital Value} = 4095 \quad \text{, when ADCIN} \geq 3\ \text{V}$$

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  - S/W – software immediate start
  - EVA – Event manager A (multiple event sources within EVA)
  - EVB – Event manager B (multiple event sources within EVB)
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS
- Sequencer can operate in “start/stop” mode, allowing multiple “time-sequenced triggers” to synchronize conversions
- EVA and EVB triggers can operate independently in dual-sequencer mode
- Sample-and-hold (S/H) acquisition time window has separate prescale control

The ADC module in the F281x has been enhanced to provide flexible interface to event managers A and B. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of 80 ns at 25-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules to service event managers A and B. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 6-4 shows the block diagram of the F281x ADC module.

The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

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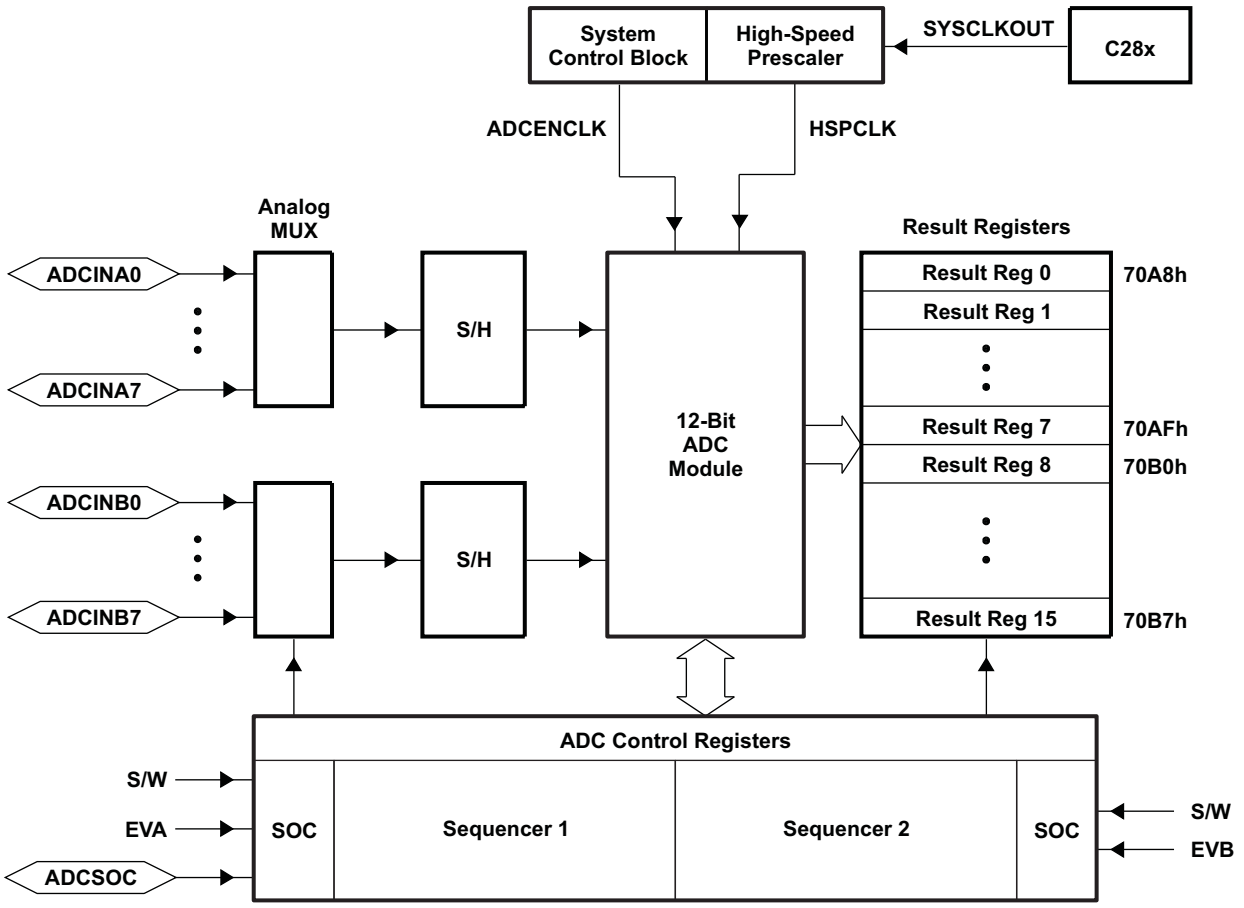


Figure 6-4. Block Diagram of the F281x ADC Module

To obtain the specified accuracy of the ADC, proper board layout is critical. To the best extent possible, traces leading to the ADCIN pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (V_{DDA1}/V_{DDA2}, AVDDREFBG) from the digital supply. For better accuracy and ESD protection, unused ADC inputs should be connected to analog ground.

Notes:

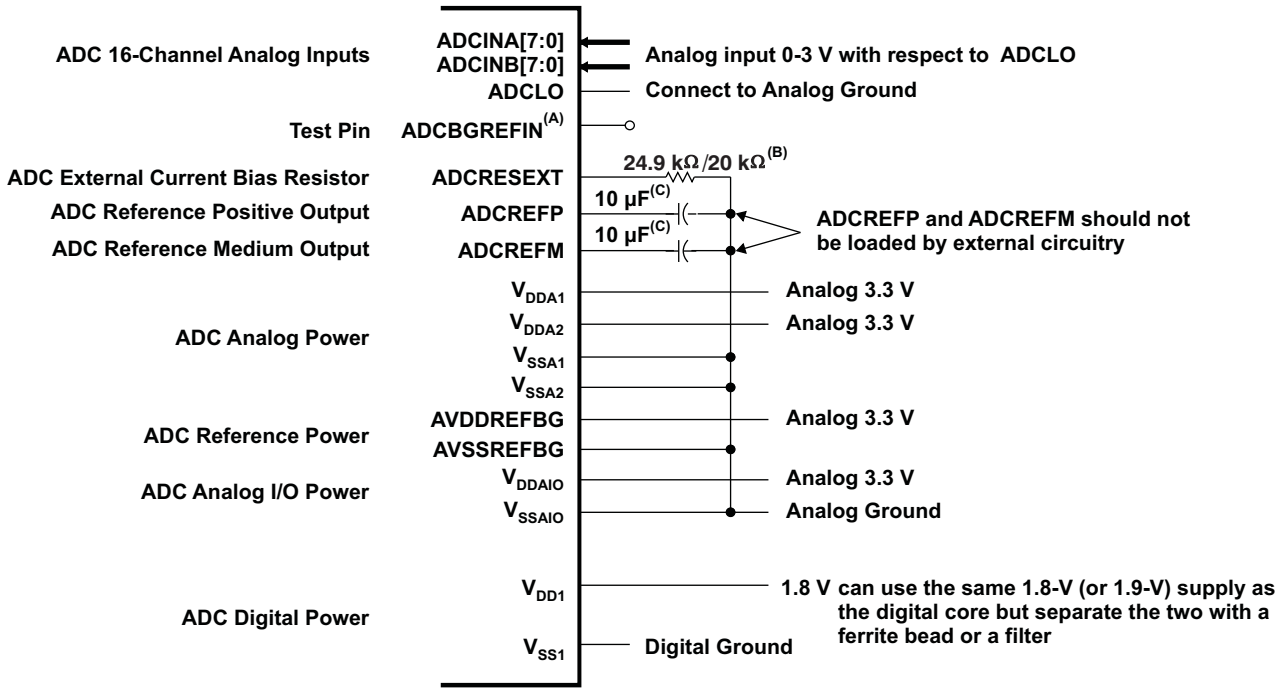
1. The ADC registers are accessed at the SYSCLKOUT rate. The internal timing of the ADC module is controlled by the high-speed peripheral clock (HSPCLK).
2. The behavior of the ADC module based on the state of the ADCENCLK and HALT signals is as follows:

   ADCENCLK: On reset, this signal will be low. While reset is active-low ($\overline{XRS}$) the clock to the register will still function. This is necessary to make sure all registers and modes go into their default reset state. The analog module will, however, be in a low-power inactive state. As soon as reset goes high, then the clock to the registers will be disabled. When the user sets the ADCENCLK signal high, then the clocks to the registers will be enabled and the analog module will be enabled. There will be a certain time delay (ms range) before the ADC is stable and can be used.

   HALT: This signal only affects the analog module. It does not affect the registers. If low, the ADC module is powered. If high, the ADC module goes into low-power mode. The HALT mode will stop the clock to the CPU, which will stop the HSPCLK. Therefore the ADC register logic will be turned off indirectly.

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Figure 6-5 shows the ADC pin-biasing for internal reference and Figure 6-6 shows the ADC pin-biasing for external reference.

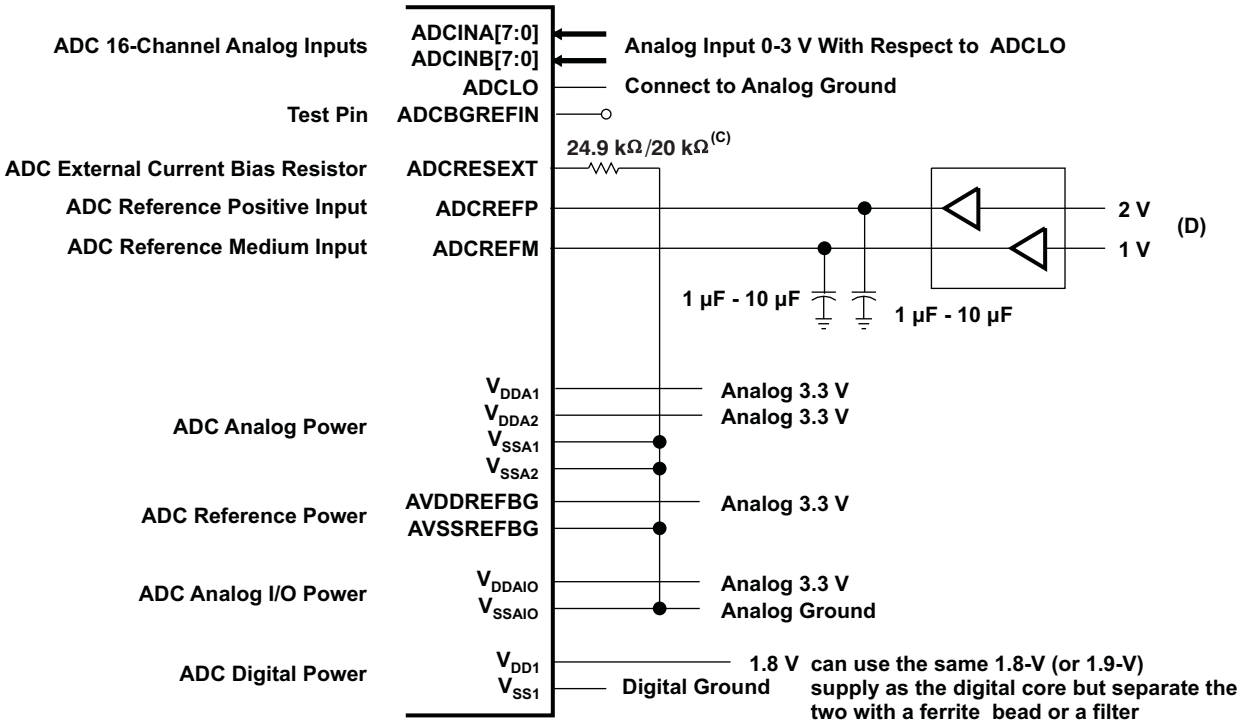


A. Provide access to this pin in PCB layouts. Intended for test purposes only.
B. Use 24.9 kΩ for ADC clock range 1–18.75 MHz; use 20 kΩ for ADC clock range 18.75–25 MHz.
C. TAIYO YUDEN EMK325F106ZH, EMK325BJ106MD, or equivalent ceramic capacitor
D. External decoupling capacitors are recommended on all power pins.
E. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 6-5. ADC Pin Connections With Internal Reference

NOTE

The temperature rating of any recommended component must match the rating of the end product.



A. External decoupling capacitors are recommended on all power pins.

B. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

C. Use 24.9 kΩ for ADC clock range 1–18.75 MHz; use 20 kΩ for ADC clock range 18.75–25 MHz.

D. It is recommended that buffered external references be provided with a voltage difference of (ADCREFP – ADCREFM) = 1 V ± 0.1% or better.
External reference is enabled using bit 8 in the ADCTRL3 Register at ADC power up. In this mode, the accuracy of external reference is critical for overall gain. The voltage ADCREFP – ADCREFM will determine the overall accuracy. Do not enable internal references when external references are connected to ADCREFP and ADCREFM. See the *TMS320x281x DSP Analog-to-Digital Converter (ADC) Reference Guide* for more information.

Figure 6-6. ADC Pin Connections With External Reference

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The ADC operation is configured, controlled, and monitored by the registers listed in Table 6-6.

Table 6-6. ADC Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
ADCTRL1	0x00 7100	1	ADC Control Register 1
ADCTRL2	0x00 7101	1	ADC Control Register 2
ADCMAXCONV	0x00 7102	1	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	0x00 7103	1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	0x00 7104	1	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	0x00 7105	1	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	0x00 7106	1	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	0x00 7107	1	ADC Auto-Sequence Status Register
ADCRESULT0	0x00 7108	1	ADC Conversion Result Buffer Register 0
ADCRESULT1	0x00 7109	1	ADC Conversion Result Buffer Register 1
ADCRESULT2	0x00 710A	1	ADC Conversion Result Buffer Register 2
ADCRESULT3	0x00 710B	1	ADC Conversion Result Buffer Register 3
ADCRESULT4	0x00 710C	1	ADC Conversion Result Buffer Register 4
ADCRESULT5	0x00 710D	1	ADC Conversion Result Buffer Register 5
ADCRESULT6	0x00 710E	1	ADC Conversion Result Buffer Register 6
ADCRESULT7	0x00 710F	1	ADC Conversion Result Buffer Register 7
ADCRESULT8	0x00 7110	1	ADC Conversion Result Buffer Register 8
ADCRESULT9	0x00 7111	1	ADC Conversion Result Buffer Register 9
ADCRESULT10	0x00 7112	1	ADC Conversion Result Buffer Register 10
ADCRESULT11	0x00 7113	1	ADC Conversion Result Buffer Register 11
ADCRESULT12	0x00 7114	1	ADC Conversion Result Buffer Register 12
ADCRESULT13	0x00 7115	1	ADC Conversion Result Buffer Register 13
ADCRESULT14	0x00 7116	1	ADC Conversion Result Buffer Register 14
ADCRESULT15	0x00 7117	1	ADC Conversion Result Buffer Register 15
ADCTRL3	0x00 7118	1	ADC Control Register 3
ADCST	0x00 7119	1	ADC Status Register
Reserved	0x00 711C – 0x00 711F	4	

(1) The above registers are Peripheral Frame 2 Registers.

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6.2.4 Enhanced Controller Area Network (eCAN) Module

The CAN module has the following features:

- Fully compliant with ISO 11898-1 (CAN 2.0B)
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A “dummy” acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE: For a SYSCLKOUT of 150 MHz, the smallest bit rate possible is 23.4 kbps.

The 28x CAN has passed the conformance test per ISO/DIS 16845. Contact TI for details.

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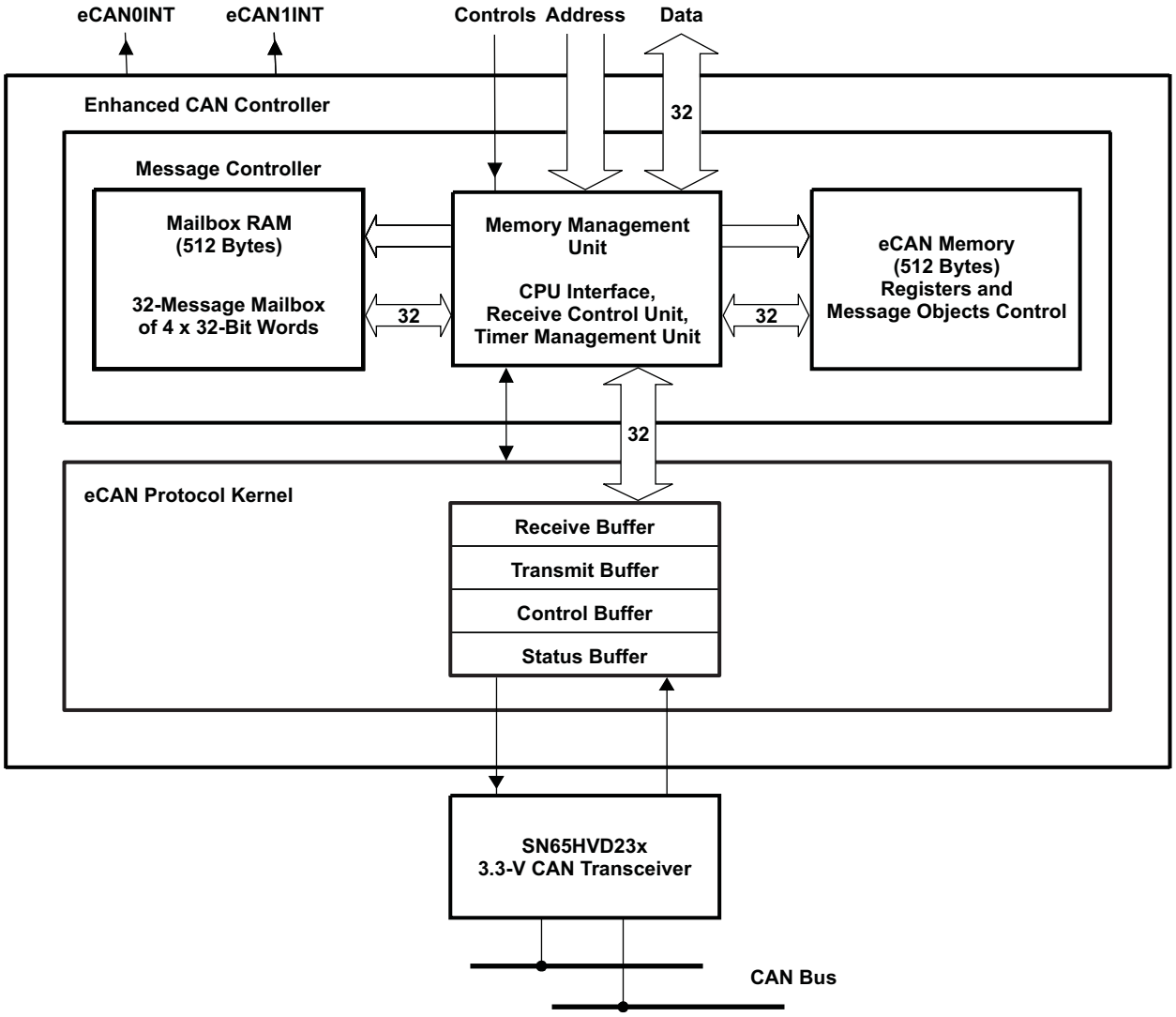


Figure 6-7. eCAN Block Diagram and Interface Circuit

Table 6-7. 3.3-V eCAN Transceivers for the TMS320F281x DSPs

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	–40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	–40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	–40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	–40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	–40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	–	–40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	–40°C to 125°C
ISO1050	3–5.5 V	None	None	None	Built-in Isolation Low Prop Delay Thermal Shutdown Failsafe Operation Dominant Time-out	–55°C to 105°C

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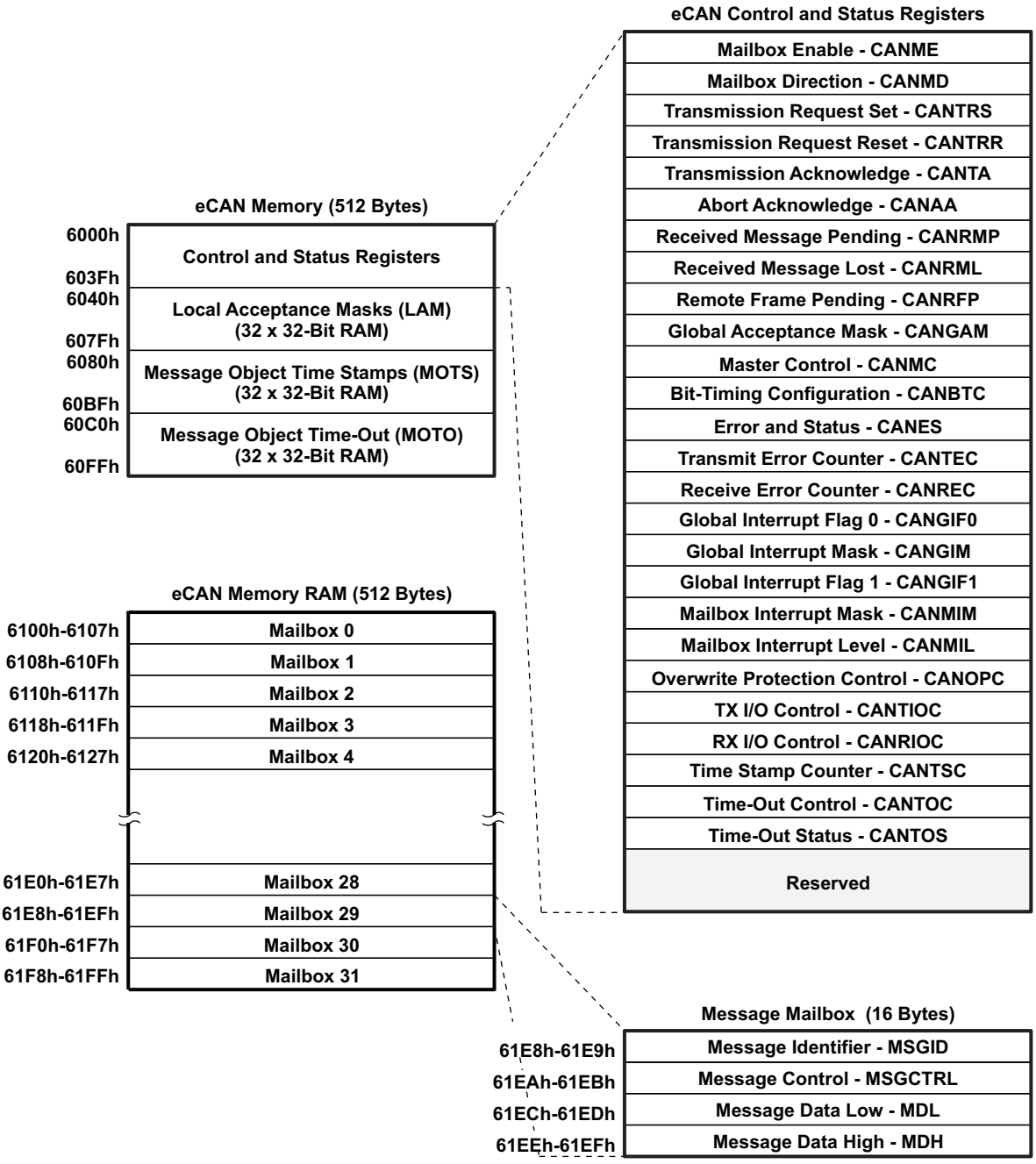


Figure 6-8. eCAN Memory Map

NOTE

If the eCAN module is not used in an application, the RAM available (LAM, MOTS, MOTO, and mailbox RAM) can be used as general-purpose RAM. The CAN module clock should be enabled for this.

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The CAN registers listed in Table 6-8 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 6-8. CAN Registers(1)

NAME	ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x00 6000	1	Mailbox enable
CANMD	0x00 6002	1	Mailbox direction
CANTRS	0x00 6004	1	Transmit request set
CANTRR	0x00 6006	1	Transmit request reset
CANTA	0x00 6008	1	Transmission acknowledge
CANAA	0x00 600A	1	Abort acknowledge
CANRMP	0x00 600C	1	Receive message pending
CANRML	0x00 600E	1	Receive message lost
CANRFP	0x00 6010	1	Remote frame pending
CANGAM	0x00 6012	1	Global acceptance mask
CANMC	0x00 6014	1	Master control
CANBTC	0x00 6016	1	Bit-timing configuration
CANES	0x00 6018	1	Error and status
CANTEC	0x00 601A	1	Transmit error counter
CANREC	0x00 601C	1	Receive error counter
CANGIF0	0x00 601E	1	Global interrupt flag 0
CANGIM	0x00 6020	1	Global interrupt mask
CANGIF1	0x00 6022	1	Global interrupt flag 1
CANMIM	0x00 6024	1	Mailbox interrupt mask
CANMIL	0x00 6026	1	Mailbox interrupt level
CANOPC	0x00 6028	1	Overwrite protection control
CANTIOC	0x00 602A	1	TX I/O control
CANRIOC	0x00 602C	1	RX I/O control
CANTSC	0x00 602E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x00 6030	1	Time-out control (Reserved in SCC mode)
CANTOS	0x00 6032	1	Time-out status (Reserved in SCC mode)

(1) These registers are mapped to Peripheral Frame 1.

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6.2.5 Multichannel Buffered Serial Port (McBSP) Module

The McBSP module has the following features:

- Compatible to McBSP in TMS320C54x/TMS320C55x DSP devices, except the DMA features
- Full-duplex communication
- Double-buffered data registers which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- A wide selection of data sizes including 8-, 12-, 16-, 20-, 24-, or 32-bits
- 8-bit data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Support A-bis mode
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Works with SPI-compatible devices
- Two 16 x 16-level FIFO for Transmit channel
- Two 16 x 16-level FIFO for Receive channel

The following application interfaces can be supported on the McBSP:

- T1/E1 framers
- MVIP switching-compatible and ST-BUS-compliant devices including:
  - MVIP framers
  - H.100 framers
  - SCSA framers
  - IOM-2 compliant devices
  - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS-compliant devices
- McBSP clock rate = CLKG = CLKSRG/(1 + CLKGDIV) , where CLKSRG source could be LSPCLK, CLKX, or CLKR. (1)

(1) Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20-MHz maximum.

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Figure 6-9 shows the block diagram of the McBSP module with FIFO, interfaced to the F281x version of Peripheral Frame 2.

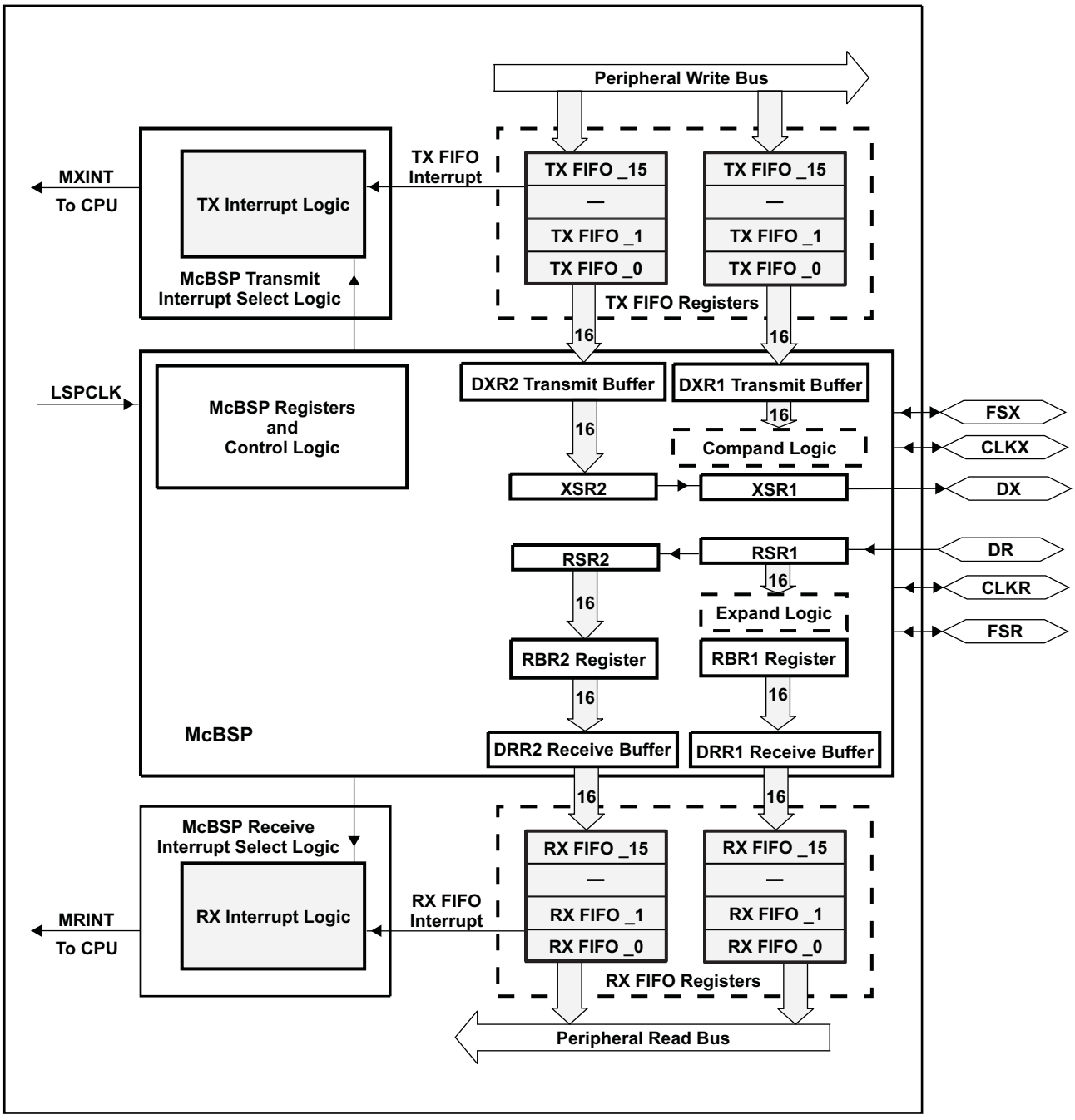


Figure 6-9. McBSP Module With FIFO

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Table 6-9 provides a summary of the McBSP registers.

Table 6-9. McBSP Registers

NAME	ADDRESS 0x00 78xxh	TYPE (R/W)	RESET VALUE (HEX)	DESCRIPTION
DATA REGISTERS, RECEIVE, TRANSMIT(1)				
–	–	–	0x0000	McBSP Receive Buffer Register
–	–	–	0x0000	McBSP Receive Shift Register
–	–	–	0x0000	McBSP Transmit Shift Register
DRR2	00	R	0x0000	McBSP Data Receive Register 2 • Read First if the word size is greater than 16 bits, else ignore DRR2
DRR1	01	R	0x0000	McBSP Data Receive Register 1 • Read Second if the word size is greater than 16 bits, else read DRR1 only
DXR2	02	W	0x0000	McBSP Data Transmit Register 2 • Write First if the word size is greater than 16 bits, else ignore DXR2
DXR1	03	W	0x0000	McBSP Data Transmit Register 1 • Write Second if the word size is greater than 16 bits, else write to DXR1 only
McBSP CONTROL REGISTERS				
SPCR2	04	R/W	0x0000	McBSP Serial Port Control Register 2
SPCR1	05	R/W	0x0000	McBSP Serial Port Control Register 1
RCR2	06	R/W	0x0000	McBSP Receive Control Register 2
RCR1	07	R/W	0x0000	McBSP Receive Control Register 1
XCR2	08	R/W	0x0000	McBSP Transmit Control Register 2
XCR1	09	R/W	0x0000	McBSP Transmit Control Register 1
SRGR2	0A	R/W	0x0000	McBSP Sample Rate Generator Register 2
SRGR1	0B	R/W	0x0000	McBSP Sample Rate Generator Register 1
MULTICHANNEL CONTROL REGISTERS				
MCR2	0C	R/W	0x0000	McBSP Multichannel Register 2
MCR1	0D	R/W	0x0000	McBSP Multichannel Register 1
RCERA	0E	R/W	0x0000	McBSP Receive Channel Enable Register Partition A
RCERB	0F	R/W	0x0000	McBSP Receive Channel Enable Register Partition B
XCERA	10	R/W	0x0000	McBSP Transmit Channel Enable Register Partition A
XCERB	11	R/W	0x0000	McBSP Transmit Channel Enable Register Partition B
PCR	12	R/W	0x0000	McBSP Pin Control Register
RCERC	13	R/W	0x0000	McBSP Receive Channel Enable Register Partition C
RCERD	14	R/W	0x0000	McBSP Receive Channel Enable Register Partition D
XCERC	15	R/W	0x0000	McBSP Transmit Channel Enable Register Partition C
XCERD	16	R/W	0x0000	McBSP Transmit Channel Enable Register Partition D
RCERE	17	R/W	0x0000	McBSP Receive Channel Enable Register Partition E
RCERF	18	R/W	0x0000	McBSP Receive Channel Enable Register Partition F
XCERE	19	R/W	0x0000	McBSP Transmit Channel Enable Register Partition E
XCERF	1A	R/W	0x0000	McBSP Transmit Channel Enable Register Partition F
RCERG	1B	R/W	0x0000	McBSP Receive Channel Enable Register Partition G
RCERH	1C	R/W	0x0000	McBSP Receive Channel Enable Register Partition H
XCERG	1D	R/W	0x0000	McBSP Transmit Channel Enable Register Partition G
XCERH	1E	R/W	0x0000	McBSP Transmit Channel Enable Register Partition H

(1) DRR2/DRR1 and DXR2/DXR1 share the same addresses of receive and transmit FIFO registers in FIFO mode.

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Table 6-9. McBSP Registers (continued)

NAME	ADDRESS 0x00 78xxh	TYPE (R/W)	RESET VALUE (HEX)	DESCRIPTION
FIFO MODE REGISTERS (applicable only in FIFO mode)				
FIFO Data Registers(2)				
DRR2	00	R	0x0000	McBSP Data Receive Register 2 – Top of receive FIFO • Read First FIFO pointers will not advance
DRR1	01	R	0x0000	McBSP Data Receive Register 1 – Top of receive FIFO • Read Second for FIFO pointers to advance
DXR2	02	W	0x0000	McBSP Data Transmit Register 2 – Top of transmit FIFO • Write First FIFO pointers will not advance
DXR1	03	W	0x0000	McBSP Data Transmit Register 1 – Top of transmit FIFO • Write Second for FIFO pointers to advance
FIFO Control Registers				
MFFTX	20	R/W	0xA000	McBSP Transmit FIFO Register
MFFRX	21	R/W	0x201F	McBSP Receive FIFO Register
MFFCT	22	R/W	0x0000	McBSP FIFO Control Register
MFFINT	23	R/W	0x0000	McBSP FIFO Interrupt Register
MFFST	24	R/W	0x0000	McBSP FIFO Status Register

(2) FIFO pointers advancing is based on order of access to DRR2/DRR1 and DXR2/DXR1 registers.

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6.2.6 Serial Communications Interface (SCI) Module

The F281x devices include two serial communications interface (SCI) modules. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

  NOTE: Both pins can be used as GPIO if not used for SCI.
- Baud rate programmable to 64K different rates (1)

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR}+1)*8} \quad \text{when BRR} \neq 0$$

$$= \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- Max bit rate = 75 MHz/16 = 4.688 x 10^6 b/s
- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

  NOTE: All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 16-level transmit/receive FIFO

(1) Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.

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The SCI port operation is configured and controlled by the registers listed in Table 6-10 and Table 6-11.

Table 6-10. SCI-A Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRA	0x00 7050	1	SCI-A Communications Control Register
SCICTL1A	0x00 7051	1	SCI-A Control Register 1
SCIHBAUDA	0x00 7052	1	SCI-A Baud Register, High Bits
SCILBAUDA	0x00 7053	1	SCI-A Baud Register, Low Bits
SCICTL2A	0x00 7054	1	SCI-A Control Register 2
SCIRXSTA	0x00 7055	1	SCI-A Receive Status Register
SCIRXEMUA	0x00 7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x00 7057	1	SCI-A Receive Data Buffer Register
SCITXBUFA	0x00 7059	1	SCI-A Transmit Data Buffer Register
SCIFFTXA(1)	0x00 705A	1	SCI-A FIFO Transmit Register
SCIFFRXA(1)	0x00 705B	1	SCI-A FIFO Receive Register
SCIFFCTA(1)	0x00 705C	1	SCI-A FIFO Control Register
SCIPRIA	0x00 705F	1	SCI-A Priority Control Register

(1) These registers are new registers for the FIFO mode.

Table 6-11. SCI-B Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRB	0x00 7750	1	SCI-B Communications Control Register
SCICTL1B	0x00 7751	1	SCI-B Control Register 1
SCIHBAUDB	0x00 7752	1	SCI-B Baud Register, High Bits
SCILBAUDB	0x00 7753	1	SCI-B Baud Register, Low Bits
SCICTL2B	0x00 7754	1	SCI-B Control Register 2
SCIRXSTB	0x00 7755	1	SCI-B Receive Status Register
SCIRXEMUB	0x00 7756	1	SCI-B Receive Emulation Data Buffer Register
SCIRXBUFB	0x00 7757	1	SCI-B Receive Data Buffer Register
SCITXBUFB	0x00 7759	1	SCI-B Transmit Data Buffer Register
SCIFFTXB(2)	0x00 775A	1	SCI-B FIFO Transmit Register
SCIFFRXB(2)	0x00 775B	1	SCI-B FIFO Receive Register
SCIFFCTB(2)	0x00 775C	1	SCI-B FIFO Control Register
SCIPRIB	0x00 775F	1	SCI-B Priority Control Register

(1) Registers in this table are mapped to peripheral bus 16 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

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Figure 6-10 shows the SCI module block diagram.

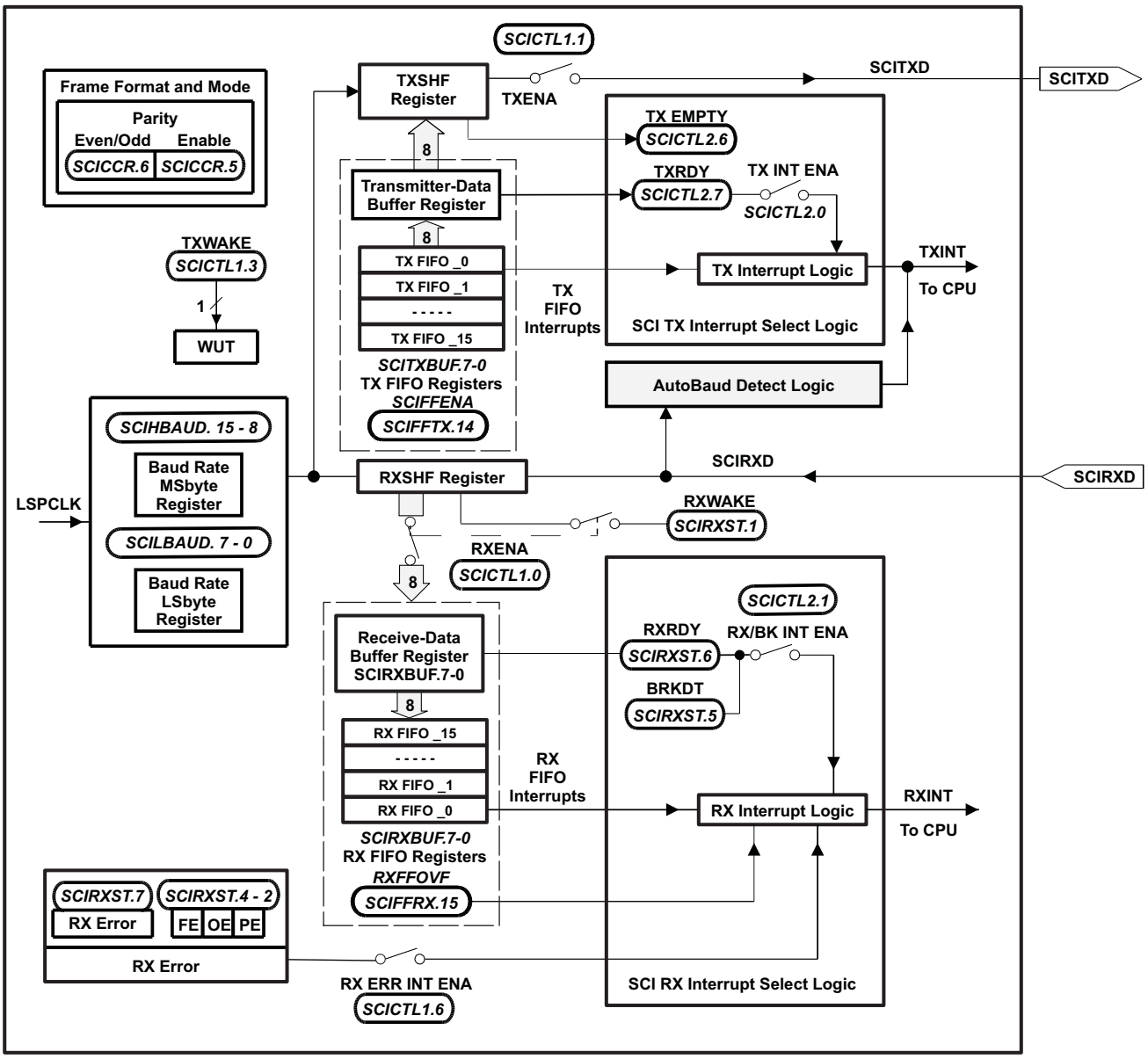


Figure 6-10. Serial Communications Interface (SCI) Module Block Diagram

6.2.7 Serial Peripheral Interface (SPI) Module

The F281x devices include the four-pin serial peripheral interface (SPI) module. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

  NOTE: All four pins can be used as GPIO, if the SPI module is not used.
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \qquad \text{when SPIBRR} \neq 0$$

$$= \frac{\text{LSPCLK}}{4} \qquad \text{when SPIBRR} = 0, 1, 2, 3$$

  Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.
- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.
  NOTE: All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- 16-level transmit/receive FIFO
- Delayed transmit control

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The SPI port operation is configured and controlled by the registers listed in Table 6-12.

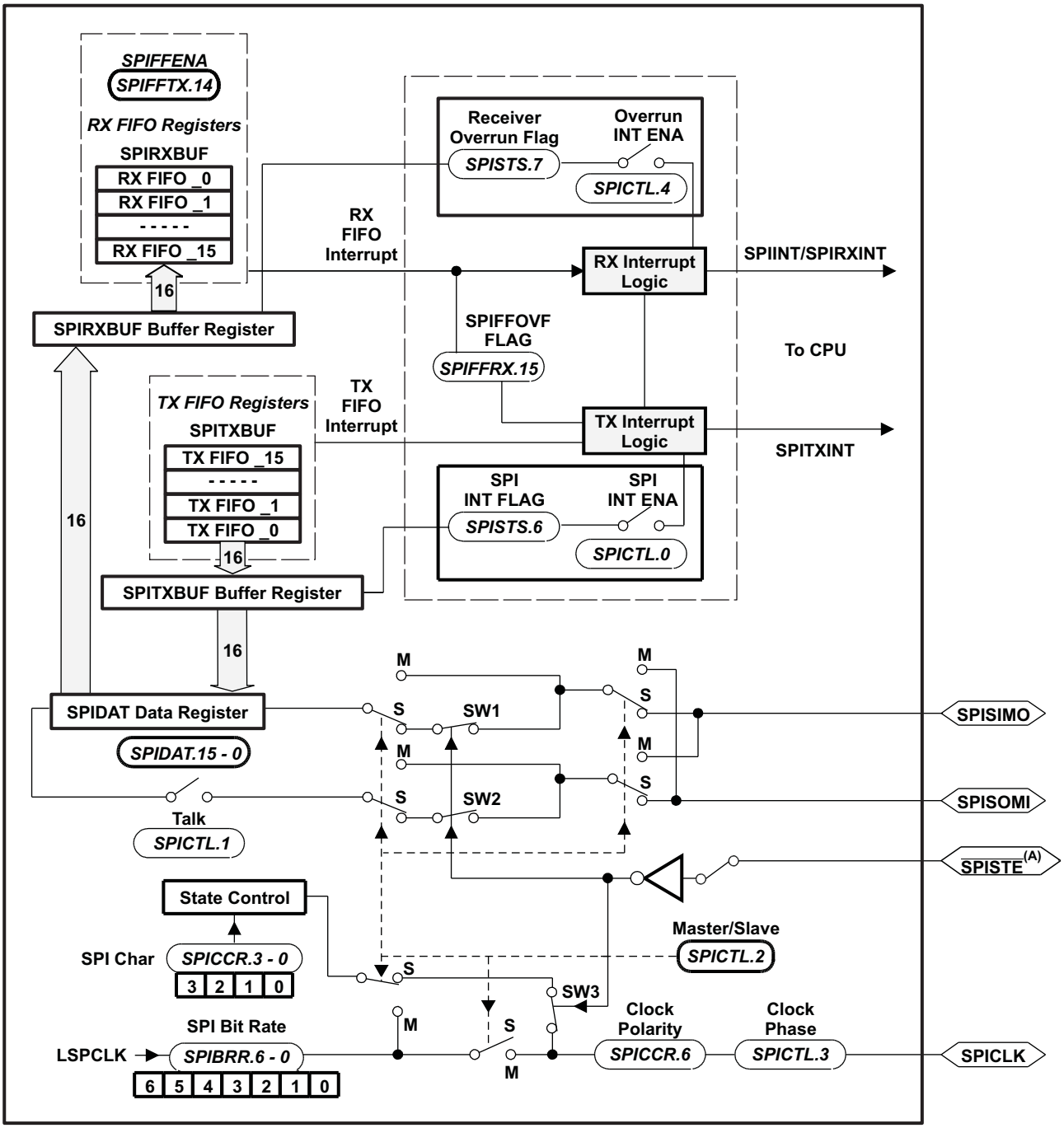
Table 6-12. SPI Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SPICCR	0x00 7040	1	SPI Configuration Control Register
SPICTL	0x00 7041	1	SPI Operation Control Register
SPISTS	0x00 7042	1	SPI Status Register
SPIBRR	0x00 7044	1	SPI Baud Rate Register
SPIRXEMU	0x00 7046	1	SPI Receive Emulation Buffer Register
SPIRXBUF	0x00 7047	1	SPI Serial Input Buffer Register
SPITXBUF	0x00 7048	1	SPI Serial Output Buffer Register
SPIDAT	0x00 7049	1	SPI Serial Data Register
SPIFFTX	0x00 704A	1	SPI FIFO Transmit Register
SPIFFRX	0x00 704B	1	SPI FIFO Receive Register
SPIFFCT	0x00 704C	1	SPI FIFO Control Register
SPIPRI	0x00 704F	1	SPI Priority Control Register

(1) These registers are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

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Figure 6-11 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 6-11. Serial Peripheral Interface Module Block Diagram (Slave Mode)

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6.2.8 GPIO MUX

The GPIO Mux registers are used to select the operation of shared pins on the F281x devices. The pins can be individually selected to operate as “Digital I/O” or connected to “Peripheral I/O” signals (via the GPxMUX registers). If selected for “Digital I/O”mode, registers are provided to configure the pin direction (via the GPxDIR registers) and to qualify the input signal to remove unwanted noise (via the GPxQUAL) registers). Table 6-13 lists the GPIO Mux Registers.

Table 6-13. GPIO Mux Registers(1)(2)(3)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPAMUX	0x00 70C0	1	GPIO A Mux Control Register
GPADIR	0x00 70C1	1	GPIO A Direction Control Register
GPAQUAL	0x00 70C2	1	GPIO A Input Qualification Control Register
Reserved	0x00 70C3	1	
GPBMUX	0x00 70C4	1	GPIO B Mux Control Register
GPBDIR	0x00 70C5	1	GPIO B Direction Control Register
GPBQUAL	0x00 70C6	1	GPIO B Input Qualification Control Register
Reserved	0x00 70C7	1	
Reserved	0x00 70C8	1	
Reserved	0x00 70C9	1	
Reserved	0x00 70CA	1	
Reserved	0x00 70CB	1	
GPDMUX	0x00 70CC	1	GPIO D Mux Control Register
GPDDIR	0x00 70CD	1	GPIO D Direction Control Register
GPDQUAL	0x00 70CE	1	GPIO D Input Qualification Control Register
Reserved	0x00 70CF	1	
GPEMUX	0x00 70D0	1	GPIO E Mux Control Register
GPEDIR	0x00 70D1	1	GPIO E Direction Control Register
GPEQUAL	0x00 70D2	1	GPIO E Input Qualification Control Register
Reserved	0x00 70D3	1	
GPFMUX	0x00 70D4	1	GPIO F Mux Control Register
GPFDIR	0x00 70D5	1	GPIO F Direction Control Register
Reserved	0x00 70D6	1	
Reserved	0x00 70D7	1	
GPGMUX	0x00 70D8	1	GPIO G Mux Control Register
GPGDIR	0x00 70D9	1	GPIO G Direction Control Register
Reserved	0x00 70DA	1	
Reserved	0x00 70DB	1	
Reserved	0x00 70DC – 0x00 70DF	4	

(1) Reserved locations return undefined values and writes are ignored.
(2) Not all inputs support input signal qualification.
(3) These registers are EALLOW protected. This prevents spurious writes from overwriting the contents and corrupting the system.

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If configured for ”Digital I/O” mode, additional registers are provided for setting individual I/O signals (via the GPxSET registers), for clearing individual I/O signals (via the GPxCLEAR registers), for toggling individual I/O signals (via the GPxTOGGLE registers), or for reading/writing to the individual I/O signals (via the GPxDAT registers). Table 6-14 lists the GPIO Data Registers. For more information, see the *TMS320x281x DSP System Control and Interrupts Reference Guide*.

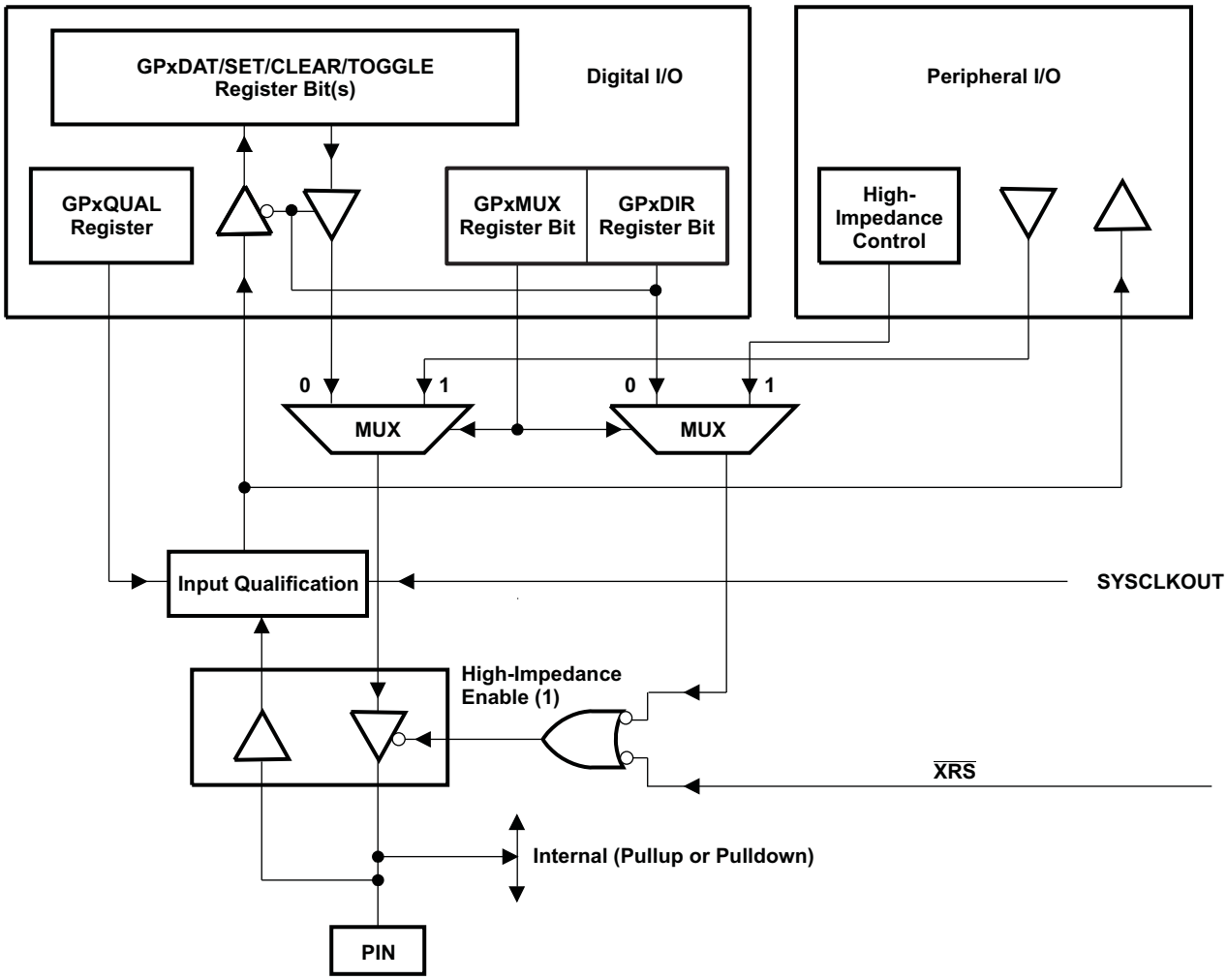
Table 6-14. GPIO Data Registers(1)(2)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPADAT	0x00 70E0	1	GPIO A Data Register
GPASET	0x00 70E1	1	GPIO A Set Register
GPACLEAR	0x00 70E2	1	GPIO A Clear Register
GPATOGGLE	0x00 70E3	1	GPIO A Toggle Register
GPBDAT	0x00 70E4	1	GPIO B Data Register
GPBSET	0x00 70E5	1	GPIO B Set Register
GPBCLEAR	0x00 70E6	1	GPIO B Clear Register
GPBTOGGLE	0x00 70E7	1	GPIO B Toggle Register
Reserved	0x00 70E8	1	
Reserved	0x00 70E9	1	
Reserved	0x00 70EA	1	
Reserved	0x00 70EB	1	
GPDDAT	0x00 70EC	1	GPIO D Data Register
GPDSET	0x00 70ED	1	GPIO D Set Register
GPDCLEAR	0x00 70EE	1	GPIO D Clear Register
GPDTOGGLE	0x00 70EF	1	GPIO D Toggle Register
GPEDAT	0x00 70F0	1	GPIO E Data Register
GPESET	0x00 70F1	1	GPIO E Set Register
GPECLEAR	0x00 70F2	1	GPIO E Clear Register
GPETOGGLE	0x00 70F3	1	GPIO E Toggle Register
GPFDAT	0x00 70F4	1	GPIO F Data Register
GPFSET	0x00 70F5	1	GPIO F Set Register
GPFCLEAR	0x00 70F6	1	GPIO F Clear Register
GPFTOGGLE	0x00 70F7	1	GPIO F Toggle Register
GPGDAT	0x00 70F8	1	GPIO G Data Register
GPGSET	0x00 70F9	1	GPIO G Set Register
GPGCLEAR	0x00 70FA	1	GPIO G Clear Register
GPGTOGGLE	0x00 70FB	1	GPIO G Toggle Register
Reserved	0x00 70FC – 0x00 70FF	4	

(1) Reserved locations will return undefined values and writes will be ignored.
(2) These registers are NOT EALLOW protected. The above registers will typically be accessed regularly by the user.

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Figure 6-12 shows how the various register bits select the various modes of operation for GPIO function.



A. In the GPIO mode, when the GPIO pin is configured for output operation, reading the GPxDAT data register only gives the value written, not the value at the pin. In the peripheral mode, the state of the pin can be read through the GPxDAT register, provided the corresponding direction bit is zero (input mode).

B. Some selected input signals are qualified by the SYSCLKOUT. The GPxQUAL register specifies the qualification sampling period. The sampling window is 6 samples wide and the output is only changed when all samples are the same (all 0's or all 1's). This feature removes unwanted spikes from the input signal.

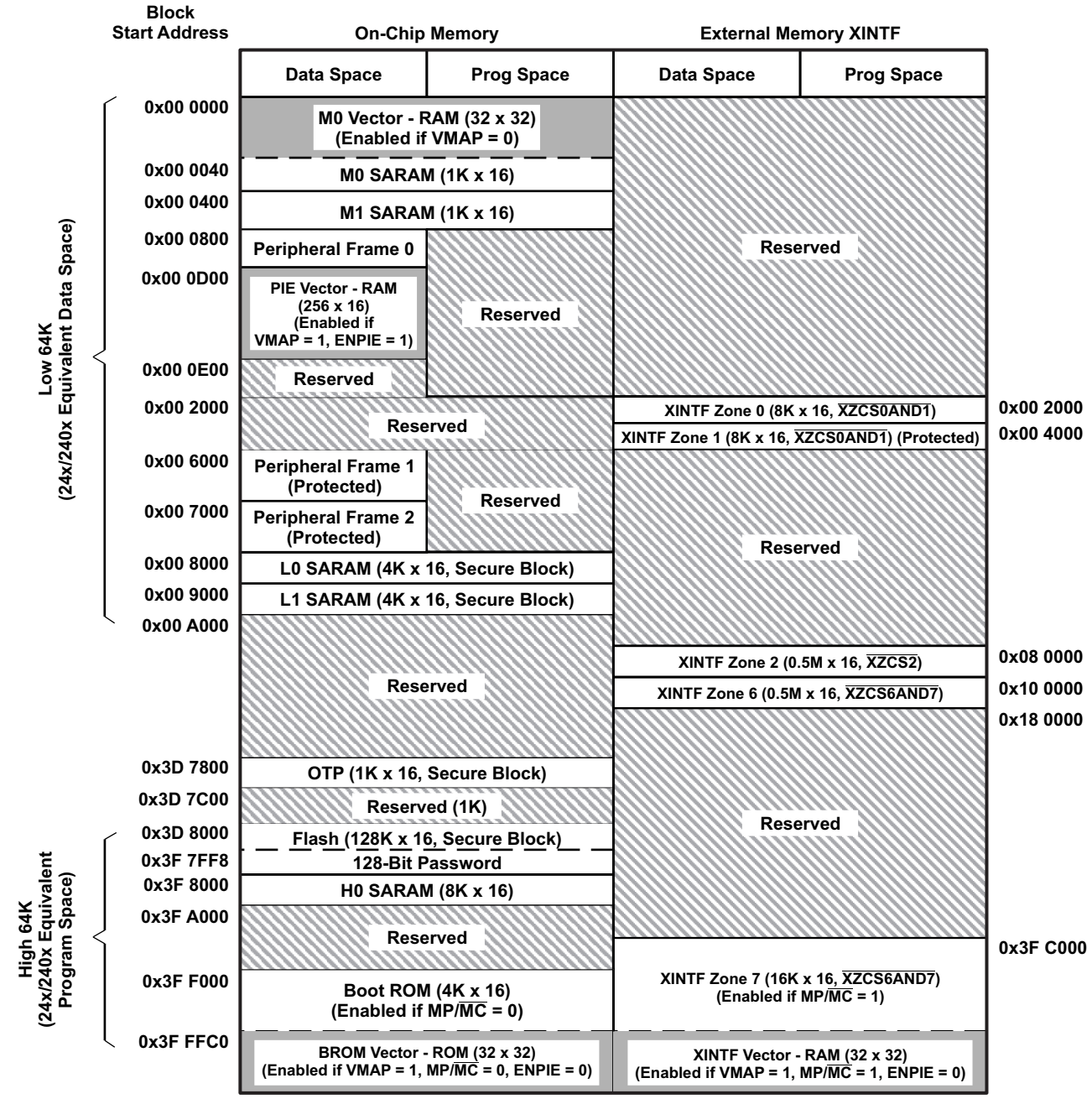
Figure 6-12. GPIO/Peripheral Pin Multiplexing

NOTE

The input function of the GPIO pin and the input path to the peripheral are always enabled. It is the output function of the GPIO pin that is multiplexed with the output path of the primary (peripheral) function. Since the output buffer of a pin connects back to the input buffer, any GPIO signal present at the pin will be propagated to the peripheral module as well. Therefore, when a pin is configured for GPIO operation, the corresponding peripheral functionality (and interrupt-generating capability) must be disabled. Otherwise, interrupts may be inadvertently triggered. This is especially critical when the $\overline{\text{PDPINTA}}$ and $\overline{\text{PDPINTB}}$ pins are used as GPIO pins, since a value of zero for GPDDAT.0 or GPDDAT.5 ($\overline{\text{PDPINTx}}$) will put PWM pins in a high-impedance state. The $\overline{\text{CxTRIP}}$ and $\overline{\text{TxCTRIP}}$ pins will also put the corresponding PWM pins in high impedance, if they are driven low (as GPIO pins) *and* bit EXTCONx.0 = 1.

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6.3 Memory Maps



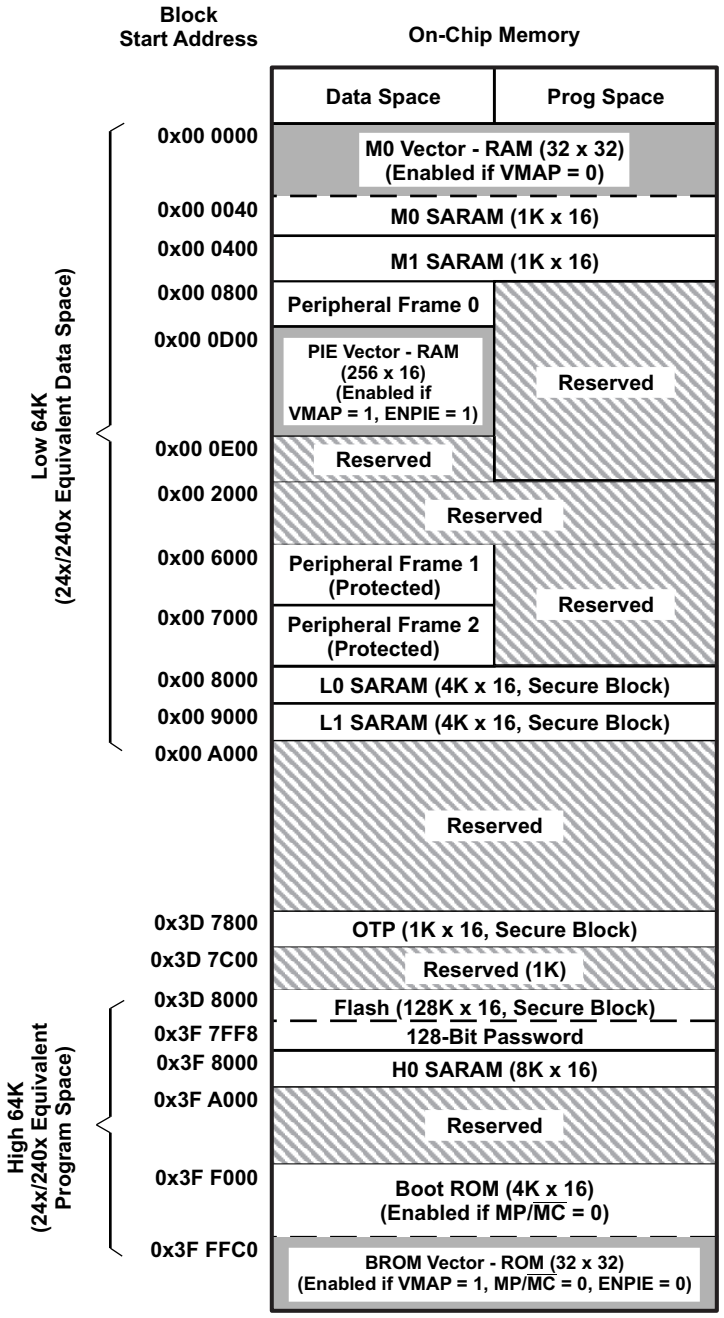
LEGEND:

Only one of these vector maps - M0 vector, PIE vector, BROM vector, XINTF vector - should be enabled at a time.

A. Memory blocks are not to scale.
B. Reserved locations are reserved for future expansion. Application should not access these areas.
C. Boot ROM and Zone 7 memory maps are active either in on-chip or XINTF zone depending on MP/$\overline{MC}$, not in both.
D. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
E. "Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.
F. Certain memory ranges are EALLOW protected against spurious writes after configuration.
G. Zones 0 and 1 and Zones 6 and 7 share the same chip select; hence, these memory blocks have mirrored locations.

Figure 6-13. F2812 Memory Map

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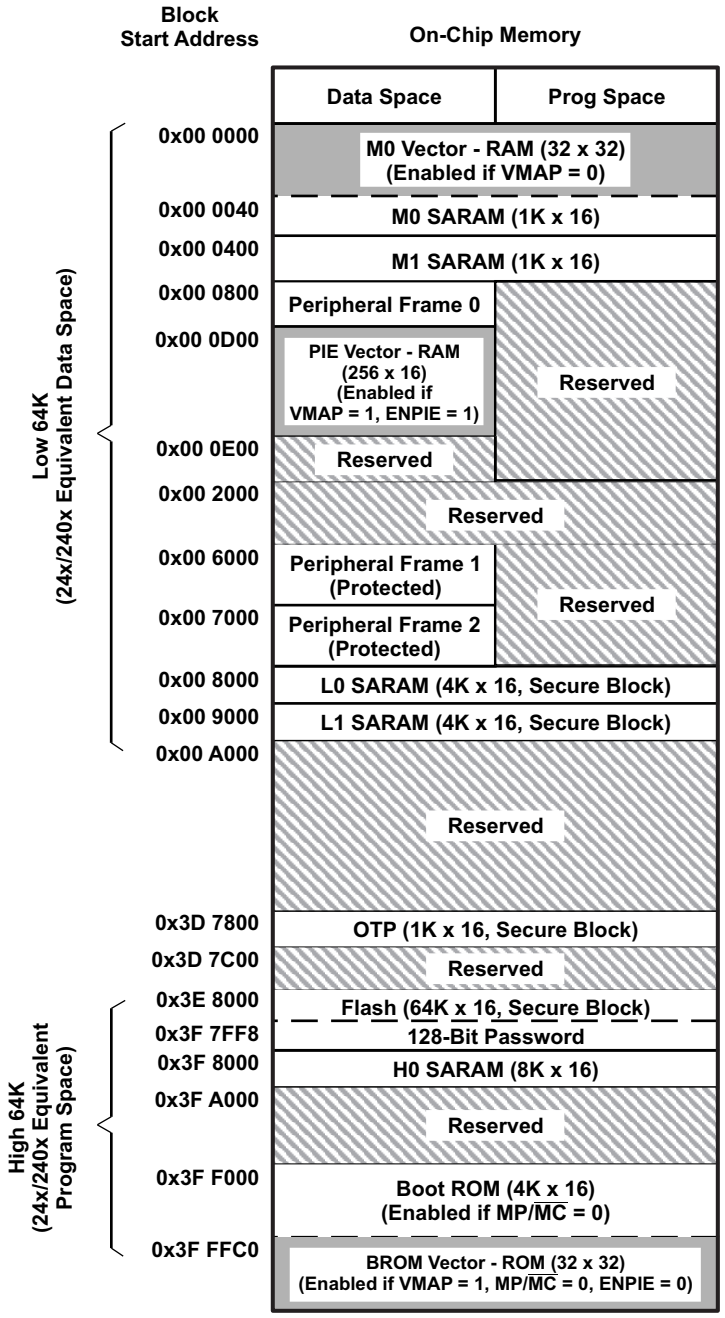


LEGEND:

Only one of these vector maps - M0 vector, PIE vector, BROM vector - should be enabled at a time.

A. Memory blocks are not to scale.
B. Reserved locations are reserved for future expansion. Application should not access these areas.
C. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
D. "Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.
E. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 6-14. F2811 Memory Map



LEGEND:

Only one of these vector maps - M0 vector, PIE vector, BROM vector - should be enabled at a time.

A. Memory blocks are not to scale.
B. Reserved locations are reserved for future expansion. Application should not access these areas.
C. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
D. "Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.
E. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 6-15. F2810 Memory Map

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Table 6-15. Addresses of Flash Sectors in F2812 and F2811

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3D 8000 0x3D 9FFF	Sector J, 8K x 16
0x3D A000 0x3D BFFF	Sector I, 8K x 16
0x3D C000 0x3D FFFF	Sector H, 16K x 16
0x3E 0000 0x3E 3FFF	Sector G, 16K x 16
0x3E 4000 0x3E 7FFF	Sector F, 16K x 16
0x3E 8000 0x3E BFFF	Sector E, 16K x 16
0x3E C000 0x3E FFFF	Sector D, 16K x 16
0x3F 0000 0x3F 3FFF	Sector C, 16K x 16
0x3F 4000 0x3F 5FFF	Sector B, 8K x 16
0x3F 6000	Sector A, 8K x 16
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 6-16. Addresses of Flash Sectors in F2810

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 0x3E BFFF	Sector E, 16K x 16
0x3E C000 0x3E FFFF	Sector D, 16K x 16
0x3F 0000 0x3F 3FFF	Sector C, 16K x 16
0x3F 4000 0x3F 5FFF	Sector B, 8K x 16
0x3F 6000	Sector A, 8K x 16
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

The “Low 64K” of the memory address range maps into the data space of the 240x. The “High 64K” of the memory address range maps into the program space of the 24x/240x. 24x/240x-compatible code will execute only from the “High 64K”memory area. Hence, the top 32K of Flash and H0 SARAM block can be used to run 24x/240x-compatible code (if MP/$\overline{MC}$ mode is low) or, on the F2812, code can be executed from XINTF Zone 7 (if MP/$\overline{MC}$ mode is high).

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The XINTF consists of five independent zones. One zone has its own chip select and the remaining four zones share two chip selects. Each zone can be programmed with its own timing (wait states) and to either sample or ignore external ready signal. This makes interfacing to external peripherals easy and glueless.

NOTE

The chip selects of XINTF Zone 0 and Zone 1 are merged into a single chip select ($\overline{\text{XZCS0AND1}}$); and the chip selects of XINTF Zone 6 and Zone 7 are merged into a single chip select ($\overline{\text{XZCS6AND7}}$). See Section 6.6, External Interface, XINTF (F2812 only), for details.

Peripheral Frame 1, Peripheral Frame 2, and XINTF Zone 1 are grouped together to enable these blocks to be “write/read peripheral block protected”. The “protected” mode ensures that all accesses to these blocks happen as written. Because of the C28x pipeline, a write immediately followed by a read, to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The C28x CPU supports a block protection mode where a region of memory can be protected to make sure that operations occur as written (the penalty is extra cycles that are added to align the operations). This mode is programmable and, by default, it will protect the selected zones.

On the F2812, at reset, XINTF Zone 7 is accessed if the XMP/$\overline{\text{MC}}$ pin is pulled high. This signal selects microprocessor or microcomputer mode of operation. In microprocessor mode, Zone 7 is mapped to high memory such that the vector table is fetched externally. The Boot ROM is disabled in this mode. In microcomputer mode, Zone 7 is disabled such that the vectors are fetched from Boot ROM. This allows the user to either boot from on-chip memory or from off-chip memory. The state of the XMP/$\overline{\text{MC}}$ signal on reset is stored in an MP/$\overline{\text{MC}}$ mode bit in the XINTCNF2 register. The user can change this mode in software and hence control the mapping of Boot ROM and XINTF Zone 7. No other memory blocks are affected by XMP/$\overline{\text{MC}}$.

I/O space is not supported on the F2812 XINTF.

The wait states for the various spaces in the memory map area are listed in Table 6-17.

Table 6-17. Wait States

AREA	WAIT-STATES	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	Fixed
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Fixed
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed
L0 and L1 SARAMs	0-wait	Fixed
OTP	Programmable, 1-wait minimum	Programmed via the Flash registers. 1-wait-state operation is possible at a reduced CPU frequency. See Section 6.1.6, Flash, for more information.
Flash	Programmable, 0-wait minimum	Programmed via the Flash registers. 0-wait-state operation is possible at reduced CPU frequency. The CSM password locations are hardwired for 16 wait states. See Section 6.1.6, Flash, for more information.
H0 SARAM	0-wait	Fixed
Boot-ROM	1-wait	Fixed
XINTF	Programmable, 1-wait minimum	Programmed via the XINTF registers. Cycles can be extended by external memory or peripheral. 0-wait operation is not possible.

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6.4 Register Map

The F281x devices contain three peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 6-18.

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 6-19.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 6-20.

Table 6-18. Peripheral Frame 0 Registers(1)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE(2)
Device Emulation Registers	0x00 0880 – 0x00 09FF	384	EALLOW protected
Reserved	0x00 0A00 – 0x00 0A7F	128	
FLASH Registers(3)	0x00 0A80 – 0x00 0ADF	96	EALLOW protected CSM Protected
Code Security Module Registers	0x00 0AE0 – 0x00 0AEF	16	EALLOW protected
Reserved	0x00 0AF0 – 0x00 0B1F	48	
XINTF Registers	0x00 0B20 – 0x00 0B3F	32	Not EALLOW protected
Reserved	0x00 0B40 – 0x00 0BFF	192	
CPU-TIMER0/1/2 Registers	0x00 0C00 – 0x00 0C3F	64	Not EALLOW protected
Reserved	0x00 0C40 – 0x00 0CDF	160	
PIE Registers	0x00 0CE0 – 0x00 0CFF	32	Not EALLOW protected
PIE Vector Table	0x00 0D00 – 0x00 0DFF	256	EALLOW protected
Reserved	0x00 0E00 – 0x00 0FFF	512	

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the user executes the EALLOW instruction. The EDIS instruction disables writes. This prevents stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

Table 6-19. Peripheral Frame 1 Registers(1)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
eCAN Registers	0x00 6000 – 0x00 60FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCAN Mailbox RAM	0x00 6100 – 0x00 61FF	256 (128 x 32)	Not EALLOW-protected
Reserved	0x00 6200 – 0x00 6FFF	3584	

(1) The eCAN control registers only support 32-bit read/write operations. All 32-bit accesses are aligned to even address boundaries.

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Table 6-20. Peripheral Frame 2 Registers(1)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
Reserved	0x00 7000 – 0x00 700F	16	
System Control Registers	0x00 7010 – 0x00 702F	32	EALLOW Protected
Reserved	0x00 7030 – 0x00 703F	16	
SPI-A Registers	0x00 7040 – 0x00 704F	16	Not EALLOW Protected
SCI-A Registers	0x00 7050 – 0x00 705F	16	Not EALLOW Protected
Reserved	0x00 7060 – 0x00 706F	16	
External Interrupt Registers	0x00 7070 – 0x00 707F	16	Not EALLOW Protected
Reserved	0x00 7080 – 0x00 70BF	64	
GPIO Mux Registers	0x00 70C0 – 0x00 70DF	32	EALLOW Protected
GPIO Data Registers	0x00 70E0 – 0x00 70FF	32	Not EALLOW Protected
ADC Registers	0x00 7100 – 0x00 711F	32	Not EALLOW Protected
Reserved	0x00 7120 – 0x00 73FF	736	
EV-A Registers	0x00 7400 – 0x00 743F	64	Not EALLOW Protected
Reserved	0x00 7440 – 0x00 74FF	192	
EV-B Registers	0x00 7500 – 0x00 753F	64	Not EALLOW Protected
Reserved	0x00 7540 – 0x00 774F	528	
SCI-B Registers	0x00 7750 – 0x00 775F	16	Not EALLOW Protected
Reserved	0x00 7760 – 0x00 77FF	160	
McBSP Registers	0x00 7800 – 0x00 783F	64	Not EALLOW Protected
Reserved	0x00 7840 – 0x00 7FFF	1984	

(1) Peripheral Frame 2 only allows 16-bit accesses. All 32-bit accesses are ignored (invalid data may be returned or written).

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6.5 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 6-21.

Table 6-21. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION	
DEVICECNF	0x00 0880 – 0x00 0881	2	Device Configuration Register	
PARTID	0x00 0882	1	Part ID Register	0x0001 or 0x0002 – F281x
REVID	0x00 0883	1	Revision ID Register	0x0001 – Silicon Revision A 0x0002 – Silicon Revision B 0x0003 – Silicon Revisions C, D 0x0004 – Reserved 0x0005 – Silicon Revision E 0x0006 – Silicon Revision F 0x0007 – Silicon Revision G
PROTSTART	0x00 0884	1	Block Protection Start Address Register	
PROTRANGE	0x00 0885	1	Block Protection Range Address Register	
Reserved	0x00 0886 – 0x00 09FF	378		

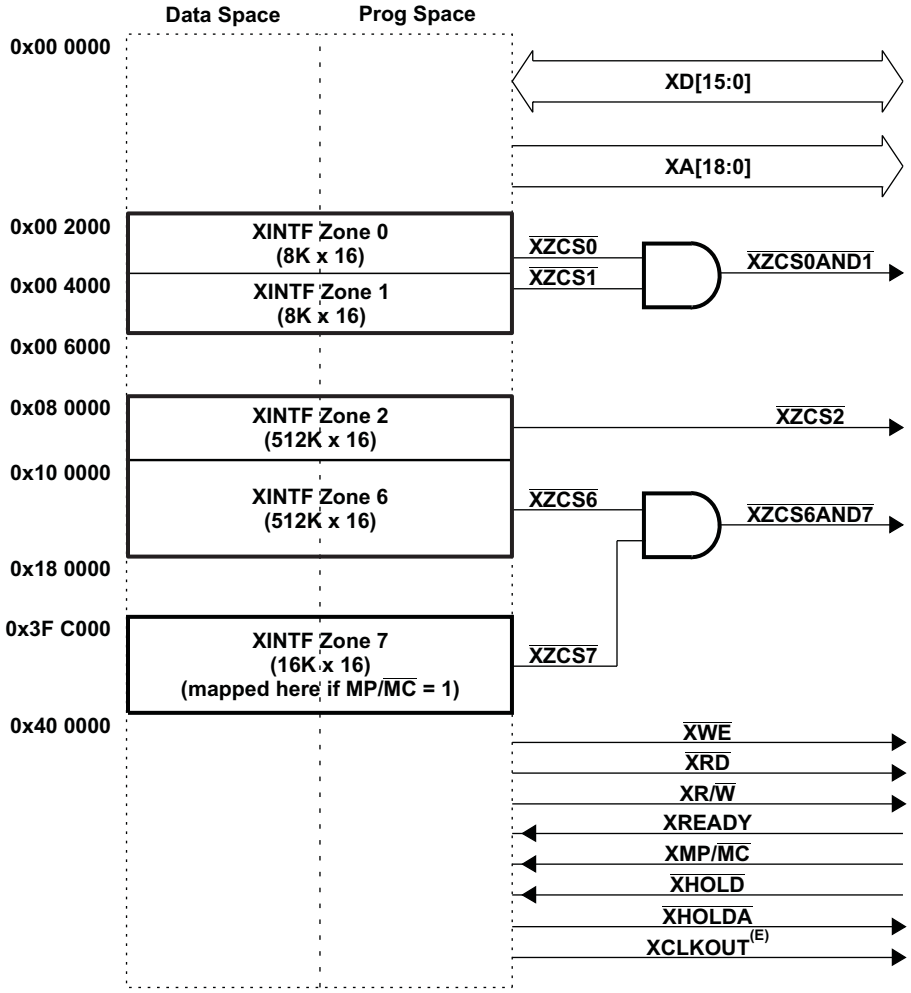
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6.6 External Interface, XINTF (F2812 Only)

This section gives a top-level view of the external interface (XINTF) that is implemented on the F2812 device.

The external interface is a non-multiplexed asynchronous bus, similar to the C240x external interface. The external interface on the F2812 is mapped into five fixed zones shown in Figure 6-16.

Figure 6-16 shows the F2812 XINTF signals.



A. The mapping of XINTF Zone 7 is dependent on the XMP/$\overline{MC}$ device input signal and the MP/$\overline{MC}$ mode bit (bit 8 of XINTCNF2 register). Zones 0, 1, 2, and 6 are always enabled.

B. Each zone can be programmed with different wait states, setup and hold timing, and is supported by zone chip selects ($\overline{XZCS0AND1}$, $\overline{XZCS2}$, $\overline{XZCS6AND7}$), which toggle when an access to a particular zone is performed. These features enable glueless connection to many external memories and peripherals.

C. The chip selects for Zone 0 and Zone 1 are ANDed internally together to form one chip select ($\overline{XZCS0AND1}$). Any external memory that is connected to $\overline{XZCS0AND1}$ is dually mapped to both Zone 0 and Zone 1.

D. The chip selects for Zone 6 and Zone 7 are ANDed internally together to form one chip select ($\overline{XZCS6AND7}$). Any external memory that is connected to $\overline{XZCS6AND7}$ is dually mapped to both Zone 6 and Zone 7. This means that if Zone 7 is disabled (via the MP/$\overline{MC}$ mode), then any external memory is still accessible via Zone 6 address space.

E. XCLKOUT is also pinned out on the F2810 and F2811 devices.

Figure 6-16. External Interface Block Diagram

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The operation and timing of the external interface, can be controlled by the registers listed in Table 6-22.

Table 6-22. XINTF Configuration and Control Register Mappings

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XTIMING0	0x00 0B20	2	XINTF Timing Register, Zone 0 can access as two 16-bit registers or one 32-bit register.
XTIMING1	0x00 0B22	2	XINTF Timing Register, Zone 1 can access as two 16-bit registers or one 32-bit register.
XTIMING2	0x00 0B24	2	XINTF Timing Register, Zone 2 can access as two 16-bit registers or one 32-bit register.
XTIMING6	0x00 0B2C	2	XINTF Timing Register, Zone 6 can access as two 16-bit registers or one 32-bit register.
XTIMING7	0x00 0B2E	2	XINTF Timing Register, Zone 7 can access as two 16-bit registers or one 32-bit register.
XINTCNF2	0x00 0B34	2	XINTF Configuration Register can access as two 16-bit registers or one 32-bit register.
XBANK	0x00 0B38	1	XINTF Bank Control Register
XREVISION	0x00 0B3A	1	XINTF Revision Register

6.6.1 Timing Registers

XINTF signal timing can be tuned to match specific external device requirements such as setup and hold times to strobe signals for contention avoidance and maximizing bus efficiency. The XINTF timing parameters can be configured individually for each zone based on the requirements of the memory or peripheral accessed by that particular zone. This allows the programmer to maximize the efficiency of the bus on a per-zone basis. All XINTF timing values are with respect to XTIMCLK, which is equal to or one-half of the SYSCLKOUT rate, as shown in Figure 5-26.

For detailed information on the XINTF timing and configuration register bit fields, see the *TMS320x281x DSP External Interface (XINTF) Reference Guide*.

6.6.2 XREVISION Register

The XREVISION register contains a unique number to identify the particular version of XINTF used in the product. For the F2812, this register will be configured as described in Table 6-23.

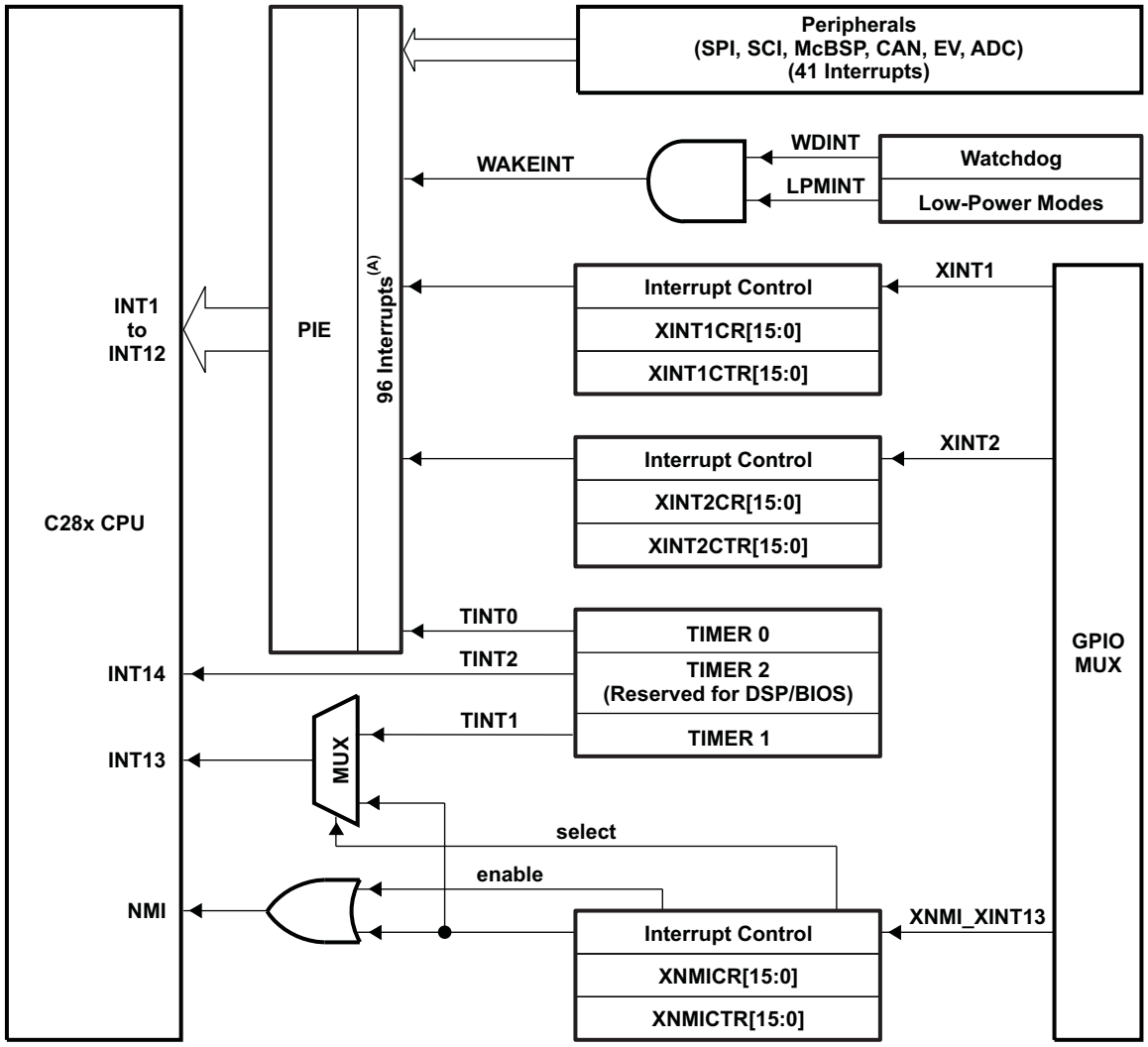
Table 6-23. XREVISION Register Bit Definitions

BIT(S)	NAME	TYPE	RESET	DESCRIPTION
15–0	REVISION	R	0x0004	Current XINTF Revision. For internal use/reference. Test purposes only. Subject to change.

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6.7 Interrupts

Figure 6-17 shows how the various interrupt sources are multiplexed within the F281x devices.



A. Out of a possible 96 interrupts, 45 are currently used by peripherals.

Figure 6-17. Interrupt Sources

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. On the F281x, 45 of these are used by peripherals as shown in Table 6-24.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. TRAP #0 attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, TRAP #0 should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, TRAP #1 through TRAP #12 will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1 and so forth.

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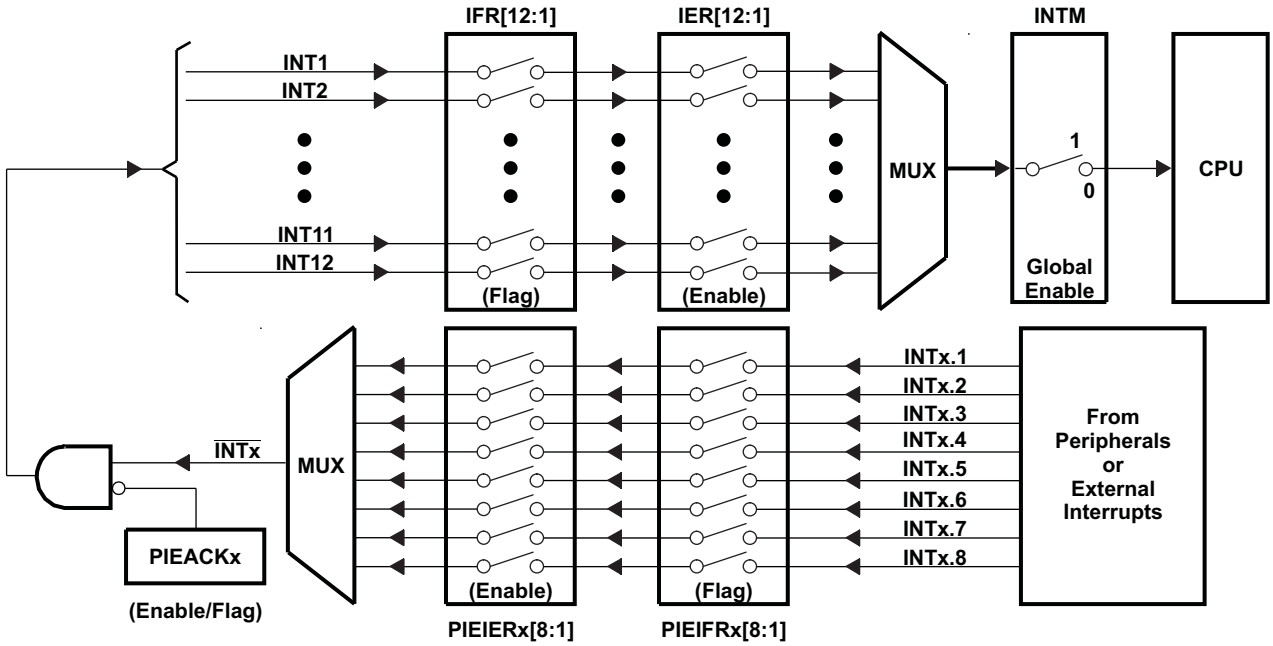


Figure 6-18. Multiplexing of Interrupts Using the PIE Block

Table 6-24. PIE Peripheral Interrupts(1)

CPU INTERRUPTS	PIE INTERRUPTS							
	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1	WAKEINT (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	Reserved	PDPINTB (EV-B)	PDPINTA (EV-A)
INT2	Reserved	T1OFINT (EV-A)	T1UFINT (EV-A)	T1CINT (EV-A)	T1PINT (EV-A)	CMP3INT (EV-A)	CMP2INT (EV-A)	CMP1INT (EV-A)
INT3	Reserved	CAPINT3 (EV-A)	CAPINT2 (EV-A)	CAPINT1 (EV-A)	T2OFINT (EV-A)	T2UFINT (EV-A)	T2CINT (EV-A)	T2PINT (EV-A)
INT4	Reserved	T3OFINT (EV-B)	T3UFINT (EV-B)	T3CINT (EV-B)	T3PINT (EV-B)	CMP6INT (EV-B)	CMP5INT (EV-B)	CMP4INT (EV-B)
INT5	Reserved	CAPINT6 (EV-B)	CAPINT5 (EV-B)	CAPINT4 (EV-B)	T4OFINT (EV-B)	T4UFINT (EV-B)	T4CINT (EV-B)	T4PINT (EV-B)
INT6	Reserved	Reserved	MXINT (McBSP)	MRINT (McBSP)	Reserved	Reserved	SPITXINTA (SPI)	SPIRXINTA (SPI)
INT7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT9	Reserved	Reserved	ECAN1INT (CAN)	ECAN0INT (CAN)	SCITXINTB (SCI-B)	SCIRXINTB (SCI-B)	SCITXINTA (SCI-A)	SCIRXINTA (SCI-A)
INT10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

(1) Out of the 96 possible interrupts, 45 interrupts are currently used. The remaining interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR.
To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
- No peripheral within the group is asserting interrupts.
- No peripheral interrupts are assigned to the group (example PIE group 12).

Table 6-25. PIE Configuration and Control Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
PIECTRL	0x0000 0CE0	1	PIE, Control Register
PIEACK	0x0000 0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0000 0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0000 0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0000 0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0000 0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0000 0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0000 0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0000 0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0000 0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0000 0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0000 0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0000 0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0000 0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0000 0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0000 0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0000 0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0000 0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0000 0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0000 0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0000 0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0000 0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0000 0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0000 0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0000 0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0000 0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0000 0CFA – 0x0000 0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

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6.7.1 External Interrupts

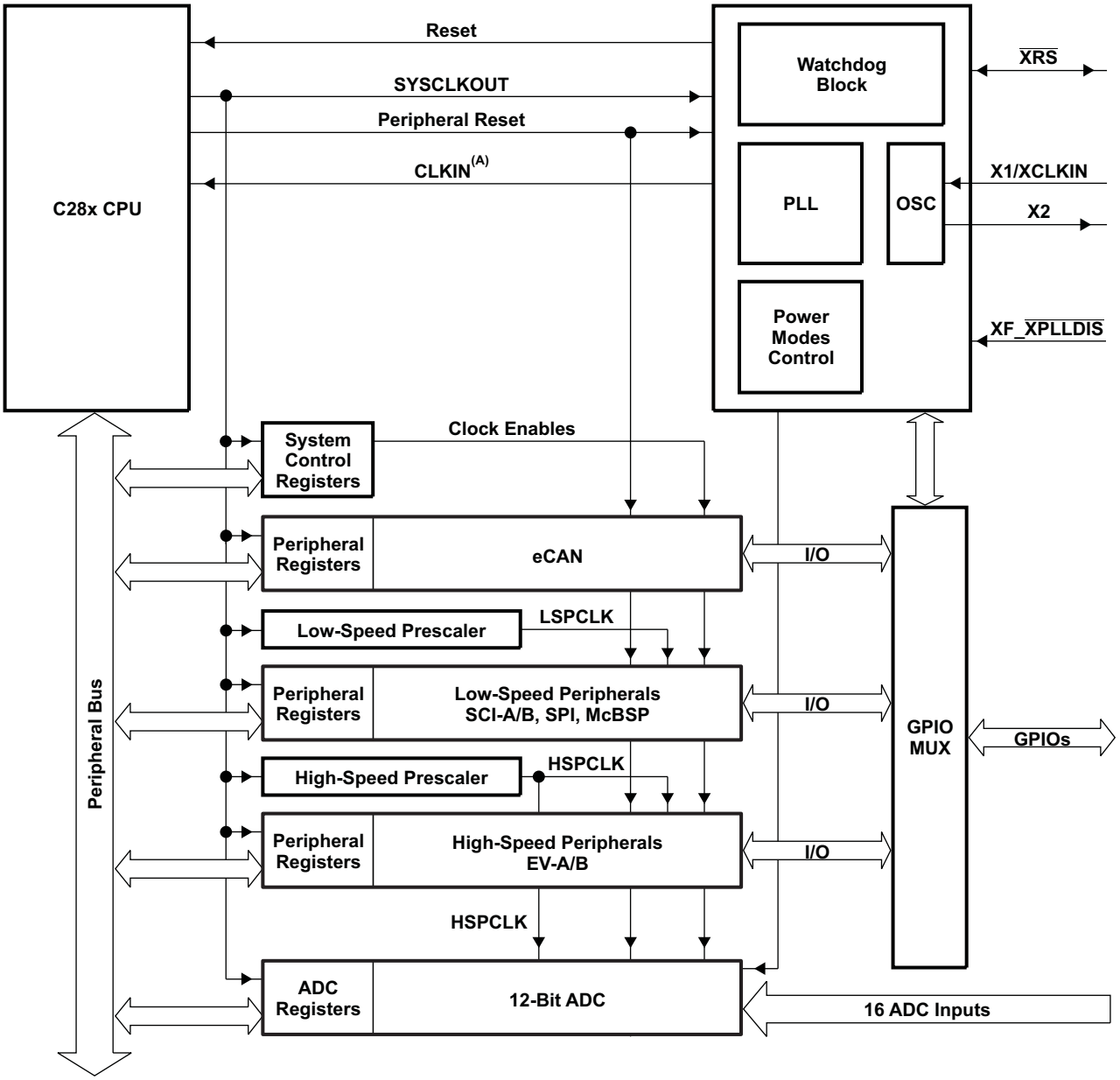
Table 6-26. External Interrupts Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 control register
XINT2CR	0x00 7071	1	XINT2 control register
Reserved	0x00 7072 – 0x00 7076	5	
XNMICR	0x00 7077	1	XNMI control register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
Reserved	0x00 707A – 0x00 707E	5	
XNMICTR	0x00 707F	1	XNMI counter register

Each external interrupt can be enabled/disabled or qualified using positive or negative going edge. For more information, see the *TMS320x281x DSP System Control and Interrupts Reference Guide*.

6.8 System Control

This section describes the F281x oscillator, PLL and clocking mechanisms, the watchdog function and the low-power modes. Figure 6-19 shows the various clock and reset domains in the F281x devices that will be discussed.



A. CLKIN is the clock input to the CPU. SYSCLKOUT is the output clock of the CPU. They are of the same frequency.

Figure 6-19. Clock and Reset Domains

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The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 6-27.

Table 6-27. PLL, Clocking, Watchdog, and Low-Power Mode Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
Reserved	0x00 7010 – 0x00 7017	8	
Reserved	0x00 7018	1	
Reserved	0x00 7019	1	
HISPCP	0x00 701A	1	High-Speed Peripheral Clock Prescaler Register for HSPCLK clock
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register for LSPCLK clock
PCLKCR	0x00 701C	1	Peripheral Clock Control Register
Reserved	0x00 701D	1	
LPMCR0	0x00 701E	1	Low-Power Mode Control Register 0
LPMCR1	0x00 701F	1	Low-Power Mode Control Register 1
Reserved	0x00 7020	1	
PLLCR	0x00 7021	1	PLL Control Register(2)
SCSR	0x00 7022	1	System Control and Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
Reserved	0x00 7024	1	
WDKEY	0x00 7025	1	Watchdog Reset Key Register
Reserved	0x00 7026 – 0x00 7028	3	
WDCR	0x00 7029	1	Watchdog Control Register
Reserved	0x00 702A – 0x00 702F	6	

(1) All of the above registers can only be accessed by executing the EALLOW instruction.
(2) The PLL control register (PLLCR) is reset to a known state by the $\overline{\text{XRS}}$ signal only. Emulation reset (through Code Composer Studio) will not reset PLLCR.

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6.9 OSC and PLL Block

Figure 6-20 shows the OSC and PLL block on F281x.

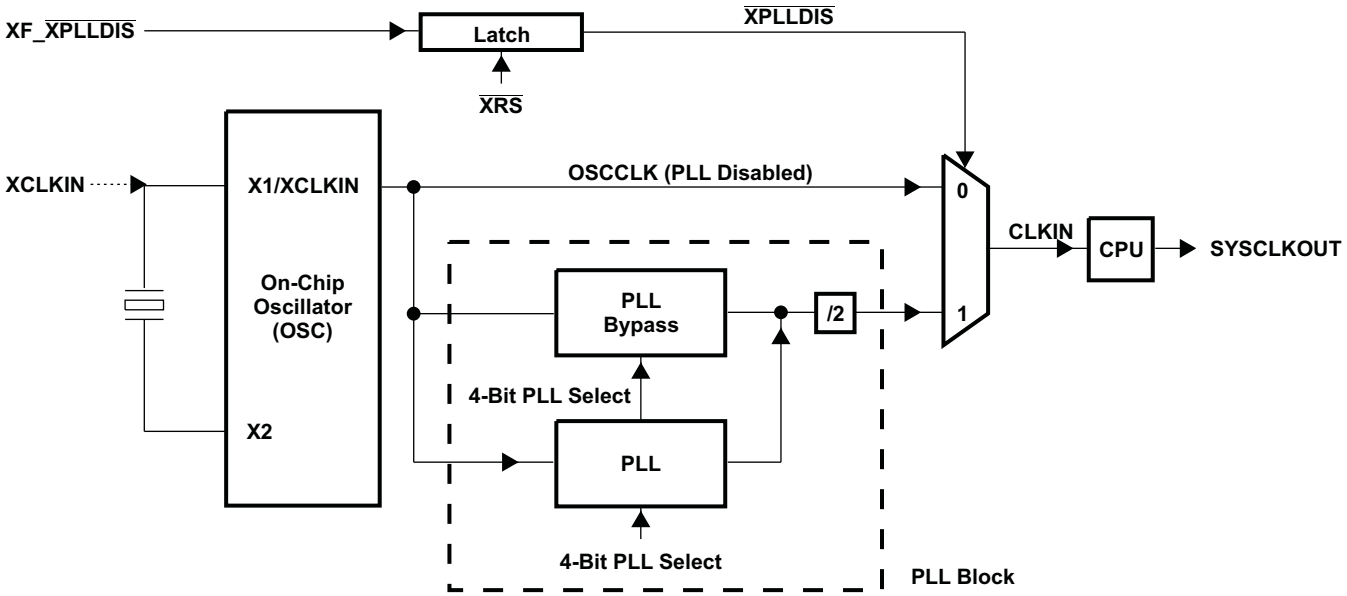


Figure 6-20. OSC and PLL Block

The on-chip oscillator circuit enables a crystal to be attached to the F281x devices using the X1/XCLKIN and X2 pins. If a crystal is not used, then an external oscillator can be directly connected to the X1/XCLKIN pin and the X2 pin is left unconnected. The logic-high level in this case should not exceed V_{DD}. The PLLCR bits [3:0] set the clocking ratio.

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Table 6-28. PLLCR Register Bit Definitions

BIT(S)	NAME	TYPE	$\overline{\text{XRS}}$ RESET(1)	DESCRIPTION
15:4	Reserved	R = 0	0:0	
3:0	DIV	R/W	0,0,0,0	SYSCLKOUT = (XCLKIN * n)/2, where n is the PLL multiplication factor. **Bit Value** / **n** / **SYSCLKOUT** 0000 / PLL Bypassed / XCLKIN/2 0001 / 1 / XCLKIN/2 0010 / 2 / XCLKIN 0011 / 3 / XCLKIN * 1.5 0100 / 4 / XCLKIN * 2 0101 / 5 / XCLKIN * 2.5 0110 / 6 / XCLKIN * 3 0111 / 7 / XCLKIN * 3.5 1000 / 8 / XCLKIN * 4 1001 / 9 / XCLKIN * 4.5 1010 / 10 / XCLKIN * 5 1011 / 11 / Reserved 1100 / 12 / Reserved 1101 / 13 / Reserved 1110 / 14 / Reserved 1111 / 15 / Reserved

(1) The PLLCR register is reset to a known state by the $\overline{\text{XRS}}$ reset line. **If a reset is issued by the debugger, the PLL clocking ratio is not changed.**

6.9.1 Loss of Input Clock

In PLL enabled mode, if the input clock XCLKIN or the oscillator clock is removed or absent, the PLL will still issue a “limp-mode” clock. The limp-mode clock will continue to clock the CPU and peripherals at a typical frequency of 1–4 MHz. The PLLCR register should have been written to with a non-zero value for this feature to work.

Normally, when the input clocks are present, the watchdog counter will decrement to initiate a watchdog reset or WDINT interrupt. However, when the external input clock fails, the watchdog counter will stop decrementing (that is, the watchdog counter does not change with the limp-mode clock). This condition could be used by the application firmware to detect the input clock failure and initiate necessary shut-down procedure for the system.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical must implement a mechanism by which the DSP will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the DSP, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the V_{DD3VFL} rail.

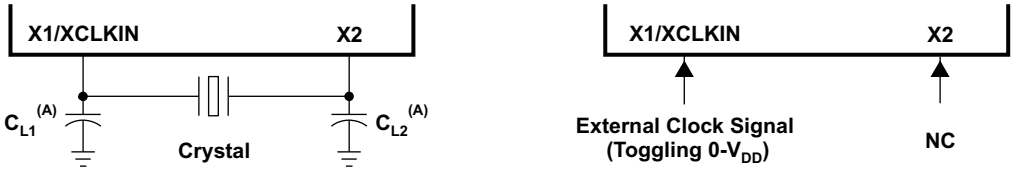
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6.10 PLL-Based Clock Module

The F281x has an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 131072 XCLKIN cycles.

The PLL-based clock module provides two modes of operation:

- **Crystal operation:** This mode allows the use of an external crystal/resonator to provide the time base to the device.
- **External clock source operation:** This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the X1/XCLKIN pin.



A. TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will ensure start-up and stability over the entire operating range.

Figure 6-21. Recommended Crystal/Clock Connection

Table 6-29. Possible PLL Configuration Modes

PLL MODE	REMARKS	SYSCLKOUT
PLL Disabled	Invoked by tying $\overline{\text{XPLLDIS}}$ pin low upon reset. PLL block is completely disabled. Clock input to the CPU (CLKIN) is directly derived from the clock signal present at the X1/XCLKIN pin.	XCLKIN
PLL Bypassed	Default PLL configuration upon power-up, if PLL is not disabled. The PLL itself is bypassed. However, the /2 module in the PLL block divides the clock input at the X1/XCLKIN pin by two before feeding it to the CPU.	XCLKIN/2
PLL Enabled	Achieved by writing a non-zero value “n” into PLLCR register. The /2 module in the PLL block now divides the output of the PLL by two before feeding it to the CPU.	(XCLKIN * n) / 2

6.11 External Reference Oscillator Clock Option

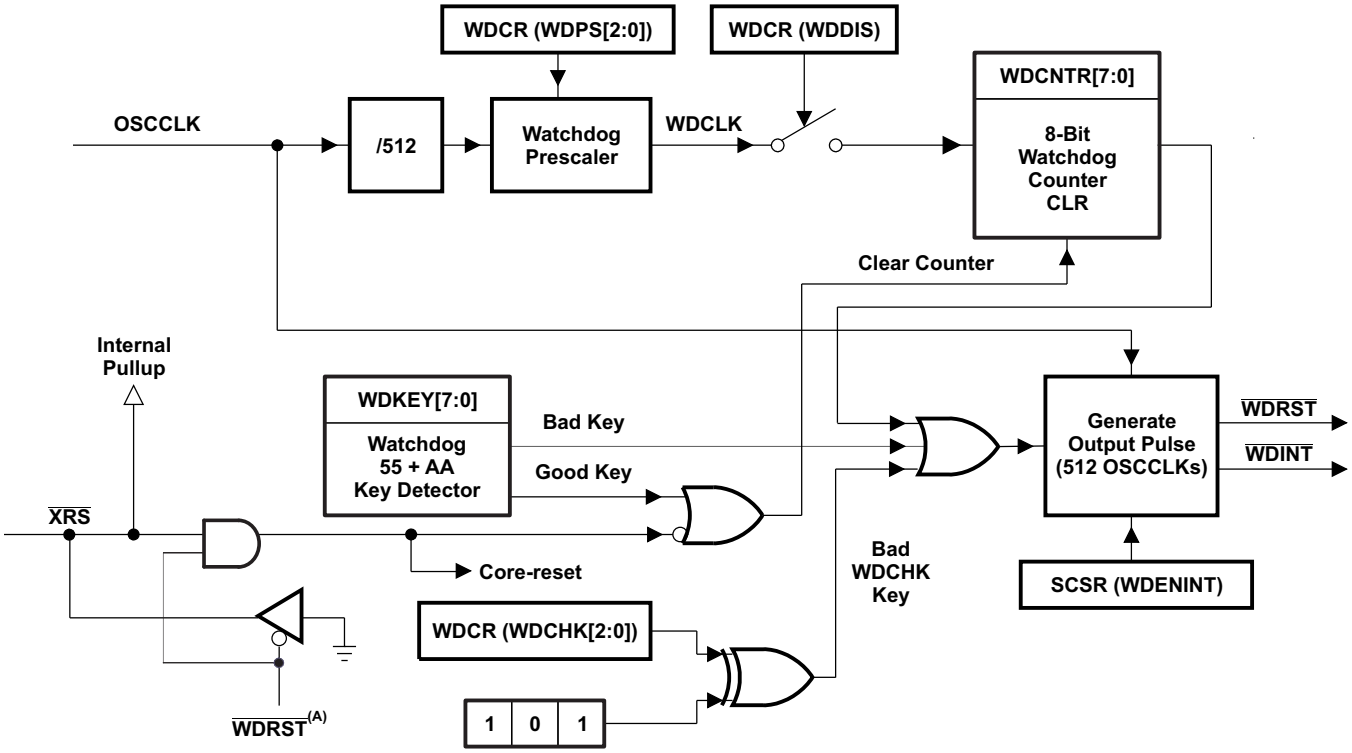
The typical specifications for the external quartz crystal for a frequency of 30 MHz are listed below:

- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 25 to 40 Ω

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6.12 Watchdog Block

The watchdog block on the F281x is identical to the one used on the 240x devices. The watchdog module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which will reset the watchdog counter. Figure 6-22 shows the various functional blocks within the watchdog module.



A. The WDRST signal is driven low for 512 OSCCLK cycles.

Figure 6-22. Watchdog Module

The WDINT signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode timer.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The WATCHDOG module will run off the PLL clock or the oscillator clock. The WDINT signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section 6.13, Low-Power Modes Block, for more details.

In IDLE mode, the WDINT signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and hence, so is the WATCHDOG.

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6.13 Low-Power Modes Block

The low-power modes on F281x are similar to the 240x devices. Table 6-30 summarizes the various modes.

Table 6-30. Low-Power Modes

MODE	LPM[1:0]	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
Normal	X,X	on	on	on	–
IDLE	0,0	on	on	on(2)	$\overline{\text{XRS}}$, $\overline{\text{WDINT}}$, Any Enabled Interrupt, XNMI, Debugger(3)
STANDBY	0,1	on (watchdog still running)	off	off	$\overline{\text{XRS}}$, $\overline{\text{WDINT}}$, XINT1, XNMI, $\overline{\text{T1/2/3/4CTRIP}}$, $\overline{\text{C1/2/3/4/5/6TRIP}}$, SCIRXDA, SCIRXDB, CANRX, Debugger(3)
HALT	1,X	off (oscillator and PLL turned off, watchdog not functional)	off	off	$\overline{\text{XRS}}$, XNMI, Debugger(3)

(1) The Exit column lists which signals or under what conditions the low-power mode will be exited. A low signal, on any of the signals, will exit the low-power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the IDLE mode will not be exited and the device will go back into the indicated low-power mode.
(2) The IDLE mode on the C28x behaves differently than on the 24x/240x. On the C28x, the clock output from the core (SYSCLKOUT) is still functional; while on the 24x/240x, the clock is turned off.
(3) On the C28x, the JTAG port can still function even if the core clock (CLKIN) is turned off.

The various low-power modes operate as follows:

IDLE Mode This mode is exited by any enabled interrupt or an XNMI that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode All other signals (including XNMI) will wake the device from STANDBY mode if selected by the LPMCR1 register. The user will need to select which signal(s) will wake the device. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode Only the $\overline{\text{XRS}}$ and XNMI external signals can wake the device from HALT mode. The XNMI input to the core has an enable/disable bit. Hence, it is safe to use the XNMI signal for this function.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them when the IDLE instruction was executed.

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7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 TI Reference Design

The TI Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all reference designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at Select TI reference designs.

8 器件和文档支持

8.1 入门

这一部分提供了当为一个 C28x 器件进行首次开发时所采取步骤的简要概括。有关这些步骤的详细情况，请参阅：

- C2000 实时控制 MCU – 工具与软件

8.2 器件和开发支持工具命名规则

为了标明产品开发周期的阶段，TI 为所有 TMS320™DSP 器件和支持工具的部件号指定了前缀。每个 TMS320 DSP 商用系列器件均具有以下三个前缀之一：TMX、TMP 或 TMS（例如，**TMS**320F2810）。德州仪器 (TI) 建议为其支持的工具使用三个可能前缀指示符中的两个：TMDX 和 TMDS。这些前缀代表了产品开发的发展阶段，即从工程原型 (TMX/TMDX) 直到完全合格的生产器件/工具 (TMS/TMDS)。

TMX	试验器件不一定代表最终器件的电气规范标准。
TMP	最终的芯片模型符合器件的电气规范标准，但是未经完整的质量和可靠性验证。
TMS	完全合格的生产器件

支持工具开发发展流程：

TMDX	还未经德州仪器 (TI) 完整内部质量测试的开发支持产品
TMDS	完全合格的开发支持产品

TMX 和 TMP 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

TMS 器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（TMX 或者 TMP）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。这个后缀表明封装类型（例如，PBK）和温度范围（如，A）。图 8-1 提供了解读任一 TMS320F281x 系列器件的完整器件名称的图例。

有关器件部件号和详细的订购信息，请参阅封装选项附录、访问 TI 网站 (www.ti.com.cn) 或联系您的 TI 销售代表。

有关裸片器件命名规则标记的其他 说明 ，请参阅 *《TMS320F281x DSP 器件勘误表》*。

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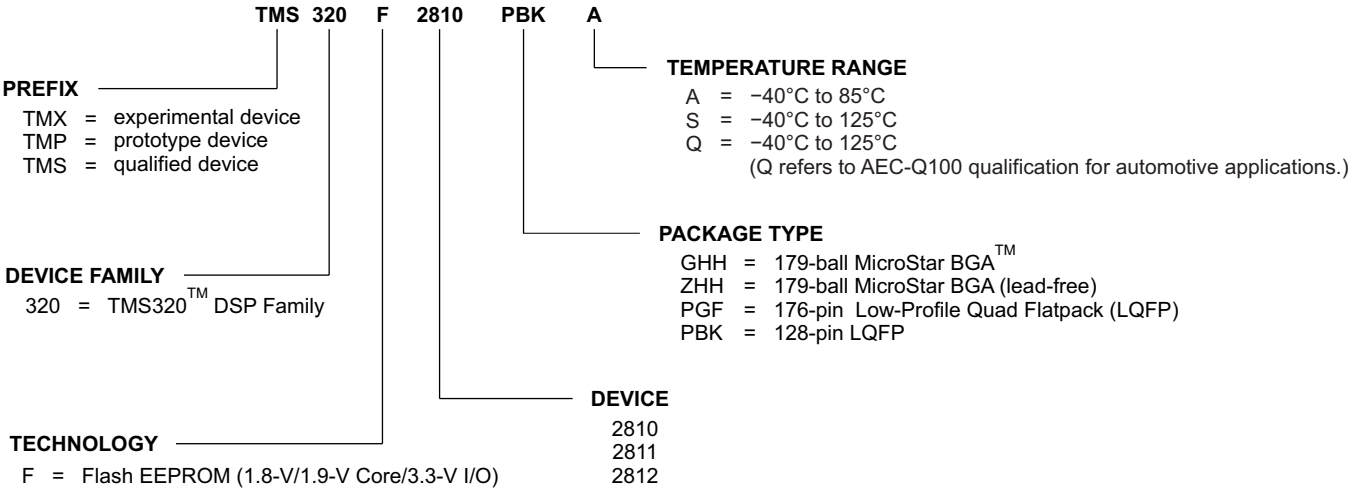


图 **8-1. TMS320F281x** 器件命名规则

8.3 工具与软件

TI 提供大量的开发工具。下面列出了部分用于评估器件性能、生成代码和开发解决方案的工具和软件。要查看所有可用的工具和软件，请访问每个器件的“工具与软件”页面，见表 8-1。

开发工具

TMS320F2812 eZdsp 入门套件 (DSK)
F2812 eZdsp ™是一个独立模块，能让评估人员检验 F2812 数字信号处理器 (DSP) 的某些特性，以确定该 DSP 是否符合其应用要求。该模块有一个单芯片并行端口，可连接 JTAG 扫描控制器。因此，该模块无需仿真器等其他开发工具即可运行。另外，该模块是为 F2812 处理器开发、演示和运行软件的出色平台。

Uniflash 独立闪存工具
CCS Uniflash 是一个独立的工具，用于在 TI MCU 上对片上闪存存储器进行编程。

软件工具

controlSUITE™ 软件套件：适用于 C2000™ 微控制器的软件开发工具
适用于 C2000 微控制器™的 controlSUITE ™是一套全面的软件基础架构、工具和文档，旨在最大限度地缩短系统开发时间。从特定于器件的驱动程序和支持软件到复杂系统应用中的完整 示例，controlSUITE 包含开发和评估等各阶段所需的资源。

用于 C2000 微控制器的 Code Composer Studio™ (CCS) 集成开发环境 (IDE)
Code Composer Studio 是支持 TI 的微控制器和嵌入式处理器产品系列的集成开发环境 (IDE)。Code Composer Studio 包含一整套用于开发和调试嵌入式应用 的工具的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。直观的 IDE 提供了单一用户界面，可帮助用户完成应用开发流程的每个步骤。熟悉的工具和界面使用户能够比以前更快地入手。Code Composer Studio 将 Eclipse 软件框架的优点和 TI 先进的嵌入式调试功能相结合，为嵌入式开发人员提供了一种功能丰富的优异开发环境。

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模型

您可以从产品的“工具与软件”页面下载各种模型。这些模型包括 I/O 缓冲器信息规范 (IBIS) 模型和边界扫描说明 语言 (BSDL) 模型。要查看所有可用的模型，请访问每个器件的“工具与软件”页面的“模型”部分，具体链接见表 8-1。

8.4 文档支持

如需接收文档更新通知，请访问 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

下面列出了介绍处理器、相关外设以及其他配套技术资料的最新文档。

勘误表

《TMS320F281x DSP 器件勘误表》介绍了不同器件版本的问题警告和使用说明。

CPU 用户指南

《TMS320C28x CPU 和指令集参考指南》介绍了 TMS320C28x 定点数字信号处理器 (DSP) 的中央处理器 (CPU) 和汇编语言指令。它还介绍了这些 DSP 上 提供 的仿真特性。

外设指南

《C2000 实时控制外设参考指南》介绍了 28x 数字信号处理器 (DSP) 的外设参考指南。

《TMS320x281x DSP 模数转换器 (ADC) 参考指南》介绍了 ADC 模块。这个模块为一个 12 位管线式 ADC。此转换器的模拟电路，在这个文档中被称为核心，其中包括前端模拟多路复用器 (MUX)、采样保持 (S/H) 电路、转换内核、电压稳压器和其它模拟支持电路。数字电路，在本文档中称为包装程序，包括可编程转换序列发生器、结果寄存器、到模拟电路、器件外设总线和其它片载模块的接口。

《TMS320x281x DSP 引导 ROM 参考指南》介绍了引导加载程序（出厂编程的引导加载软件）的用途和 特性 。它还介绍了器件的片上引导 ROM 的其它内容，并识别了所有信息在该存储器内的位置。

《TMS320x281x DSP 事件管理器 (EV) 参考指南》介绍了 EV 模块，该模块具有广泛的功能和 特性， 特别适用于运动控制和电机控制 应用。EV 模块包括通用 (GP) 计时器、完全比较/PWM 单元、捕捉单元和正交编码器脉冲 (QEP) 电路。

《TMS320x281x DSP 外部接口 (XINTF) 参考指南》介绍了 281x 数字信号处理器 (DSP) 的外部接口 (XINTF)。

《TMS320x281x DSP 多通道缓冲串口 (McBSP) 参考指南》介绍了 281x 器件上提供的 McBSP。McBSP 允许 DSP 与系统中其他器件间的直接连接。

《TMS320x281x DSP 系统控制和中断参考指南》介绍了 281x 数字信号处理器 (DSP) 的各种中断和系统控制 功能 。

《TMS320x281x 增强型控制器局域网 (eCAN) 参考指南》介绍了在电气噪声较大的环境中使用已确立的协议与其他控制器进行串行通信的 eCAN。借助 32 个完全可配置的邮箱和时间戳功能，eCAN 模块提供了多用途和稳健的串行通信接口。C28x DSP 中采用的 eCAN 模块符合 ISO11898-1 (CAN 2.0B) 标准（有效）。

《TMS320x281x 串行通信接口 (SCI) 参考指南》介绍了 SCI，这是一种双线制异步串行端口，通常称为 UART。SCI 模块支持 CPU 与其他异步外设之间使用标准非归零码 (NRZ) 格式的数字通信。

《TMS320x281x 串行外设接口参考指南》介绍了 SPI，这是一种高速同步串行输入/输出 (I/O) 端口，允许按照已编程的位传输速率将具有编程长度（1 到 16 位）的串行比特流移入或移出器件。SPI 用于 DSP 控制器与外部外设或其它处理器之间的通信。

工具指南

《TMS320C28x 汇编语言工具 v18.12.0.LTS 用户指南》介绍了用于 TMS320C28x 器件的汇编语言工具（用于开发汇编语言代码的汇编程序和其他工具）、汇编器指令、宏、通用对象文件格式和符号调试指令。

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《TMS320C28x 优化 C/C++ 编译器 v18.12.0.LTS 用户指南》介绍了 TMS320C28x C/C++ 编译器。此编译器接受 ANSI 标准 C/C++ 源代码，并为 TMS320C28x 器件生成 TMS320 DSP 汇编语言源代码。

《TMS320C28x DSP/BIOS 5.x 应用编程接口 (API) 参考指南》介绍了如何使用 DSP/BIOS 进行开发。

应用报告

SMT 和封装应用手册网站列出了有关 TI 表面贴装技术 (SMT) 的文档以及涵盖各种封装相关主题的应用手册。

《TMS320x28xx eCAN 应用报告的编程示例》包含解释如何针对不同的操作模式设置 eCAN 模块的几个编程示例。此文档的目的是帮助您在编辑 eCAN 时能够加快速度。为了有助于理解，所有程序已经被添加了详细注释。

《F2810、F2811 和 F2812 ADC 校准应用报告》介绍了一种用于提高 F2810/F2811/F2812 器件上 12 位模数转换器 (ADC) 绝对精度的方法。由于固有增益和偏移错误，ADC 的绝对精度受到影响。这份报告注释中描述的方法能够改进 ADC 的绝对精度以达到好于 0.5% 的水平。本应用注释附带一个从 F2812 eZdsp 上的 RAM 执行的示例程序 (ADCcalibration，spra989.zip)。

《IBIS（I/O 缓冲器信息规范）建模简介》讨论了 IBIS 的各个方面，包括其历史、优势、兼容性、模型生成流程、输入/输出结构建模中的数据要求以及未来趋势。

《半导体封装方法》介绍了准备向最终用户发货时半导体器件所用的封装方法。

《计算嵌入式处理器的有效使用寿命》介绍了如何计算 TI 嵌入式处理器 (EP) 在电子系统中运行时的有效使用寿命。本文档的目标读者为希望确定 TI EP 的可靠性是否符合终端系统可靠性要求的总工程师。

《计算任务剖面的 FIT》说明了如何使用 TI 的可靠性降额工具计算系统任务剖面在加电条件下的组件级 FIT。

《半导体和 IC 封装热指标》介绍了传统和全新的热指标，并将它们应用于系统级结温估算方面。

《C2000™ 微控制器串行闪存编程》介绍了如何使用闪存内核和 ROM 加载程序对器件进行串行编程。

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8.5 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **8-1.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TMS320F2810	单击此处	单击此处	单击此处	单击此处	单击此处
TMS320F2811	单击此处	单击此处	单击此处	单击此处	单击此处
TMS320F2812	单击此处	单击此处	单击此处	单击此处	单击此处

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 商标

Code Composer Studio, DSP/BIOS, 179 焊球, C2000, Piccolo, MicroStar BGA, TMS320C2000, TMS320, eZdsp, 适用于 C2000 微控制器, controlSUITE, 用于 C2000 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.
eZdsp is a trademark of Spectrum Digital Incorporated.
All other trademarks are the property of their respective owners.

8.8 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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9 机械、封装和可订购信息

9.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

要了解关于 TI 封装的更多信息，请访问封装信息网站。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F2810PBKA	ACTIVE	LQFP	PBK	128	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320F2810PBKA TMS	Samples
TMS320F2810PBKQ	ACTIVE	LQFP	PBK	128	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	320F2810PBKQ TMS	Samples
TMS320F2810PBKQR	ACTIVE	LQFP	PBK	128	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	320F2810PBKQ TMS	Samples
TMS320F2810PBKS	ACTIVE	LQFP	PBK	128	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	320F2810PBKS TMS	Samples
TMS320F2811PBKA	ACTIVE	LQFP	PBK	128	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320F2811PBKA TMS	Samples
TMS320F2811PBKQ	ACTIVE	LQFP	PBK	128	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	320F2811PBKQ TMS	Samples
TMS320F2811PBKS	ACTIVE	LQFP	PBK	128	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	320F2811PBKS TMS	Samples
TMS320F2812GBBA	ACTIVE	NFBGA	GBB	179	160	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	TMS 320F2812GBBA	Samples
TMS320F2812GBBAR	ACTIVE	NFBGA	GBB	179	1000	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	TMS 320F2812GBBA	Samples
TMS320F2812GBBS	ACTIVE	NFBGA	GBB	179	160	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 125	TMS 320F2812GBBS	Samples
TMS320F2812PGFA	ACTIVE	LQFP	PGF	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	320F2812PGFA TMS	Samples
TMS320F2812PGFAG4	ACTIVE	LQFP	PGF	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	320F2812PGFA TMS	Samples
TMS320F2812PGFQ	ACTIVE	LQFP	PGF	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	320F2812PGFQ TMS	Samples
TMS320F2812PGFS	ACTIVE	LQFP	PGF	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	320F2812PGFS TMS	Samples
TMS320F2812ZAYA	ACTIVE	NFBGA	ZAY	179	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	TMS 320F2812ZAYA	Samples
TMS320F2812ZAYAR	ACTIVE	NFBGA	ZAY	179	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	TMS 320F2812ZAYA	Samples
TMS320F2812ZAYS	ACTIVE	NFBGA	ZAY	179	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	TMS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										320F2812ZAYS	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMS320F2810, TMS320F2810-Q1, TMS320F2811, TMS320F2811-Q1, TMS320F2812, TMS320F2812-Q1 :

- Catalog : TMS320F2810, TMS320F2811, SM320F2812, TMS320F2812

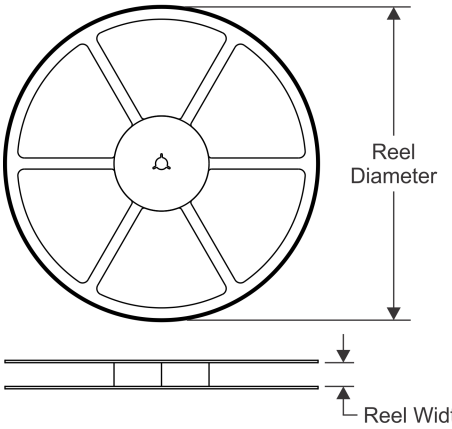
- Automotive : TMS320F2810-Q1, TMS320F2811-Q1, TMS320F2812-Q1
- Enhanced Product : SM320F2812-EP
- Military : SMJ320F2812, SMJ320F2812

NOTE: Qualified Version Definitions:

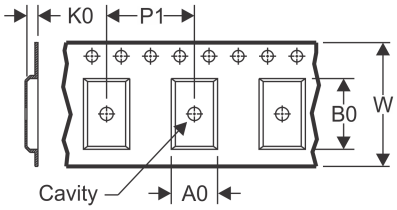
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

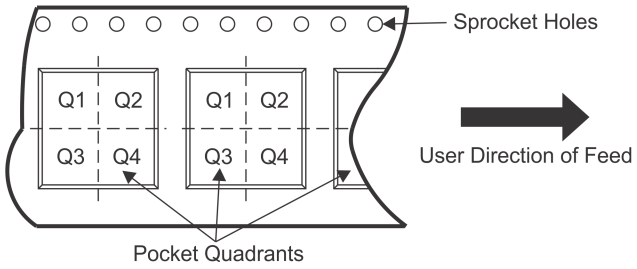


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

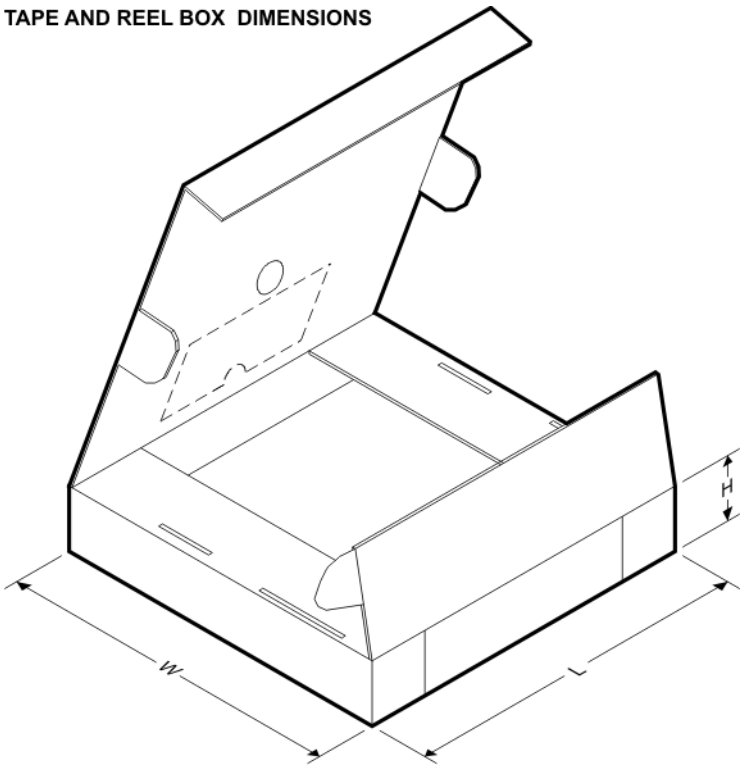
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS320F2812GBBAR	NFBGA	GBB	179	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
TMS320F2812ZAYAR	NFBGA	ZAY	179	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1

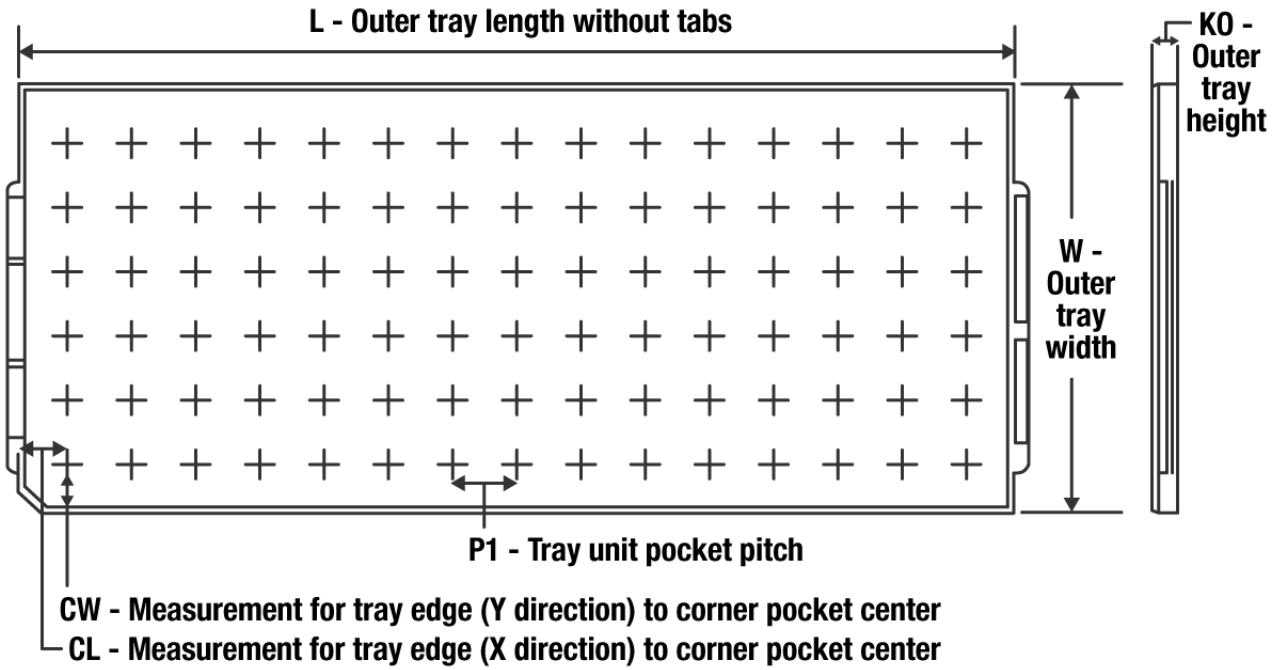
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMS320F2812GBBAR	NFBGA	GBB	179	1000	336.6	336.6	41.3
TMS320F2812ZAYAR	NFBGA	ZAY	179	1000	336.6	336.6	41.3

TRAY



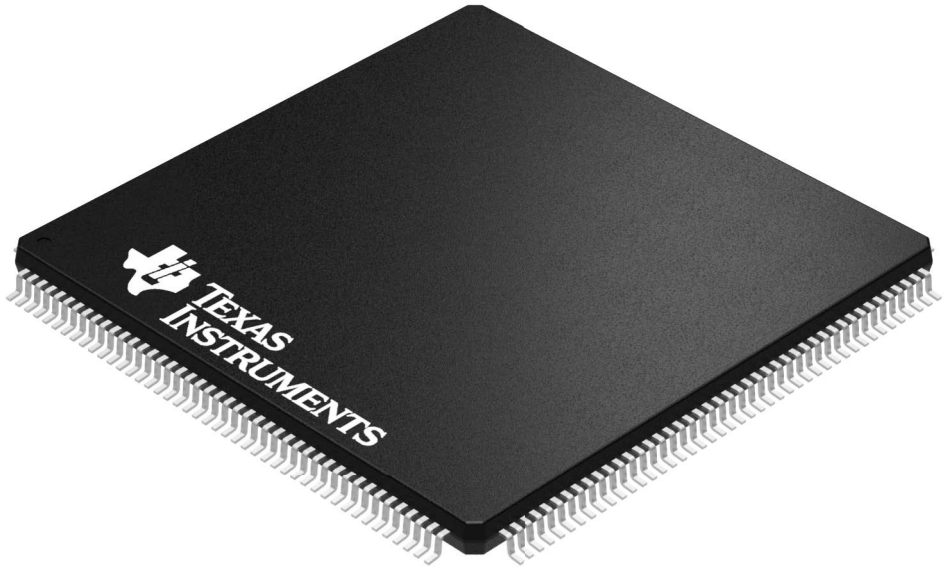
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F2810PBKA	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F2810PBKQ	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F2810PBKS	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F2811PBKA	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F2811PBKQ	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F2811PBKS	PBK	LQFP	128	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F2812GBBA	GBB	NFBGA	179	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65
TMS320F2812GBBS	GBB	NFBGA	179	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65
TMS320F2812PGFA	PGF	LQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F2812PGFAG4	PGF	LQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F2812PGFQ	PGF	LQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F2812PGFS	PGF	LQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F2812ZAYA	ZAY	NFBGA	179	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65
TMS320F2812ZAYS	ZAY	NFBGA	179	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65

PGF 176 LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



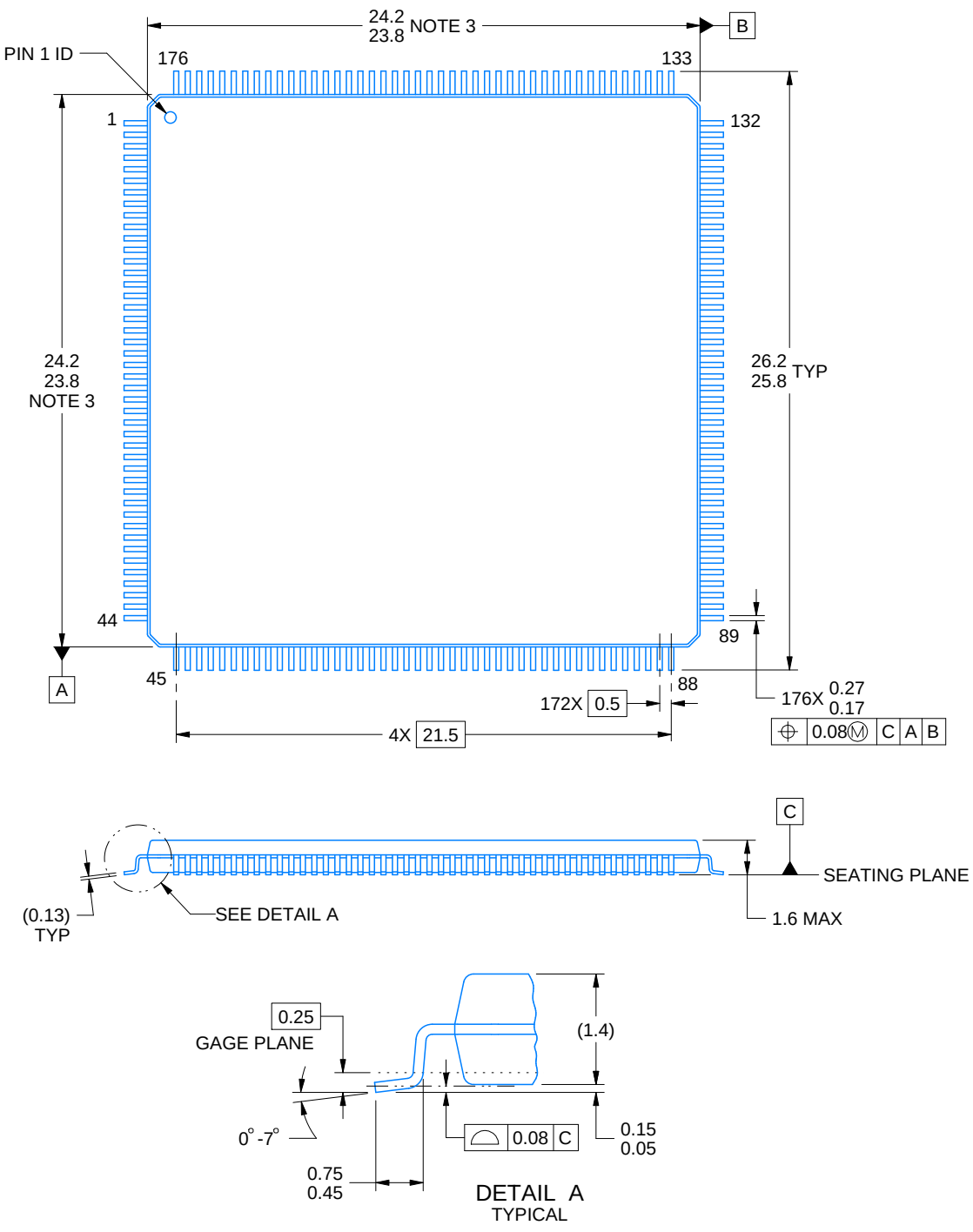
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PGF0176A

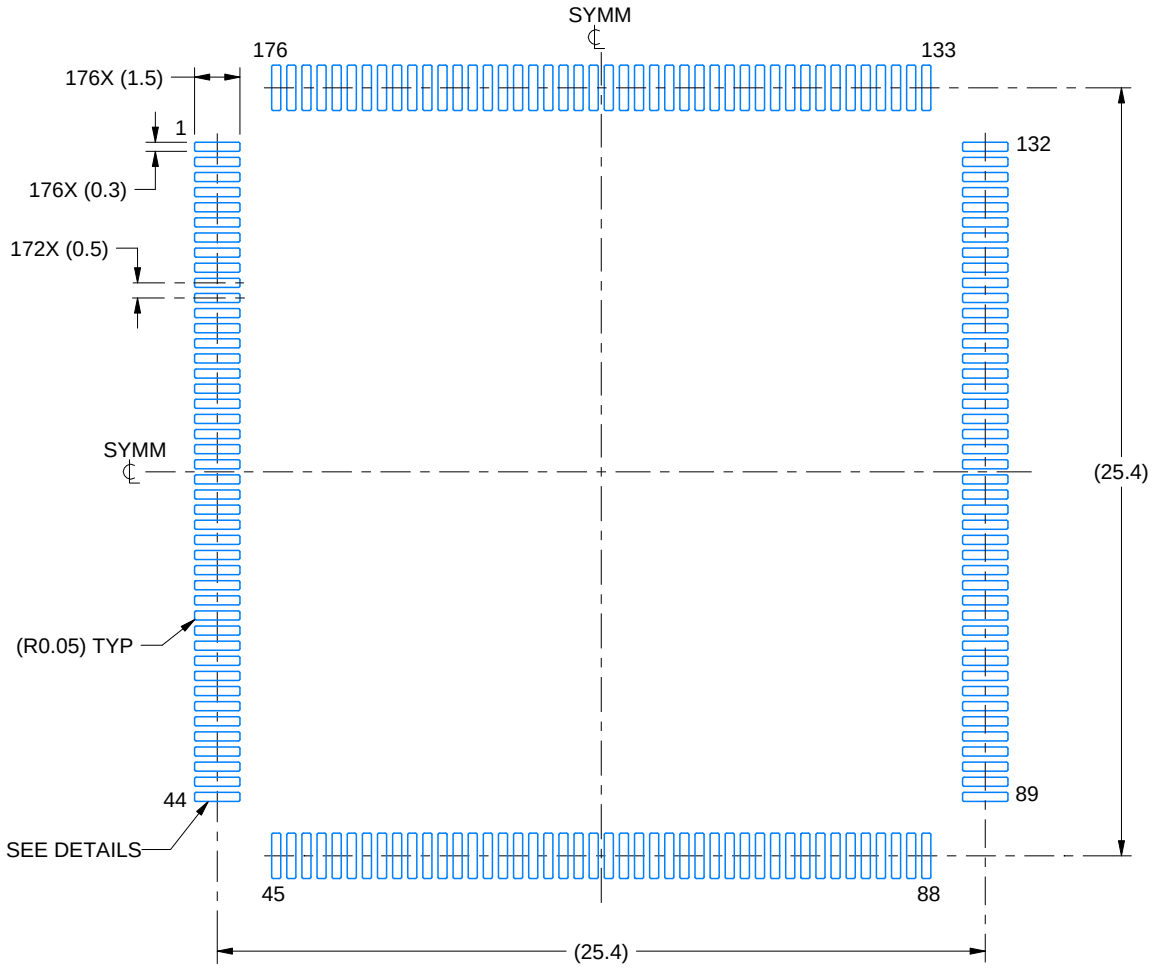
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

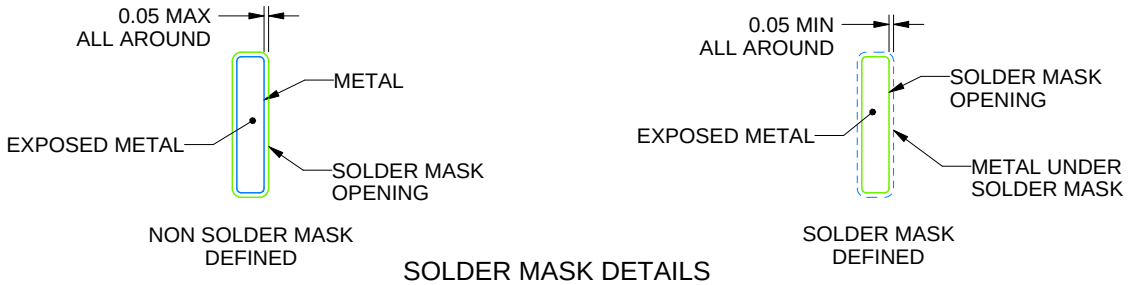


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X

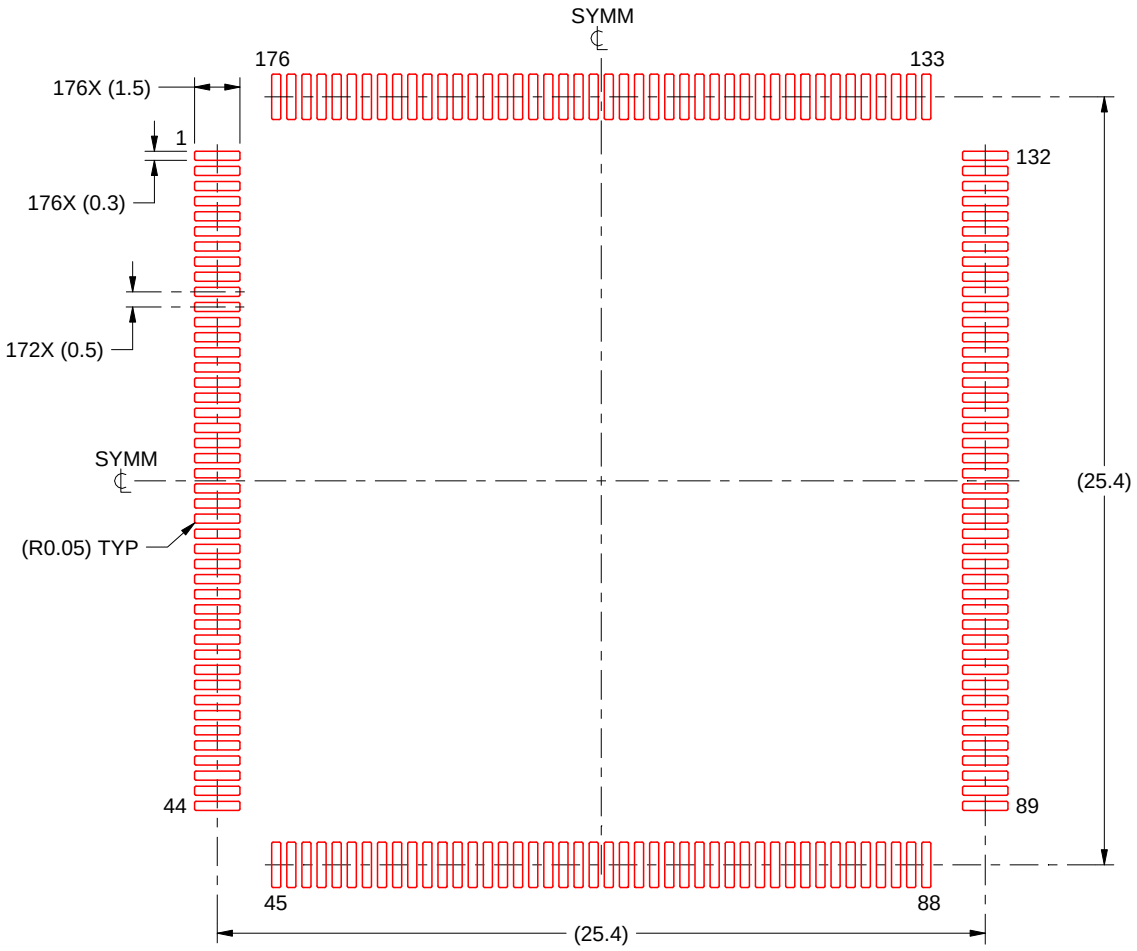


SOLDER MASK DETAILS

4215177/A 05/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



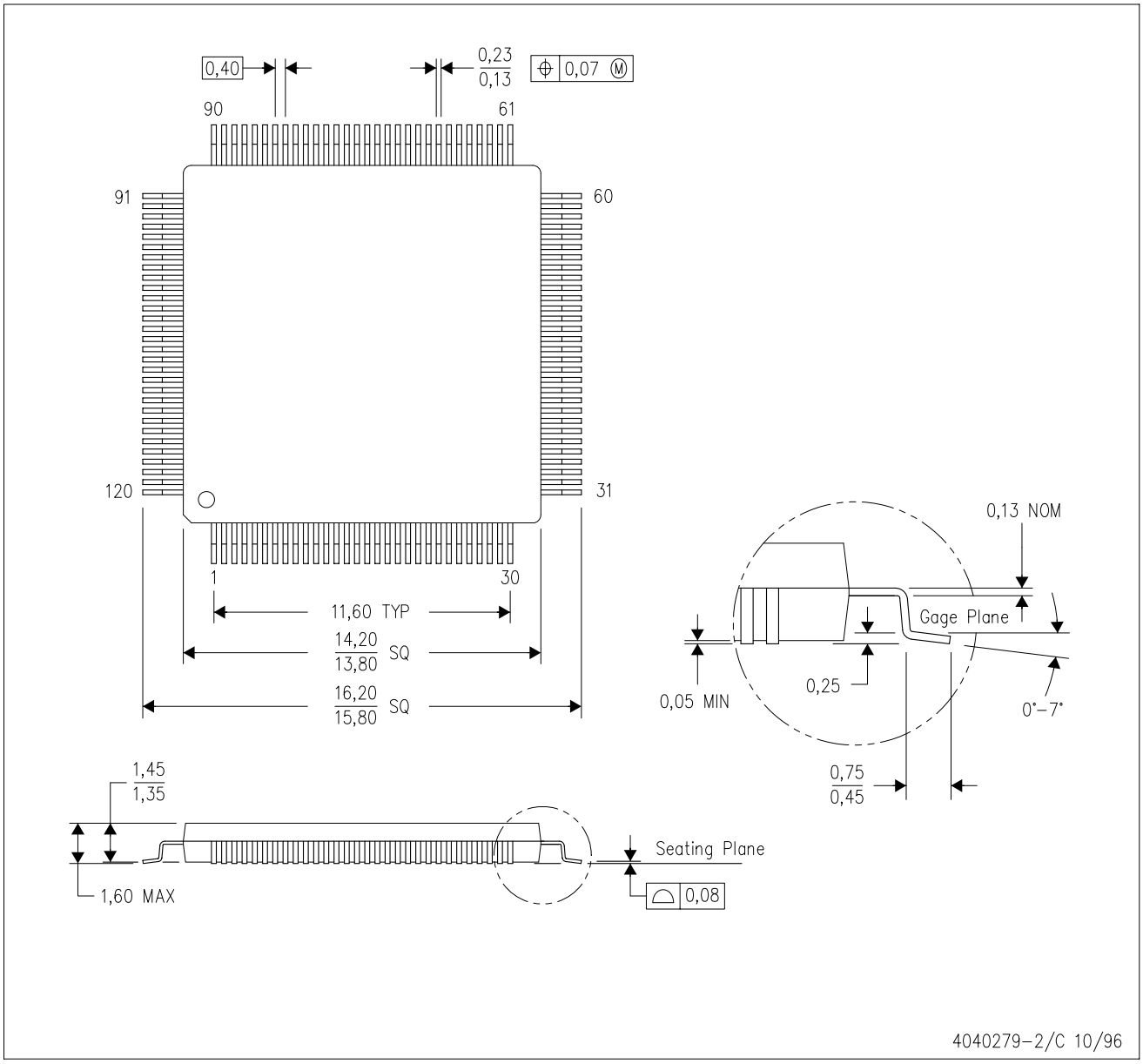
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215177/A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PBK (S–PQFP–G120) PLASTIC QUAD FLATPACK



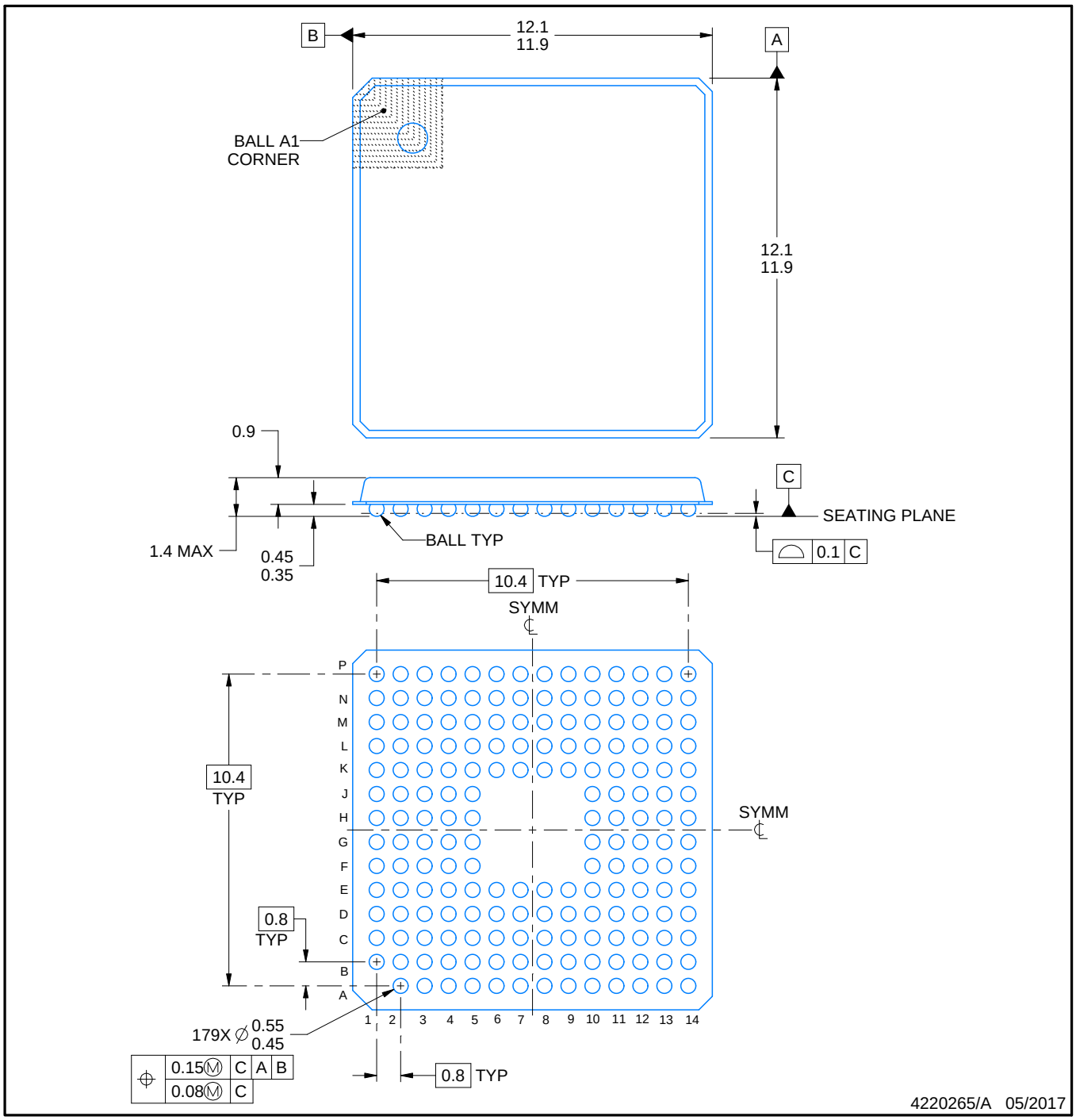
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–026

PACKAGE OUTLINE

ZHH0179A

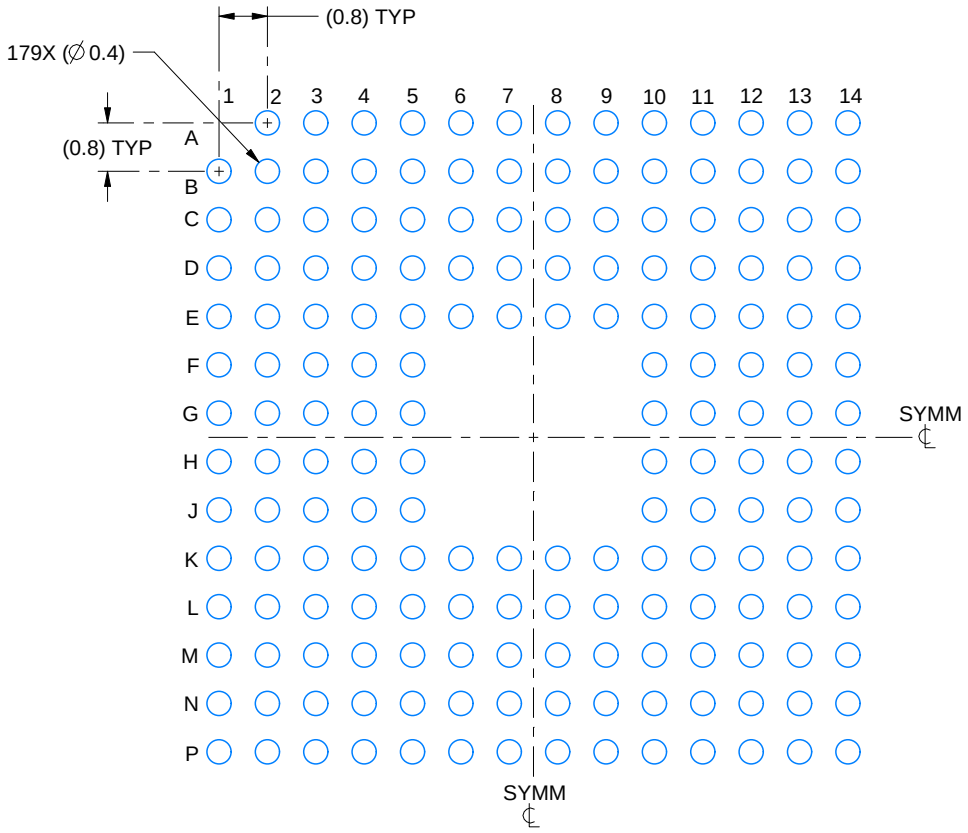
UBGA - 1.4 mm max height

BALL GRID ARRAY

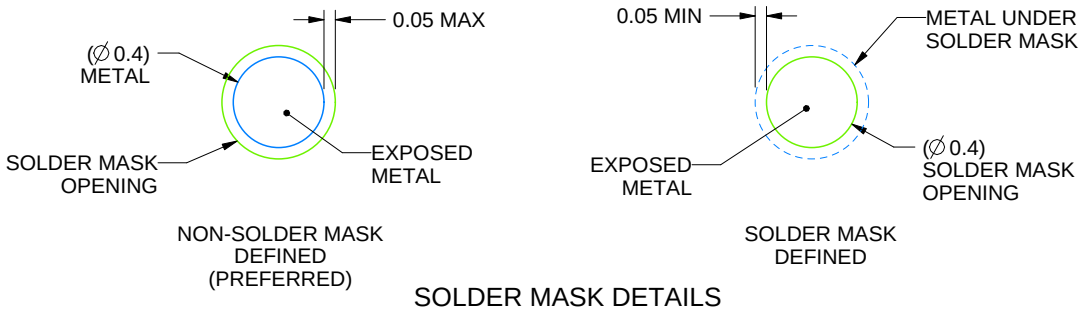


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4220265/A 05/2017

NOTES: (continued)

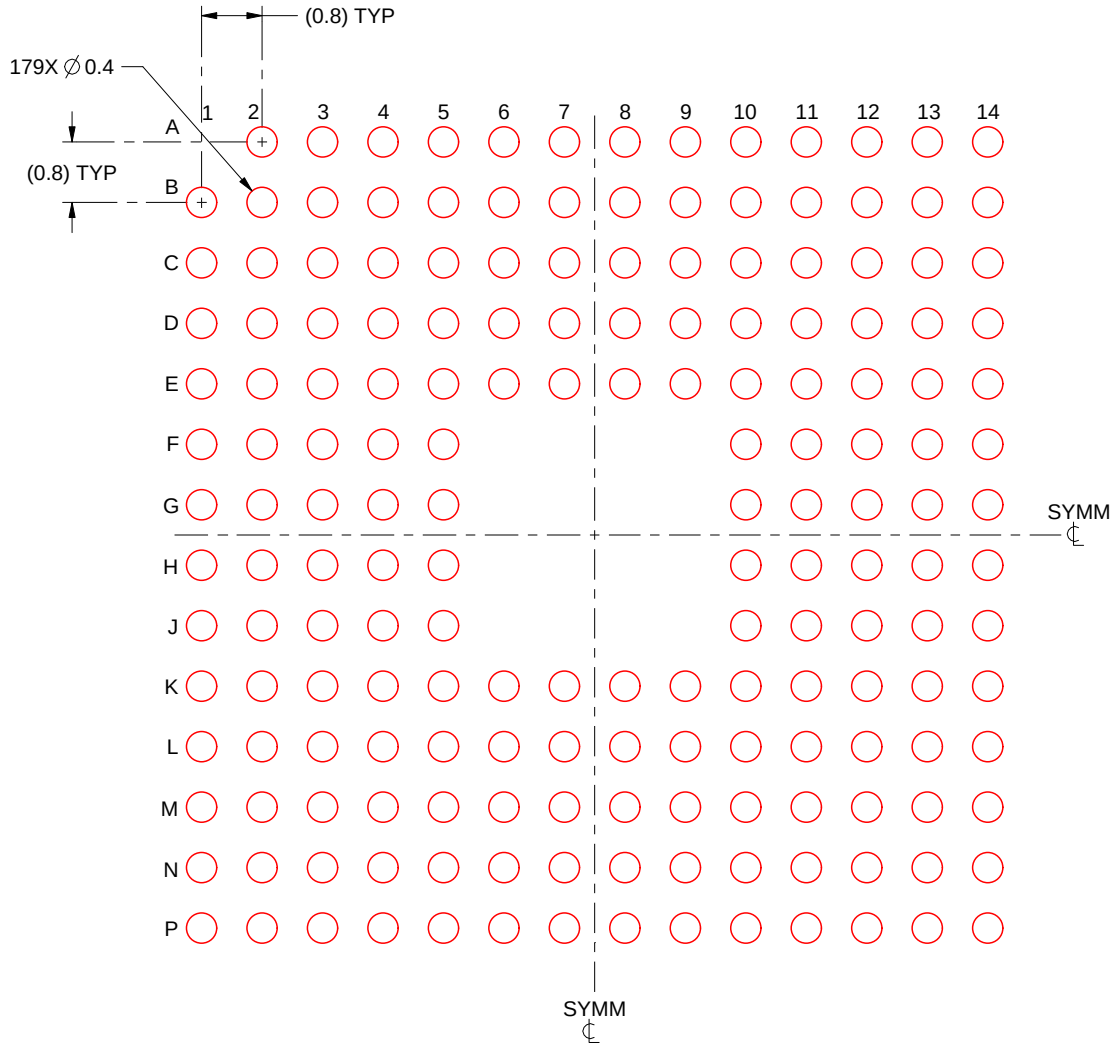
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SSZA002 (www.ti.com/lit/ssza002).

EXAMPLE STENCIL DESIGN

ZHH0179A

UBGA - 1.4 mm max height

BALL GRID ARRAY



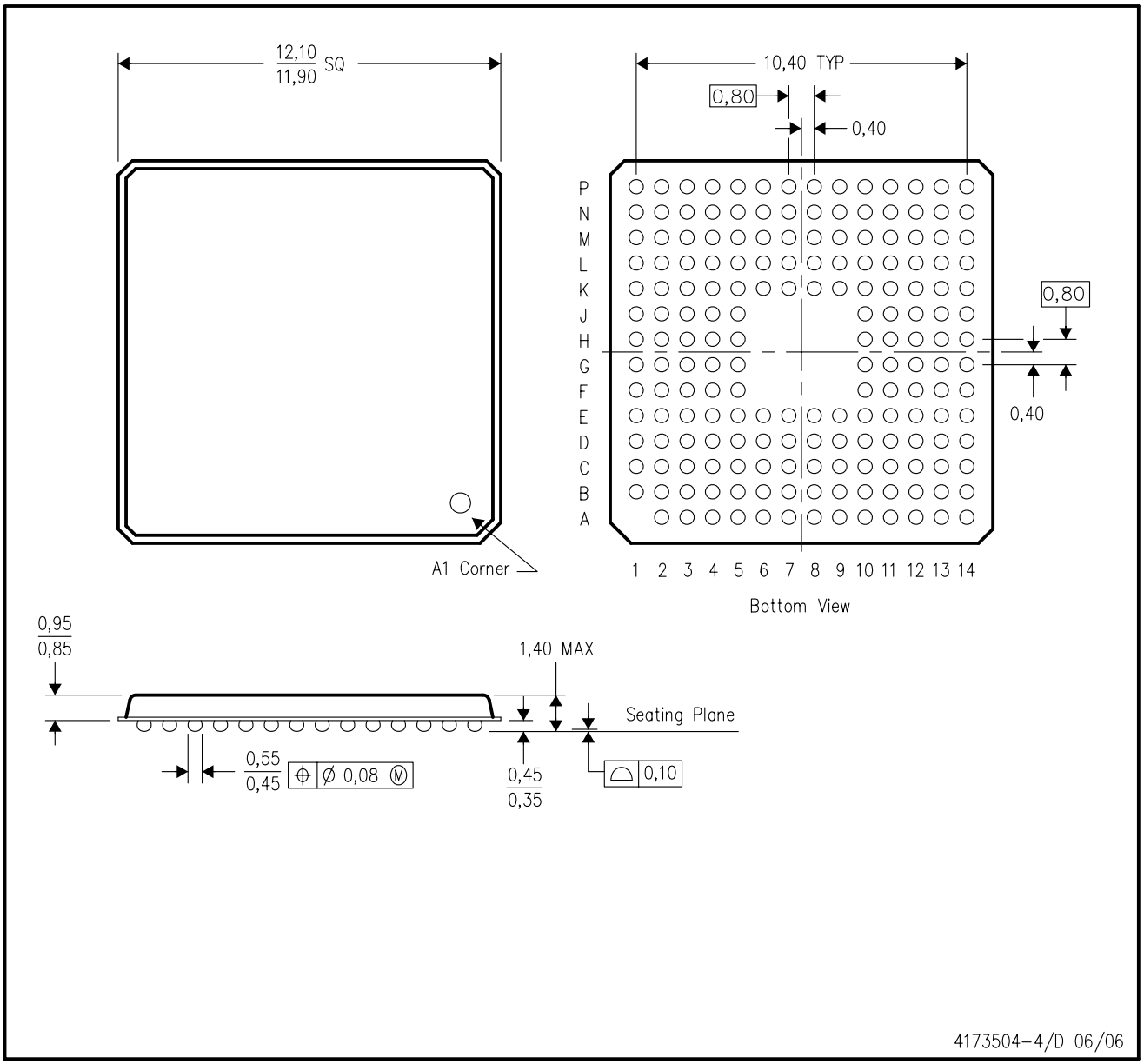
SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 10X

4220265/A 05/2017

NOTES: (continued)

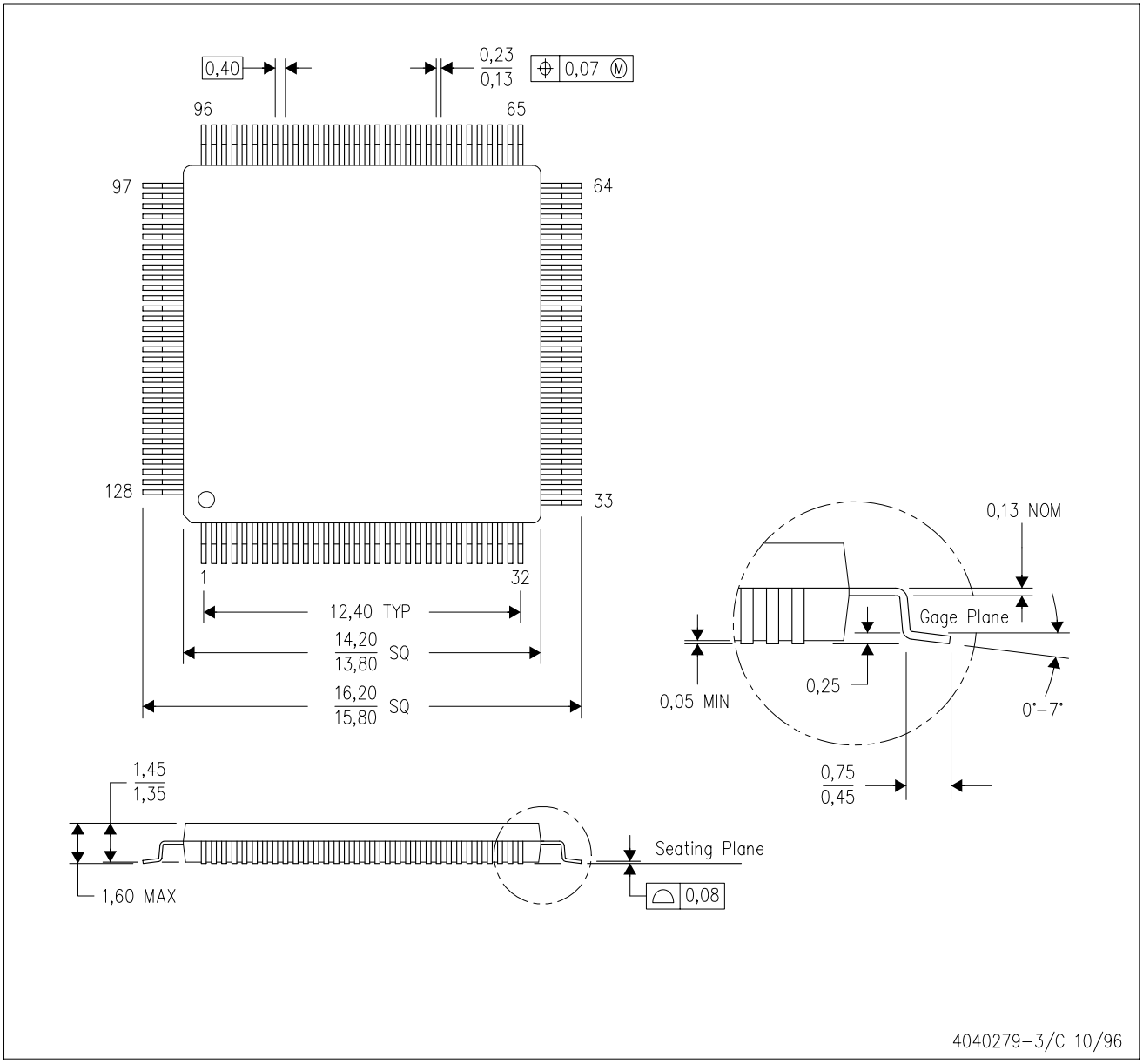
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

GHH (S–PBGA–N179) PLASTIC BALL GRID ARRAY



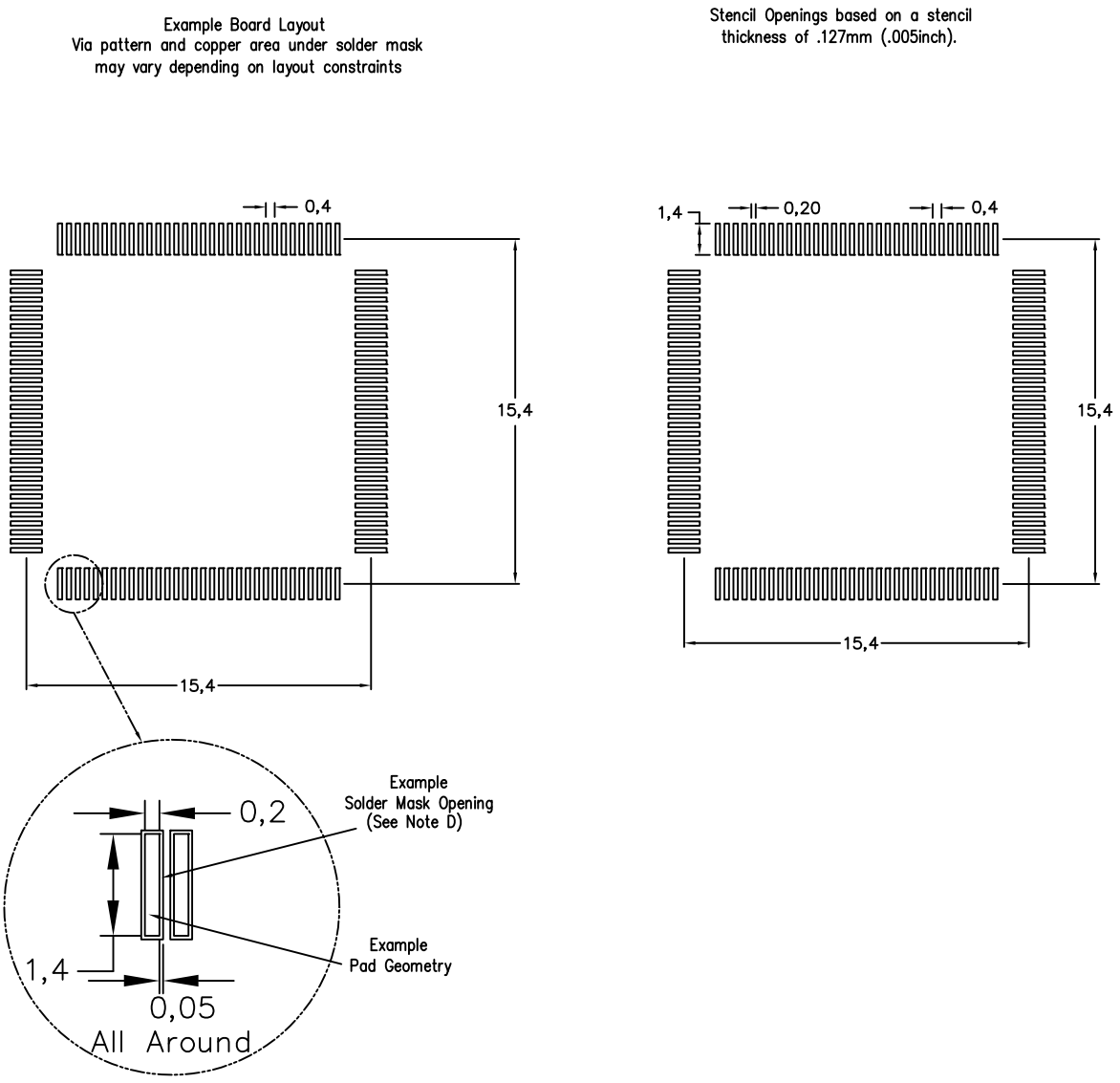
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration

PBK (S–PQFP–G128) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–026

PBK (S–PQFP–G128) PLASTIC QUAD FLAT PACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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