TPDxE05U06 适用于超高速（最高可达 6GBPS）接口的单通道、4 通道、6 通道 ESD 保护器件

1 特性

- IEC 61000-4-2 4 级 ESD 保护
  - ±12kV 接触放电
  - ±15kV 空气间隙放电
- IEC 61000-4-4 EFT 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 2.5A (8/20μs)
- IO 电容为 0.42pF 至 0.5pF（典型值）
- 直流击穿电压为 6.5V（最小值）
- 超低泄漏电流为 10nA（最大值）
- 低 ESD 钳位电压
- 工业温度范围：–40°C 至 +125°C
- 简易直通布线封装
- 业界通用的 SOD-523 封装 (1.60mm × 0.80mm × 0.65mm)

2 应用

- HDMI 1.4*b*
- HDMI 2.0
- USB 3.0
- MHL
- LVDS 接口
- DisplayPort
- PCI-express®
- eSata 接口
- V-by-One® HS

3 说明

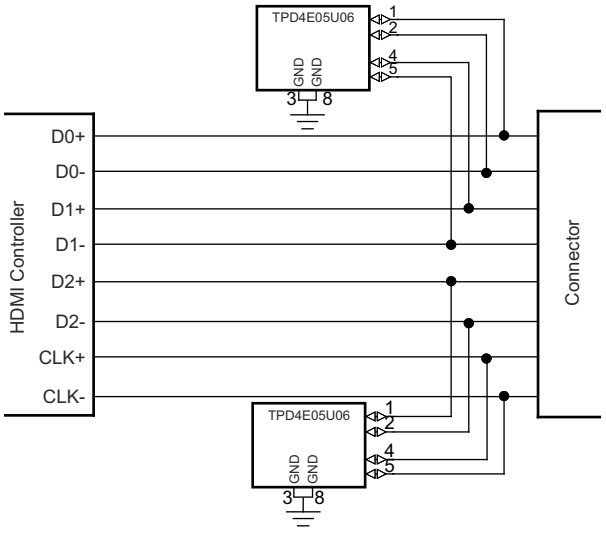
TPDxE05U06 是基于单向瞬态电压抑制器 (TVS) 的静电放电 (ESD) 保护二极管产品系列，具有超低电容。每个器件的 ESD 冲击消散值高于 IEC 61000-4-2 国际标准规定的最高水平。TPDxE05U06 的超低负载电容使其非常适用于保护任何高速信号引脚。

TPDxE05U06 的典型应用包括 HDMI 1.4*b*、HDMI 2.0、USB 3.0、MHL、LVDS、DisplayPort、PCI-Express®、eSata 和 V-by-One® HS 中的高速信号线。

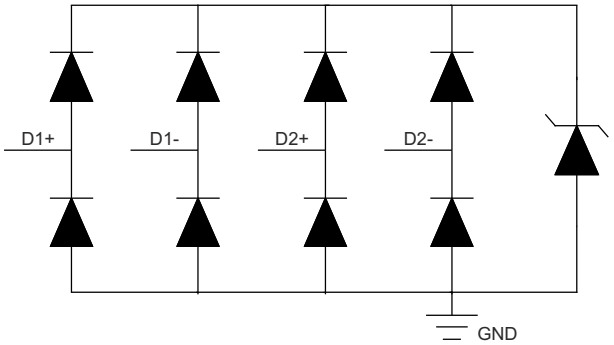
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E05U06	X1SON (2)	0.60mm x 1.00mm
	SOD-523 (2)	0.80mm × 1.20mm
TPD4E05U06	USON (10)	2.50mm x 1.00mm
TPD6E05U06	USON (14)	3.50mm × 1.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



TPD4E05U06 功能框图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (January 2017) to Revision N (February 2022) — **Page**

- 将 SOD-523 封装信息从封装尺寸 (0.8mm × 1.2mm) 更新为引线至引线尺寸 (1.60mm × 0.80mm × 0.65mm).. 1

Changes from Revision L (January 2017) to Revision M (December 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 更新了 *特性* 部分，以包含 SOD-523 封装信息.....1
- 在 *器件信息* 表中添加了 DYA 封装.....1
- Added the DYA package to the *Pin Configuration and Functions* section.....4
- Changed the minimum *DC breakdown voltage* from *6 V* to *6.5 V* in the *Detailed Description* section.....12
- Changed the minimum *reverse standoff voltage* from *5 V* to *5.5 V* in the *Detailed Description* section.....12
- Updated the *Related Documentation* section.....19

Changes from Revision K (November 2016) to Revision L (January 2017) — **Page**

- Updated DPY pinout image.....4
- Updated title from TPD4E05U06 to TPD6E05U06 in 图 7-3 11

Changes from Revision J (March 2016) to Revision K (November 2016) — **Page**

- Changed min value of V_{BR} from *6 V* to *6.5 V* in the *Electrical Characteristics* table.....6

Changes from Revision I (June 2015) to Revision J (March 2016) — **Page**

- 将 *X2SON* 的所有实例替换为 *X1SON* 1
- Update the *Pin Functions* table 4
- Added the *Power Supply Recommendations* section.....16

Changes from Revision H (May 2015) to Revision I (June 2015) — **Page**

- 添加了商标.....1
- Corrected TPD6E05U06 Pin 13 name.....4
- Corrected TLP definition.....6

Changes from Revision G (July 2014) to Revision H (May 2015) — **Page**

- 添加了其他应用.....1

- Updated with HDMI 2.0 Eye Diagrams 14

Changes from Revision F (November 2013) to Revision G (July 2014) **Page**

- 新增 61000-4-4 EFT 标准 1
- Added *Thermal Information* table 6
- Added *Handling Ratings* table 6
- Added the *Detailed Description* section 11
- Added the *Application and Implementation* section 13
- Added Layout section. 17

Changes from Revision * (December 2012) to Revision A (December 2012) **Page**

- 向文档新增 TPS2EUSB30A 器件 1

Changes from Revision A (December 2012) to Revision B (January 2013) **Page**

- Added Insertion Loss Graphic 9
- Added Eye Diagrams 14

Changes from Revision B (January 2013) to Revision C (March 2013) **Page**

- 更改了 IO 电容范围 1
- Changed test conditions and typ values for V_{clamp} 6
- Added typ R_{DYN} values for DQA and RVZ packages 6
- Added C_L values for DQA and RVZ packages 6
- Changed CURRENT vs VOLTAGE graphic 9
- Changed Insertion Loss graphic 9
- Changed HDMI Eye Diagrams 14

Changes from Revision C (March 2013) to Revision D () **Page**

- 更新了“标题” 1
- Removed Ordering Information table 4

Changes from Revision D (August 2013) to Revision E (November 2013) **Page**

- 更新了文档格式 1
- 添加了其他应用 1

5 Pin Configuration and Functions

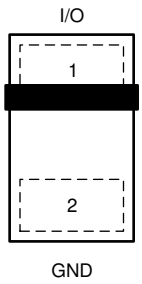


图 5-1. DPY Package 2-Pin X1SON Top View

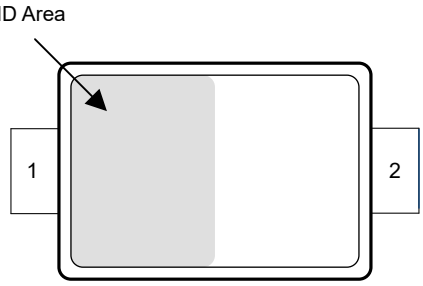


图 5-2. DYA Package 2-Pin SOD-523 Top View

表 5-1. Pin Functions TPD1E05U06 DPY and DYA

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	Ground	Ground; Connect to ground
I/O	1	I/O	ESD protected channel(1)

(1) Place as close to the connector as possible.

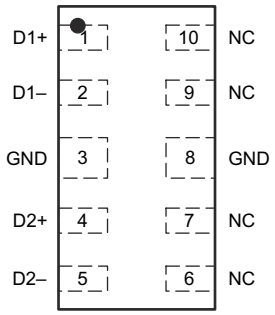


图 5-3. DQA Package 10-Pin USON Top View

表 5-2. Pin Functions TPD4E05U06 DQA

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1+	1	I/O	ESD protected channel(1)
D1–	2	I/O	ESD protected channel(1)
D2+	4	I/O	ESD protected channel(1)
D2–	5	I/O	ESD protected channel(1)
GND	3	Ground	Ground; Connect to ground
GND	8		
NC	6	—	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

(1) Place as close to the connector as possible.

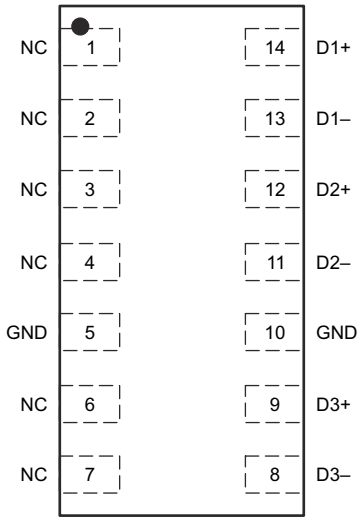


图 5-4. RVZ Package 14-Pin USON Top View

表 5-3. Pin Functions TPD6E05U06 RVZ

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1+	14	I/O	ESD protected channel(1)
D1–	13	I/O	ESD protected channel(1)
D2+	12	I/O	ESD protected channel(1)
D2–	11	I/O	ESD protected channel(1)
D3+	9	I/O	ESD protected channel(1)
D3–	8	I/O	ESD protected channel(1)
GND	5	Ground	Ground; Connect to ground
GND	10		
NC	1	—	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	2		
NC	3		
NC	4		
NC	6		
NC	7		

(1) Place as close to the connector as possible.

6 Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Electrical Fast Transient (2) (3)	IEC 61000-4-4 (5/50ns)		80	A
Peak Pulse (2) (3)	IEC 61000-4-5 Current (8/20us)		2.5	A
	IEC 61000-4-5 Power (8/20us)		40	W
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

6.1 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge – DPY, DQA, and RVZ	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	V
$V_{(ESD)}$	Electrostatic discharge – DYA	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±4000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1500 V may actually have higher performance.

6.2 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±12000	V
		IEC 61000-4-2 air-gap discharge	±15000	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	0		5.5	V
T_A	Operating free-air temperature	-40		125	°C

6.3 Thermal Information

THERMAL METRIC (1)		TPD1E05U06		TPD4E05U06	TPD6E05U06	UNIT
		DPY (X1SON)	DYA (SOD523)	DQA (USON)	RVZ (USON)	
		2 PINS	2 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	697.3	772.1	327	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	471	444.6	189.5	119.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	575.9	540.4	257.7	92.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	175.7	159.9	60.9	22	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	575.1	533.9	257	91.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION		MIN	TYP	MAX	UNIT
INPUT - OUTPUT RESISTANCE								
V_{RWM}	Reverse stand-off voltage		I_{IO} < 10 µA				5.5	V
V_{BR}	Break-down voltage		I_{IO} = 1 mA		6.5		8.5	V
V_{Clamp}	Clamp voltage		I_{PP} = 1 A, TLP, from I/O to GND (1)			10		V
			I_{PP} = 5 A, TLP, from I/O to GND (1)			14		
			I_{PP} = 1 A, TLP, from GND to I/O (1)			3		
			I_{PP} = 5 A, TLP, from GND to I/O (1)			7		
I_{LEAK}	Leakage current		V_{IO} = 2.5 V			0.01	10	nA
R_{DYN}	Dynamic resistance	DPY package	I/O to GND (2)			0.8		Ω
			GND to I/O (2)			0.8		
		DYA package	I/O to GND (2)			0.8		
			GND to I/O (2)			0.7		
		DQA package	I/O to GND (2)			0.8		
			GND to I/O (2)			0.8		
		RVZ package	I/O to GND (2)			0.8		
			GND to I/O (2)			0.8		
CAPACITANCE								
C_L	Line capacitance (3)		V_{IO} = 2.5 V; f = 1 MHz , I/O to GND	TPD1E05U06 DPY package		0.42		pF
				TPD1E05U06 DYA package		0.42		
				TPD4E05U06 DQA package		0.5		
				TPD6E05U06 RVZ package		0.47		
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of input capacitance		GND Pin = 0 V, f = 1 MHz, VBIAS = 2.5 V, Channel x pin to GND – channel y pin to GND			0.05	0.07	pF

6.4 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{CROSS}	Channel to channel input capacitance	GND Pin = 0 V, f = 1 MHz, VBIAS = 2.5 V, between channel pins		0.01	0.06	pF

(1) Transition line pulse with 100 ns width, 200 ps rise time.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A.
(3) Capacitance data is taken at 25°C.

6.5 Typical Characteristics

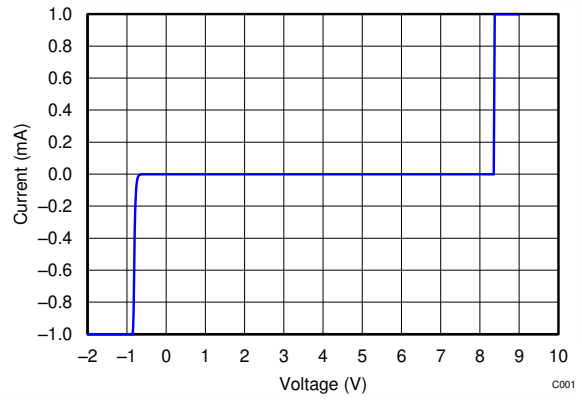


图 6-1. DC Voltage Sweep I-V Curve

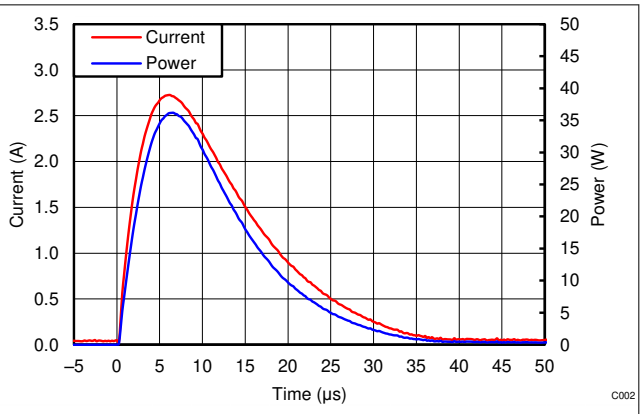


图 6-2. Surge Curve (tp = 8/20 µs), Pin IO to GND

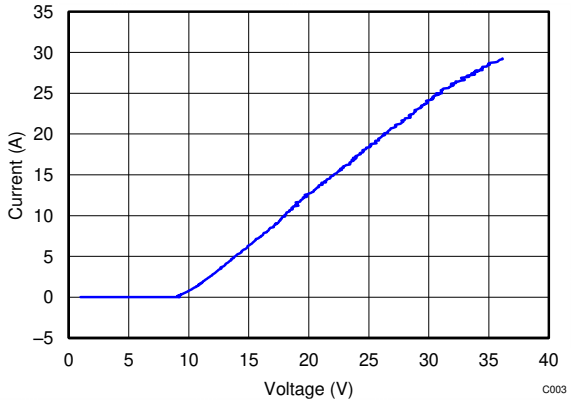


图 6-3. Positive TLP Plot IO to GND

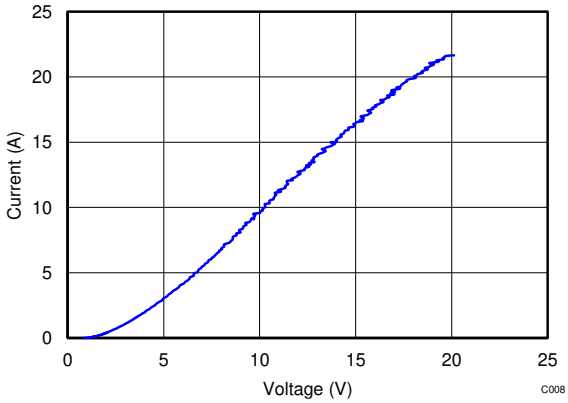


图 6-4. Negative TLP Plot IO to GND

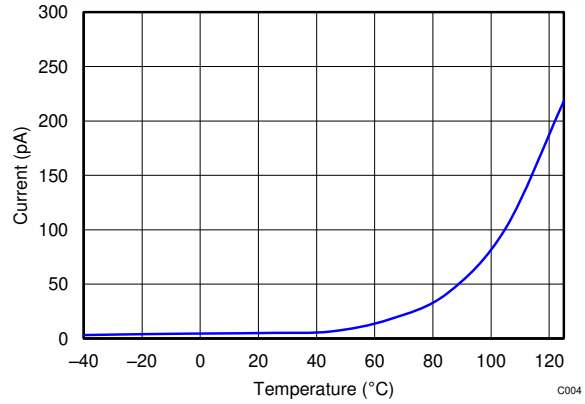


图 6-5. Leakage vs Temperature

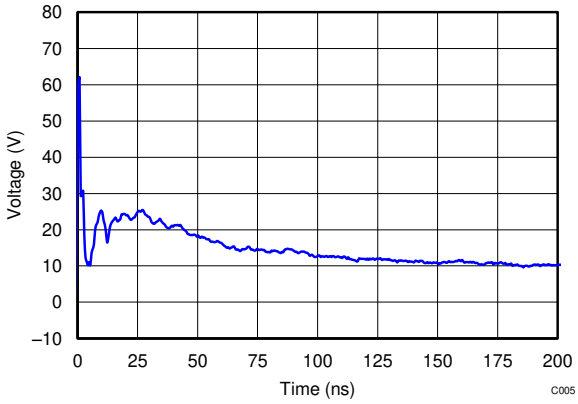


图 6-6. 8-kV IEC Waveform

6.5 Typical Characteristics (continued)

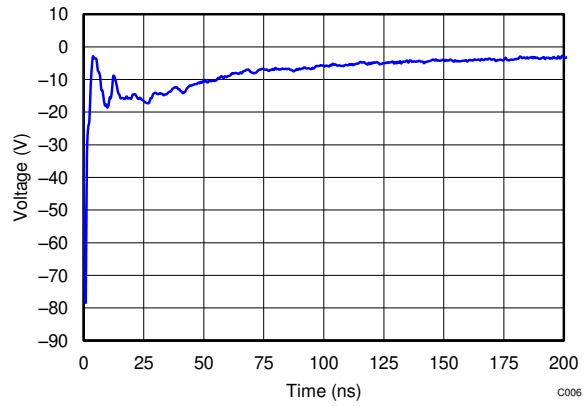


图 6-7. –8-kV IEC Waveform

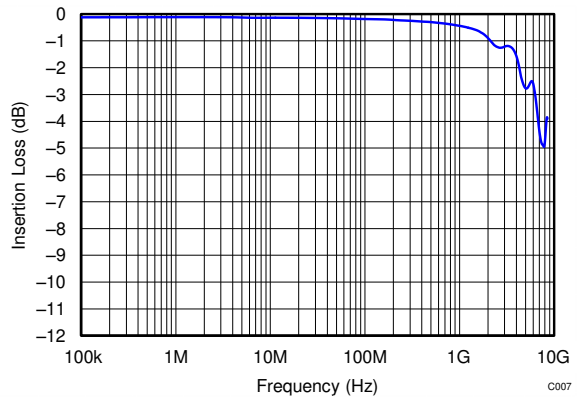


图 6-8. TPD1E05U06 Insertion Loss

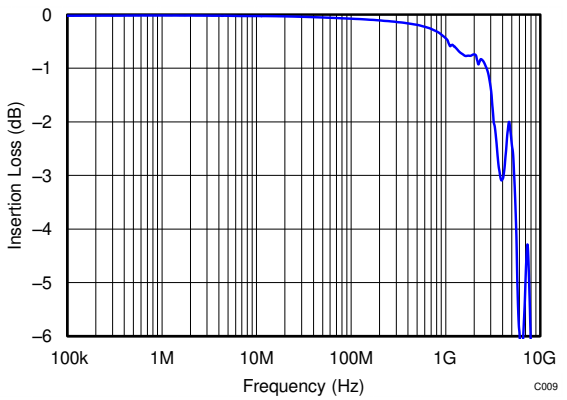


图 6-9. TPD4E05U06 Insertion Loss

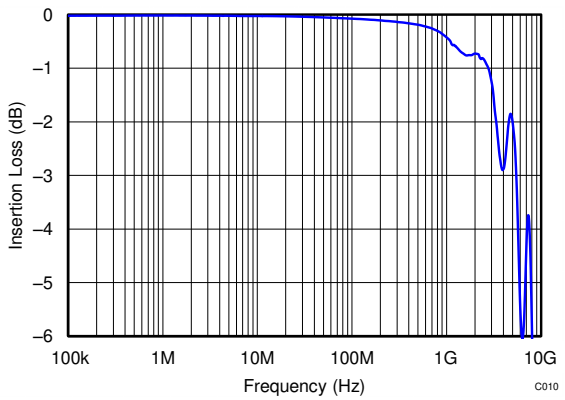


图 6-10. TPD6E05U06 Insertion Loss

7 Detailed Description

7.1 Overview

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

7.2 Functional Block Diagram

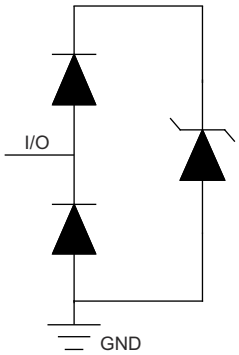


图 7-1. TPD1E05U06 Block Diagram

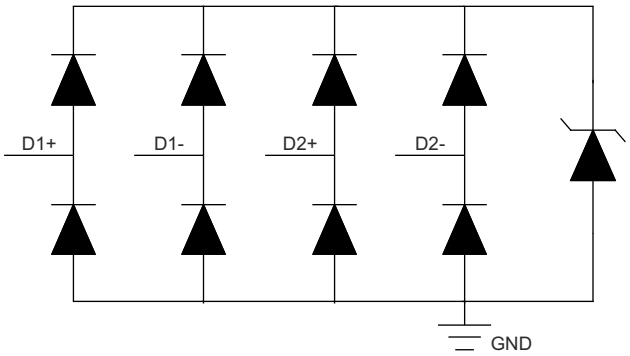


图 7-2. TPD4E05U06 Block Diagram

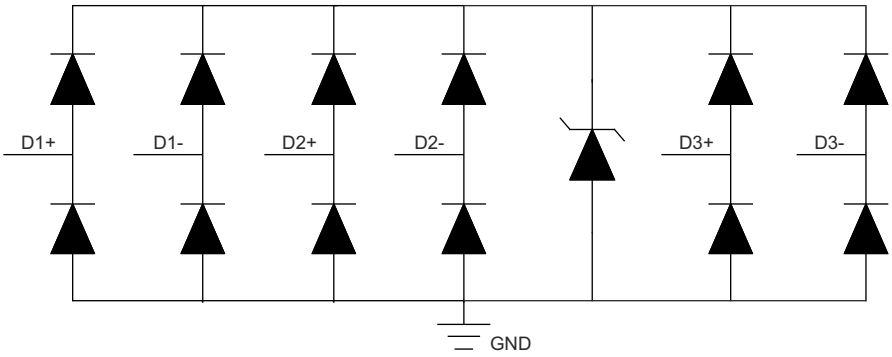


图 7-3. TPD6E05U06 Block Diagram

7.3 Feature Description

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

7.3.1 ±15-kV IEC61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground. This has been validated on the TPD4E05U06 only.

7.3.3 IEC61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 I/O Capacitance

The capacitance between each I/O pin to ground is 0.42 pF (TPD1E05U06), 0.5 pF (TPD4E05U06) or 0.47 pF (TPD6E05U06). These devices support data rates up to 6 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

7.3.6 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of 2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V (I_{PP} = 1 A).

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPDxE05U06 is a passive integrated circuit that triggers when voltages are above VBR or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPDxE05U06 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPDxE05U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Applications

8.2.1 HDMI 2.0 Application

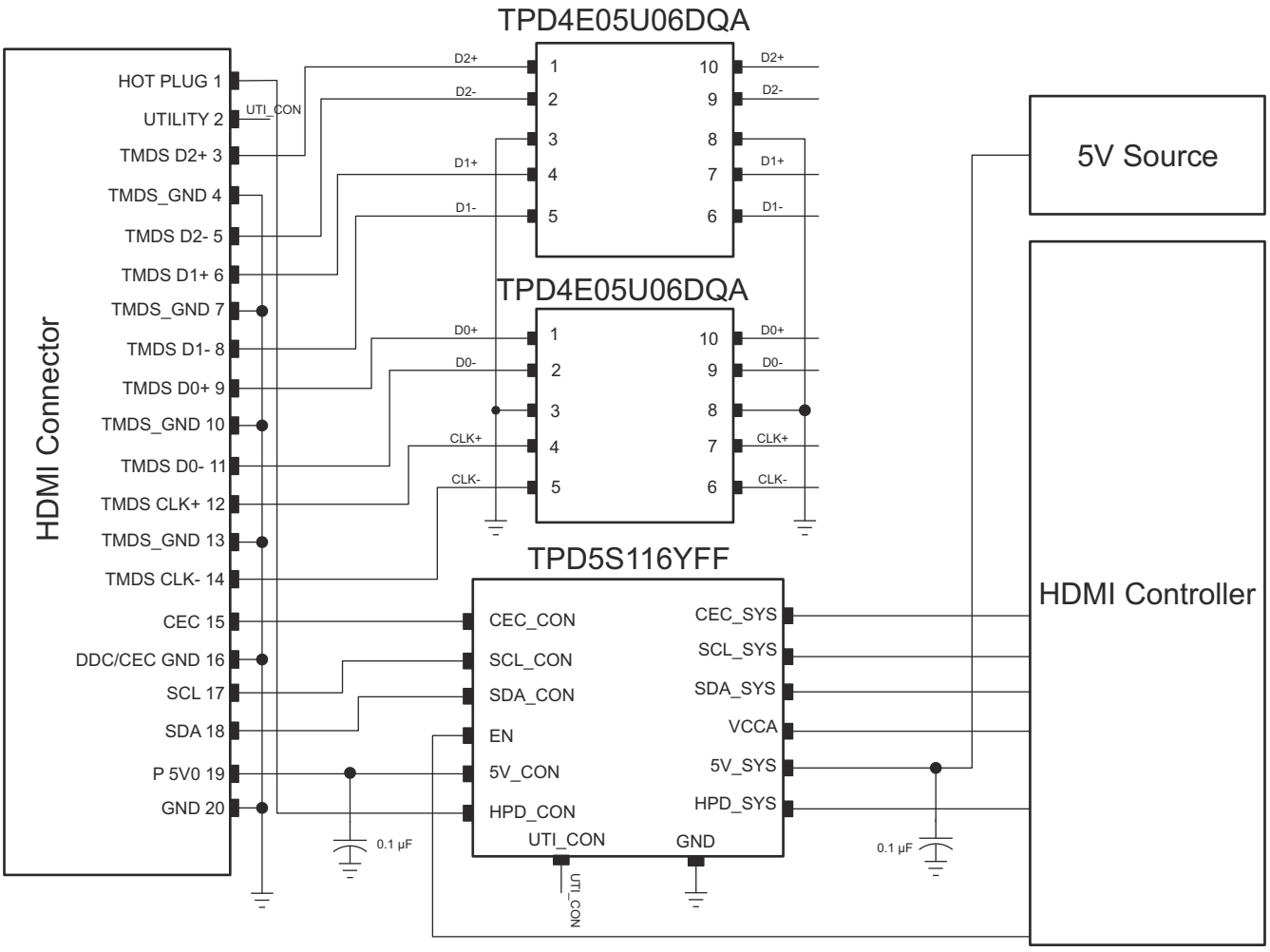


图 8-1. HDMI 2.0 Schematic

8.2.1.1 Design Requirements

For this design example, the two TPD4E05U06 devices, and a TPD5S116 are being used in an HDMI 2.0 application. This provides a complete port protection scheme.

Given the HDMI 2.0 application, the parameters listed in 表 8-1 are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 2, 4, or 5	0 V to 5 V
Operating frequency	3 GHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Signal Range on Pin 1, 2, 4, or 5

The TPD4E05U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels is going to protect which signal lines. Any I/O supports a signal range of 0 to 5.5 V.

8.2.1.3 Application Curves

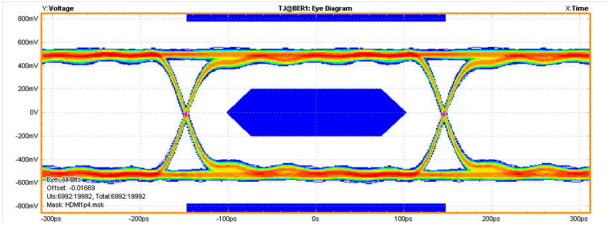


图 8-2. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram Unpopulated EVM

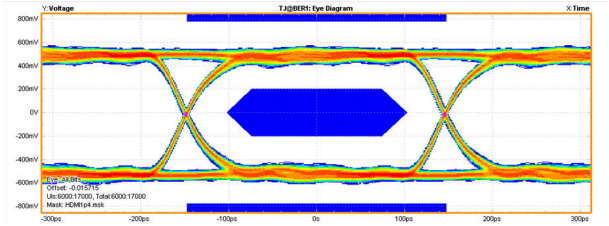


图 8-3. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD1E05U06

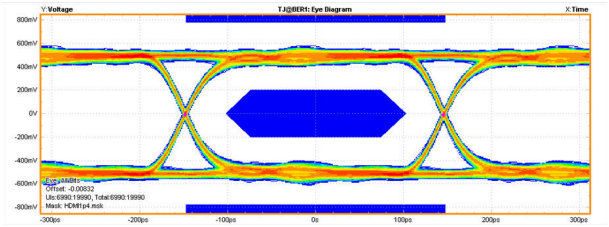


图 8-4. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD4E05U06

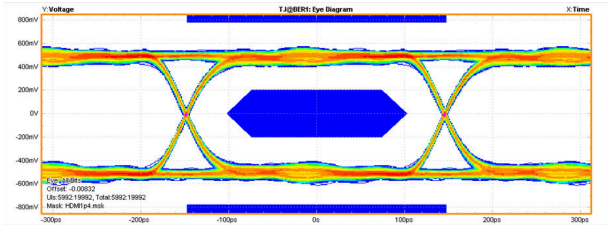


图 8-5. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD6E05U06

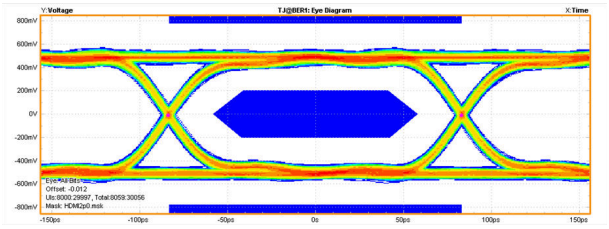


图 8-6. 6-Gbps HDMI 2.0 (TP1) Eye Diagram Unpopulated EVM

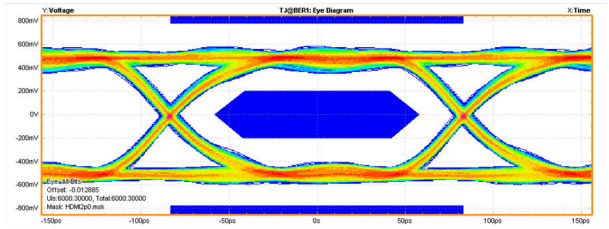


图 8-7. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD1E05U06

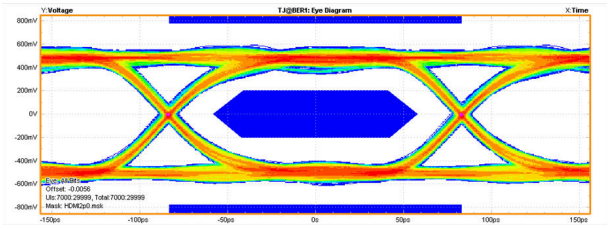


图 8-8. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD4E05U06

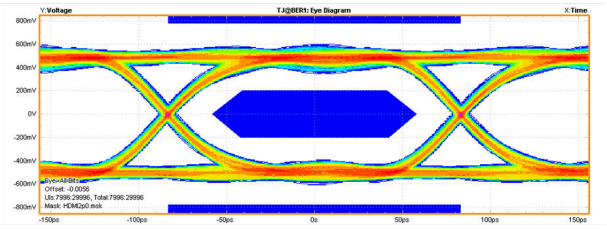


图 8-9. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD6E05U06

8.2.2 HDMI 2.0 Application

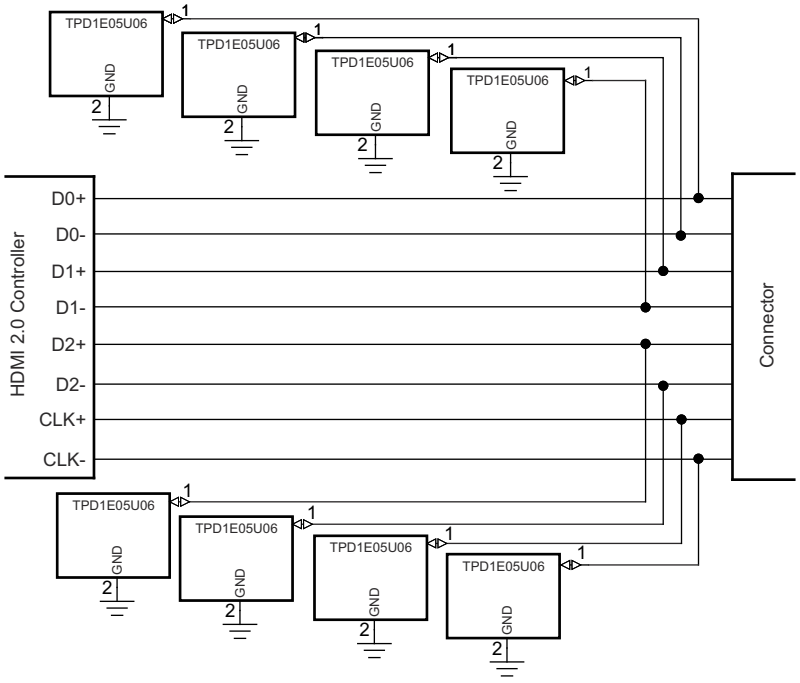


图 8-10. HDMI 2.0 Schematic

8.2.2.1 Design Requirements

For this design example, the TPD1E05U06 and the TPD5S116 are used to protect the data pairs and control lines of the HDMI 2.0 connection. This provides full HDMI 2.0 port protection.

Given the HDMI 2.0 application, the following parameters in 表 8-2 are known.

表 8-2. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on data lines	0 V to 5 V
Operating frequency	3 GHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Signal Range

The TPD1E05U06 has 1 protection channel for signal lines, supporting a signal range of 0 V to 5.5 V.

8.2.2.2.2 Operating Frequency

The TPD1E05U06 has 0.42 pF of capacitance, which supports HDMI 2.0 data rates.

8.2.2.3 Application Curves

Refer to the 节 8.2.1.3 section.

9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care must be taken to make sure that the maximum voltage specifications for each line are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

10.2.1 TPD4E05U06 Layout Example

This application is typical of an HDMI 1.4 layout.

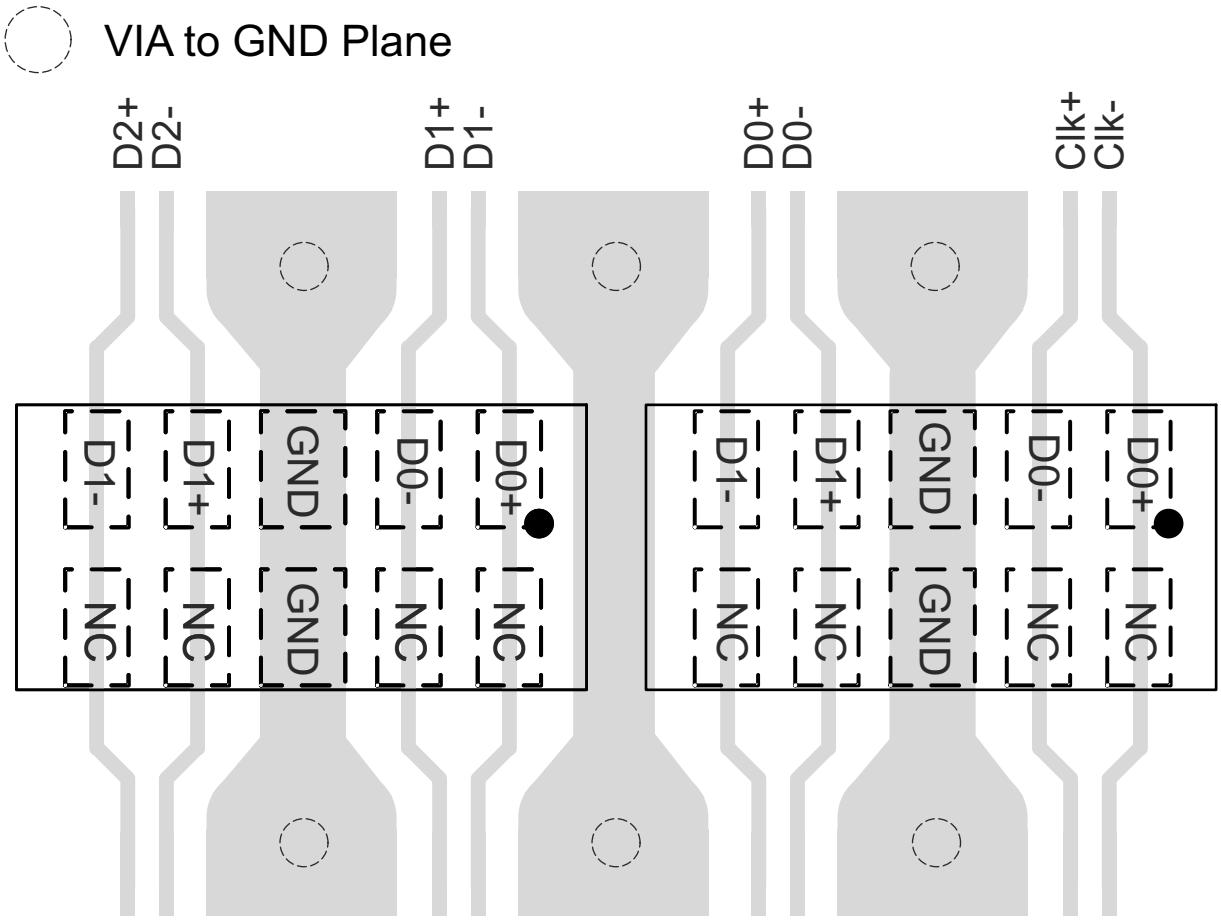


图 10-1. TPD4E05U06 Layout

10.2.2 TPD1E05U06 Layout Example

This application is typical of an HDMI 2.0 layout.

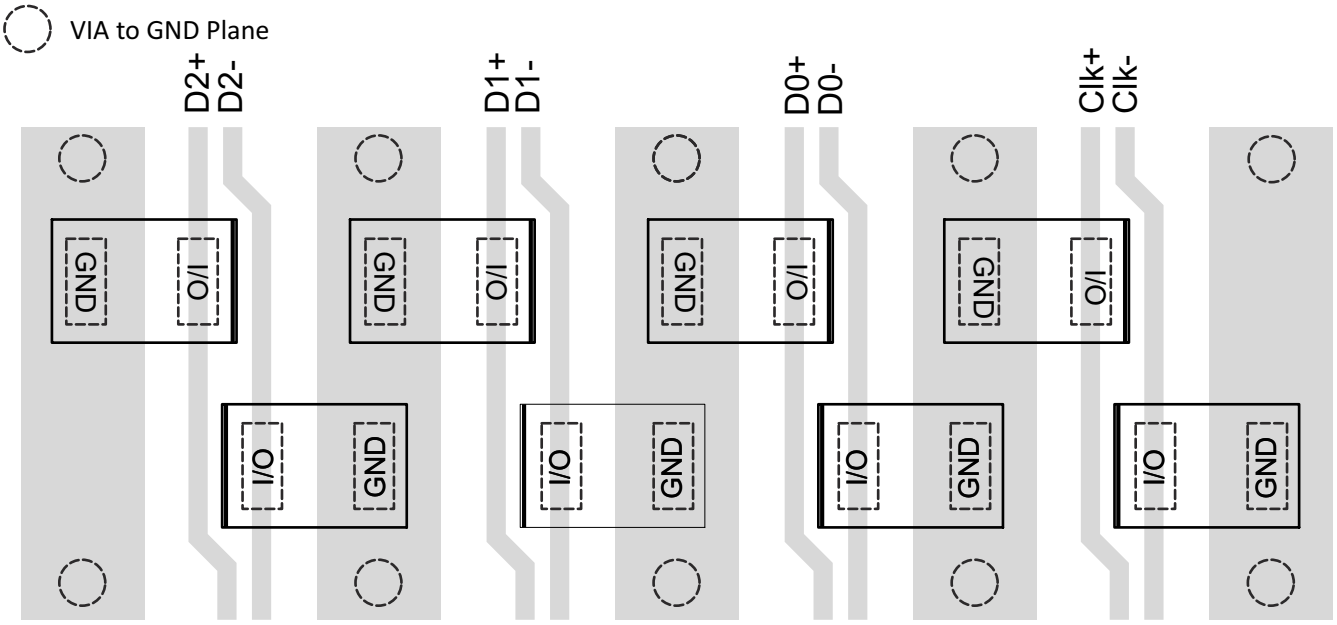


图 10-2. TPD1E05U06 Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet
- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *TPD6E05U06RVZ EVM* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *ESD PROTECTION DIODES EVM* user's guide
- Texas Instruments, *TPD1E05U06DPY EVM* user's guide
- Texas Instruments, *TPD4E05U06DQA EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
PCI-express® and PCI-Express® are registered trademarks of PCI-SIG .
V-by-One® is a registered trademark of Thine Electronics, Inc.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E05U06DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BK, C1, C6) C2	Samples
TPD1E05U06DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BK, C1, C6) C2	Samples
TPD1E05U06DYAR	ACTIVE	SOT-5X3	DYA	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	1KS	Samples
TPD4E05U06DQAR	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BLG, BRG) BRY	Samples
TPD6E05U06RVZR	ACTIVE	USON	RVZ	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BV, BVY)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD1E05U06, TPD4E05U06 :

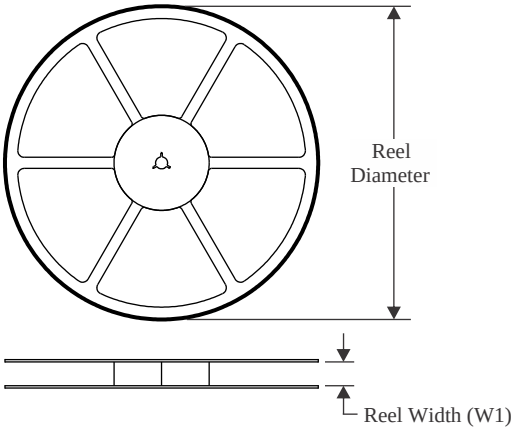
- Automotive : TPD1E05U06-Q1, TPD4E05U06-Q1

NOTE: Qualified Version Definitions:

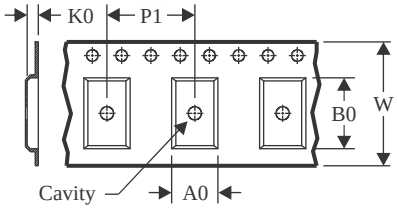
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

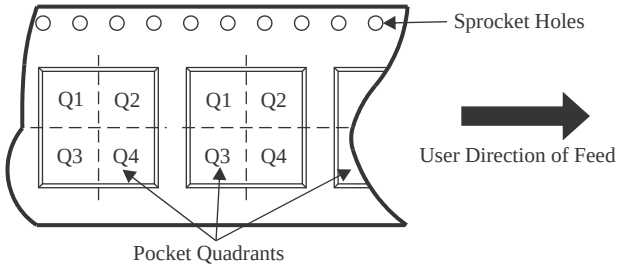


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

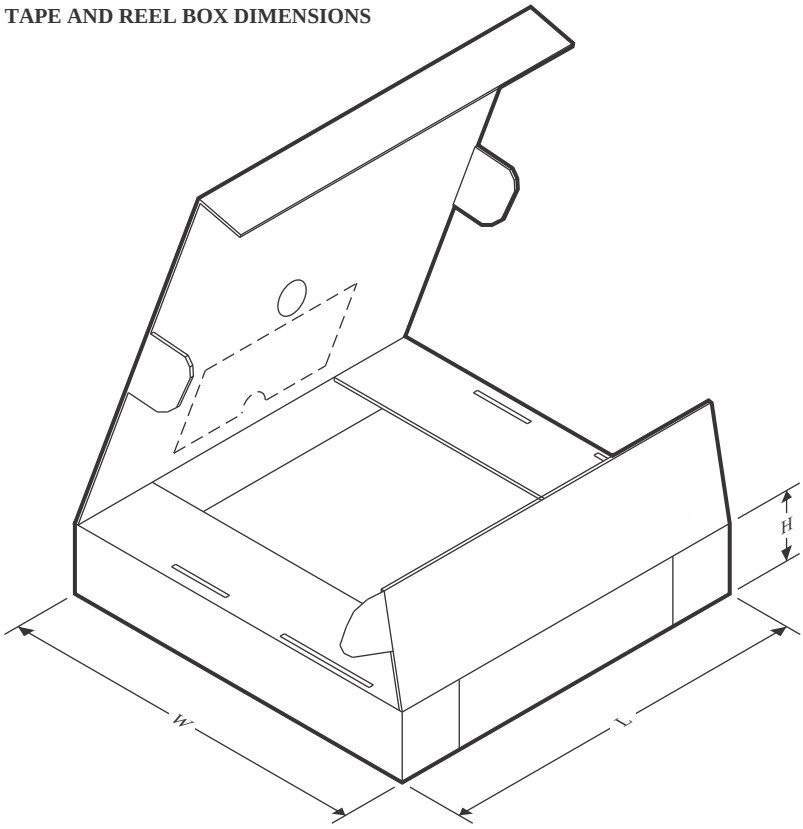
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E05U06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E05U06DPYR	X1SON	DPY	2	10000	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E05U06DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E05U06DPYT	X1SON	DPY	2	250	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E05U06DYAR	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	4.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	8.4	1.23	2.7	0.6	4.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	9.5	1.23	2.7	0.7	4.0	8.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	180.0	13.2	1.65	3.8	0.7	4.0	12.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	178.0	13.5	1.6	3.75	0.7	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

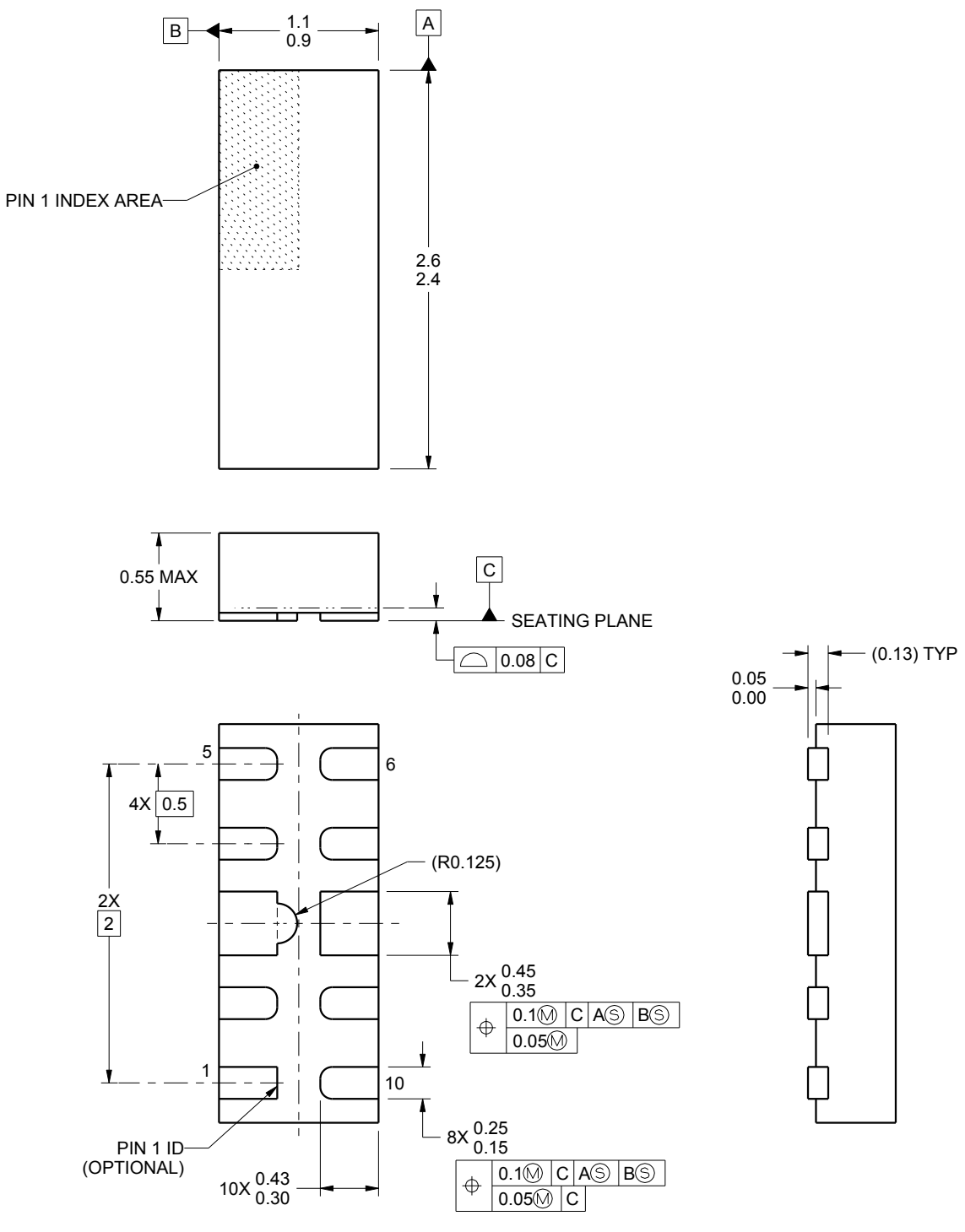
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E05U06DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E05U06DPYR	X1SON	DPY	2	10000	203.2	196.8	33.3
TPD1E05U06DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E05U06DPYT	X1SON	DPY	2	250	203.2	196.8	33.3
TPD1E05U06DYAR	SOT-5X3	DYA	2	3000	210.0	200.0	42.0
TPD4E05U06DQAR	USON	DQA	10	3000	189.0	185.0	36.0
TPD4E05U06DQAR	USON	DQA	10	3000	203.2	196.8	33.3
TPD4E05U06DQAR	USON	DQA	10	3000	184.0	184.0	19.0
TPD6E05U06RVZR	USON	RVZ	14	3000	184.0	184.0	19.0
TPD6E05U06RVZR	USON	RVZ	14	3000	189.0	185.0	36.0

PACKAGE OUTLINE

DQA0010A

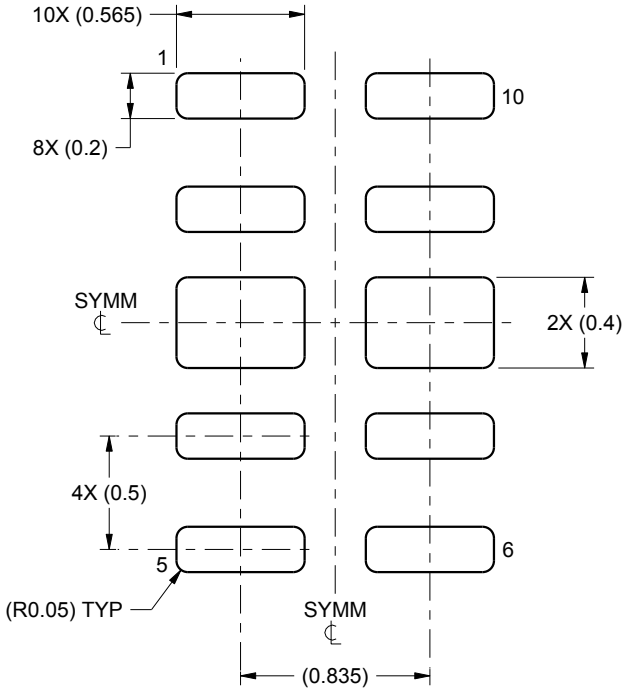
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

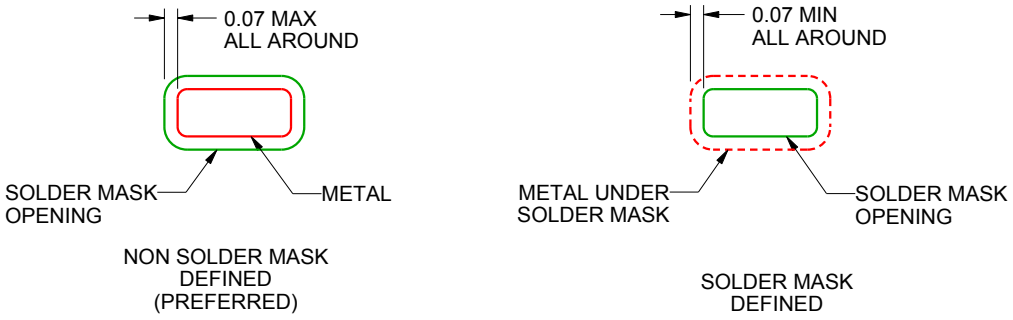


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

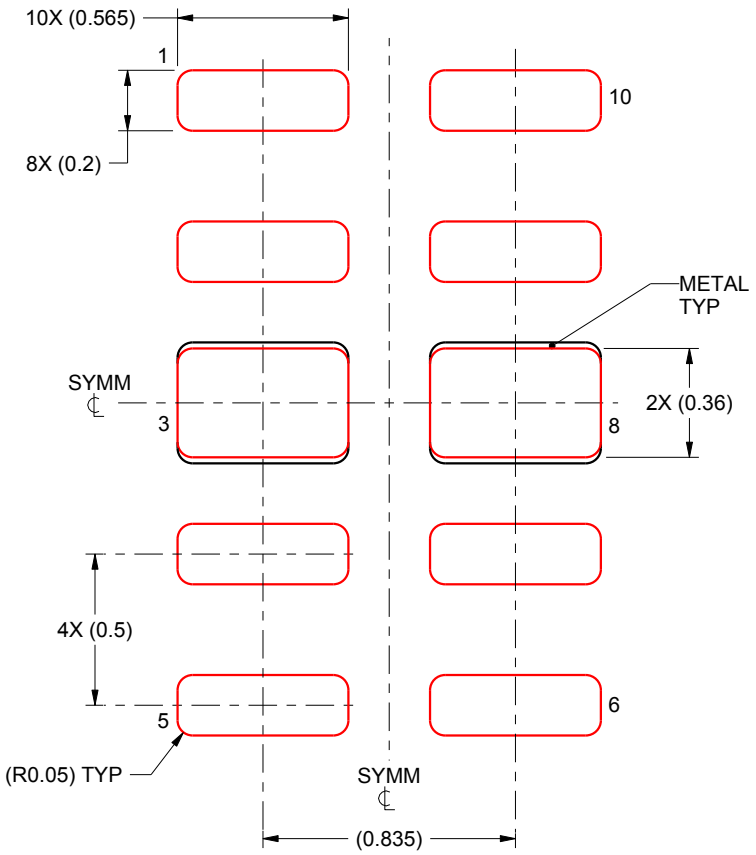
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

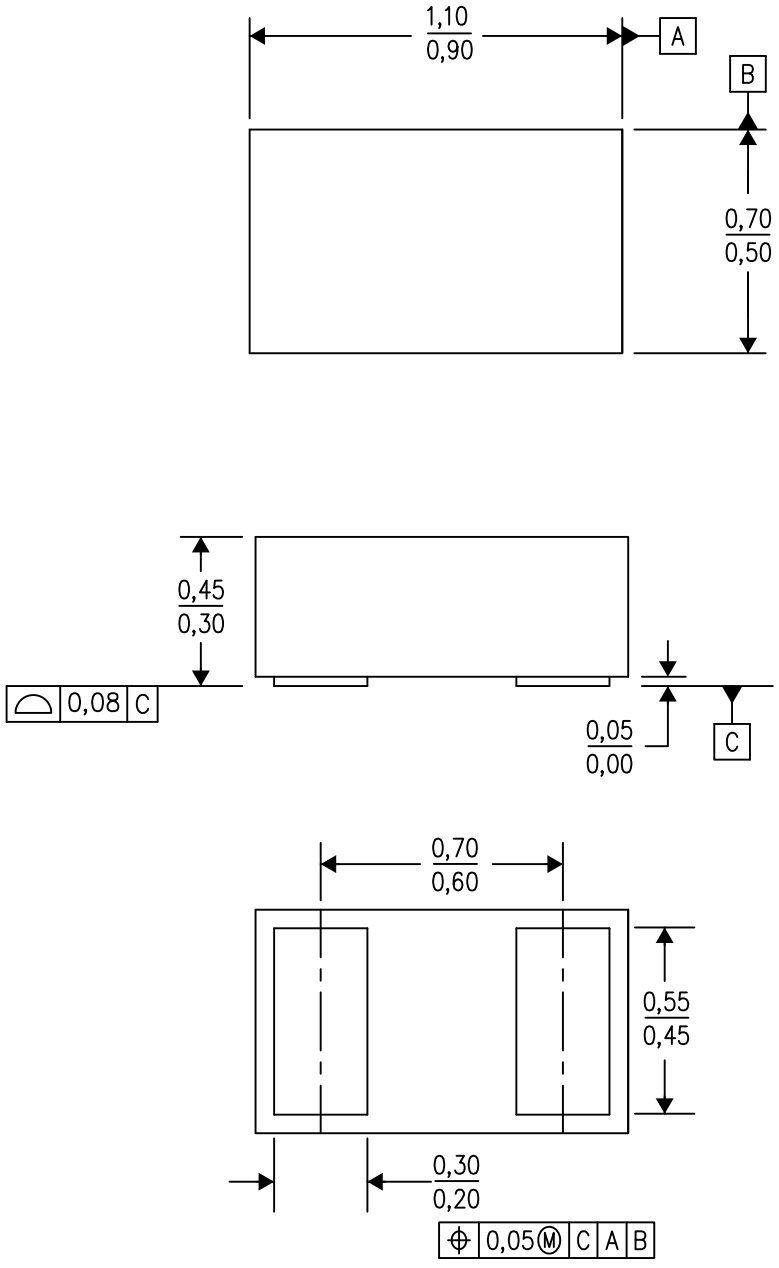
EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

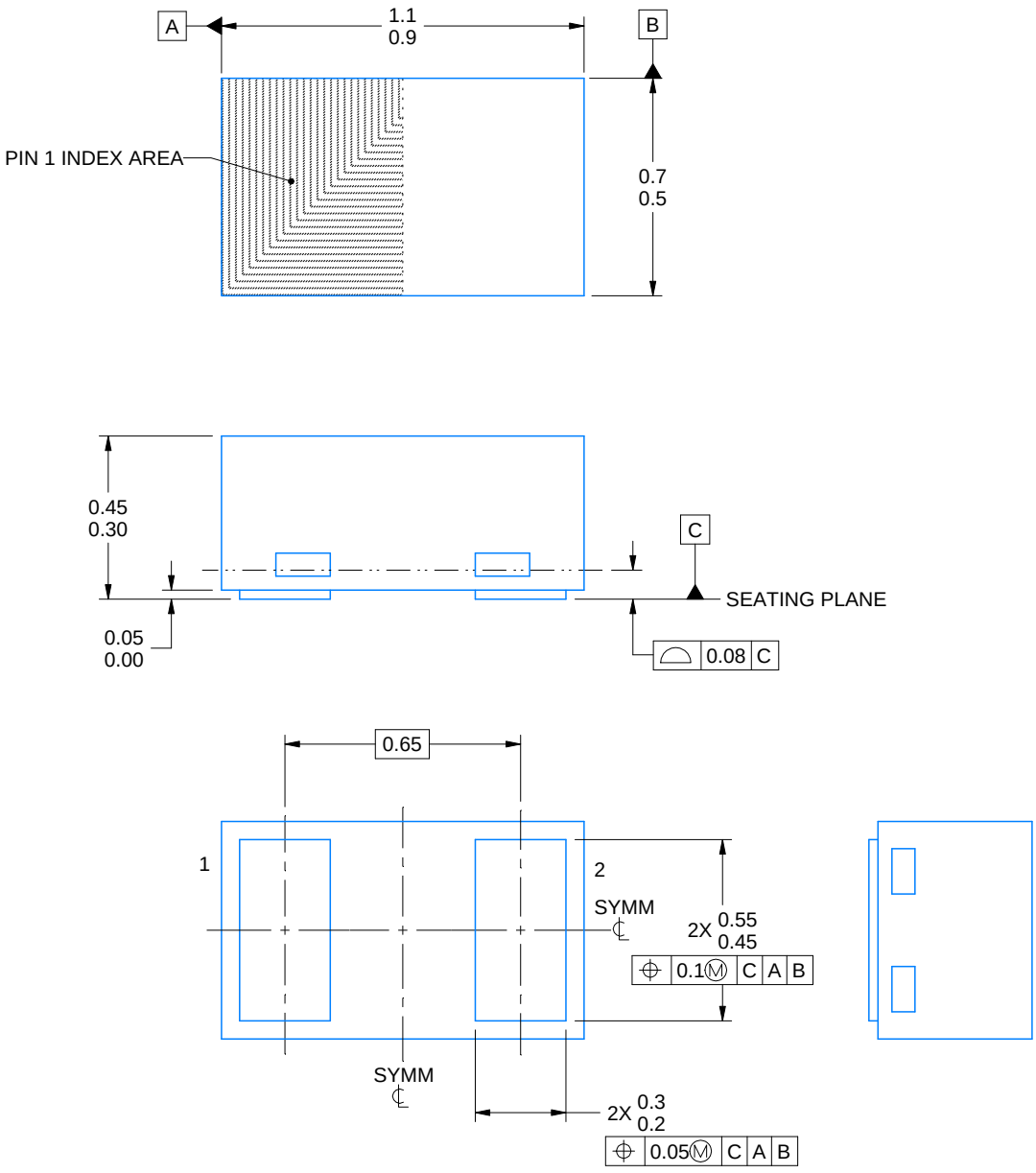
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

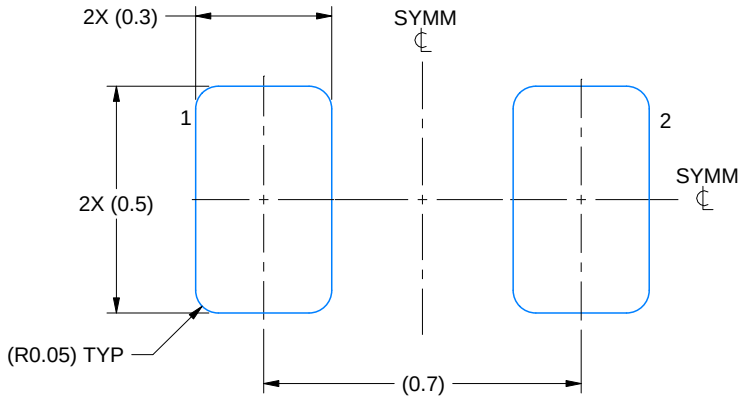
PLASTIC SMALL OUTLINE - NO LEAD



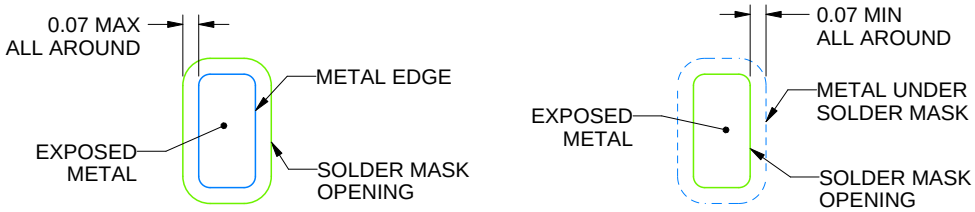
4224561/B 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/B 03/2021

NOTES: (continued)

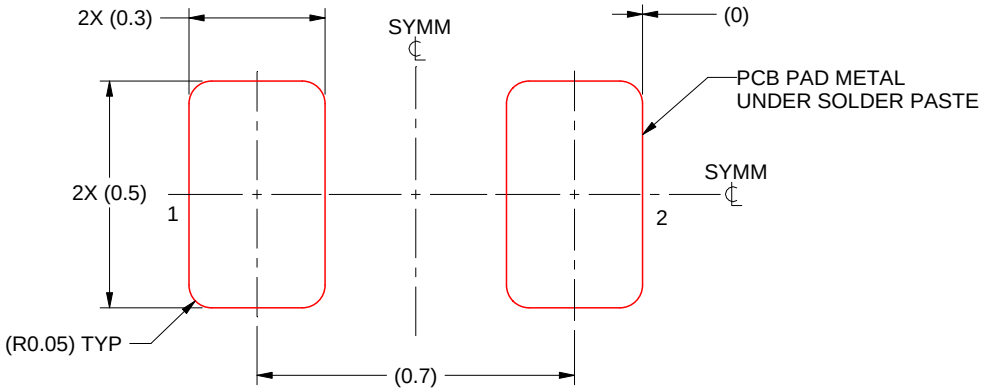
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



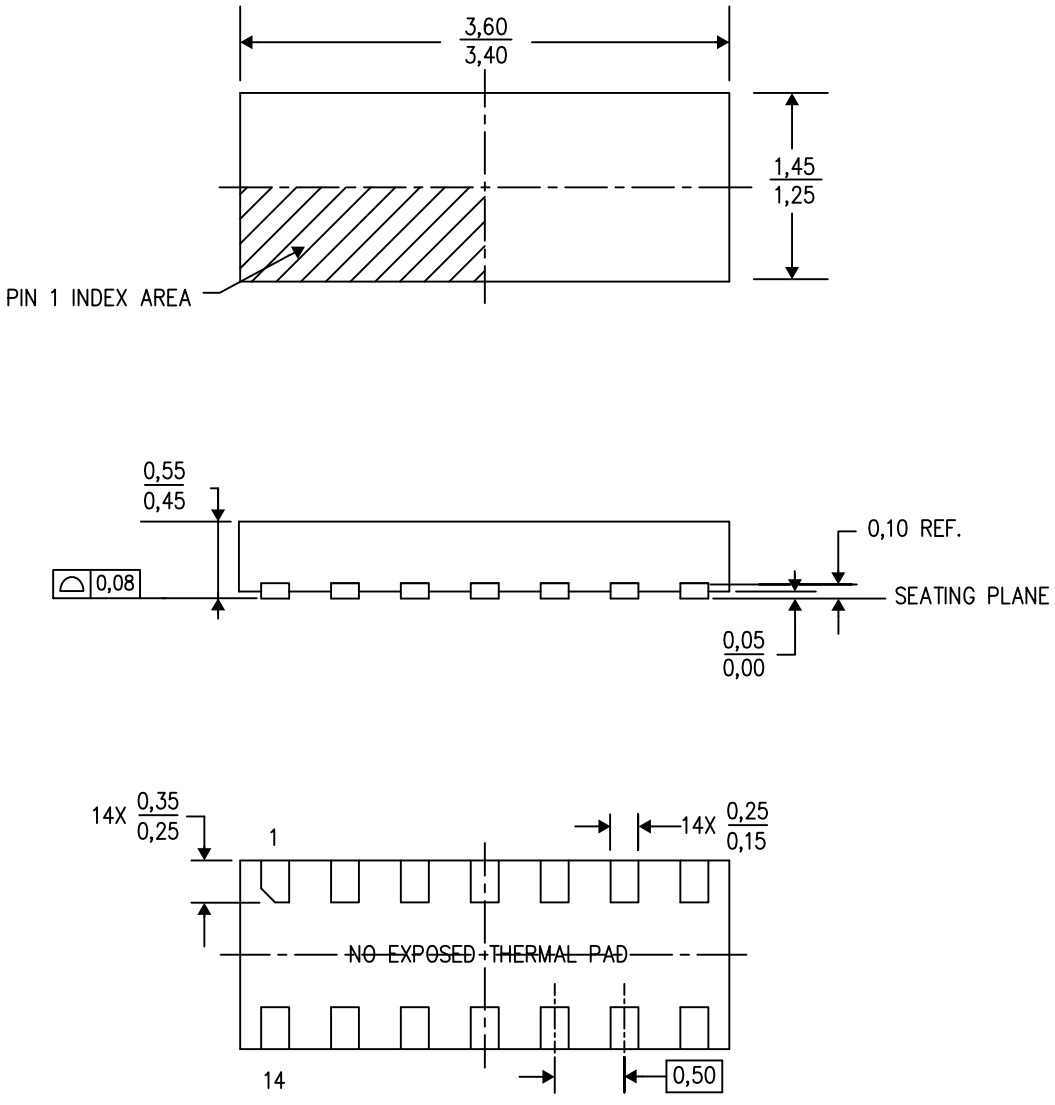
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

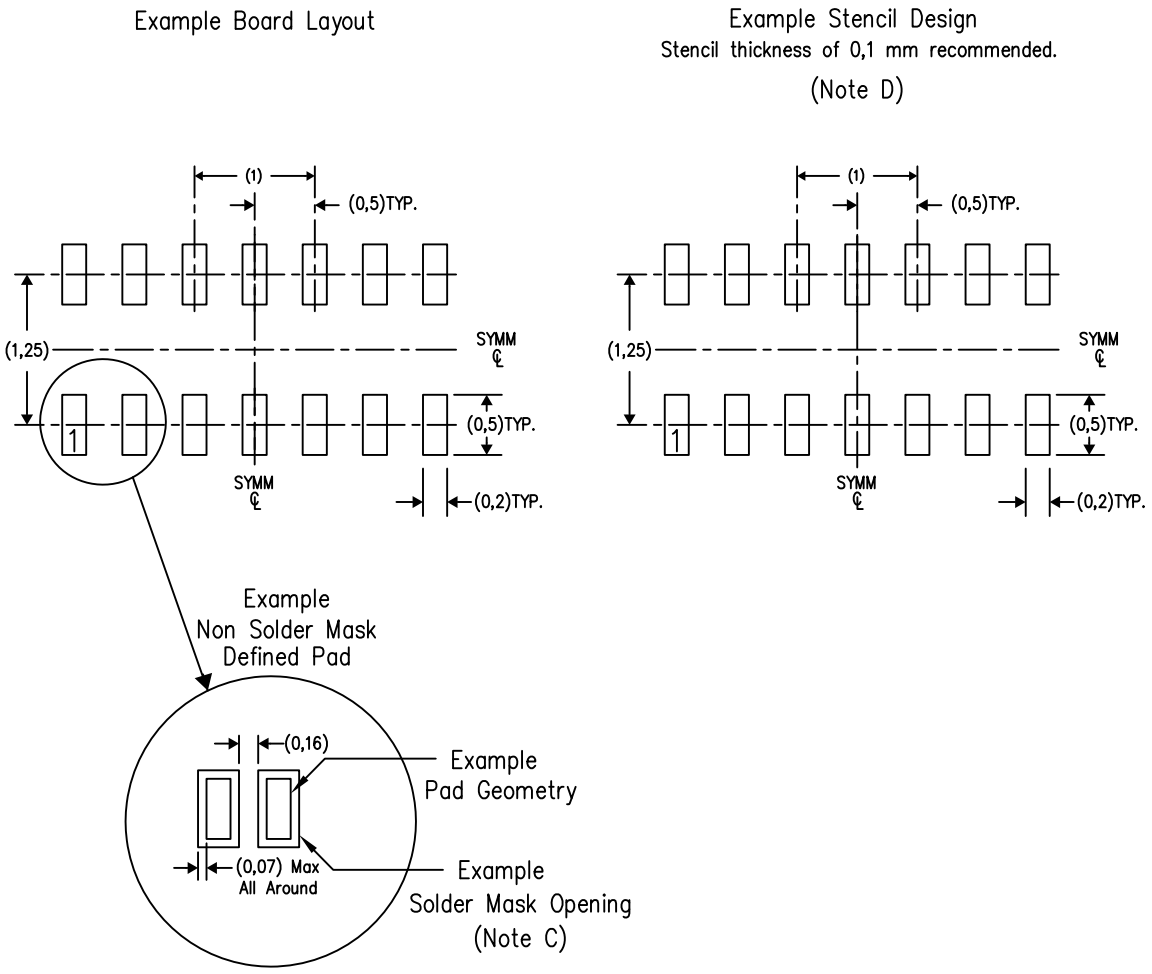
RVZ (R–PUSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



4218112/B 04/14

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RVZ (R–PUSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



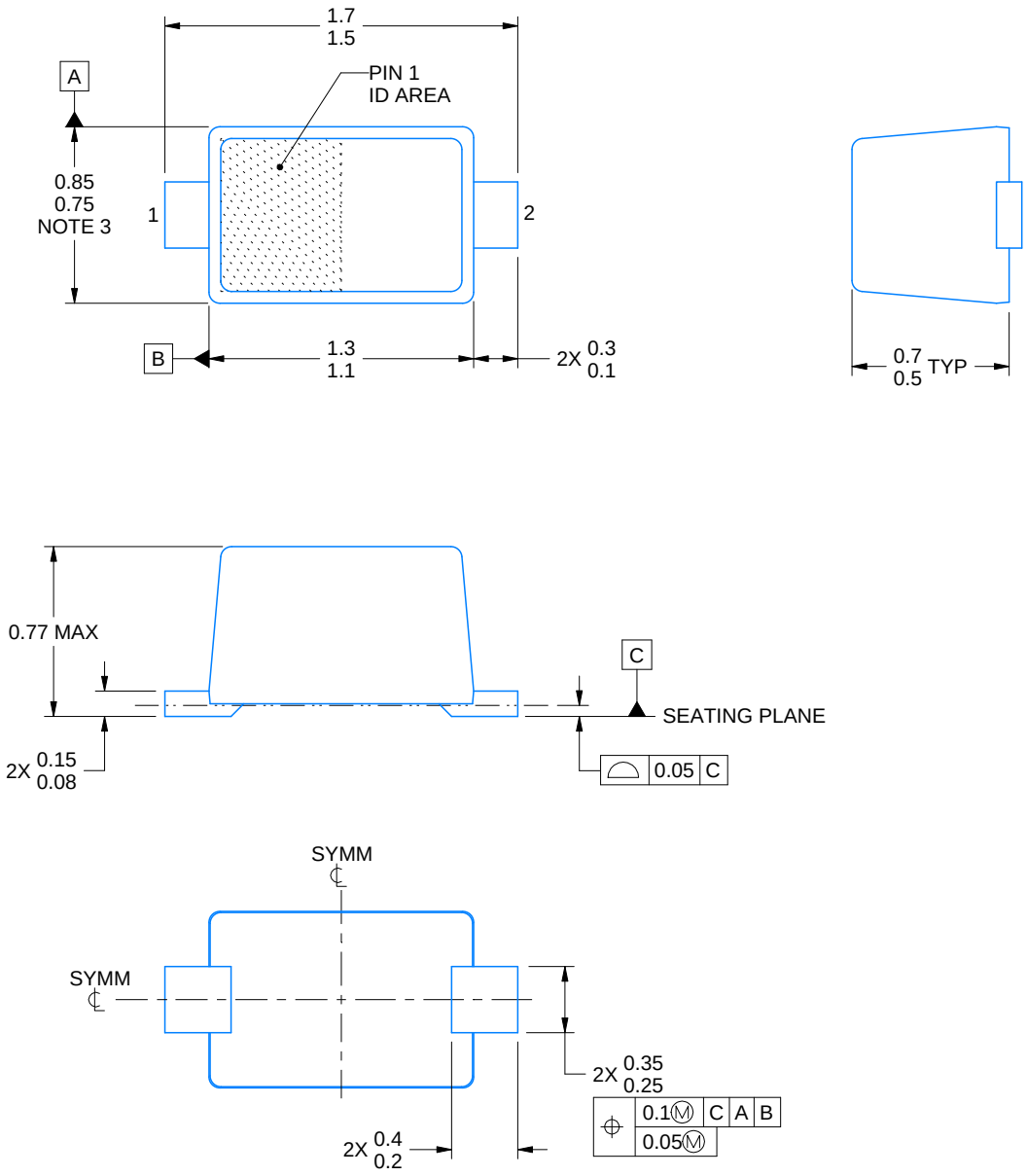
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



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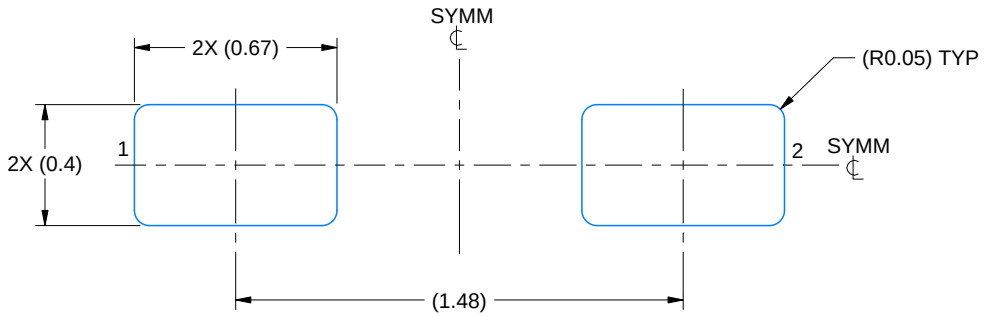
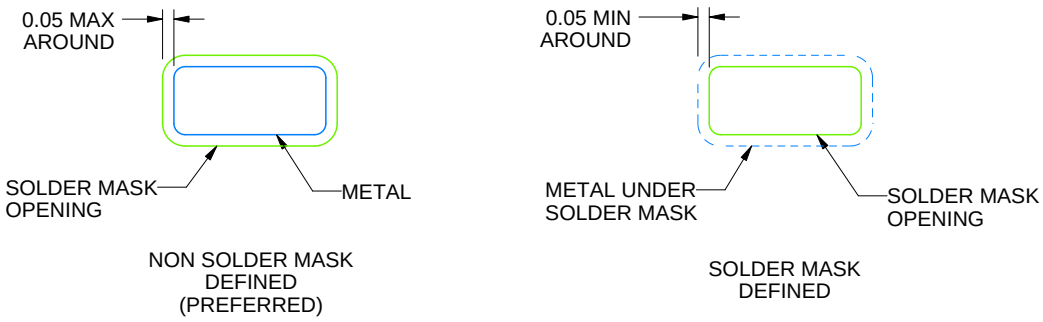
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

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NOTES: (continued)

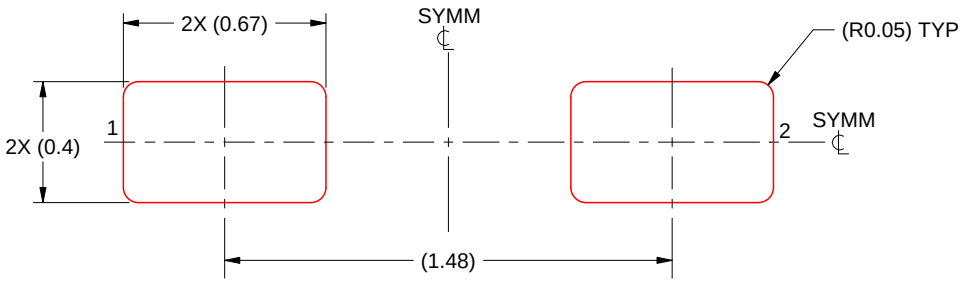
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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