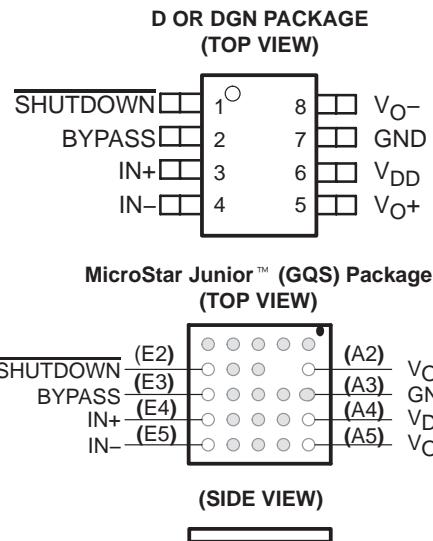


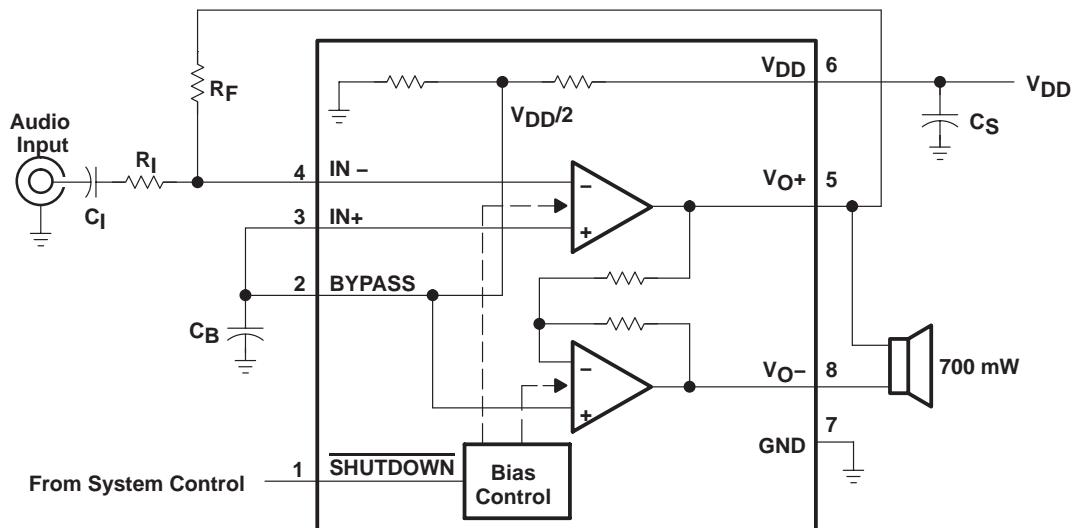
- Fully Specified for 3.3-V and 5-V Operation
- Wide Power Supply Compatibility
2.5 V – 5.5 V
- Power Supply Rejection at 217 Hz
 - 84 dB at $V_{DD} = 5$ V
 - 81 dB at $V_{DD} = 3.3$ V
- Output Power for $R_L = 8 \Omega$
 - 700 mW at $V_{DD} = 5$ V
 - 250 mW at $V_{DD} = 3.3$ V
- Ultralow Supply Current in Shutdown Mode . . . 1.5 nA
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
 - SOIC
 - PowerPAD™ MSOP
 - MicroStar Junior™ (BGA)

description

The TPA751 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA751 can deliver 250-mW of continuous power into a BTL 8- Ω load at less than 0.6% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation is optimized for narrower band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with a supply current of 1.5 nA during shutdown. The TPA751 is available in a 3.0 \times 3.0 mm MicroStar Junior™ (BGA), 8-pin SOIC surface-mount package and a surface-mount PowerPAD™ MSOP.



NOTE: The shaded terminals are used for thermal connections to the ground plane.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD and MicroStar Junior are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TPA751

700-mW MONO LOW-VOLTAGE AUDIO POWER AMPLIFIER WITH DIFFERENTIAL INPUTS

SLOS336C – DECEMBER 2000 – REVISED OCTOBER 2002

AVAILABLE OPTIONS

		PACKAGED DEVICES		
		MicroStar-Junior (BGA)‡ (GQS)	SMALL OUTLINE† (D)	MSOP‡ (DGN)
Device	TPA751GQS	TPA751D	TPA751DGN	
Package symbolization	TPA751	TPA751	ATC	

† In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.

‡ The D, DGN, and GQS packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA751DR).

Terminal Functions

TERMINAL		I/O	DESCRIPTION	
NAME	NO.			
	GQS		D, DGN	
BYPASS	E3	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1- μ F to 2.2- μ F capacitor when used as an audio amplifier.
GND	§	7		GND is the ground connection.
IN –	E5	4	I	IN – is the inverting input. IN – is typically used as the audio input terminal.
IN +	E4	3	I	IN + is the noninverting input. IN + is typically tied to the BYPASS terminal for SE input.
SHUTDOWN	E2	1	I	SHUTDOWN places the entire device in shutdown mode when held low ($I_{DD} = 1.5$ nA).
V _{DD}	A4	6		V _{DD} is the supply voltage terminal.
V _O +	A5	5	O	V _O + is the positive BTL output.
V _O –	A2	8	O	V _O – is the negative BTL output.

§ A1, A3, A5, B1–B5, C1–C5, D1–D5 are electrical and thermal connections to the ground plane.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)¶

Supply voltage, V _{DD}	6 V
Input voltage, V _I	-0.3 V to V _{DD} +0.3 V
Continuous total power dissipation	Internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T _A	-40°C to 85°C
Operating junction temperature range, T _J	-40°C to 150°C
Storage temperature range, T _{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

¶ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A = 25°C	DERATING FACTOR	T _A = 70°C	T _A = 85°C
GQS	1.66 W	13.3 mW/°C	1.06 W	866 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W#	17.1 mW/°C	1.37 W	1.11 W

See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of that document.

|| See the Texas Instruments document, *MicroStar Junior™ Made Easy Application Brief* (SSYA009A) for board layout information on the MicroStar Junior package.

TPA751
700-mW MONO LOW-VOLTAGE AUDIO POWER AMPLIFIER
WITH DIFFERENTIAL INPUTS
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recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
High-level input voltage, V_{IH} , (SHUTDOWN)	0.9 V_{DD}		V
Low-level input voltage, V_{IL} , (SHUTDOWN)		0.1 V_{DD}	V
Operating free-air temperature, T_A	-40	85	°C

electrical characteristics at specified free-air temperature, $V_{DD} = 3.3$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OSl} $	SHUTDOWN = V_{DD} , $R_L = 8 \Omega$, $RF = 10 \text{ k}\Omega$		20		mV
PSRR	$V_{DD} = 3.2$ V to 3.4 V		85		dB
I_{DD}	SHUTDOWN = V_{DD} , $RF = 10 \text{ k}\Omega$		1.25	2.5	mA
$I_{DD(\text{SD})}$	SHUTDOWN = 0 V, $RF = 10 \text{ k}\Omega$		1.5	1000	nA
$ I_{IH} $	SHUTDOWN, $V_{DD} = 3.3$ V, $V_i = V_{DD}$		1		µA
$ I_{IL} $	SHUTDOWN, $V_{DD} = 3.3$ V, $V_i = 0$ V		1		µA

operating characteristics, $V_{DD} = 3.3$ V, $T_A = 25^\circ\text{C}$, $R_L = 8 \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	THD = 0.2%, See Figure 9	250			mW
THD + N	$P_O = 250$ mW, $f = 200$ Hz to 4 kHz, See Figure 7	0.55%			
B_{OM}	$A_V = -2$ V/V, THD = 2%, See Figure 7	20			kHz
B_1	Unity-gain bandwidth	1.4			MHz
	Open loop, See Figure 15				
	Supply ripple rejection ratio	79			dB
V_n	$A_V = -1$ V/V, $C_B = 0.1 \mu\text{F}$, See Figure 19	17			µV(rms)

NOTE 1: Output power is measured at the output terminals of the device at $f = 1$ kHz.

electrical characteristics at specified free-air temperature, $V_{DD} = 5$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OSl} $	SHUTDOWN = V_{DD} , $R_L = 8 \Omega$, $RF = 10 \text{ k}\Omega$		20		mV
PSRR	$V_{DD} = 4.9$ V to 5.1 V		78		dB
I_{DD}	SHUTDOWN = V_{DD} , $RF = 10 \text{ k}\Omega$		1.45	2.5	mA
$I_{DD(\text{SD})}$	SHUTDOWN = 0 V, $RF = 10 \text{ k}\Omega$		5	1500	nA
$ I_{IH} $	SHUTDOWN, $V_{DD} = 5.5$ V, $V_i = V_{DD}$		1		µA
$ I_{IL} $	SHUTDOWN, $V_{DD} = 5.5$ V, $V_i = 0$ V		1		µA

operating characteristics, $V_{DD} = 5$ V, $T_A = 25^\circ\text{C}$, $R_L = 8 \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	THD = 0.5%, See Figure 13	700†			mW
THD + N	$P_O = 250$ mW, $f = 200$ Hz to 4 kHz, See Figure 11	0.5%			
B_{OM}	$A_V = -2$ V/V, THD = 2%, See Figure 11	20			kHz
B_1	Unity-gain bandwidth	1.4			MHz
	Open loop, See Figure 16				
	Supply ripple rejection ratio	80			dB
V_n	$A_V = -1$ V/V, $C_B = 0.1 \mu\text{F}$, See Figure 20	17			µV(rms)

† The GQS and DGN packages, properly mounted, can conduct 700 mW RMS power continuously. The D package, can only conduct 350 mW RMS power continuously, with peaks to 700 mW.

PARAMETER MEASUREMENT INFORMATION

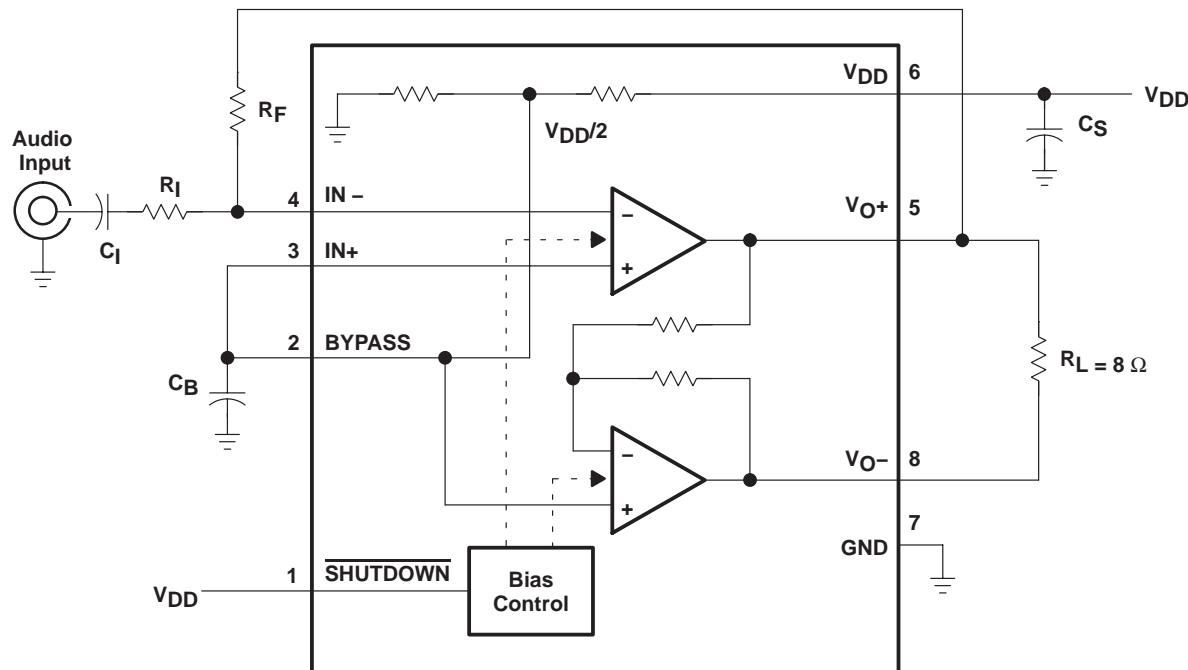


Figure 1. BTL Mode Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
ksvr	Supply ripple rejection ratio	vs Frequency 2	
IDD	Supply current	vs Supply voltage 3, 4	
PO	Output power	vs Supply voltage 5	
		vs Load resistance 6	
THD+N	Total harmonic distortion plus noise	vs Frequency 7, 8, 11, 12	
		vs Output power 9, 10, 13, 14	
Open loop gain and phase		vs Frequency 15, 16	
Closed loop gain and phase		vs Frequency 17, 18	
Vn	Output noise voltage	vs Frequency 19, 20	
PD	Power dissipation	vs Output power 21, 22	

TYPICAL CHARACTERISTICS

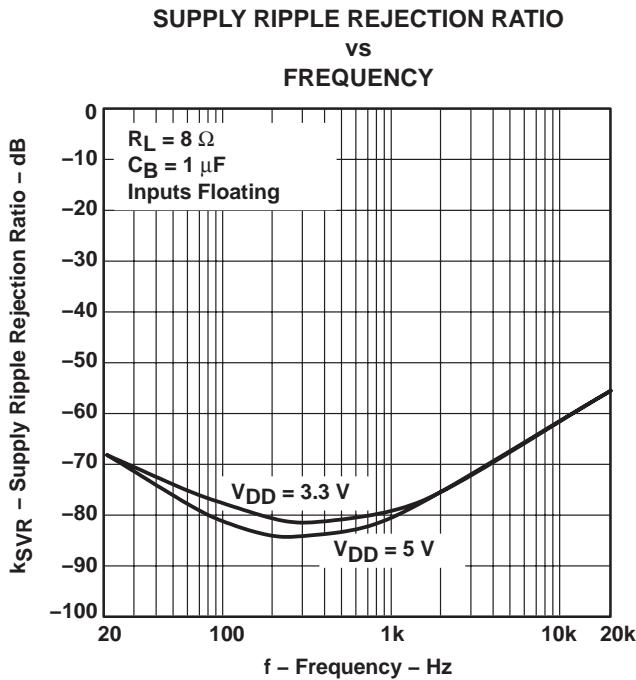


Figure 2

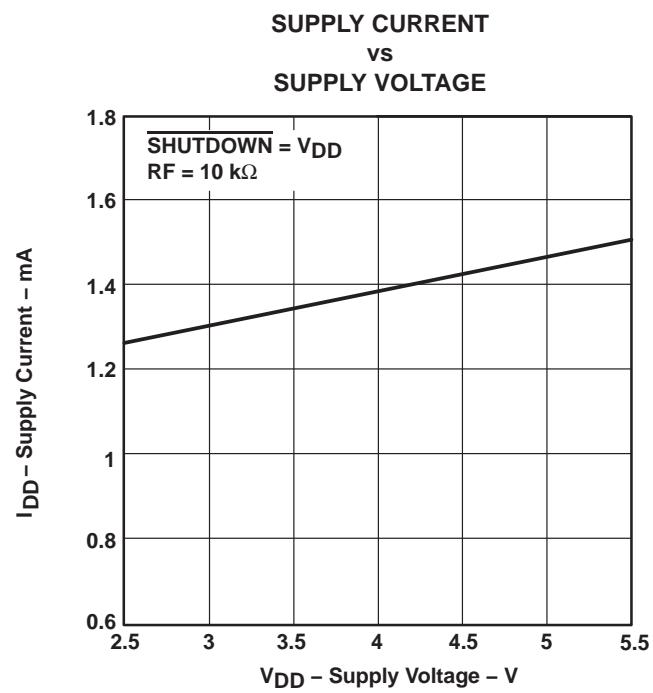


Figure 3

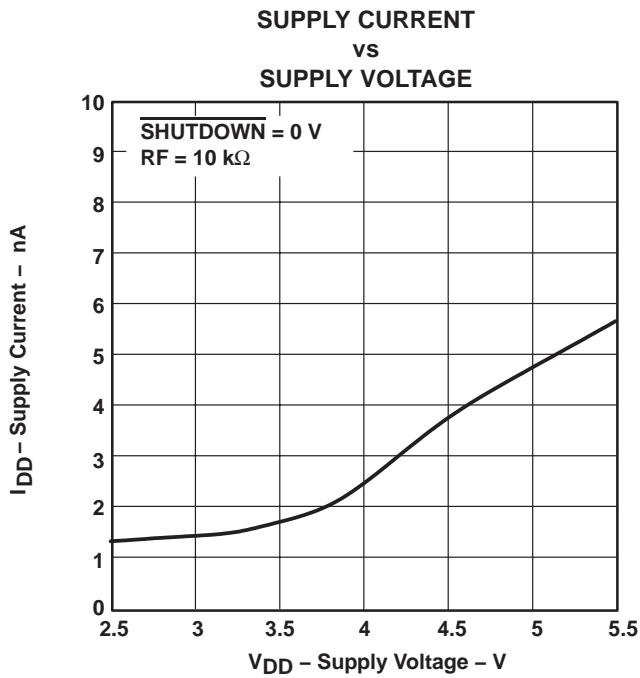


Figure 4

TYPICAL CHARACTERISTICS

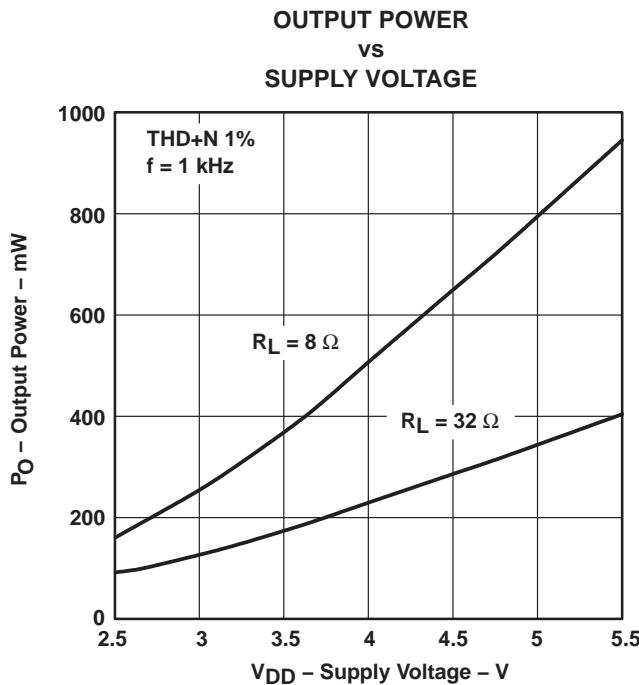


Figure 5

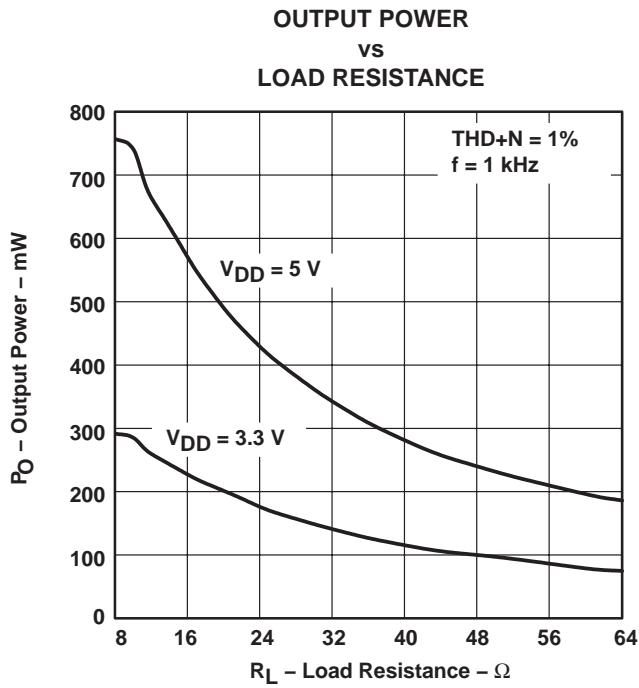


Figure 6

TYPICAL CHARACTERISTICS

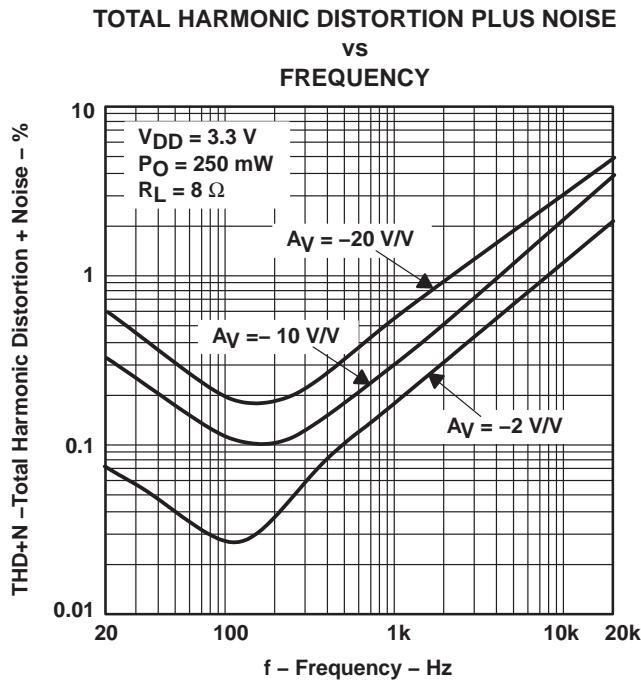


Figure 7

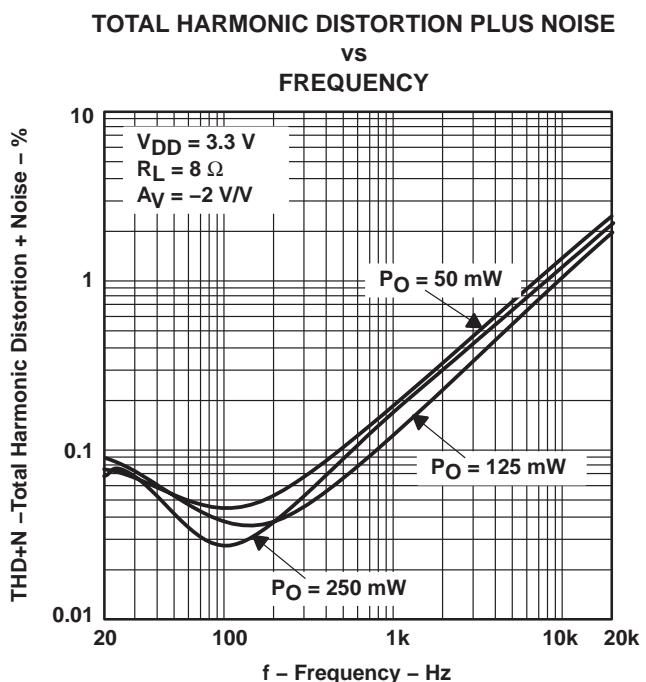


Figure 8

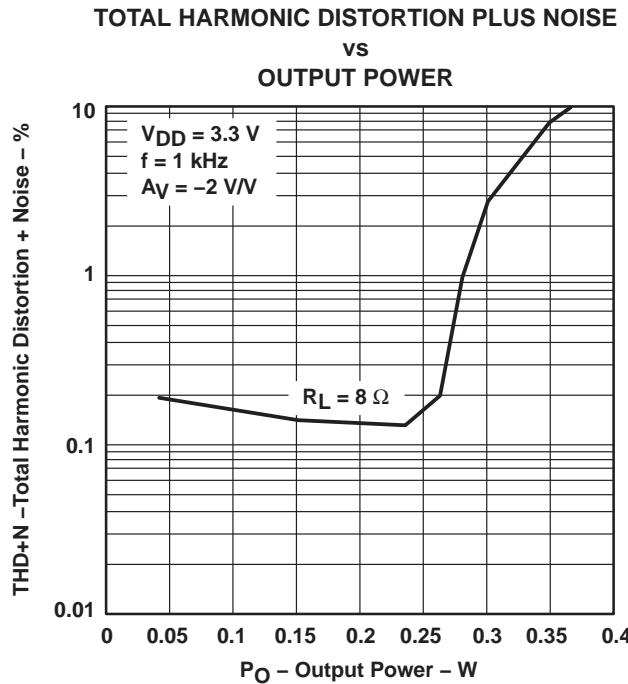


Figure 9

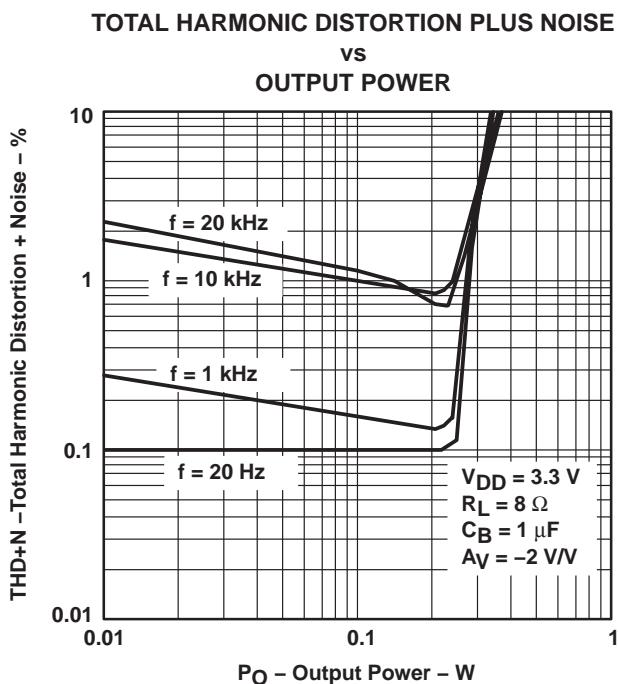


Figure 10

TYPICAL CHARACTERISTICS

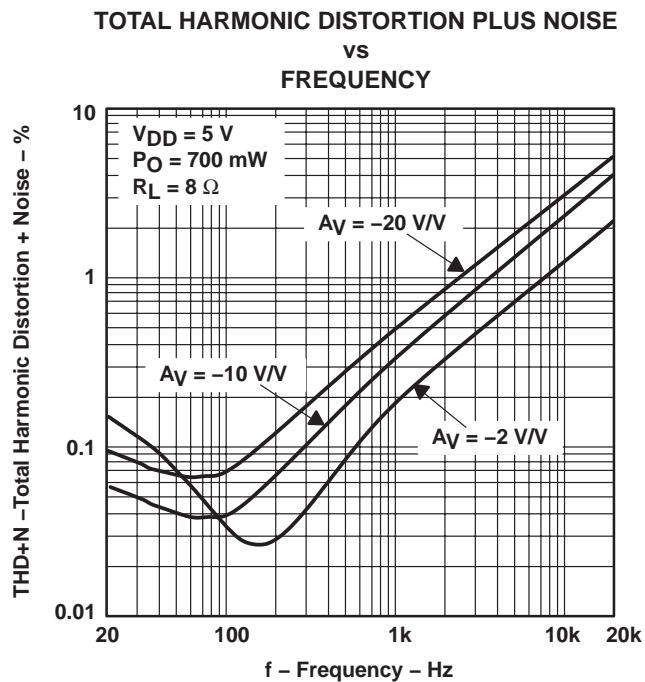


Figure 11

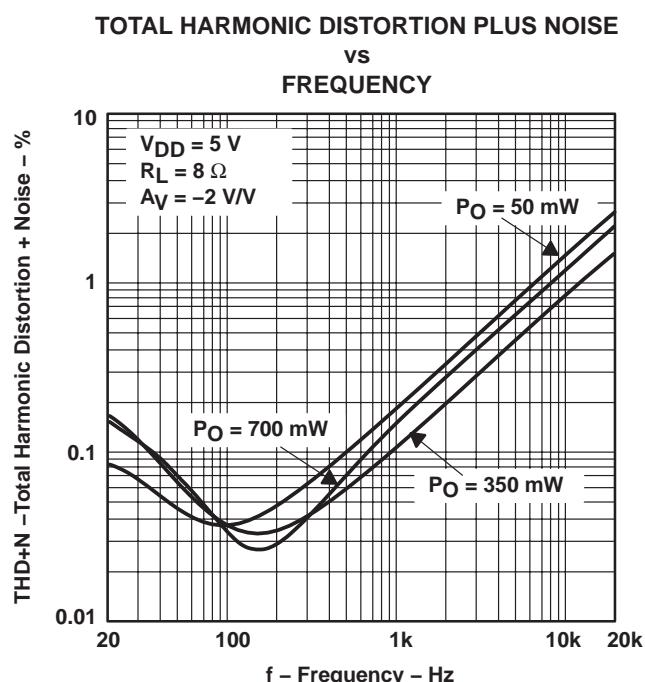


Figure 12

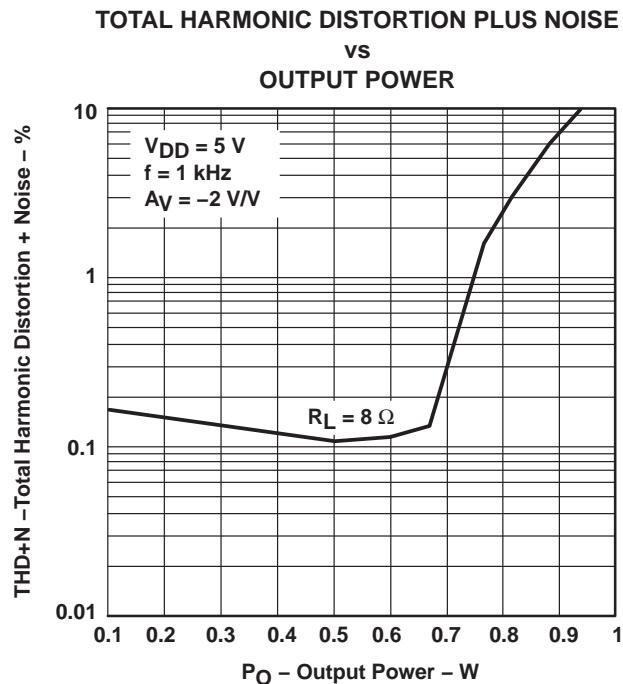


Figure 13

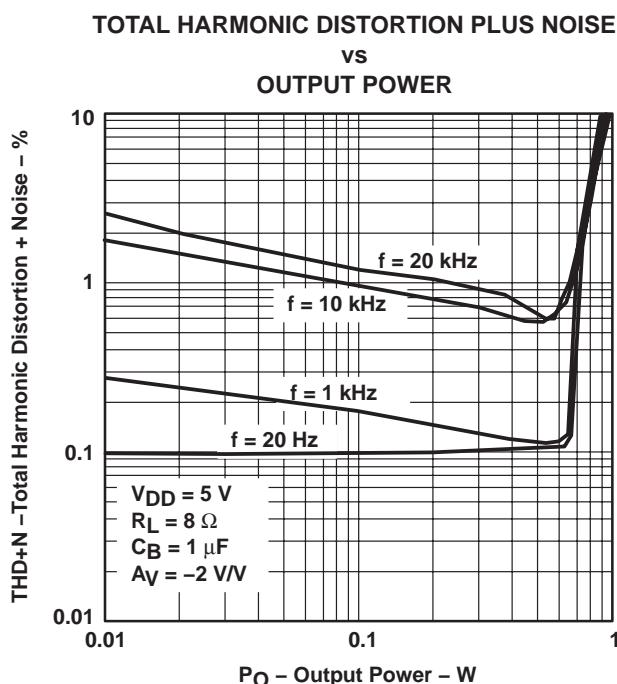


Figure 14

TYPICAL CHARACTERISTICS

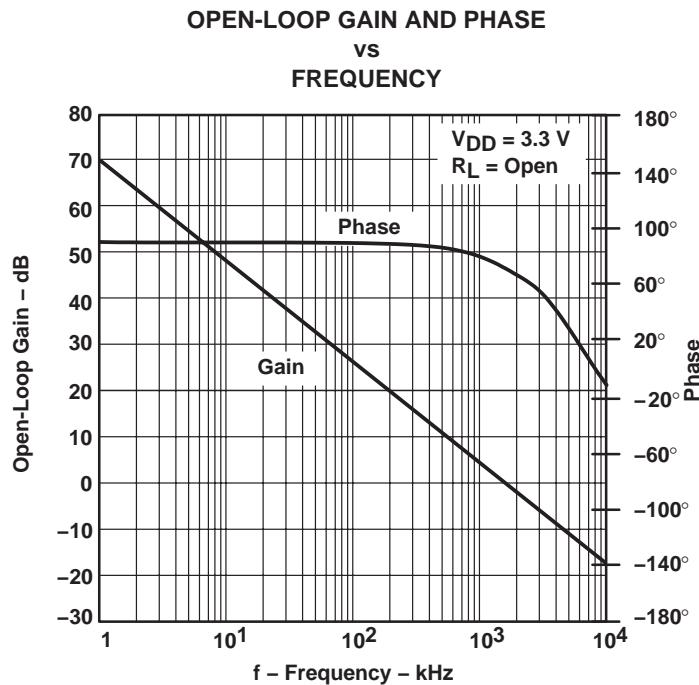


Figure 15

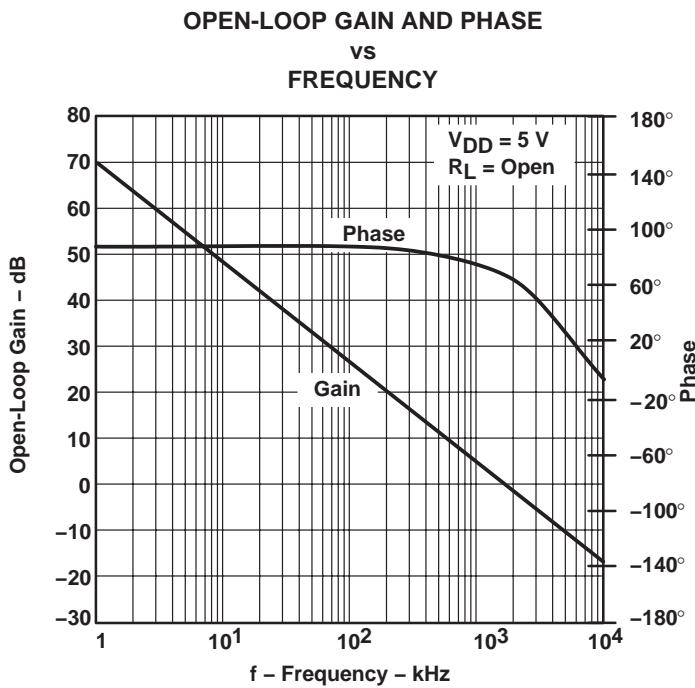


Figure 16

TYPICAL CHARACTERISTICS

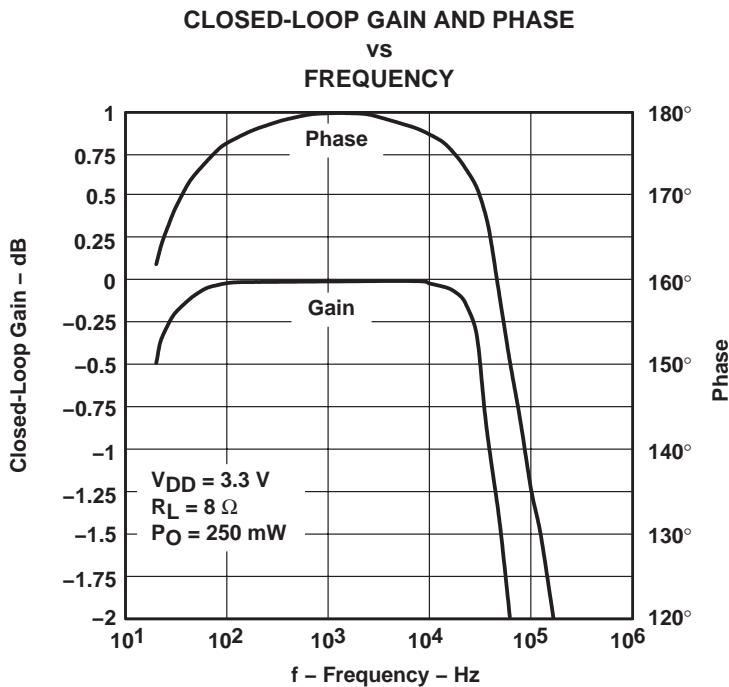


Figure 17

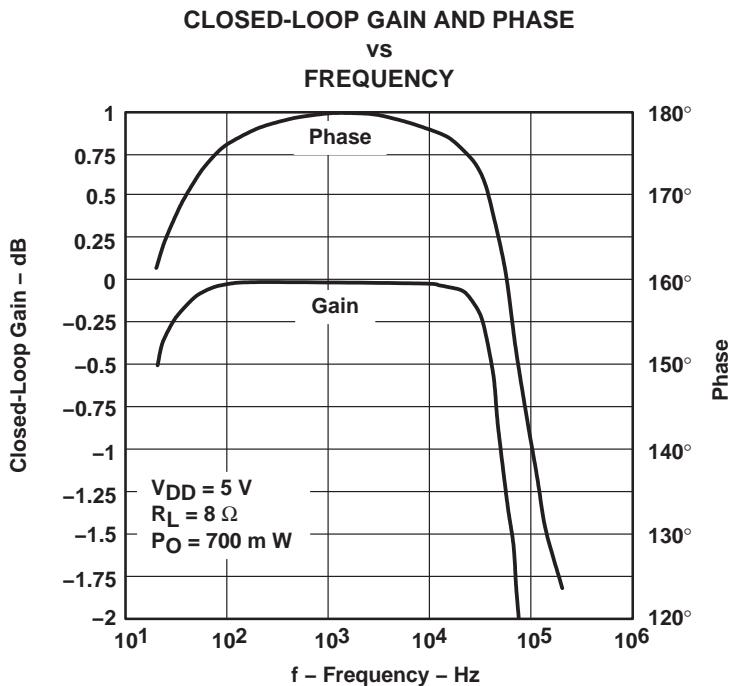


Figure 18

TYPICAL CHARACTERISTICS

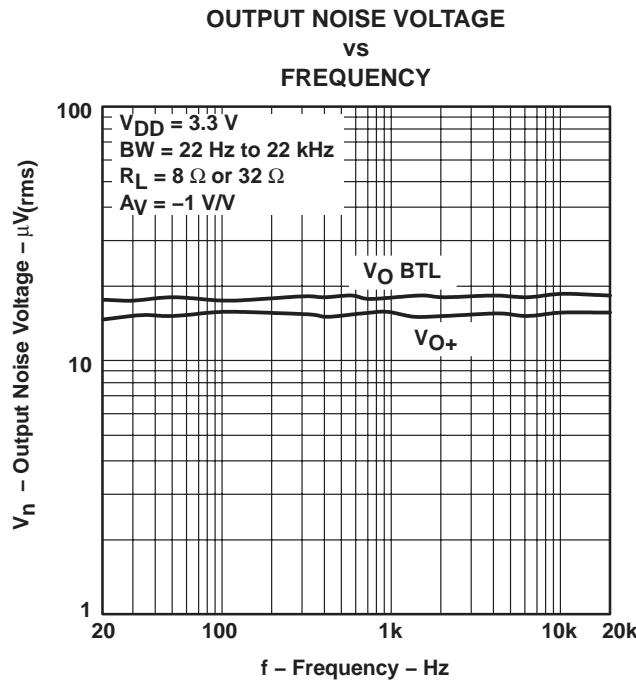


Figure 19

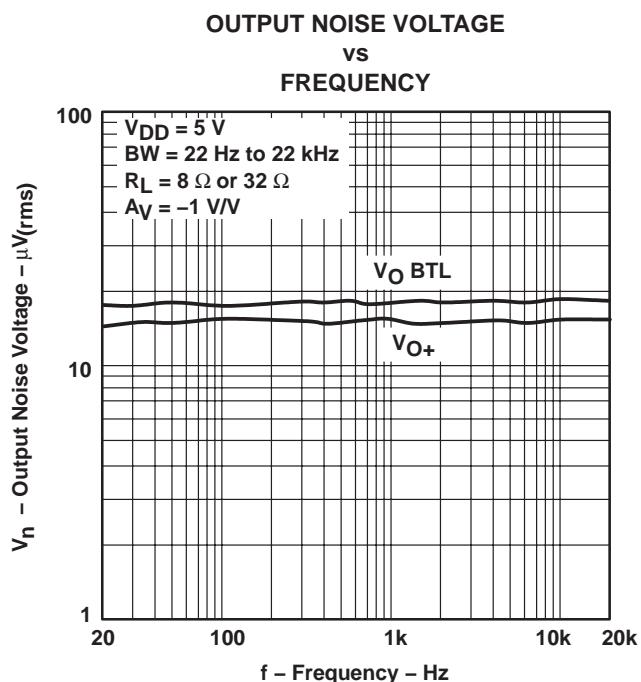


Figure 20

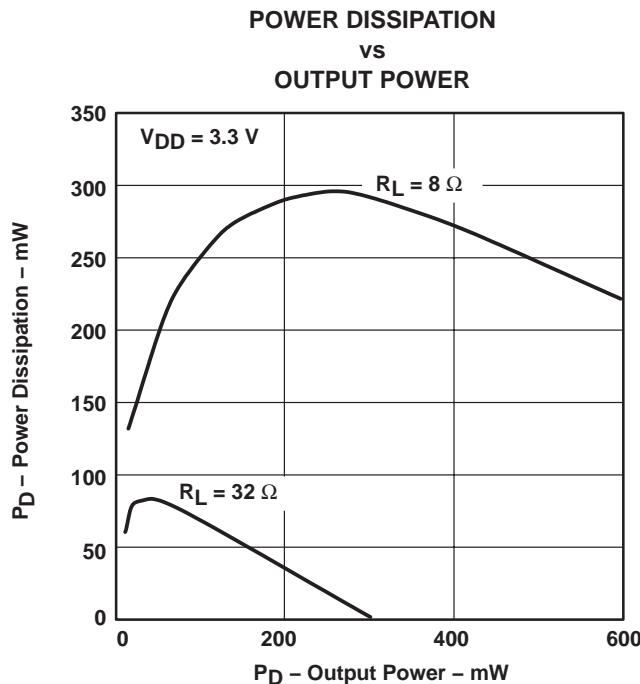


Figure 21

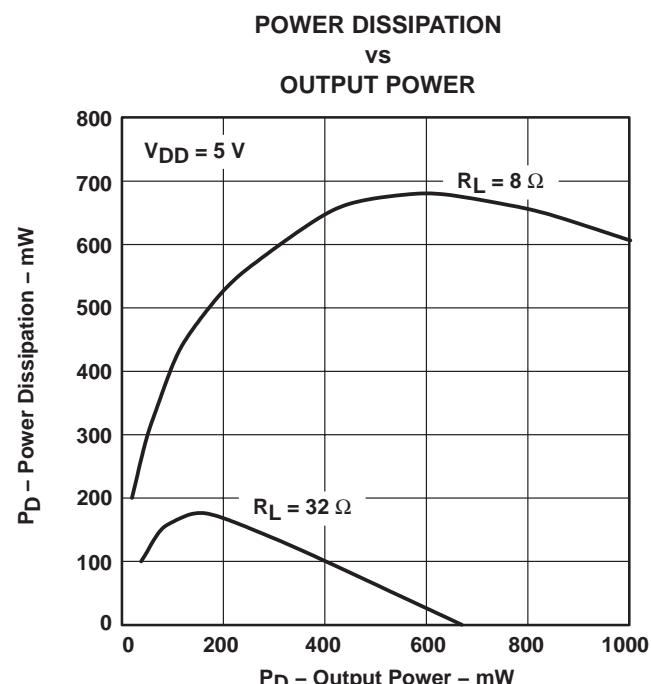


Figure 22

APPLICATION INFORMATION

bridged-tied load

Figure 23 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA751 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This, in effect, doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields $4 \times$ the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (1)$$

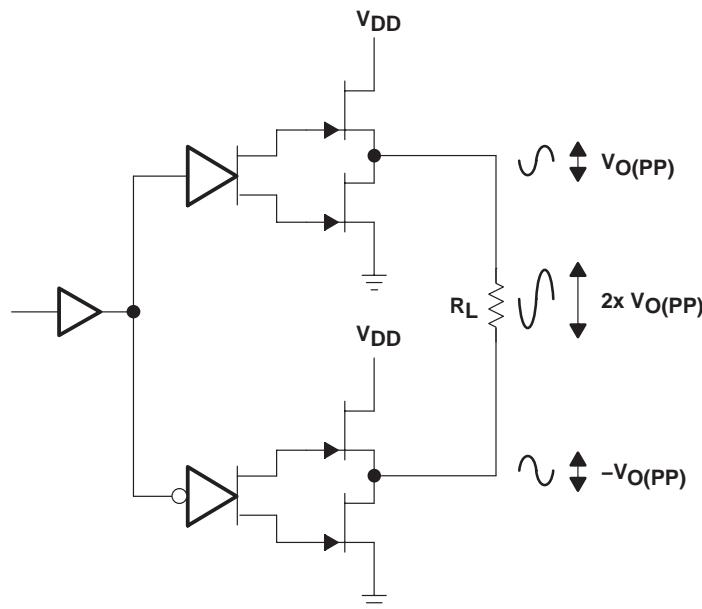


Figure 23. Bridge-Tied Load Configuration

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8- Ω speaker from a singled-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 24. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μ F to 1000 μ F), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency-limiting effect, due to the high pass filter network created with the speaker impedance and the coupling capacitance, is calculated with equation 2.

$$f_C = \frac{1}{2\pi R_L C_C} \quad (2)$$

APPLICATION INFORMATION

bridged-tied load (continued)

For example, a $68\text{-}\mu\text{F}$ capacitor with an $8\text{-}\Omega$ speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

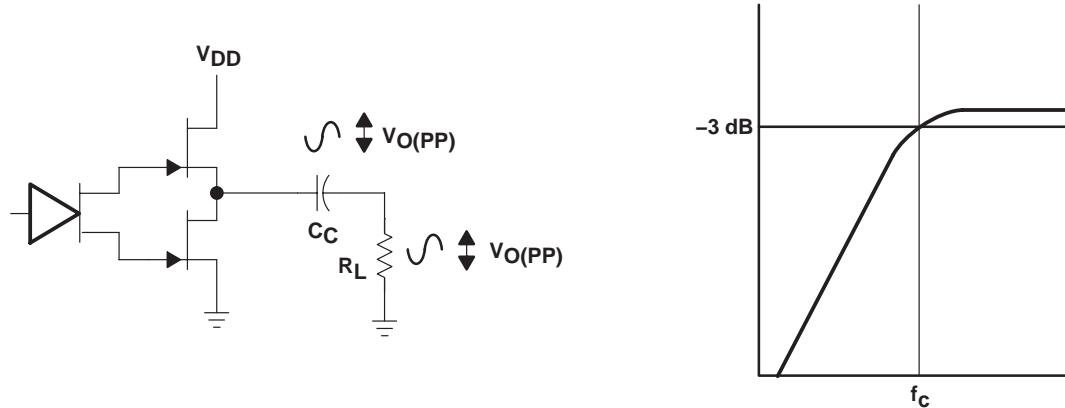


Figure 24. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces $4\times$ the output power of a SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

The primary cause of linear amplifier inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop, can be calculated by subtracting the RMS value of the output voltage from V_{DD} . The internal voltage drop multiplied by the RMS value of the supply current, $I_{DD\text{rms}}$, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 25).

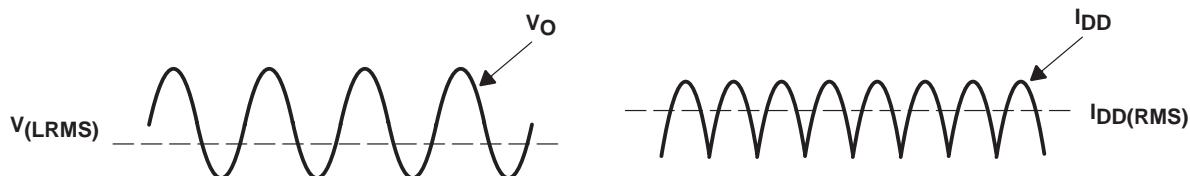


Figure 25. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application, the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \quad (3)$$

where

$$P_L = \frac{V_L \text{rms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD} I_{DD\text{avg}} \text{ and } I_{DD\text{avg}} = \frac{1}{\pi} \int_0^{\pi} \frac{V_P}{R_L} \sin(t) dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

therefore,

$$P_{SUP} = \frac{2 V_{DD} V_P}{\pi R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2 R_L}}{\frac{2 V_{DD} V_P}{\pi R_L}} = \frac{\pi V_P}{4 V_{DD}}$$

where

$$V_P = \sqrt{2 P_L R_L}$$

therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}} \quad (4)$$

P_L = Power delivered to load

P_{SUP} = Power drawn from power supply

V_{LRMS} = RMS voltage on BTL load

R_L = Load resistance

V_P = Peak voltage on BTL load

$I_{DD\text{avg}}$ = Average current drawn from the power supply

V_{DD} = Power supply voltage

η_{BTL} = Efficiency of a BTL amplifier

APPLICATION INFORMATION

application schematics

Figure 26 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of -10 V/V .

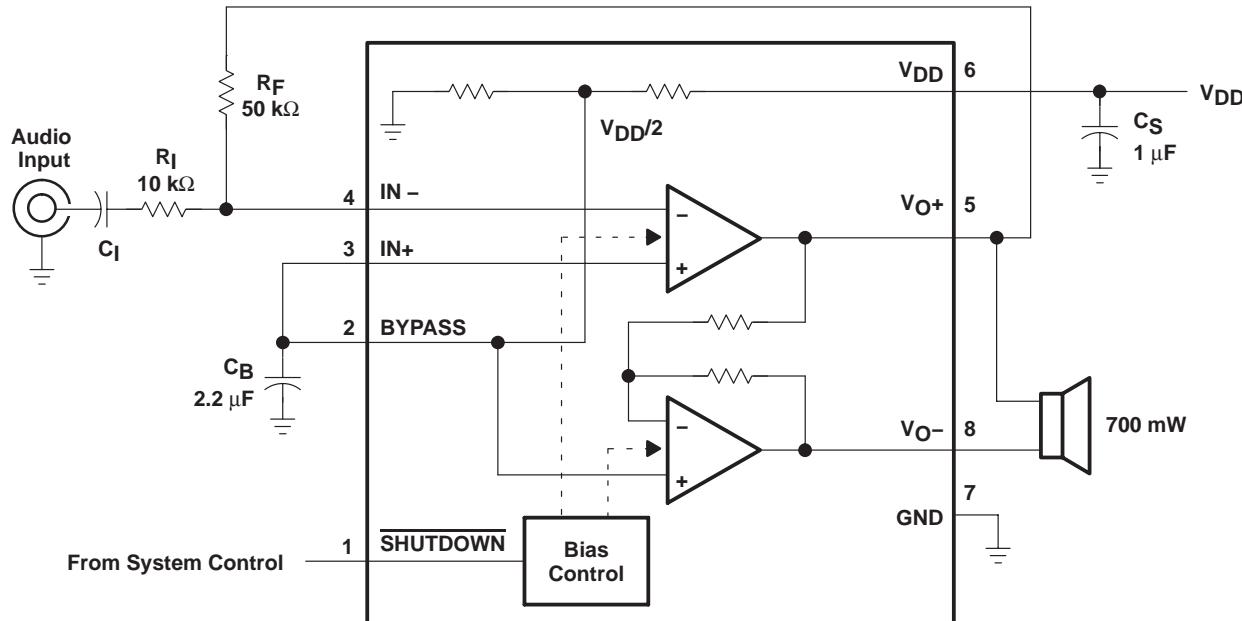


Figure 26. TPA751 Application Circuit

Figure 27 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of -10 V/V with a differential input.

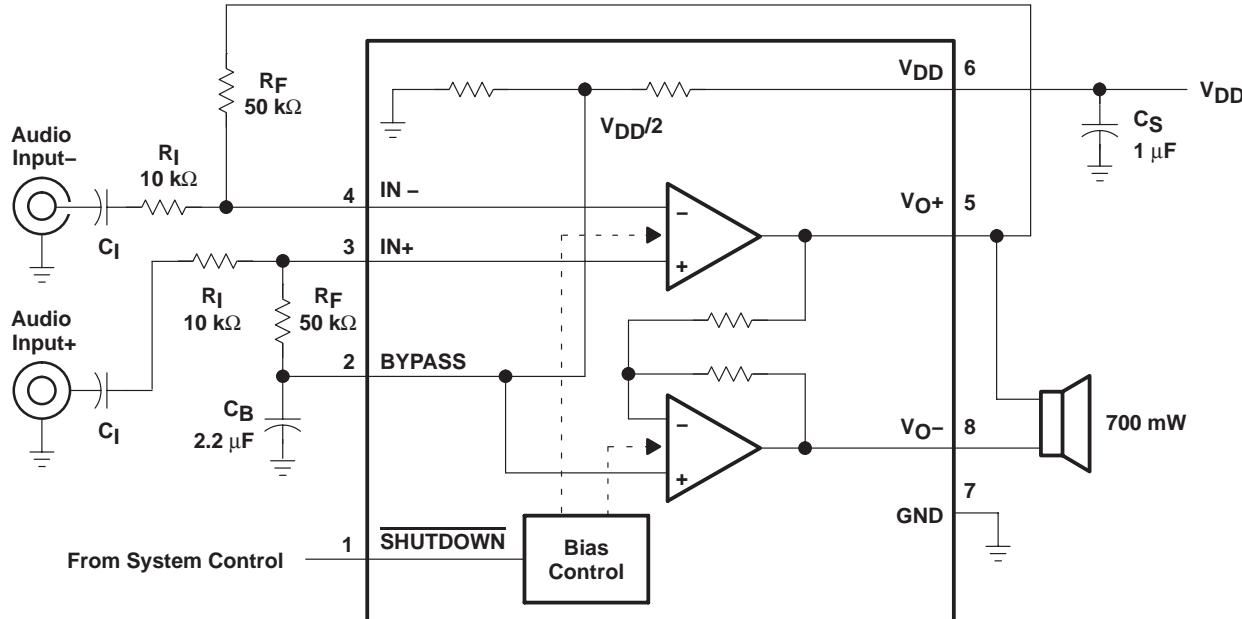


Figure 27. TPA751 Application Circuit With Differential Input

APPLICATION INFORMATION

application schematics (continued)

It is important to note that using the additional R_F resistor connected between IN+ and BYPASS causes $V_{DD}/2$ to shift slightly, which could influence the THD+N performance of the amplifier. Although an additional external operational amplifier could be used to buffer BYPASS from R_F , tests in the lab have shown that the THD+N performance is only minimally affected by operating in the fully differential mode as shown in Figure 27. The following sections discuss the selection of the components used in Figures 26 and 27.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA751 is set by resistors R_F and R_I according to equation 5 for BTL mode.

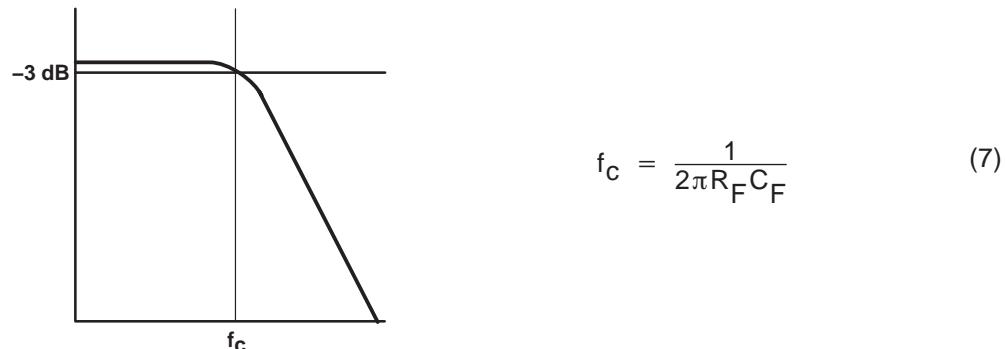
$$\text{BTL gain} = -2 \left(\frac{R_F}{R_I} \right) \quad (5)$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA751 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 k Ω and 20 k Ω . The effective impedance is calculated in equation 6.

$$\text{Effective impedance} = \frac{R_F R_I}{R_F + R_I} \quad (6)$$

As an example, consider an input resistance of 10 k Ω and a feedback resistor of 50 k Ω . The BTL gain of the amplifier would be -10 V/V and the effective impedance at the inverting terminal would be 8.3 k Ω , which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 k Ω , the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 k Ω . This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 7.

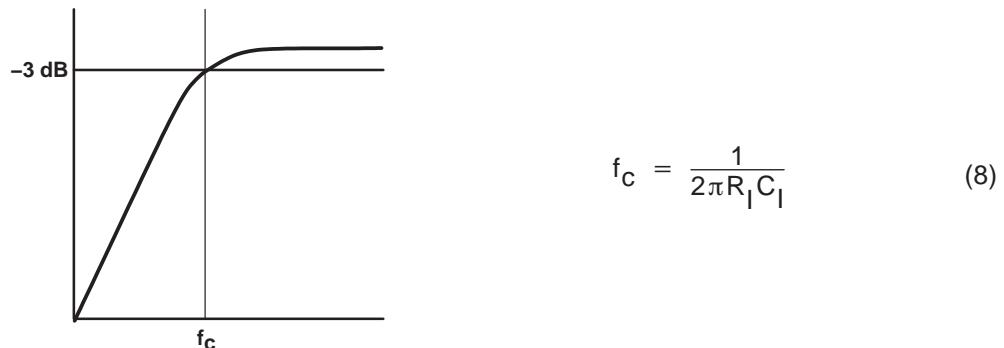


For example, if R_F is 100 k Ω and C_F is 5 pF, then f_c is 318 kHz, which is well outside of the audio range.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.



The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 k Ω and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

In this example, C_I is 0.40 μ F, so one would likely choose a value in the range of 0.47 μ F to 1 μ F. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I , C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA751 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μ F, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μ F or greater placed near the audio power amplifier is recommended.

APPLICATION INFORMATION**midrail bypass capacitor, C_B**

The midrail bypass capacitor, C_B , is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-k Ω source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained. This insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{(C_B \times 250 \text{ k}\Omega)} \leq \frac{1}{(R_F + R_I) C_I} \quad (10)$$

As an example, consider a circuit where C_B is 2.2 μF , C_I is 0.47 μF , R_F is 50 k Ω , and R_I is 10 k Ω . Inserting these values into the equation 10 we get:

$$18.2 \leq 35.5$$

which satisfies the rule. Bypass capacitor, C_B , values of 0.1 μF to 2.2 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA751 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA751 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V as opposed to $V_{O(PP)} = 4$ V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8- Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power of operation from 5-V supplies for a given output-power level.

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA751 data sheet, one can see that when the TPA751 is operating from a 5-V supply into an 8- Ω speaker that 700 mW peaks are available. Converting watts to dB:

$$P_{\text{dB}} = 10 \log \frac{P_W}{P_{\text{ref}}} = 10 \log \frac{700 \text{ mW}}{1 \text{ W}} = -1.5 \text{ dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

- 1.5 dB – 15 dB = -16.5 (15 dB headroom)
- 1.5 dB – 12 dB = -13.5 (12 dB headroom)
- 1.5 dB – 9 dB = -10.5 (9 dB headroom)
- 1.5 dB – 6 dB = -7.5 (6 dB headroom)
- 1.5 dB – 3 dB = -4.5 (3 dB headroom)

Converting dB back into watts:

$$\begin{aligned} P_W &= 10^{P_{\text{dB}}/10} \times P_{\text{ref}} \\ &= 22 \text{ mW} \text{ (15 dB headroom)} \\ &= 44 \text{ mW} \text{ (12 dB headroom)} \\ &= 88 \text{ mW} \text{ (9 dB headroom)} \\ &= 175 \text{ mW} \text{ (6 dB headroom)} \\ &= 350 \text{ mW} \text{ (3 dB headroom)} \end{aligned}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 700 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8- Ω system, the internal dissipation in the TPA751 and maximum ambient temperatures is shown in Table 1.

Table 1. TPA751 Power Rating, 5-V, 8- Ω , BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	D PACKAGE (SOIC)	DGN PACKAGE (MSOP)	GQS PACKAGE (MicroStar Junior™)
			MAXIMUM AMBIENT TEMPERATURE	MAXIMUM AMBIENT TEMPERATURE	MAXIMUM AMBIENT TEMPERATURE
700	700 mW	675	34°C	110°C	99°C
700	350 mW (3 dB)	595	47°C	115°C	105°C
700	176 mW (6 dB)	475	68°C	122°C	114°C
700	88 mW (9 dB)	350	89°C	125°C	123°C
700	44 mW (12 dB)	225	111°C	125°C	125°C

Table 1 shows that the TPA751 can be used to its full 700-mW rating without any heat sinking in still air up to 110°C, 34°C, and 99°C for the DGN package (MSOP), D package (SOIC), and GQS (MicroStar Junior™) package, respectively.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA751D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA751	Samples
TPA751DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATC	Samples
TPA751DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATC	Samples
TPA751DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA751	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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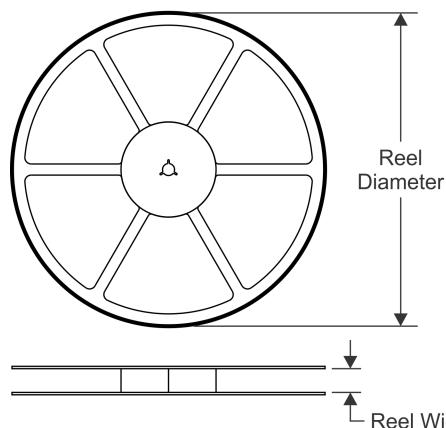
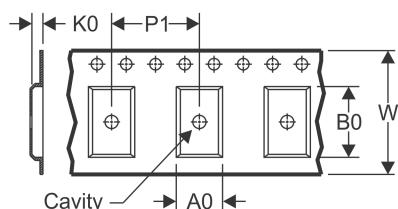
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PACKAGE OPTION ADDENDUM

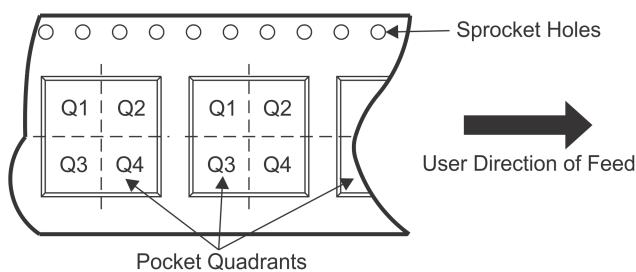
10-Dec-2020

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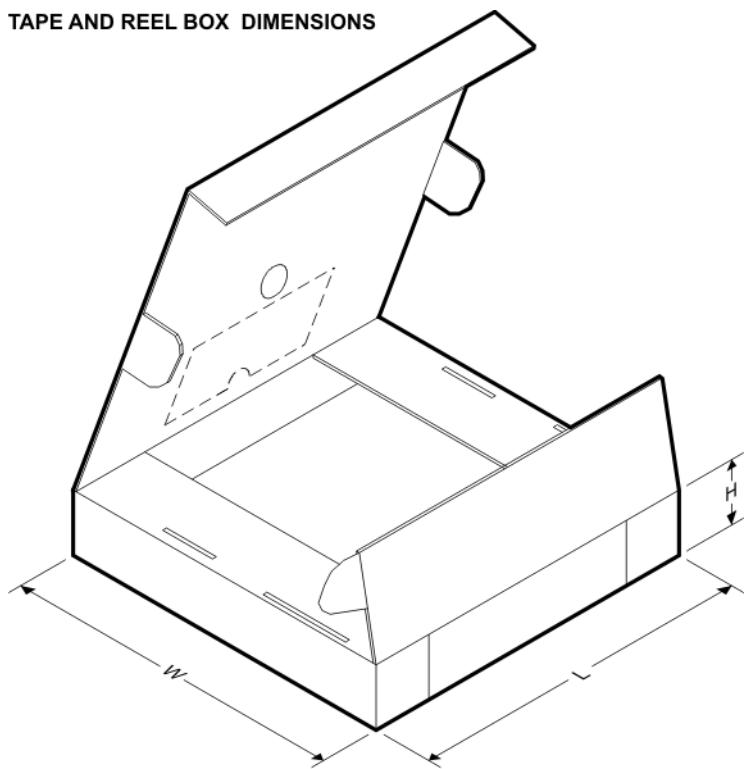
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


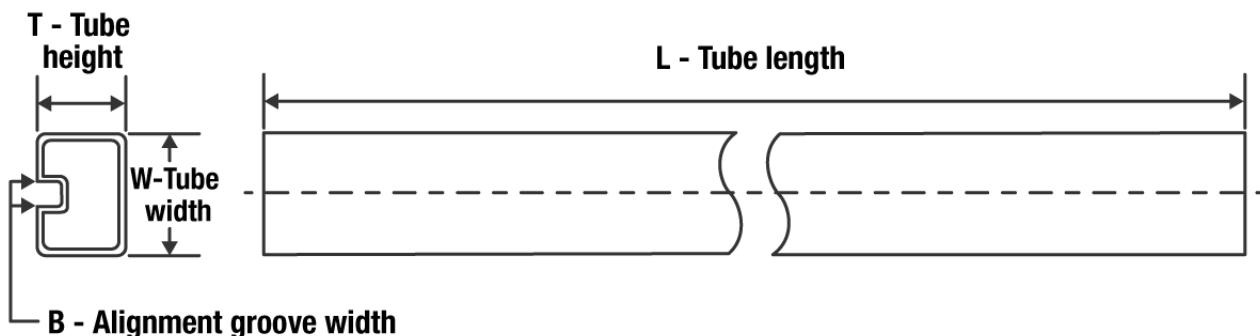
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA751DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA751DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA751DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA751DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPA751D	D	SOIC	8	75	507	8	3940	4.32

GENERIC PACKAGE VIEW

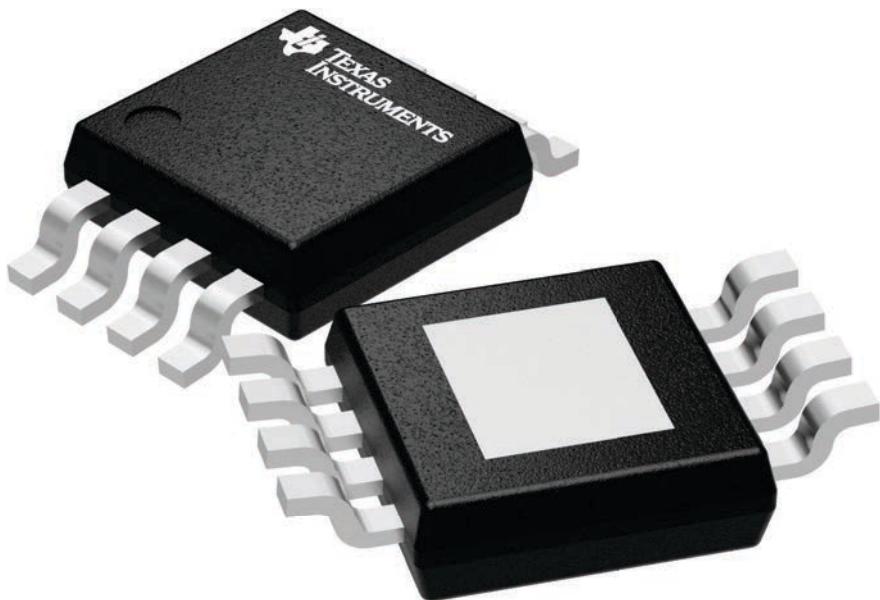
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

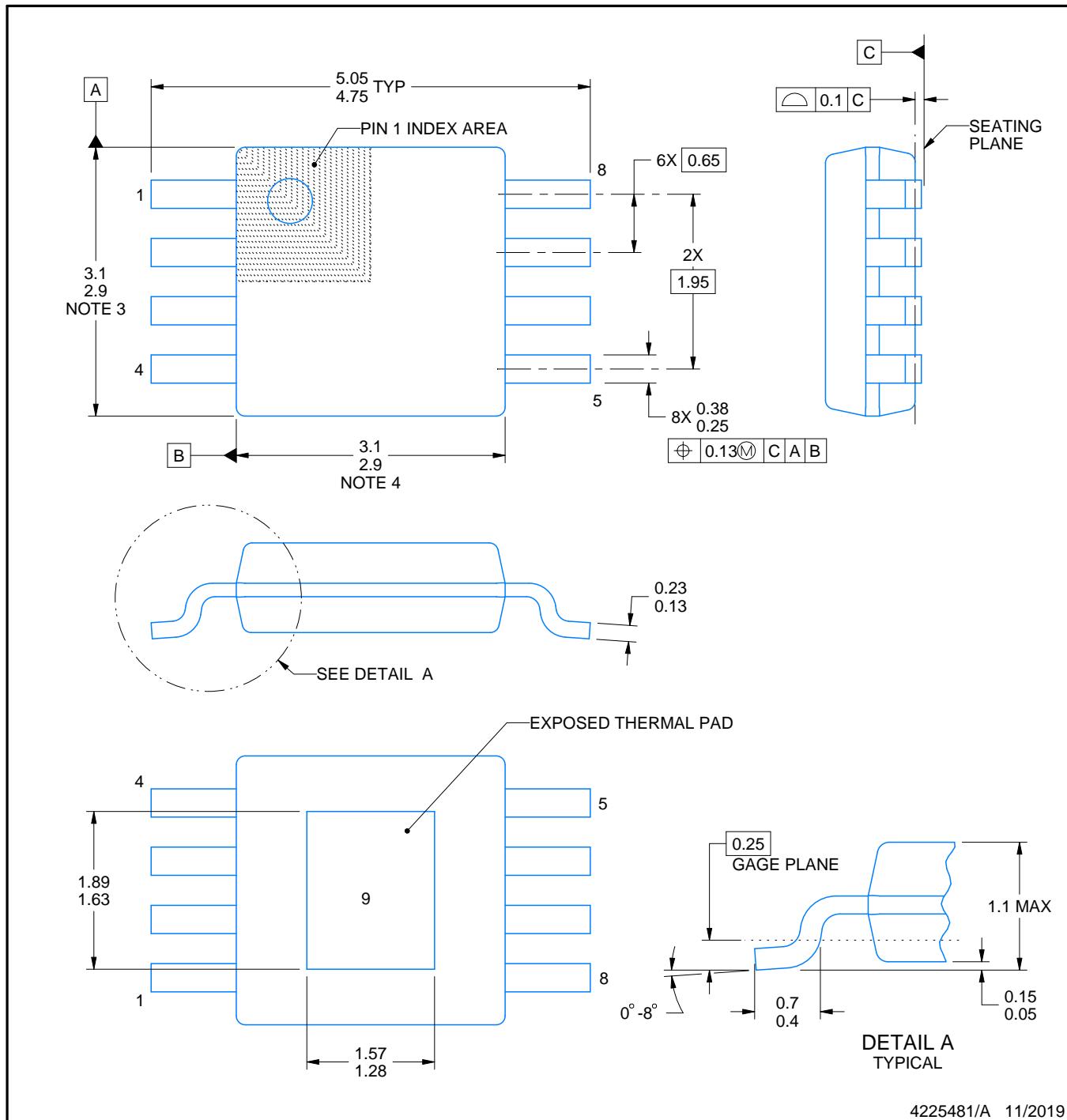
PACKAGE OUTLINE



DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

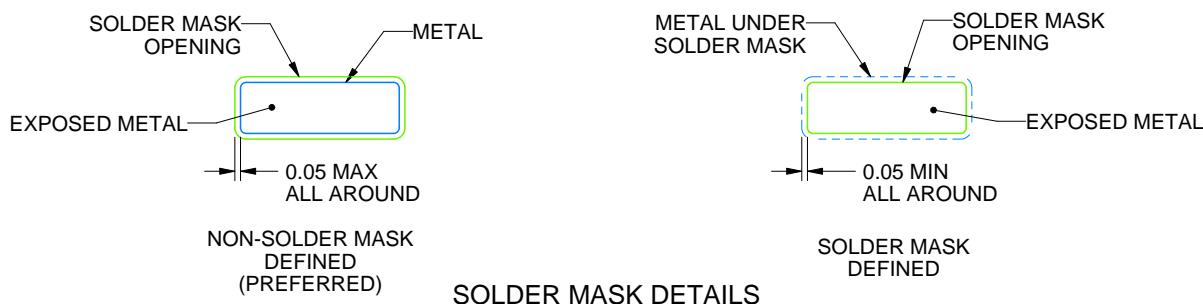
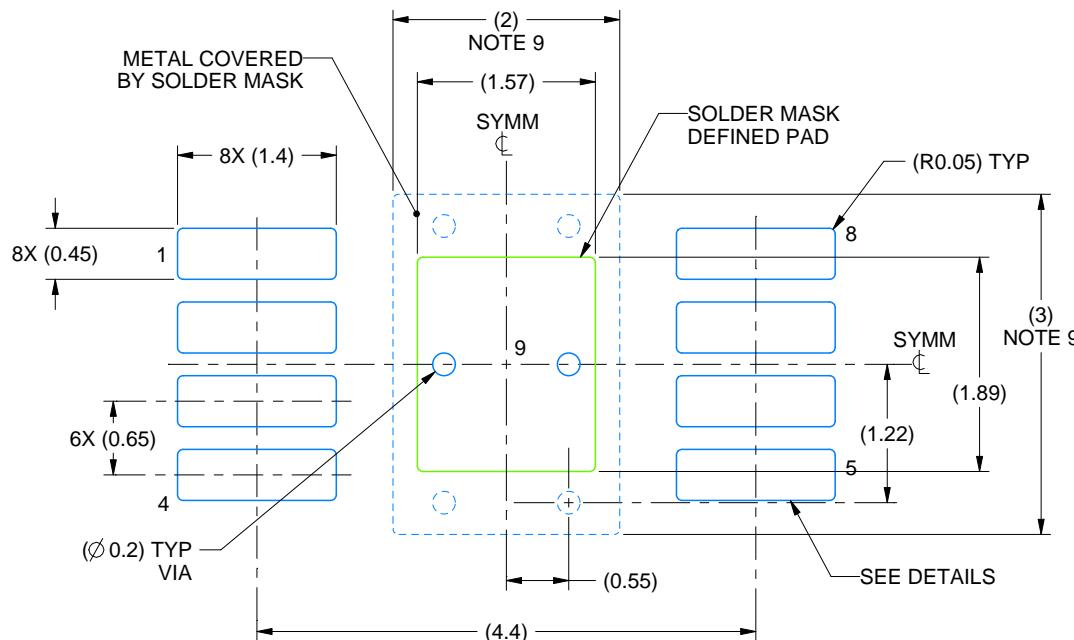
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225481/A 11/2019

NOTES: (continued)

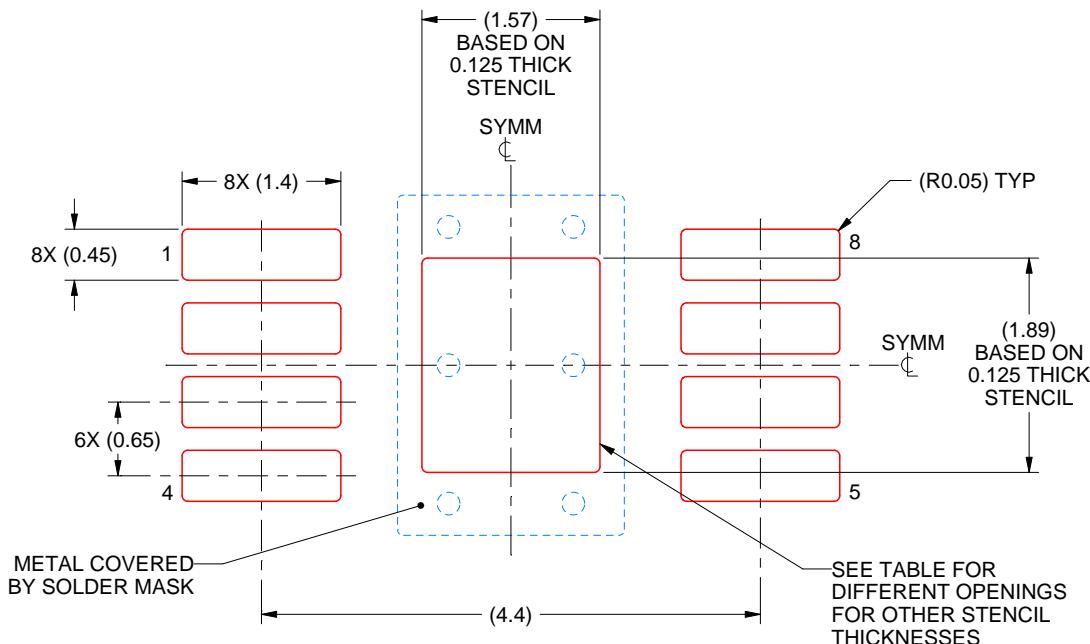
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



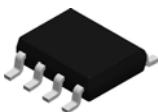
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

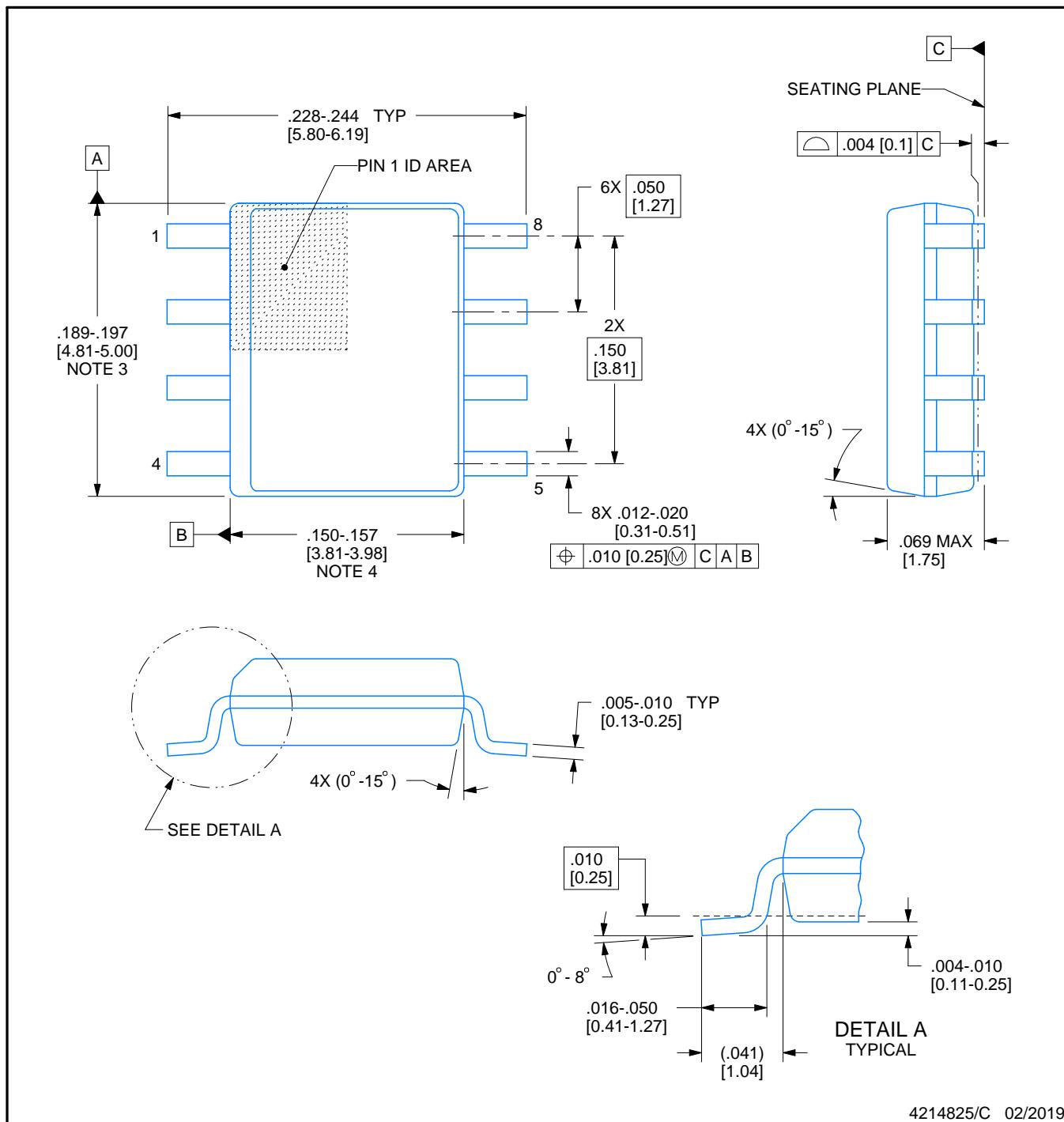


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

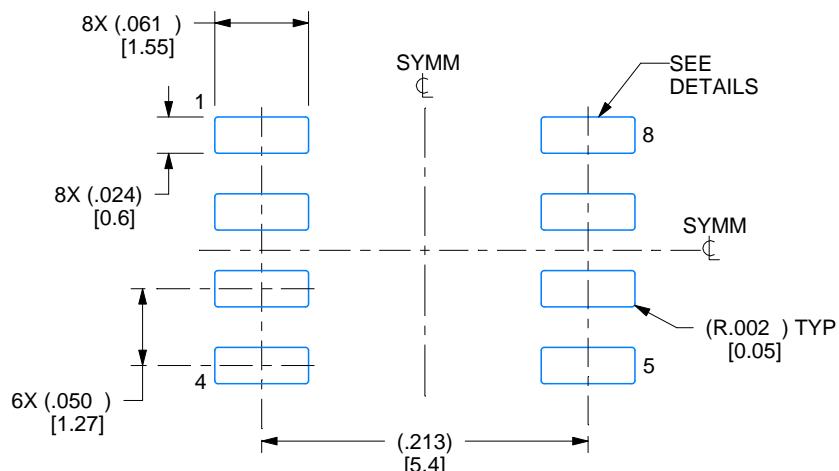
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

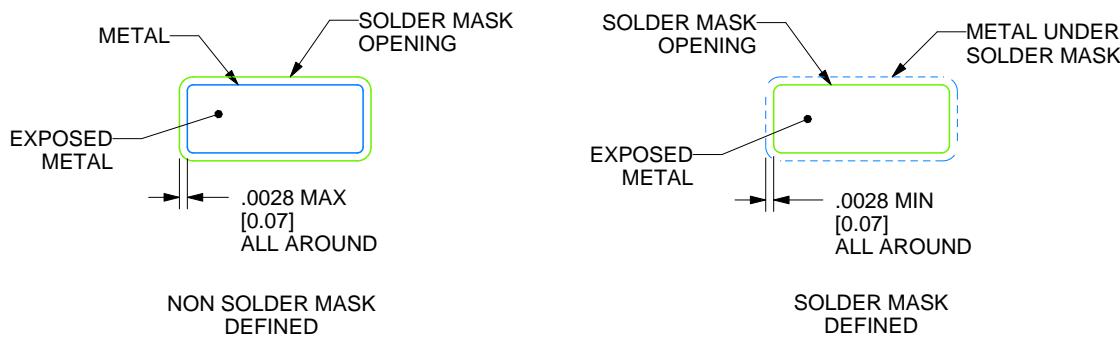
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

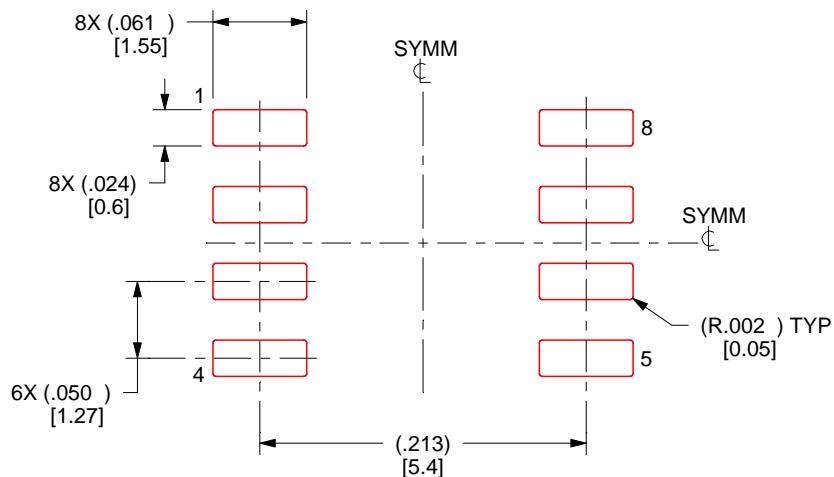
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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