

SLVS399A − JANUARY 2002 − REVISED MAY 2006

ADJUSTABLE LDO AND SWITCH WITH DUAL CURRENT LIMIT FOR USB HIGH-POWER PERIPHERAL POWER MANAGEMENT

FEATURES

- **Complete Power Management Solution for USB High-Power Peripherals**
- **250 mA Low-Dropout Regulator (LDO) With Enable and 325 mA (Typ) Current Limit**
- **LDO Supports 2.7 V to 5.5 V V_{IN} and 0.9 V to 3.3 V Adjustable V_{OUT}**
- **40 mΩ (Typ) High-Side MOSFET With Dual Current Limit**
- **Undervoltage Lockout and Power Good for LDO and Switch**
- **CMOS- and TTL-Compatible Enable Inputs**
- **85 μA (Typ) Supply Current**
- **5 μA (Typ) Standby Supply Current**
- **Available in 14-Pin HTSSOP (PowerPAD™)**
- **−40°C to +85°C Ambient Temperature Range**
- **Alternative to TPS2148/58 3.3-V LDO With 3.3-V Switch and 5-V Switch**

APPLICATIONS

- **High-Power USB™ Peripherals**
  - **ADSL Modems**
  - **Digital Still and PC Cameras**
  - **Zip Drives**
  - **Speakers**
- **DSP Sequencing**

DESCRIPTION

The TPS2140/41/50/51 is a USB 1.0 and 2.0 Specification-compatible IC containing a dual-current-limiting power switch and an adjustable low dropout regulator (LDO). Both the switch and LDO limit inrush current by controlling the turnon slew rate. The unique dual-current-limiting feature of the switch allows USB peripherals to utilize high-value capacitance at the output of the switch, while keeping the inrush current low. During turnon, the switch limits the current delivered to the capacitive load to less than 100 mA. When the output voltage from the switch reaches about 93% of the input voltage, the switch power good output goes high, and the switch current limit increases to 800mA (minimum), at which point higher current loads can be turned on. The higher current limit provides short circuit protection while allowing the peripheral to draw maximum current from the USB bus.

The switch and LDO function independently, providing flexibility in DSP applications requiring separate core and I/O voltages. For example, in a DSP application operating from a 3.3-V rail, the LDO can supply the DSP core voltage down to 0.9 V, while the switch powers the 3.3-V (typical) DSP I/O supply. If supply sequencing is required, the LDO power good output can be used to enable the switch.

AVAILABLE OPTIONS

T_A	DESCRIPTION	TARGET APPLICATION	PACKAGE AND PIN COUNT	PACKAGED DEVICES	
				ACTIVE LOW (SWITCH)	ACTIVE HIGH (SWITCH)
−40°C to 85°C	Adjustable LDO and 3.3 V switch with dual current limit	DSP	HTSSOP-14	TPS2140IPWP	TPS2150IPWP
	Adjustable LDO and 5 V switch with dual current limit	USB	HTSSOP-14	TPS2141IPWP	TPS2151IPWP

NOTE: All options available taped and reeled. Add an R suffix (e.g., TPS2140IPWPR)

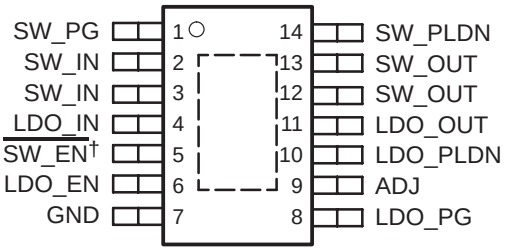
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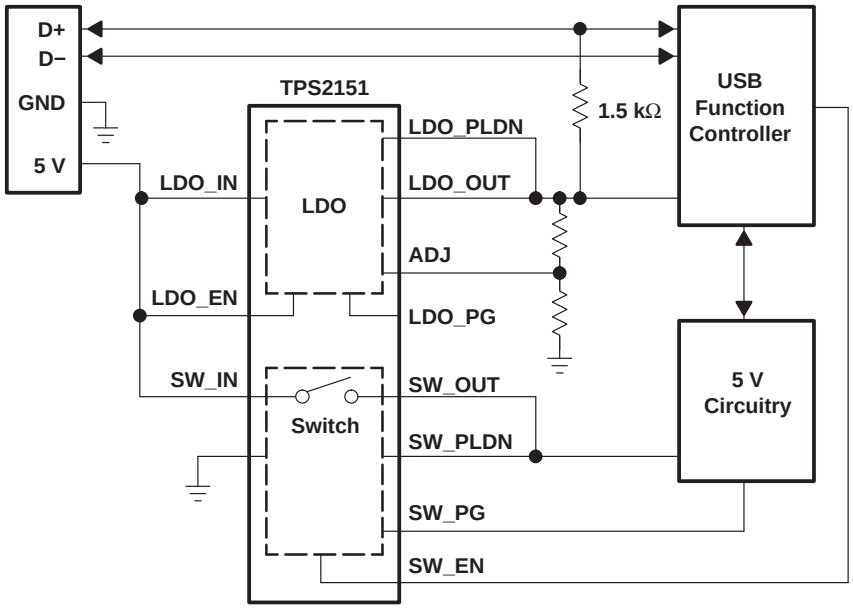
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TPS2140/41/50/51
PWP PACKAGE
(TOP VIEW)

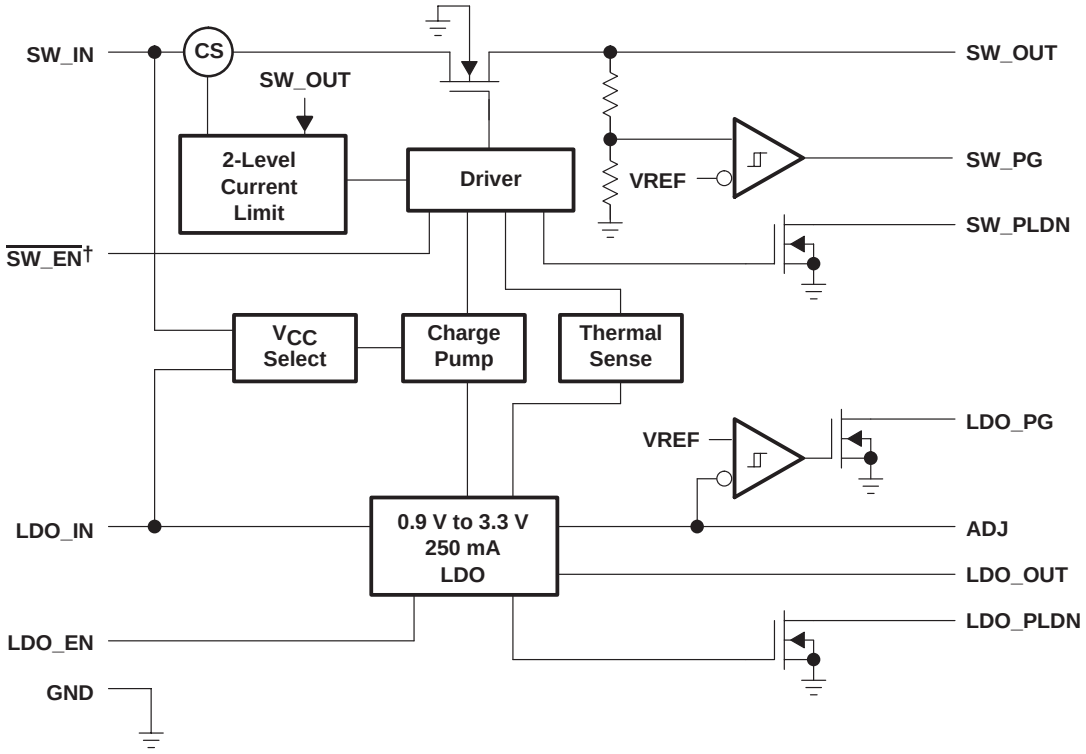


† Pin 5 is active high for TPS2150 and TPS2151.

USB peripheral application



functional block diagram



† The pin is active low for TPS2140 and TPS2141, with an internal pullup.
The pin is active high for TPS2150 and TPS2151, with an internal pulldown.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADJ	9	I	Feedback adjustment of LDO regulator to set output voltage
GND	7		Ground
LDO_EN	6	I	Enable signal for LDO regulator, active high, no internal pullup or pulldown
LDO_IN	4	I	Input of LDO regulator
LDO_OUT	11	O	Output of LDO regulator
LDO_PG	8	O	Power good signal for LDO output, open-drain, active high
LDO_PLDN	10	I	Output pulldown pin used for LDO when connected to LDO_OUT
$\overline{\text{SW_EN}}$ or SW_EN	5	I	Active-high enable for switch on TPS2150 and TPS2151 devices with internal pulldown Active-low enable for switch on TPS2140 and TPS2141 devices with internal pullup
SW_IN	2, 3	I	Input of the switch
SW_OUT	12, 13	O	Output of switch
SW_PG	1	O	Power good signal for switch output, active high logic-level signal, no external pullup required.
SW_PLDN	14	I	Output pulldown pin used for switch when connected to SW_OUT.

detailed description

GND

Ground

SW_IN

SW_IN is the input to an integrated N-channel MOSFET, which has a maximum on-state resistance of 65 mΩ. Configured as a high-side switch, the power switch prevents current, flow from OUT to IN and IN to OUT when disabled. The power switch is rated at 500 mA, continuous current and has a dual current limit feature.

dual current limit

The current limiter for the switch limits the initial current drawn from SW_IN to 100 mA maximum. The user can estimate the amount of time it takes to charge a capacitor (CL) connected to SW_OUT by using the following relationship:

$$CL \times V_{I(SW_IN)} / 0.1 < t_{CHG} < CL \times V_{I(SW_IN)} / 0.05$$

Capacitance in farads. If $V_{I(SW_IN)} = 5$ V, then

$$50 \times CL < t_{CHG} < 100 \times CL$$

When the voltage at output SW_OUT rises above 93% of the voltage at SW_IN, the current limit is increased to 1800 mA maximum. The SW_PG can be used to turn on loads which may draw more than 50 mA.

In the event of an overload on SW_OUT, the protection circuit limits the current delivered to 1800 mA maximum. As the output voltage drops and it crosses 80% of the SW_IN voltage, the current limiter reverts back to the low-current limit mode of 100 mA maximum.

SW_IN also serves as one of the two inputs to an internal voltage selector that provides operating voltage to the whole device. The other input to the selector is LDO_IN.

SW_OUT

SW_OUT is the output of the internal power-distribution switch.

$\overline{\text{SW_EN}}$ or SW_EN

The logic input disables or enables the power switch. This signal is active low ($\overline{\text{SW_EN}}$) for TPS2140/41 and active high (SW_EN) for TPS2150/51. $\overline{\text{SW_EN}}$ has an internal pullup and SW_EN has an internal pulldown.

SW_PG

SW_PG signals the presence of an undervoltage condition on SW_OUT. The pin is driven by a CMOS output buffer and is pulled low during an undervoltage condition. To minimize erroneous SW_PG responses from transients on the voltage rail, the voltage sense circuit incorporates a rising and falling edge deglitch filter. When SW_OUT voltage is lower than 88% of 3.3 V for TPS2140/50, or 5 V for TPS2141/51, SW_PG goes low to indicate an undervoltage condition on SW_OUT.

SW_PLDN

SW_PLDN is an open drain output incorporated to provide a discharge path. When the power switch is on, this pin is open; otherwise it is pulled down to ground. When this pin is connected to SW_OUT, the output voltage fall time is reduced but the rise time remains unaffected.

LDO_IN

The LDO_IN serves as the input to the internal LDO. The adjustable LDO has a dropout voltage of 0.5 V maximum and is rated for 250 mA of continuous current. LDO_IN is also used as one of the two inputs for V_{CC} selection.

detailed description (continued)

LDO_OUT

LDO_OUT is the output of the internal LDO. It has an output voltage range of 0.9 V to 3.3 V.

LDO_EN

LDO_EN is used to enable or disable the internal LDO and is compatible with CMOS and TTL logic. LDO_EN is an active high input.

ADJ

ADJ is used to adjust the LDO output voltage (LDO_OUT) anywhere between 0.9 V and 3.3 V by connecting a resistor divider from LDO_OUT to ground (ADJ connects to the center point of the resistor divider).

LDO_PG

LDO_PG signals the presence of an undervoltage condition on LDO_OUT. LDO_PG is an open-drain output and is pulled low during an undervoltage condition. To minimize erroneous LDO_PG responses from transients on the voltage rail, the voltage sense circuit incorporates a 150-µs falling deglitch filter. When the LDO_OUT voltage is lower than 94% of a threshold voltage (set by an external resistor divider), LDO_PG goes low to indicate an undervoltage condition. A pullup resistor from LDO_PG to a power rail is required for proper operation.

LDO_PLDN

LDO_PLDN is an open drain output incorporated to provide a discharge path. When the LDO is on, this pin is open; otherwise, it is pulled down to ground. When this pin is connected to LDO_OUT, the output voltage fall time is reduced but the rise time remains unaffected.

current sense

Both the power switch and the LDO have integrated current sense circuits. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver reduces the gate voltage until the current drops back to the limiting value.

thermal sense

A dual-threshold thermal trip is implemented to protect the device. The lower thermal trip point is used to protect the device during an overcurrent condition. The higher thermal trip point is used to protect the device when the junction temperature rises but not due to an overcurrent condition.

undervoltage lockout

A voltage sense circuit monitors both input voltages on SW_IN and LDO_IN. When the input voltage is below its respective threshold, a control signal turns off the related channel (the power switch or the LDO).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for bus switch and LDO: $V_{I(SW_IN)}$ . . . . . −0.3 V to 6 V
$V_{I(LDO_IN)}$ . . . . . −0.3 V to 6 V
Output voltage range for bus switch and LDO: $V_{O(SW_OUT)}$ . . . . . −0.3 V to 6 V
$V_{O(LDO_OUT)}$ . . . . . −0.3 V to 6 V
Input voltage range for pulldown transistors: $V_{I(SW_PLDN)}$, $V_{I(LDO_PLDN)}$ . . . . . −0.3 V to 6 V
Logic input/output voltage range: $V_{I(SW_EN)}$ or $V_{I(/SW_EN)}$, $V_{I(LDO_EN)}$, $V_{I(ADJ)}$, $V_{I(SW_PG)}$, $V_{I(LDO_PG)}$ . . . . . −0.3 V to 6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output current for bus switch and LDO: $I_{O(SW_OUT)}$ . . . . . Internally Limited
$I_{O(LDO_OUT)}$ . . . . . Internally Limited
Sink current for pulldown switches: $I_{I(SW_PLDN)}$ . . . . . 0 mA to 30 mA
$I_{I(LDO_PLDN)}$ . . . . . 0 mA to 30 mA
Output current for logic outputs: $I_{O(SW_PG)}$ . . . . . −10 mA to 10 mA
$I_{O(LDO_PG)}$ . . . . . 0 mA to 10 mA
Operating virtual junction temperature range, T_J . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A \le 85°C$ POWER RATING
PWP-14	2266.7 mW	26.7 mW/°C	1066.7 mW	666.7 mW

NOTE: This device is mounted on an JEDEC low-k board (2 oz traces on surface), 1 W power applied with no air flow.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(SW_IN)}$, TPS2140 and TPS2150	2.7	5.5	V
	$V_{I(SW_IN)}$, TPS2141 and TPS2151	4.1	5.5	
	$V_{I(LDO_IN)}$	2.7	5.5	
	$V_{I(SW_EN)}$ or $V_{I(/SW_EN)}$, $V_{I(LDO_EN)}$	0	5.5	
	$V_{I(SW_PLDN)}$, $V_{I(LDO_PLDN)}$	0	5.5	
Output current, I_O	$I_{O(SW_OUT)}$ at T_J = 110°C		0.6	A
	$I_{O(LDO_OUT)}$ at T_J =110°C		0.25‡	
Operating virtual junction temperature, T_J		−40	110	°C

‡ Assuming the power dissipation does not exceed the device’s thermal limit. Refer to the *power dissipation and junction temperature* section for the power dissipation calculation.

electrical characteristics over recommended operating junction temperature range, $V_{I(SW_IN)}$ = 3.3 V for TPS2140/50, $V_{I(SW_IN)}$ = 5 V for TPS2141/51, $V_{I(LDO_IN)}$ = 5 V, all outputs unloaded (unless otherwise noted)

general

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power switch operating supply current I_{OP_SW}	TPS2140, TPS2150	2.7 V < $V_{I(SW_IN)}$ < 5.5 V, $V_{I(LDO_IN)}$ = 0, $V_{I(SW_EN)}$ = 5.5 V or $V_{I(/SW_EN)}$ = 0 V, $V_{I(LDO_EN)}$ = 0 V, No load		85	110	µA
	TPS2141, TPS2151	4.1 V< $V_{I(SW_IN)}$ < 5.5 V, $V_{I(LDO_IN)}$ = 0, $V_{I(SW_EN)}$ = 5.5 V or $V_{I(/SW_EN)}$ = 0 V, $V_{ILDO_EN)}$ = 0 V, No load		85	110	
Power switch standby supply current I_{STBY_SW}	TPS2140, TPS2150	2.7 V< $V_{I(SW_IN)}$ <5.5 V, $V_{I(LDO_IN)}$ = 0, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5.5 V, $V_{I(LDO_EN)}$ = 0 V, No load		5	10	
	TPS2141, TPS2151	4.1 V< $V_{I(SW_IN)}$ < 5.5 V, $V_{I(LDO_IN)}$ = 0, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5.5 V, $V_{I(LDO_EN)}$ = 0 V, No load		5	10	
LDO operating supply current I_{OP_LDO}		2.7 V< $V_{I(LDO_IN)}$ <5.5 V, $V_{I(SW_IN)}$ = 0 V, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5.5 V, $V_{I(LDO_EN)}$ = 5 V, No load		90	120	µA
LDO standby supply current I_{STBY_LDO}		2.7 V< $V_{I(LDO_IN)}$ <5.5 V, $V_{I(SW_IN)}$ = 0 V, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5.5 V, $V_{I(LDO_EN)}$ = 0 V, No load		5	10	
Power switch and LDO total operating supply current I_{OP_TOTAL}	TPS2140, TPS2150	2.7 V< $V_{I(SW_IN)}$ <5.5 V, $V_{I(SW_EN)}$ = 5.5 V or $V_{I(/SW_EN)}$ = 0 V, $V_{I(LDO_EN)}$ = 5 V, No load 2.7 V< $V_{I(LDO_IN)}$ <5.5 V			150	µA
	TPS2141, TPS2151	4.1 V< $V_{I(SW_IN)}$ <5.5 V, $V_{I(SW_EN)}$ = 5.5 V or $V_{I(/SW_EN)}$ = 0 V, $V_{I(LDO_EN)}$ = 5 V, No load 2.7 V< $V_{I(LDO_IN)}$ <5.5 V			150	
Power switch and LDO total standby supply current I_{STBY_TOTAL}	TPS2140, TPS2150	2.7 V< $V_{I(SW_IN)}$ <5.5 V, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5.5 V, $V_{I(LDO_EN)}$ = 0 V, No load 2.7 V<$V_{I(LDO_IN)}$ <5.5 V			10	
	TPS2141, TPS2151	4.1 V< $V_{I(SW_IN)}$ <5.5 V, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5.5 V, $V_{I(LDO_EN)}$ = 0 V, No load 2.7 V<$V_{I(LDO_IN)}$ <5.5 V			10	

electrical characteristics over recommended operating junction temperature range, $V_{I(SW_IN)}$ = 3.3 V for TPS2140/50, $V_{I(SW_IN)}$ = 5 V for TPS2141/51, $V_{I(LDO_IN)}$ = 5 V, all outputs unloaded (unless otherwise noted) (continued)

power switch

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Switch on resistance (SW_IN to SW_OUT)	TPS2140, TPS2150	T_J = 25°C, I = 500 mA, $V_{I(SW_EN)}$ = 3.3 V or $V_{I(/SW_EN)}$ = 0 V			40	50	mΩ
		T_J = 110°C, I = 500 mA, $V_{I(SW_EN)}$ = 3.3 V or $V_{I(/SW_EN)}$ = 0 V				65	
	TPS2141, TPS2151	T_J = 25°C, I = 500 mA, $V_{I(SW_EN)}$ = 5 V or $V_{I(/SW_EN)}$ = 0 V			40	50	
		T_J = 110°C, I = 500 mA, $V_{I(SW_EN)}$ = 5 V or $V_{I(/SW_EN)}$ = 0 V				65	
Switch current limit	Switch low-current-limit cutoff threshold, $V_{COFF(SW_OUT)}$	Low current limit is disabled when $V_{O(SW_OUT)}$ is above this %$V_{I(SW_IN)}$ level		91%	93%	96%	
	Switch low-current-limit cutin threshold, $V_{CIN(SW_OUT)}$	Low current limit is enabled $V_{O(SW_OUT)}$ is below this %$V_{I(SW_IN)}$ level		76%	79%	82%	
	Low-current-limit mode: Ramp-up current limit, IRCL			50	75	99	mA
	Low-current-limit mode: Short-circuit dc current limit, I_{OS}	SW_OUT is enabled into a short to ground	T_J = 25°C	50	75	99	
			T_J = 110°C	47	75	99	
	High-current-limit mode: Overload dc current limit, I_{OL}		T_J = 25°C	900	1300	1800	
			T_J = 110°C	800	1300	1800	
Switch forward leakage current I_{LK_SW}	Current into pin SW_OUT	$V_{O(SW_OUT)}$ = 0 V, $V_{I(SW_IN)}$ = 5.5 V, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5 V			10		µA
Switch reverse leakage current I_{RLK_SW}	Current into pin SW_OUT	$V_{O(SW_OUT)}$ = 5.5 V, $V_{I(SW_IN)}$ = 0 V, $V_{I(SW_EN)}$ = 0 V or $V_{I(/SW_EN)}$ = 5 V			10		
Switch pulldown transistor current		$V_{I(SW_PLDN)}$ = 3.3 V		9	15		mA
		$V_{I(PLDN_SW)}$ = 1 V			5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

timing parameters, power switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turnon time	C_L = 10 µF, No load		1		ms
t_{off}	Turnoff time	C_L = 10 µF, SW_OUT is connected to SW_PLDN, No load		8		
t_r	Rise time	C_L = 10 µF, No load		0.5		
t_f	Fall time	C_L = 10 µF, SW_OUT is connected to SW_PLDN, No load		5		

undervoltage lockout, SW_IN

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch UVLO rising threshold	TPS2140, TPS2150				2.7	V
	TPS2141, TPS2151				4.1	
Switch UVLO falling threshold	TPS2140, TPS2150		2.3		2.45	
	TPS2141, TPS2151		3.5		3.9	
UVLO hysteresis‡			250			mV

‡ Not tested in production.

electrical characteristics over recommended operating junction temperature range, $V_{I(SW_IN)}$ = 3.3 V for TPS2140/50, $V_{I(SW_IN)}$ = 5 V for TPS2141/51, $V_{I(LDO_IN)}$ = 5 V, all outputs unloaded (unless otherwise noted) (continued)

adjustable voltage regulator (V_{set} = 0.9 V to 3.3 V)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{O(LDO_OUT)}$	Output voltage total tolerance	$V_{I(LDO_IN)}$ = V_{set} + 0.6 V to 5.5 V and $V_{I(LDO_IN)}$ > 2.7 V, $I_{O(LDO_OUT)}$ = 5 mA to 250 mA		−4%		3%	
$V_{O(LDO_OUT)}$	Line regulation	$V_{I(LDO_IN)}$ = $V_{O(LDO_OUT)}$ + 0.6 V to 5.5 V and $V_{I(LDO_IN)}$ > 2.7 V, $I_{O(LDO_OUT)}$ = 5 mA			0.03	0.1	%/V
$V_{O(LDO_OUT)}$	Load regulation	$V_{I(LDO_IN)}$=$V_{O(LDO_OUT)}$ + 0.6 V to 5.5 V and $V_{I(LDO_IN)}$ > 2.7 V, $I_{O(LDO_OUT)}$ = 5 mA to 250 mA (a percentage of V_{set})			0.6%	1.3%	
V_{SET}	Regulated output voltage set range	$V_{I(LDO_IN)} \geq V_{O(LDO_OUT)}$ + 0.6 V $V_{I(LDO_IN)} \geq$ 2.7 V, $I_{O(LDO_OUT)}$ = 0 mA to 250 mA		0.9		3.3	V
V_{ref}	ADJ reference voltage				0.8		V
V_{DROP}	Drop-out voltage	$V_{I(LDO_IN)} - V_{SET}$ = −0.1 V, $I_{O(LDO_OUT)}$ = 250 mA			0.18	0.5	V
PSRR	Power supply rejection ratio, 20 log(Vac/Vo)‡	Vac = 1 kHz sine wave, 100 mV_{pp} superimposed on LDO_IN, C_L = 4.7 µF, ESR = 0.25 Ω, I_O = 5 mA			50		dB
LDO current limit	Short circuit peak current‡	LDO_OUT is enabled into a short to ground	T_J = −40°C to 110°C		0.7	2	A
	Overload or short circuit dc current limit	LDO_OUT is over-loaded or enabled into a short to ground	T_J = −40°C to 110°C	250	325	500	mA
LDO forward leakage current I_{LK_LDO}	Current into pin LDO_OUT	$V_{O(LDO_OUT)}$ = 0 V, $V_{I(LDO_IN)}$ = 5.5 V, $V_{I(EN_LDO)}$ = 0 V				10	µA
LDO reverse leakage current I_{RLK_LDO}	Current into pin LDO_OUT	$V_{O(LDO_OUT)}$ = 5.5 V, $V_{I(LDO_IN)}$ = 0 V, $V_{I(EN_LDO)}$ = 0 V				10	
t_{ON_LDO}	Turnon time	From 50% $V_{I(EN_LDO)}$ to 90% $V_{O(LDO_OUT)}$, R_L = $V_{O(LDO_OUT)}$/0.2, C_L = 10 µF (20%)		0.1	0.35	1	ms
t_{OFF_LDO}	Turnoff time	From 50% $V_{I(EN_LDO)}$ to 10% $V_{O(LDO_OUT)}$, R_L = $V_{O(LDO_OUT)}$/0.2, C_L = 10 µF (20%)		0.1	0.4	1	
	$V_{O(LDO_OUT)}$ ramp-up time (0% to 90%)	$V_{I(EN_LDO)}$ = 5V, $V_{I(LDO_IN)}$ ramping up from 10% to 90% in 0.1 ms, R_L = $V_{O(LDO_OUT)}$/0.2, C_L = 10 µF (20%)		0.1	0.65	1	
LDO pulldown transistor current		$V_{I(PLDN_LDO)}$ = 3.3 V		9	15		mA
		$V_{I(LDO_PLDN)}$ = 1 V			5		

‡ Not tested in production.

undervoltage lockout, LDO_IN

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO UVLO rising threshold				2.7	V
LDO UVLO falling threshold		2.25		2.45	V
UVLO hysteresis‡		250			mV

‡ Not tested in production.

electrical characteristics over recommended operating junction temperature range, $V_{I(SW_IN)}$ = 3.3 V for TPS2140/50, $V_{I(SW_IN)}$ = 5 V for TPS2141/51, $V_{I(LDO_IN)}$ = 5 V, all outputs unloaded (unless otherwise noted) (continued)

logic section ($\overline{SW_EN}$, SW_EN, LDO_EN, ADJ, SW_PG, LDO_PG)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic input current	$I_{I(/SW_EN)}$, source	$V_{I(/SW_EN)}$ = 0 V	1		5	µA
	$I_{I(SW_EN)}$, sink	$V_{I(SW_EN)}$ = 5 V	1		5	
	$I_{I(LDO_EN)}$	$V_{I(EN_LDO)}$ = 0 V – 5.5 V	−1		1	
Logic input high level	$V_{IH_MIN(/SW_EN)}$		2			V
	$V_{IH_MIN(SW_EN)}$		2			
	$V_{IH_MIN(LDO_EN)}$		2			
Logic input low level	$V_{IL_MAX(/SW_EN)}$				0.8	V
	$V_{IL_MAX(SW_EN)}$				0.8	
	$V_{IL_MAX(LDO_EN)}$				0.8	
Floating input voltage	$V_{IF(/SW_EN)}$	$\overline{SW_EN}$ pin is open	2.5			V
	$V_{IF(SW_EN)}$	SW_EN pin is open			0.4	
LDO feedback input current	$I_{I(ADJ)}$	$V_{I(ADJ)}$ = 0 V – 5.5 V	−1		1	µA
SW_PG sense threshold, V_{TH_SW}	TPS2140, TPS2150	Percentage of $V_{I(SW_IN)}$	85%	88%	90%	
	TPS2141, TPS2151					
LDO_PG sense threshold, V_{TH_LDO}		A percentage of output voltage set point V_{SET}, derived from a resistor divider	92%	94%	96%	
PG hysteresis (all)‡	V_{TH_HYS}		2%	2.5%	3.5%	
SW_PG rising edge deglitch‡	$t_{d_SWPG_rise}$		1	2.5		ms
PG falling edge deglitches times (all)‡	$t_{d_PG_fail}$		50	150		µs
SW_PG minimum output high state voltage	$V_{OH_MIN(SW_PG)}$	Source current $I_{O(SW_PG)}$ = 1 mA, $V_{I(SW_OUT)} > V_{TH_SW}$	$V_{I(SW_IN)}$ –0.5			V
SW_PG maximum output low state voltage	$V_{OL_MAX(SW_PG)}$	Sink current $I_{O(SW_PG)}$ = 1 mA, $V_{I(SW_OUT)} < V_{TH_SW}$			0.5	
LDO_PG maximum output low state voltage	$V_{OH_MIN(LDO_PG)}$	Sink current $I_{O(SW_PG)}$ = 1 mA, $V_{I(LDO_OUT)} < V_{TH_LDO}$			0.5	
LDO_PG leakage current	$I_{LK(LDO_PG)}$	$V_{O(LDO_PG)}$ = 5.5 V		1		µA

‡ Not tested in production.

thermal shutdown characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low thermal shutdown (whole device)	Over temperature trip point‡	Switch and/or LDO in current limit	125		137	°C
	Hysteresis‡			10		
High thermal shutdown (whole device)	Over temperature trip point‡	Switch and LDO are not in current limit	155		170	°C
	Hysteresis‡			10		

‡ Not tested in production.

PARAMETER MEASUREMENT INFORMATION

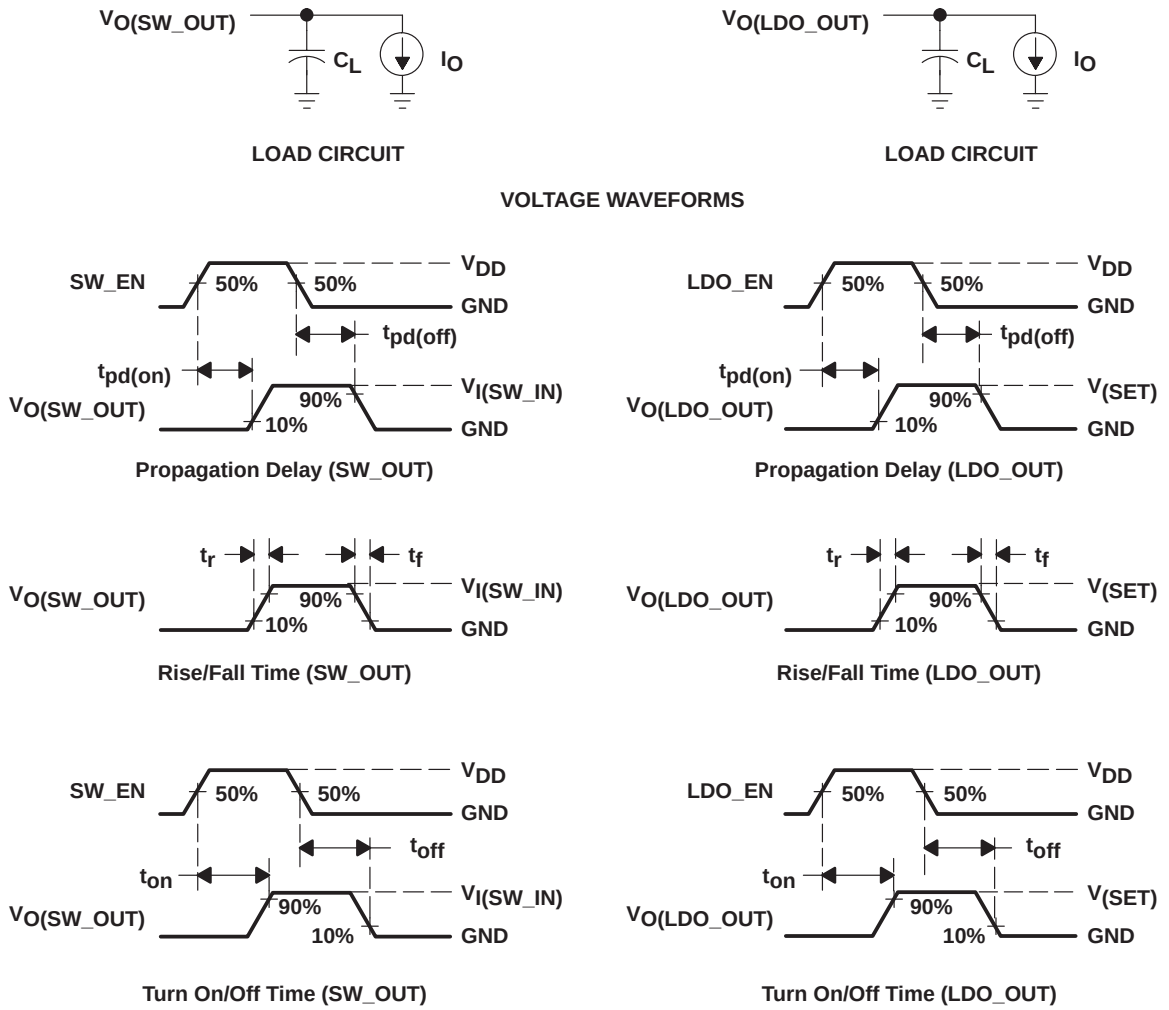


Figure 1. Test Circuits and Voltage Waveforms

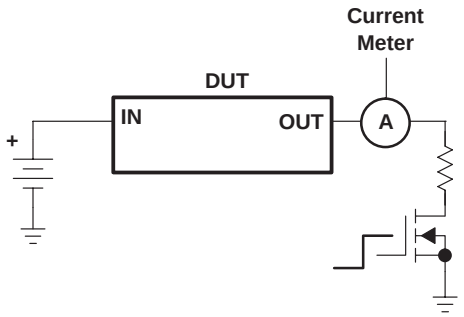


Figure 2. Current Limit Test Circuit

PARAMETER MEASUREMENT INFORMATION

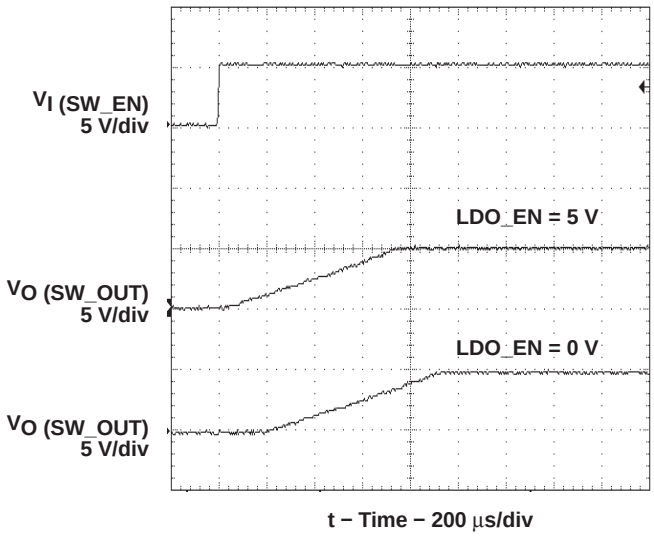


Figure 3. Switch Turnon Delay and Rise Time With 10-μF Load (SW_OUT Shorted With SW_PLDN)

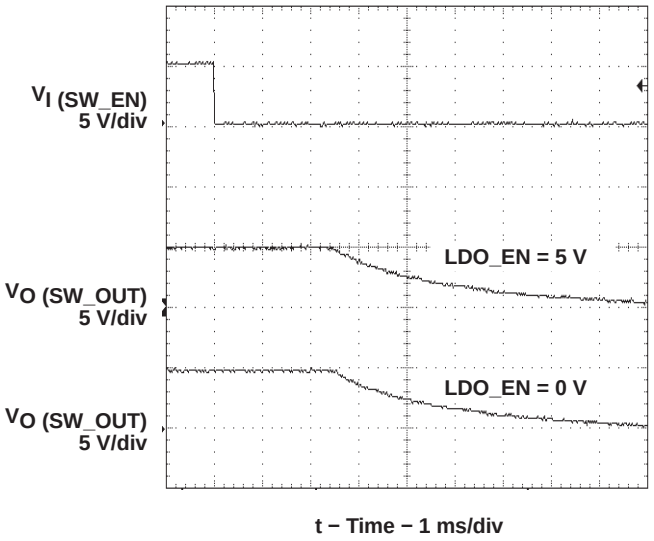


Figure 4. Switch Turnoff Delay and Fall Time With 10-μF Load (SW_OUT Shorted With SW_PLDN)

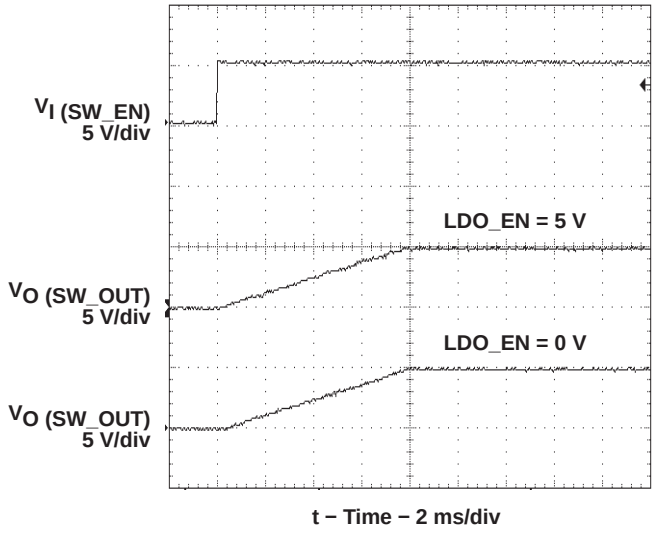


Figure 5. Switch Turnon Delay and Rise Time With 120-μF Load (SW_OUT Shorted With SW_PLDN)

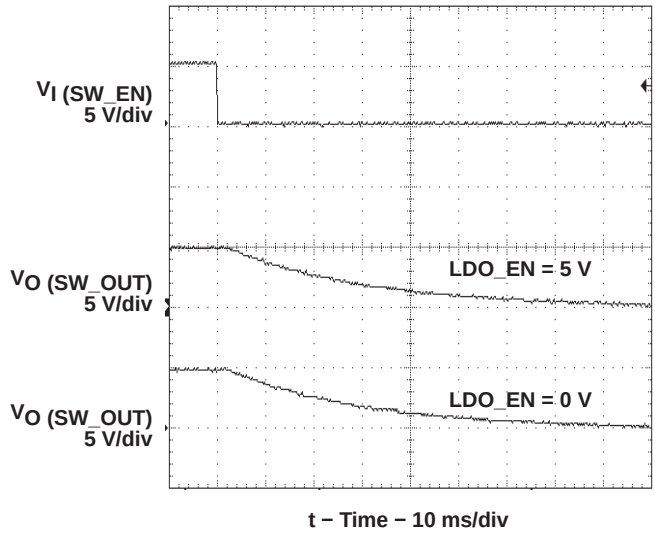


Figure 6. Switch Turnoff Delay and Fall Time With 120-μF Load (SW_OUT Shorted With SW_PLDN)

PARAMETER MEASUREMENT INFORMATION

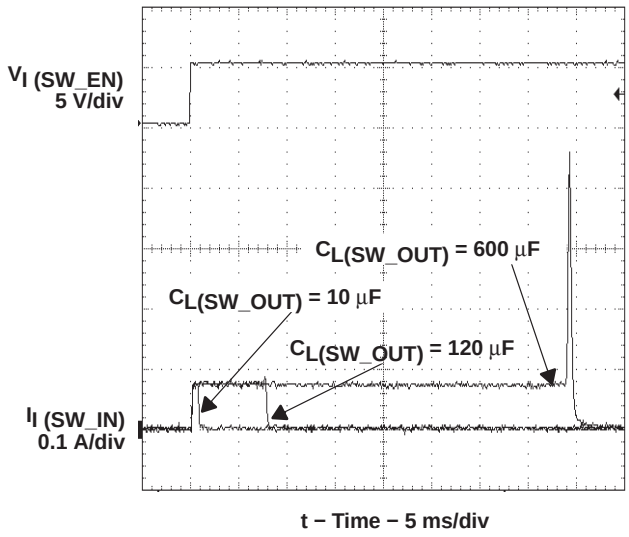


Figure 7. Switch Turnon Inrush Current With Different Load Capacitance

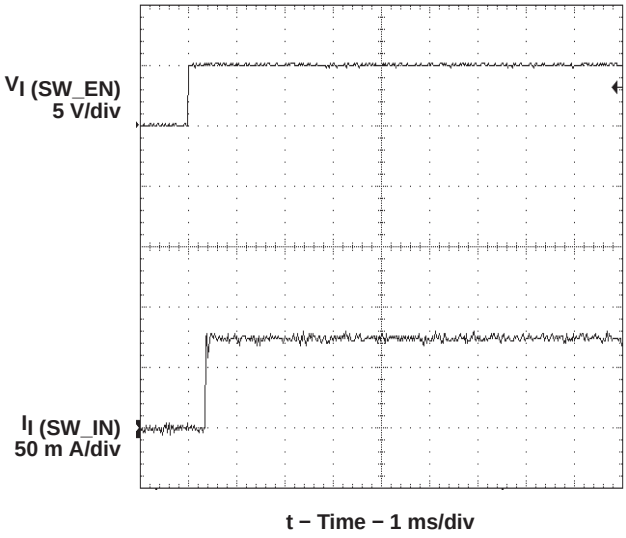


Figure 8. Switch Short-Circuit Current, With Switch Enabled Into a Short Circuit

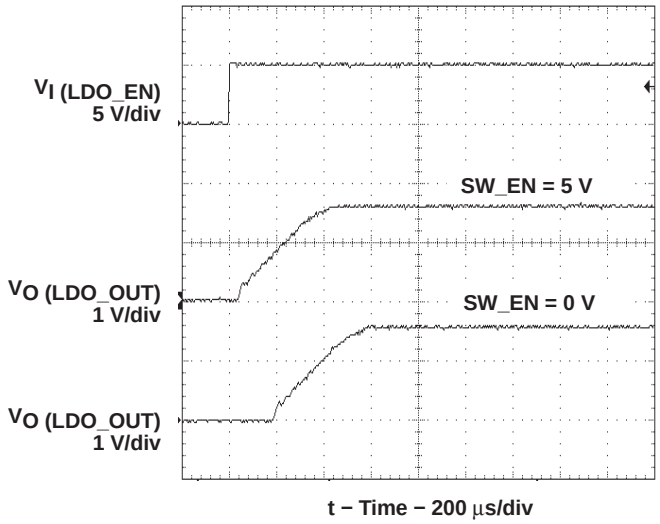


Figure 9. LDO Turnon Delay and Rise Time With 4.7 μF Load (LDO_OUT Shorted With LDO_PLDN)

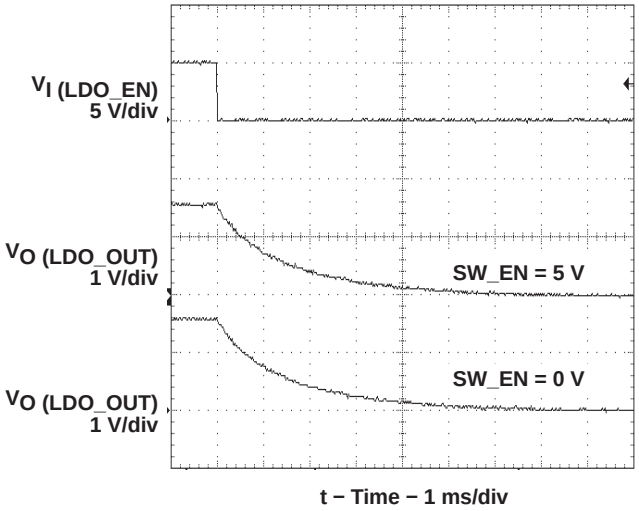


Figure 10. LDO Turnoff Delay and Fall Time With 4.7 μF Load (LDO_OUT Shorted With LDO_PLDN)

PARAMETER MEASUREMENT INFORMATION

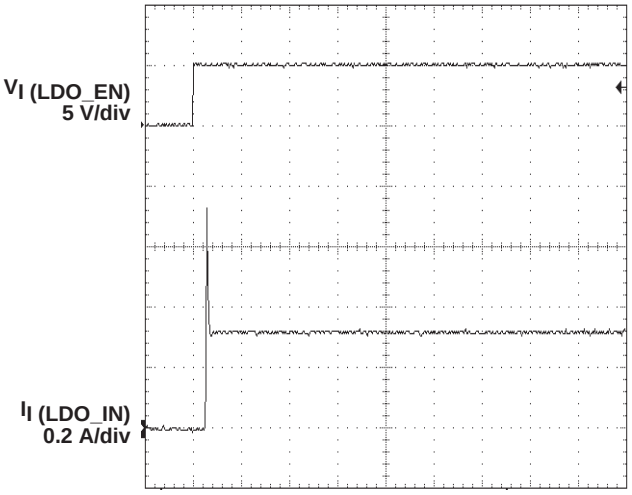


Figure 11. LDO Short-Circuit Current, With LDO Enabled Into a Short Circuit

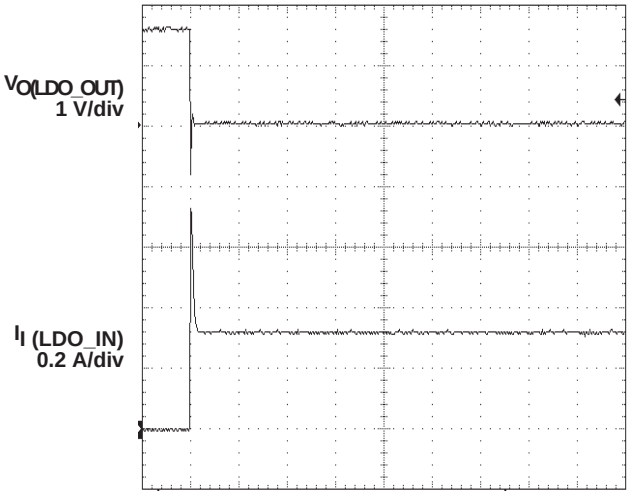


Figure 12. LDO Short-Circuit Current, With Short Circuit Connected Into Enabled LDO

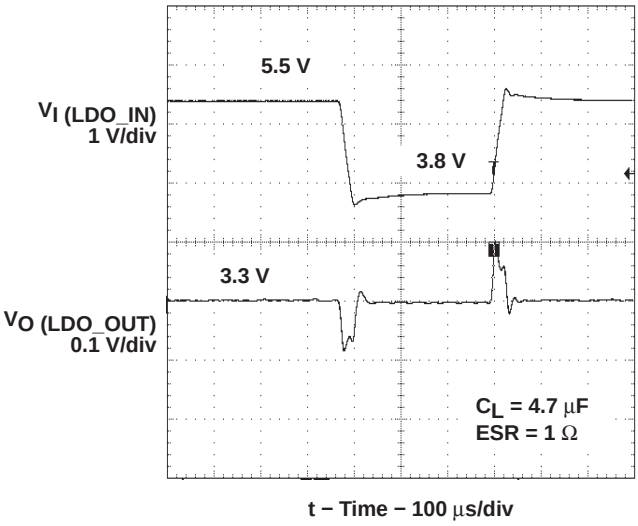


Figure 13. LDO Line Transient Response

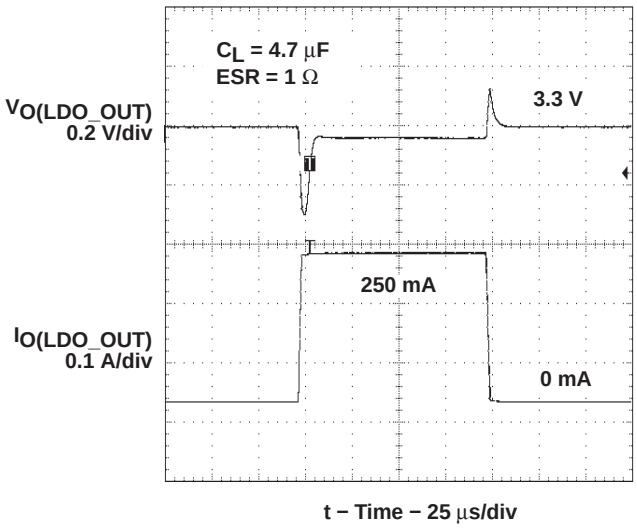


Figure 14. LDO Load Transient Response

PARAMETER MEASUREMENT INFORMATION

**LDO TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
LOAD CURRENT**

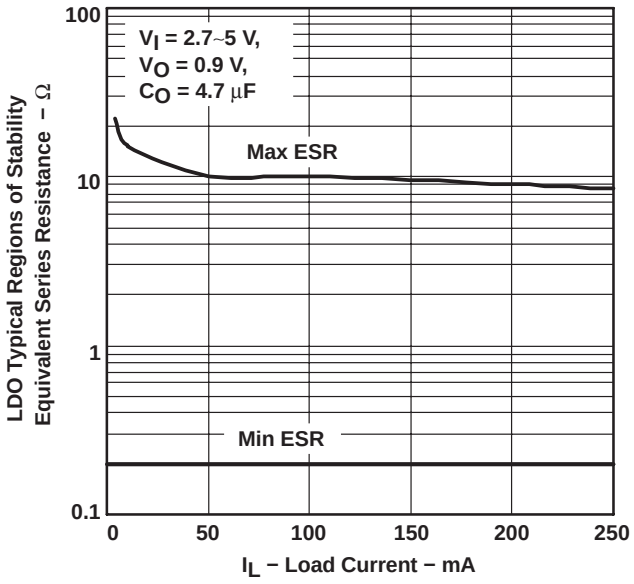


Figure 15

**LDO TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
LOAD CURRENT**

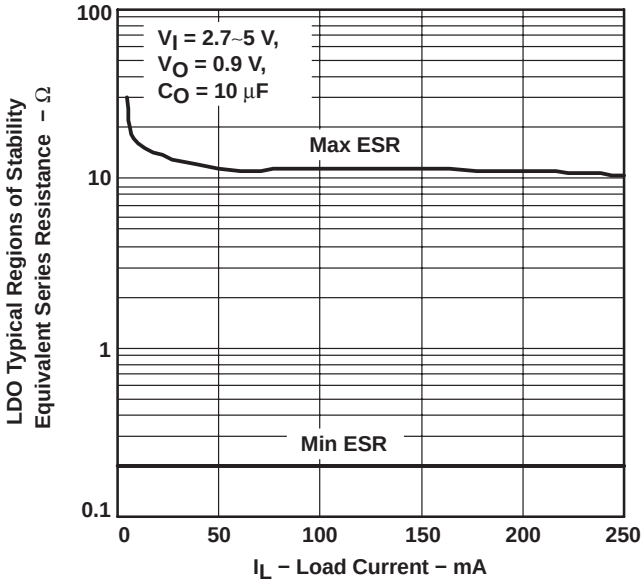


Figure 16

**LDO TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
LOAD CURRENT**

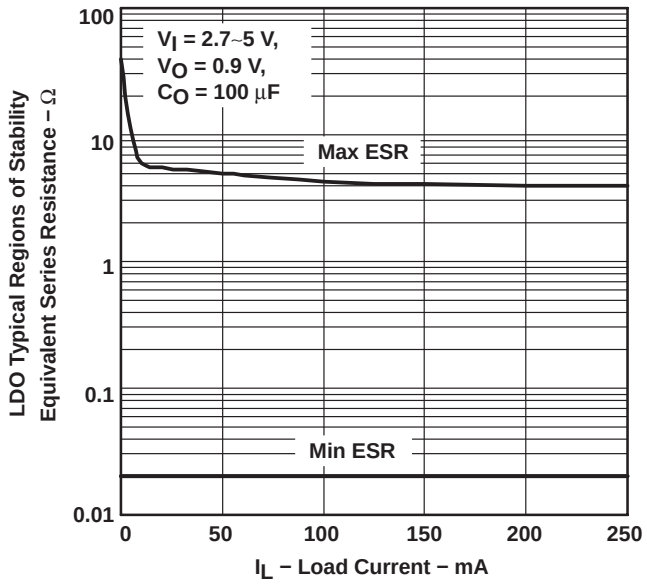


Figure 17

**SUPPLY CURRENT
vs
JUNCTION TEMPERATURE**

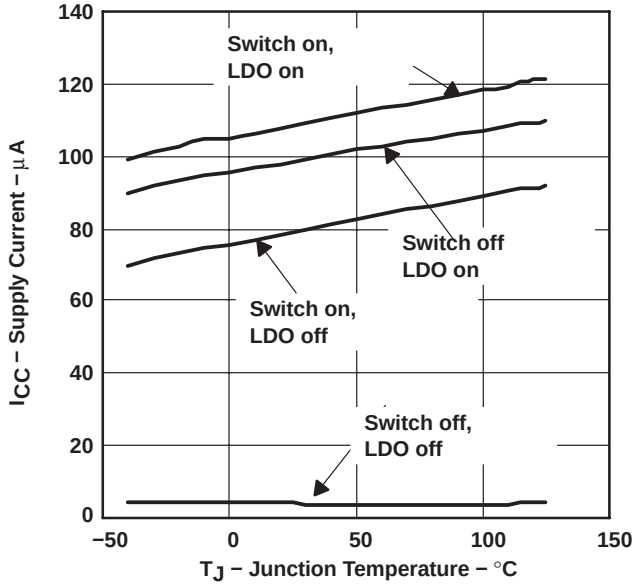


Figure 18

PARAMETER MEASUREMENT INFORMATION

SUPPLY CURRENT vs SUPPLY VOLTAGE

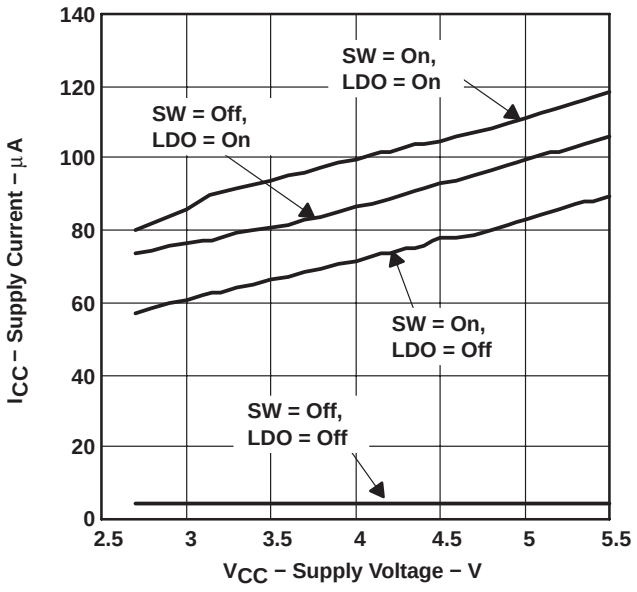


Figure 19

SWITCH STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

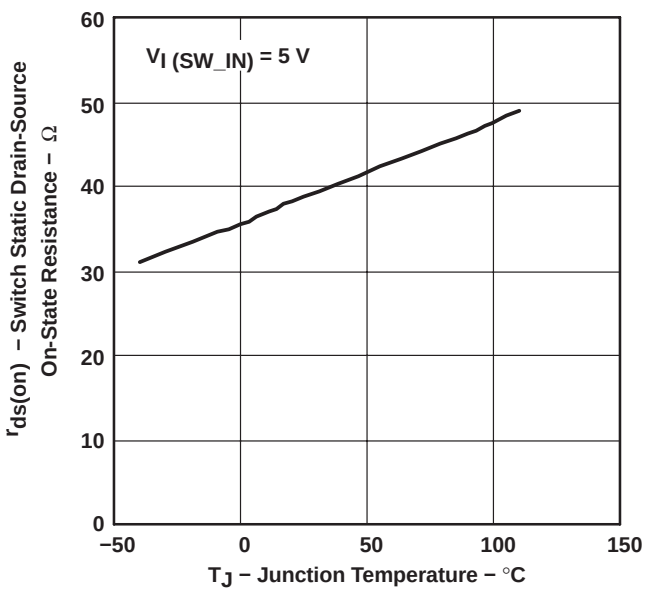


Figure 20

TPS2140
STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs SUPPLY VOLTAGE

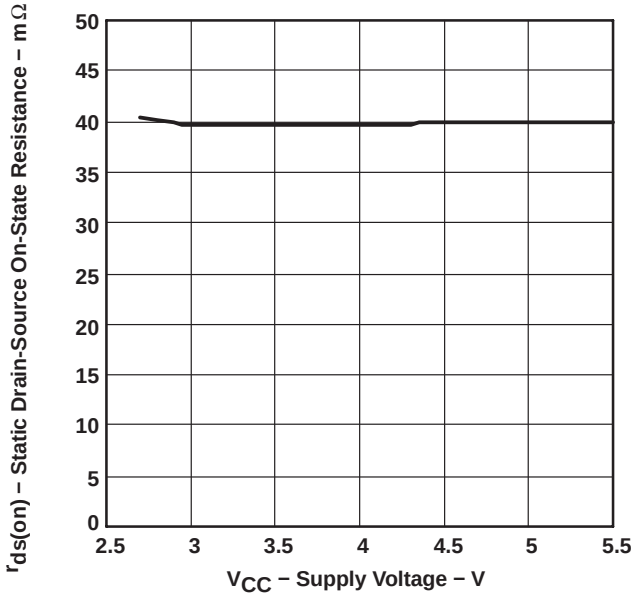


Figure 21

SWITCH SHORT-CIRCUIT CURRENT vs JUNCTION TEMPERATURE

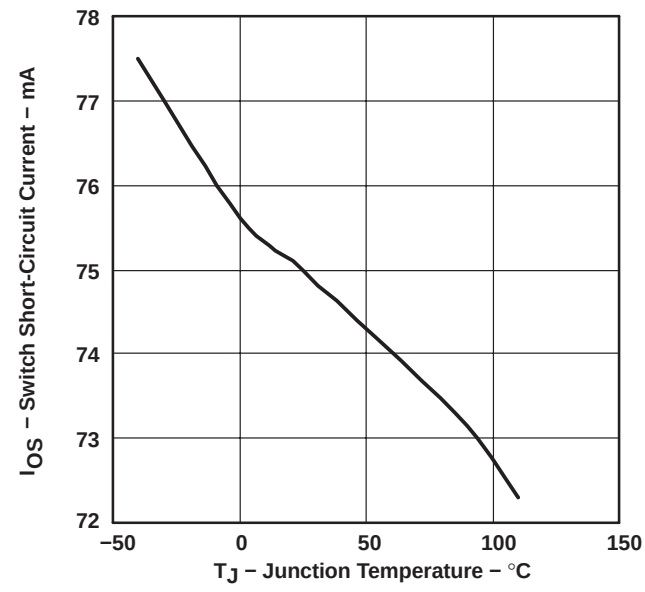


Figure 22

PARAMETER MEASUREMENT INFORMATION

SWITCH SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

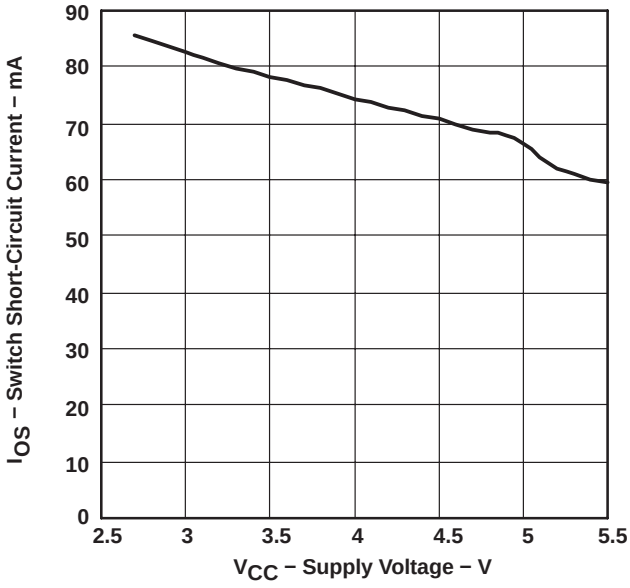


Figure 23

LDO SHORT-CIRCUIT CURRENT vs JUNCTION TEMPERATURE

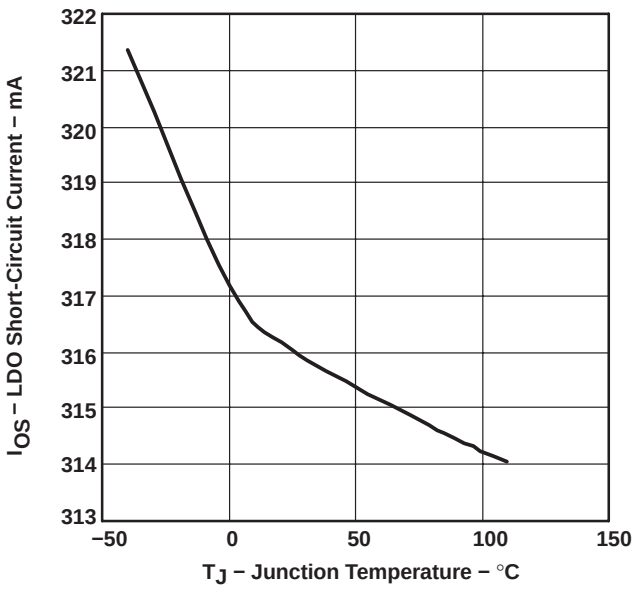


Figure 24

LDO SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

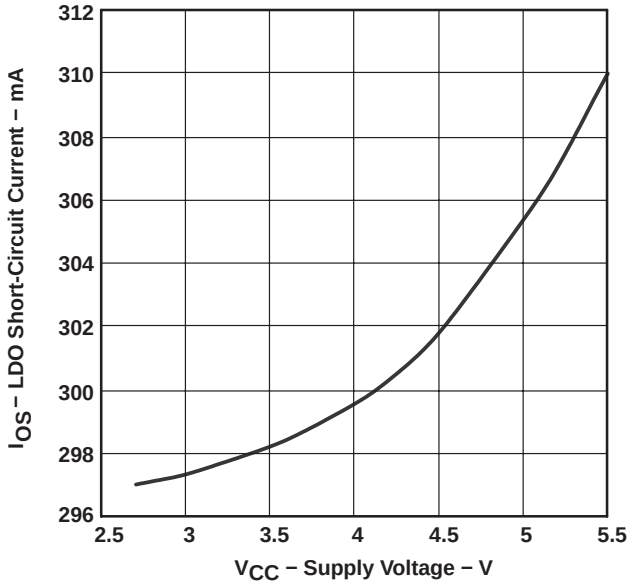


Figure 25

APPLICATION INFORMATION

external capacitor requirements on power lines

Ceramic bypass capacitors (0.01 μF to 0.1 μF) between SW_IN and GND and LDO_IN and GND, close to the device, are recommended to improve load transient response and noise rejection. Bulk capacitors (4.7 μF or higher) between SW_IN and GND and LDO_IN and GND are also recommended, especially if load transients in the hundreds of milliamps with fast rise times are anticipated. A 66-μF bulk capacitor is recommended from SW_OUT to ground, especially when the output load is heavy. This precaution helps reduce transients seen on the power rails. Additionally, bypassing the outputs with a 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

LDO output capacitor requirements

Stabilizing the internal control loop of the LDO requires an output capacitor connected between LDO_OUT and GND. The minimum recommended capacitance is 4.7 μF with an ESR value between 200 mΩ and 8.5 Ω. Solid tantalum electrolytic, aluminum electrolytic and multilayer ceramic capacitors are all suitable, provided they meet the ESR requirements (see Figures 15, 16, and 17). The adjustable LDO (for output voltages lower than 3 V) requires a bypass capacitor across the feedback resistor as shown in Figure 26. The nominal value of this capacitor is determined by using the following equation:

$$C_f = \frac{1}{\left(63.7 \times 10^3 \times 2 \times 3.14 \times R1\right)} - 4\ pF \quad (1)$$

where R1 is derived by programming the adjustable LDO (see programming the adjustable LDO regulator section shown below).

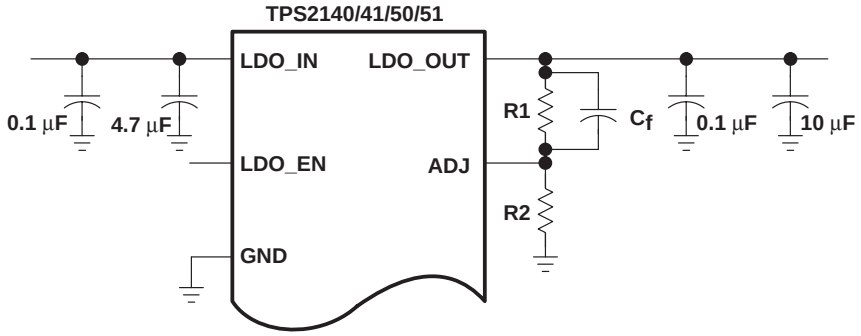


Figure 26. LDO External Resistor Divider

programming the adjustable LDO regulator

The output voltage of the TPS2140/41/50/51 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using equation 2:

$$LDO_OUT = V_{ref}\left(1 + \frac{R1}{R2}\right) \quad (2)$$

where V_{ref} = 0.8 V typical (internal reference voltage).

Resistors R1 and R2 should be chosen for approximately 4-μA (minimum) divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as a minimum load is required to sink the LDO forward leakage and maintain regulation. The recommended design procedure is to choose R2 = 200 kΩ to set the divider current at 4-μA and then solve the LDO_OUT equation for R1.

APPLICATION INFORMATION

programming the adjustable LDO regulator (continued)

Table 1. Output Voltage Programming Guide

OUTPUT VOLTAGE	R1	R2	Cf
3.3	619 kΩ	200 kΩ	NR†
3.0	549 kΩ	200 kΩ	NR†
2.5	422 kΩ	200 kΩ	2 pF
1.8	249 kΩ	200 kΩ	6 pF
1.5	174 kΩ	200 kΩ	10.3 pF
1.0	49.9 kΩ	200 kΩ	46 pF

† NR − Not required

overcurrent

When an overcurrent condition is detected, the device maintains a constant output current. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output is shorted before the device is enabled. Once enabled the TPS2140/41/50/51 sense the short and immediately switch to a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2140/41/50/51 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

dual current limit

The TPS2140/41/50/51 has a dual-current-limited power switch. When the output voltage of the power switch is below a defined power-good threshold voltage, the typical current the switch can conduct is approximately 75 mA. Therefore, the inrush current can be limited to about 75 mA even if there is a very large capacitor on the load. When the switch output voltage reaches the power-good threshold voltage, the internal controller enables the higher current limit, which is at least 0.8 A and at most 1.8 A. This dual-current-limit feature completely solves the large inrush current problems that most power management applications experience. Figure 7 shows the inrush currents with different load capacitance. The current spike at C_L = 600 µF is due to voltage difference between input and output once the higher current limit is enabled.

Because the lower current limit is only about 75 mA, the initial resistive load or equivalent load current on the switch output must be less than 50 mA, excluding the load capacitors.

APPLICATION INFORMATION

power dissipation and junction temperature

The major source of power dissipation for the TPS2140/41/50/51 comes from the internal voltage regulator and the N-channel MOSFET. Checking the power dissipation and junction temperature is always a good design practice and it starts with determining the $r_{DS(on)}$ of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the graphs shown in the Typical Characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated using:

$$P_D = r_{DS(on)} \times I^2 \quad (3)$$

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = \left(V_I - V_{O(min)}\right) \times I_O \quad (4)$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(LDO)} + P_{D(switch)} \quad (5)$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (6)$$

Where:

T_A = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance °C/W, equal to inverting the derating factor found on the power dissipation table in this data sheet.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The overcurrent faults force the TPS2140/41/50/51 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

If either the power distribution switch or the LDO is in overcurrent, a thermal sensor trips at approximately 135°C, turning off both circuits. Normal operation resumes when the die temperature drops approximately 10°C. If neither the power distribution switch nor the LDO is in overcurrent, a second thermal sensor trips at approximately 160°C. Normal operation resumes when the die temperature drops approximately 10°C.

APPLICATION INFORMATION

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the device (LDO and switch) is in the off state at power up. The UVLO also keeps the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO is also activated whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This function facilitates the design of hot-insertion systems where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches are turned on with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a multiplexed serial bus operating at either 12 Mbps, or 1.5 Mbps for USB 1.1, or 480 Mbps for USB 2.0. The USB interface is designed to accommodate the bandwidth required by PC peripherals such as keyboards, printers, scanners, and mice. The four-wire USB interface was conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

The TPS2140/41/50/51 are well suited for USB hub and peripheral applications. The internal LDO can be used to provide the 3.3-V power needed by the controller while the switch distributes power to the downstream functions.

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus−powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

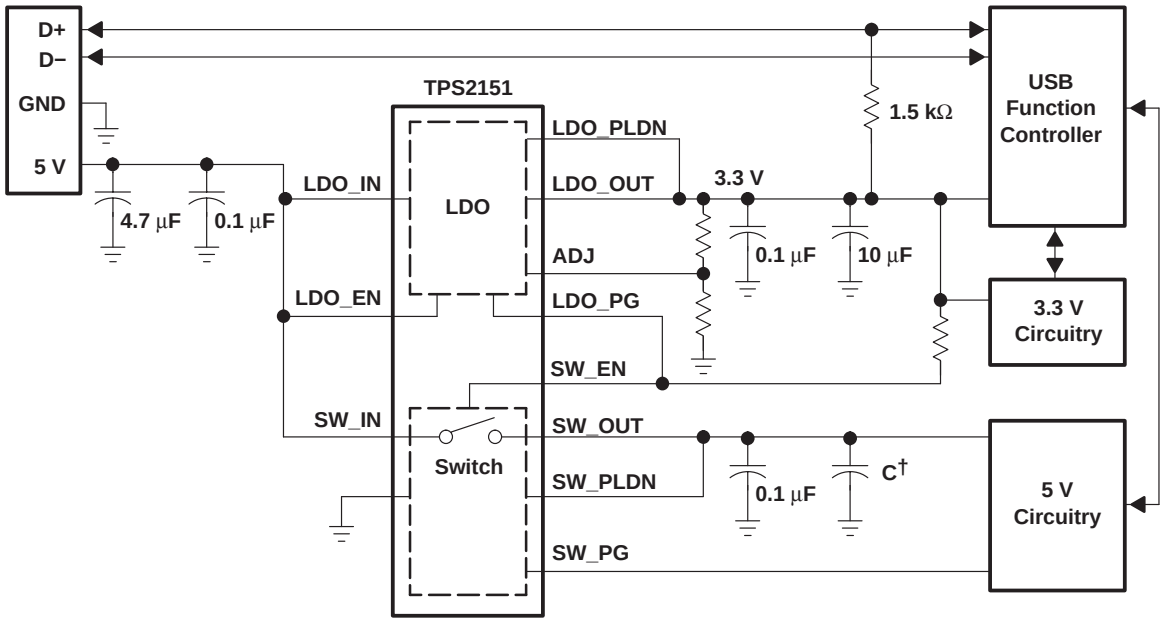
APPLICATION INFORMATION

USB power-distribution requirements (continued)

The feature set of the TPS2140/41/50/51 allows them to meet the requirements of functions. The integrated current-limiting is required by hubs and peripheral functions. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions.

USB applications

Figure 27 shows the TPS2151 being used in a USB bus-powered peripheral design. The internal 3.3-V LDO is used to provide power for the USB function controller as well as to the 1.5-kΩ pullup resistor. One example of USB bus-powered peripheral applications is the USB ADSL modem, which needs several power rails and power sequencing.



† C can be very high-value capacitance

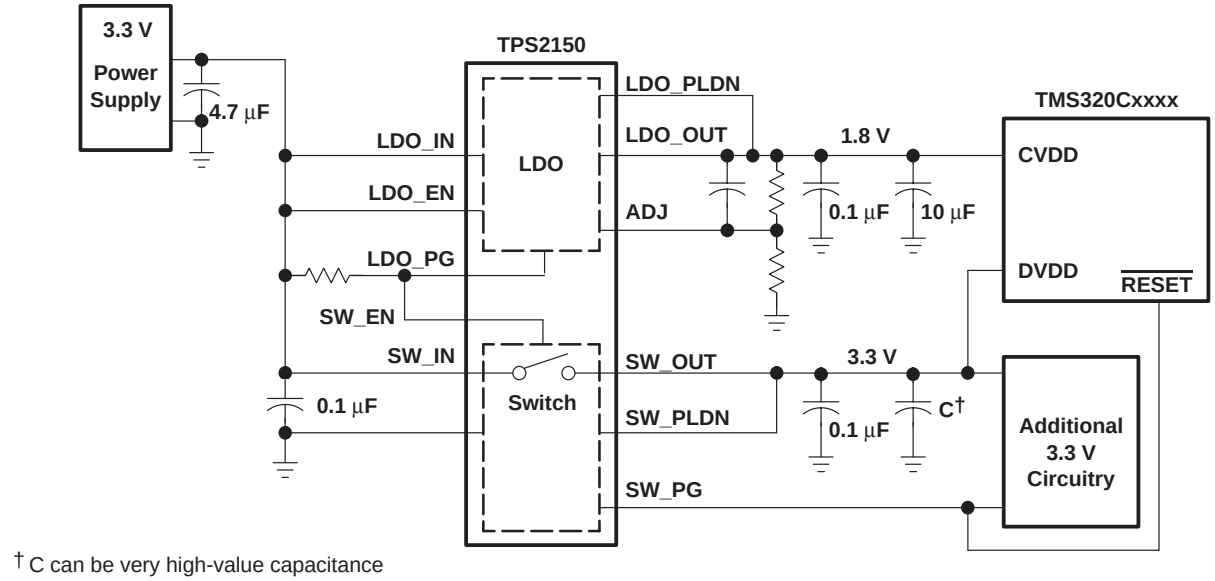
Figure 27. Bus-Powered USB Peripheral Application

APPLICATION INFORMATION

DSP applications

Figure 28 shows the TPS2150 in a DSP application. DSPs use 1.8-V core voltage and 3.3-V I/O voltage. In this type of application the TPS2150 adjustable LDO is configured for a 1.8-V output specifically for the DSP core voltage.

The additional 3.3-V circuitry is powered through the switch of the TPS2150 only after the DSP is up and running.



† C can be very high-value capacitance

Figure 28. DSP Power Sequencing Application

system level design consideration of DSP power application

System level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as (or prior to and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus preventing bus contention with other chips on the board.

For some DSP systems, the core supply may be required to provide a considerable amount of current until the I/O supply is powered up. This extra current condition is a result of uninitialized logic within the DSP(s). Decreasing the amount of time between the core supply power up and the I/O supply power up can minimize the effects of this current draw.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2140IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2140I	Samples
TPS2141IPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2141I	Samples
TPS2141IPWPG4	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2141I	Samples
TPS2141IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2141I	Samples
TPS2141IPWPRG4	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2141I	Samples
TPS2150IPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2150I	Samples
TPS2150IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2150I	Samples
TPS2151IPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2151I	Samples
TPS2151IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2151I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

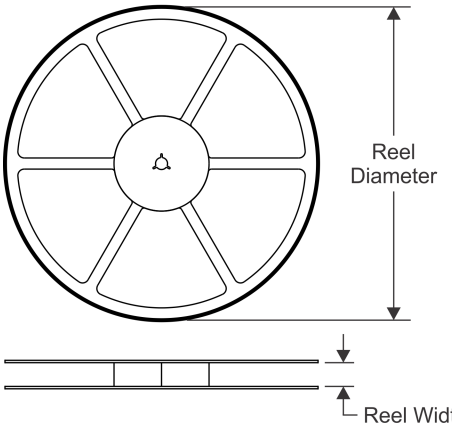
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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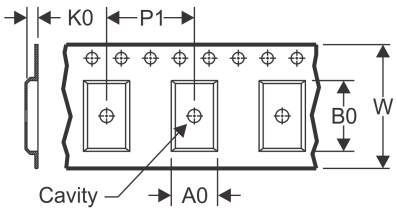
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

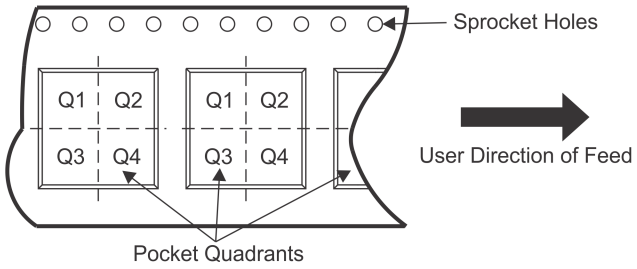


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

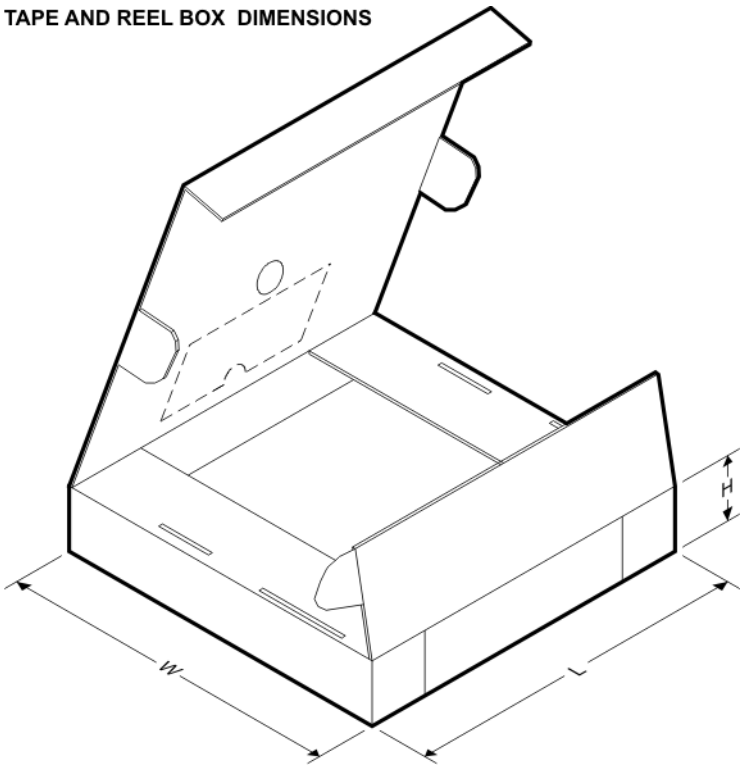
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2140IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2141IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2150IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2151IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

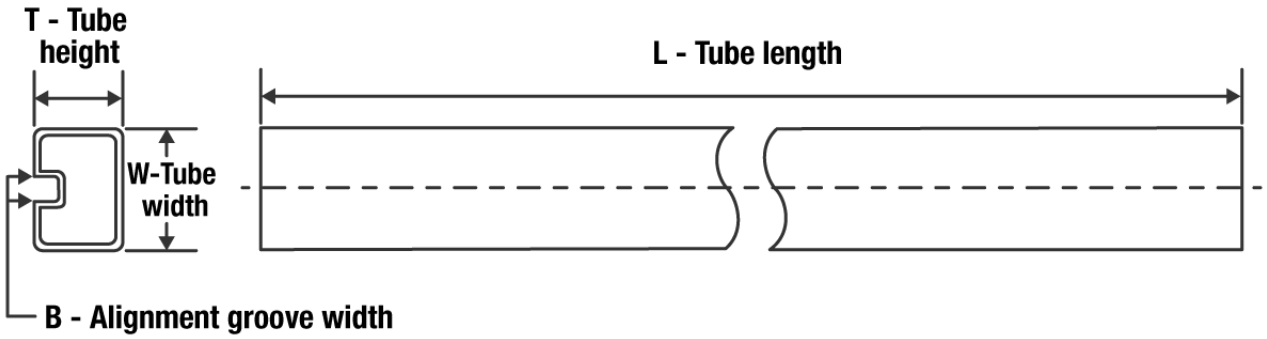
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2140IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS2141IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS2150IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS2151IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

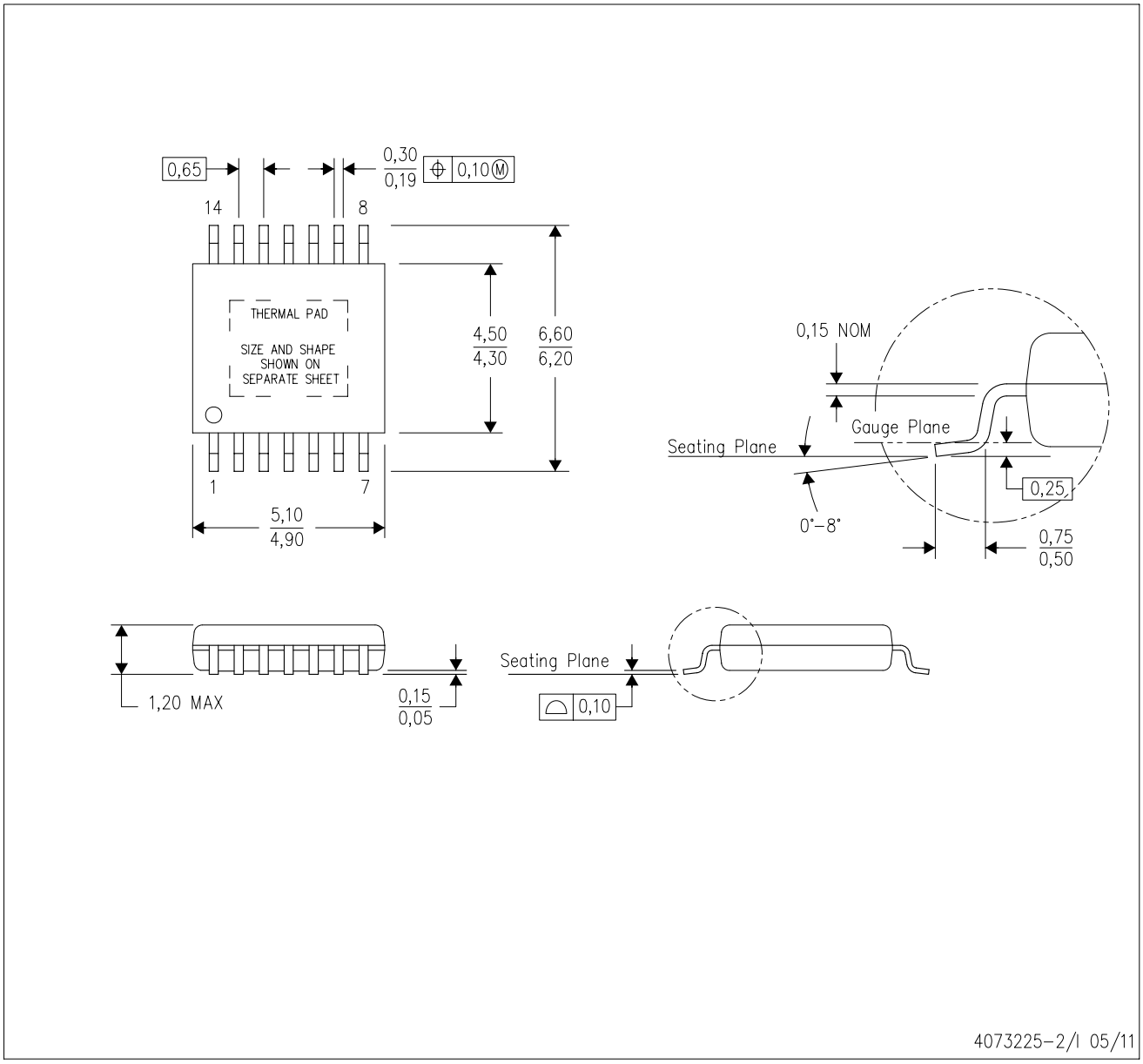
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2141IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2141IPWPG4	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2150IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2151IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

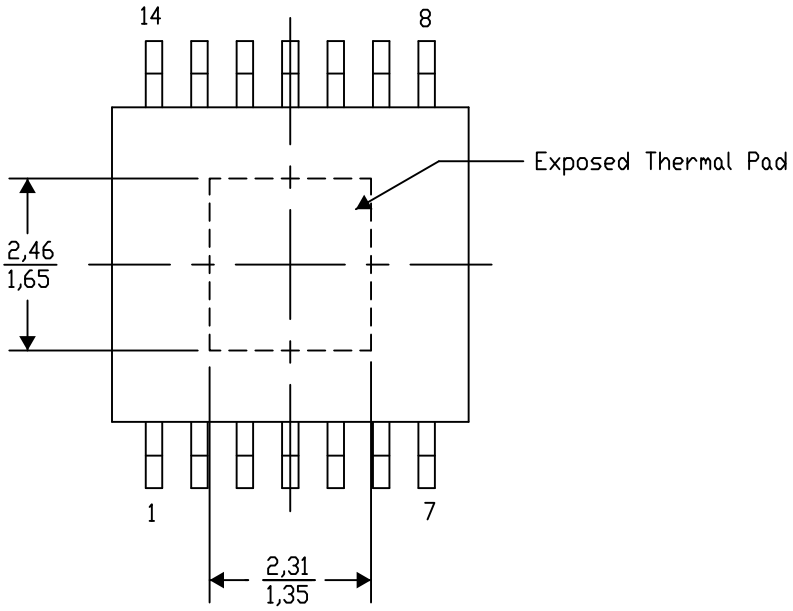
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

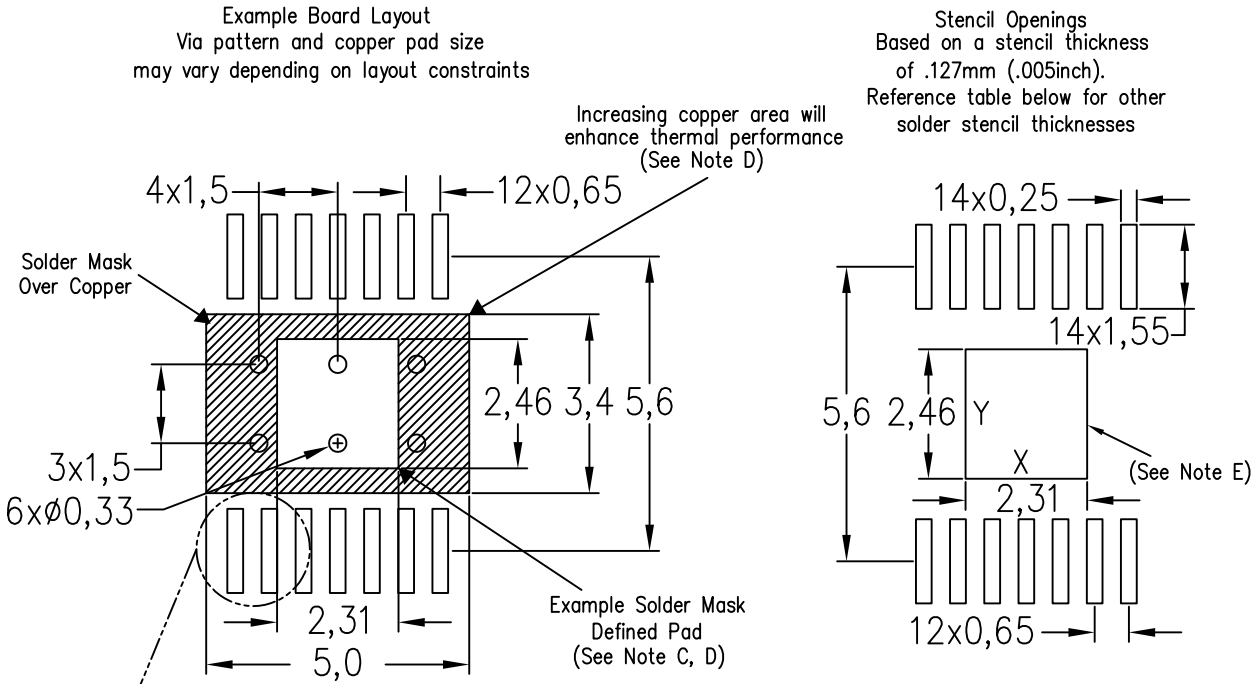
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

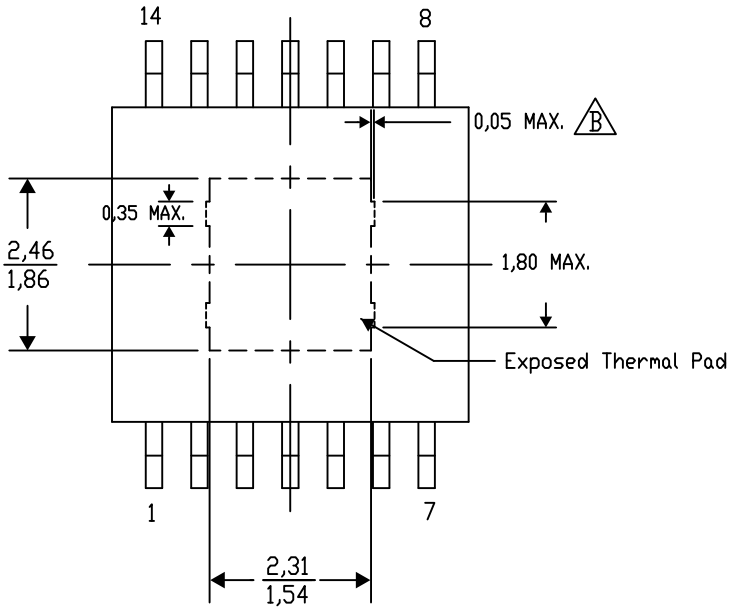
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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Top View

Exposed Thermal Pad Dimensions

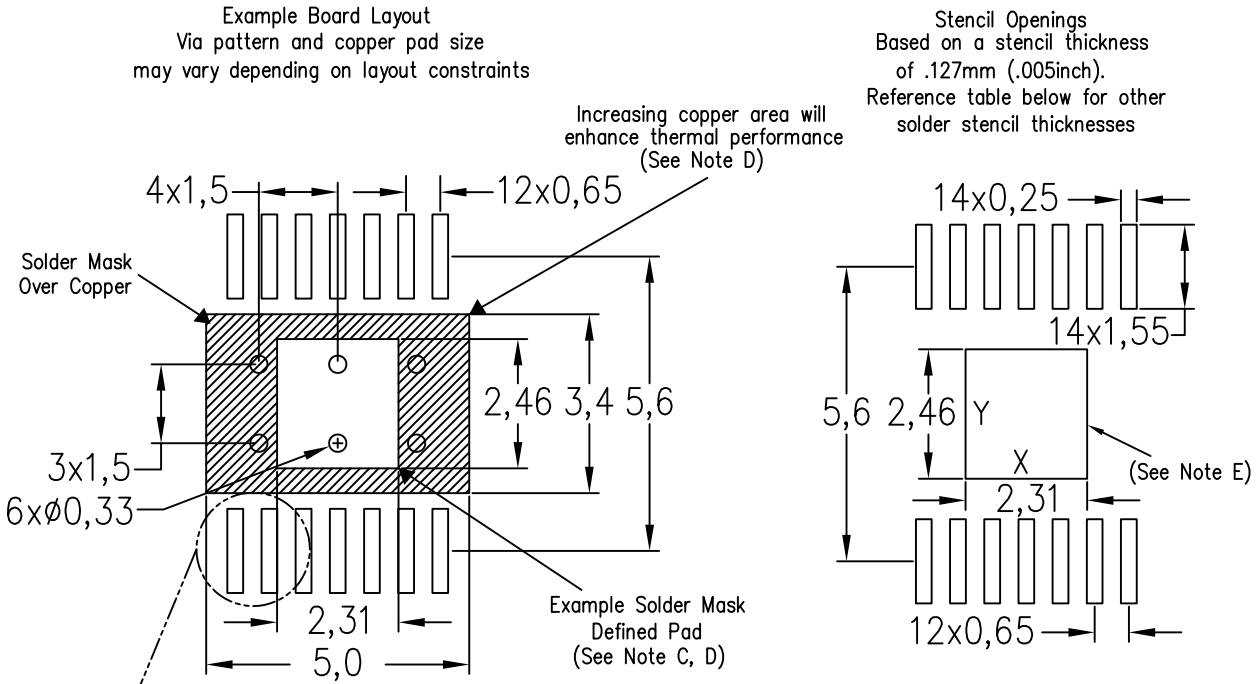
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
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F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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