

# TPS23523: -48V 热插拔 and Single OR-ing 控制器

## 1 特性

- -10V 至 -80V 直流工作电压，绝对最大电压为 -200V
- 软启动电容器断开
- 双路热插拔栅极驱动器
- 400 $\mu$ A 栅极拉电流
- 双路限流（基于  $V_{DS}$ ）
  - 25mV  $\pm$ 4% ( $V_{DS}$  低时)
  - 3mV  $\pm$ 25% ( $V_{DS}$  高时)
- 可编程过压 ( $\pm$ 1.5%) 与欠压 ( $\pm$ 2%)
  - 可编程迟滞 ( $\pm$ 11%)
- 集成式 OR-ing 控制器
  - 调整电压: 25mV  $\pm$ 15mV
  - 快速关断电压: -6mV  $\pm$ 4mV
- 超时而重试
- 16 引脚 TSSOP 封装

## 2 应用

- 远程无线电单元
- 基带单元
- 路由器和切换器
- 小型基站
- -48V 电信基础设施

## 3 说明

TPS23523 是一款集成式热插拔 OR-ing 控制器，可使大功率电信系统符合严苛的瞬态要求。该器件具有 200V 的绝对最大额定电压，因此可轻松通过雷击浪涌测试 (IEC61000-4-5)。借助软启动电容器断开功能，可通过限制浪涌电流来使用较小的热插拔 FET，而不会影响瞬态响应。双路热插拔栅极驱动器可以在需要多个热插拔 FET 的应用中节省空间并降低 BOM 成本。400 $\mu$ A 拉电流支持快速恢复，有助于避免雷击浪涌测试期间的系统复位。借助双路限流功能，可轻松达到 ATIS 0600315.2013 等标准所规定的掉电和输入阶跃要求。最后，该器件还可提供带可编程阈值和迟滞的精确欠压和过压保护。

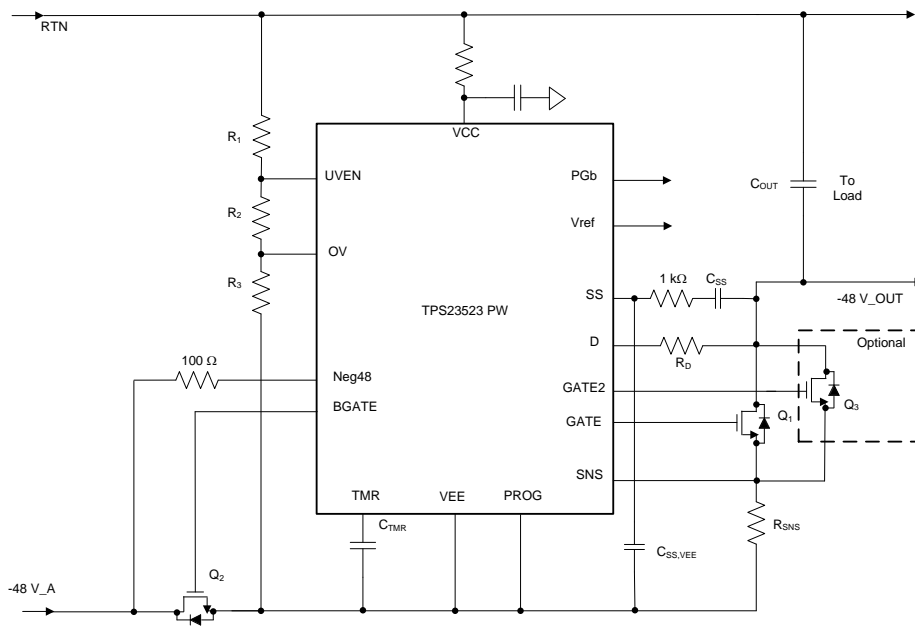
TPS23523 集成有 OR-ing 控制器，因此非常适合用于需要反向连接保护和反向电流保护的 -48V 系统。输入下降时，OR-ing 控制器可保护输出，从而避免系统复位。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TPS23523	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 简化原理图



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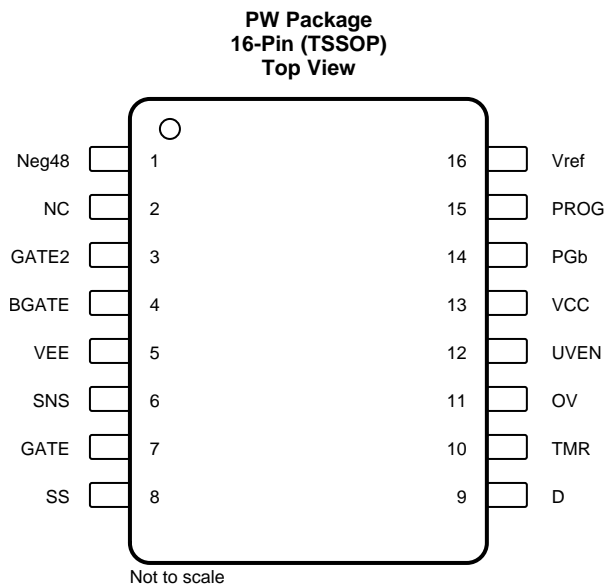
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## 4 修订历史记录

Changes from Original (December 2017) to Revision A	Page
• Added a row for $V_D$ in the <i>Absolute Maximum Ratings</i> table .....	4
• Added tablenote 2 to the <i>Absolute Maximum Ratings</i> table .....	4
• Updated <a href="#">Equation 12</a> .....	20
• Updated <a href="#">Equation 22</a> .....	22

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Neg48	1	I	Input to the OR-ing controller for the –48 feed. The TPS23523 will regulate the drop from VEE to Neg48 to 25 mV to mimic an ideal diode.
NC	2		No connect to space high voltage pins.
GATE2	3	O	Gate driver for the 2nd hot swap FET. NC if feature isn't used.
BGATE	4	O	Gate driver for the OR-ing FET.
VEE	5	GND	This pin corresponds to the IC GND. Kelvin sense to the bottom of R <sub>SNS</sub> to ensure accurate current limit.
SNS	6	I	Sense pin, used to measure current and regulate it. Kelvin Sense to R <sub>SNS</sub> to ensure accurate current limits.
GATE	7	O	Gate drive for the main hot swap FET.
SS	8	O	Pin used for soft starting the output. Connect a capacitor (C <sub>SS</sub> ) between the SS pin and -48V_OUT. The dv/dt rate on the -48V_OUT pin is proportional to the gate sourcing current divided by C <sub>SS</sub> .
D	9	I	Pin used to sense the drain of the hot swap FET and to program the threshold where the hot swap switches from the CL1 and CL2. Connect a resistor from this pin to the drain of the hot swap FET (also called -48V_OUT) to program the threshold.
TMR	10	O	Timer pin used to program the duration when the hot swap FET can be in current limit. Program this time by adding a capacitor between the TMR pin and VEE.
OV	11	I	Input overvoltage comparator. Tie a resistor divider to program the threshold where the device turns off due to overvoltage event.
UVEN	12	I	Input undervoltage comparator. Tie a resistor divider to program the threshold where the device turns on.
VCC	13	S	Clamped supply. Tie to RTN through resistor.
PGb	14	O	Power Good Bar, which is an open drain output that indicated when the power is good and the load can start drawing full power. PGb goes low when the hot swap is fully on and the DC/DC can draw full power.
PROG	15	I	Adjust current limit and fast trip threshold by tying to VEE, floating, or tying to VEE through resistor.
Vref	16	O	5V reference output. Connect to the base of a BJT to generate a rail that can be used to power current monitors and digital Isolators.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	$V_{VCC}$ (current into $V_{CC}$ <10 mA)	-0.3	20	V
Input voltage	$V_{SNS}$ , $V_{OV}$	-0.3	6.5	V
	$V_{UVEN}$ , $V_{SS}$	-0.3	30	V
	$V_D^{(2)}$	-0.3	40	V
Input voltage	$V_{Neg48}$	-0.3	200	V
	$V_{Neg48}$ through 100- $\Omega$ resistor	-1	200	V
	$V_{Neg48}$ through 1-k $\Omega$ resistor	-2	200	V
Output voltage	$V_{GATE}$ , $V_{GATE2}$ , $V_{BGATE}$	-0.3	VCC	V
	$V_{TMR}$ , $V_{PROG}$ , $V_{VREF}$	-0.3	6.5	V
Output voltage	$V_{PGb}$	-0.3	200	V
Operating junction temperature, $T_J$		-40	125	$^{\circ}$ C
Storage temperature, $T_{stg}$		-55	150	$^{\circ}$ C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Current into the Pin D should be limited to < 1 mA through RD resistor

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{VCC}$	Supply voltage (current into $V_{CC}$ <10 mA)	0		20	V
$V_{SNS}$ , $V_{OV}$	Input voltage	0		5.5	V
$V_{UVEN}$ , $V_D$ , $V_{SS}$	Input voltage	0		18	V
$V_{Neg48}$	Input voltage, through 100- $\Omega$ resistor	-0.2		150	V
$V_{GATE}$ , $V_{GATE2}$ , $V_{BGATE}$	Output voltage	0		VCC	V
$V_{TMR}$ , $V_{PROG}$ , $V_{VREF}$	Output voltage	0		5.5	V
$V_{PGb}$	Output voltage	0		80	V
$C_{SS}$	Capacitance	1		200	nF
$R_{SS}$	Resistance	1		10	k $\Omega$
$R_D$	Resistance	120		2,000	k $\Omega$
$R_{NEG48V}$	Resistance	100		1	k $\Omega$

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS23523	UNIT
		PW (TSSOP)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	98.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	31.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	44.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	43.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

–40°C ≤ T<sub>J</sub> ≤ 125°C, 1.1 mA < I<sub>VCC</sub> < 10 mA, V<sub>(UVEN)</sub> = 2 V, V<sub>(OV)</sub> = V<sub>(SNS)</sub> = V<sub>(D)</sub> = 0 V, V<sub>(SS)</sub> = GATEx = Hi-Z, V<sub>(TMR)</sub> = 0 V, –1 V < V<sub>(NEG48Vx)</sub> < 150 V, V<sub>ref</sub> = V<sub>PROG</sub> = Hi-Z; All pin voltages are relative to VEE (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>VCC – Clamped Supply</b>						
V <sub>(UVLO_VCC)</sub>	UVLO on VCC	rising	9	9.5	10	V
V <sub>(UVLO_VCC,hyst)</sub>	UVLO hysteresis on VCC	hysteresis	1		V	
V <sub>(VCC)</sub>	VCC regulation	1.1 < I <sub>(VCC)</sub> < 10 mA (current into VCC)	12	14.5	18	V
I <sub>Q</sub>	Quiescent Current	V <sub>VCC</sub> = 10 V. Off	1		mA	
		V <sub>VCC</sub> = 10 V. On	1		mA	
		V <sub>VCC</sub> = 10 V, Gate and BGATE in regulation	1.1		mA	
<b>UVEN – Undervoltage and Enable</b>						
V <sub>(UVEN_T)</sub>	Threshold voltage for V <sub>(UVEN)</sub>		0.985	1	1.015	V
I <sub>(UV_hyst)</sub>	Hysteresis current, sourcing from UV pin	V <sub>UV</sub> = 1.5 V	9	10	11.2	μA
<b>OV – Overvoltage</b>						
V <sub>(OV_T)</sub>	Threshold voltage for V <sub>OV</sub>		0.98	1	1.02	V
I <sub>(OV_hyst)</sub>	Hysteresis current, sourcing from OV pin	V <sub>OV</sub> = 1.5 V	9	10	11.2	μA
<b>TMR – Timer</b>						
V <sub>TMR</sub>	Voltage on timer when part times out.	V <sub>D</sub> = 0 V, TMR ↑, measure V <sub>TMR</sub> when V <sub>GATE</sub> = 0	1.47	1.5	1.53	V
V <sub>TMR2</sub>	Voltage on timer when part times out.	V <sub>D</sub> = 1 V, TMR ↑, measure V <sub>TMR</sub> when V <sub>GATE</sub> = 0	0.735	0.75	0.765	V
I <sub>TMR,SRS</sub>	Timer Sourcing current when in fault condition or when retrying.	V <sub>SNS</sub> = 0.1 V, V <sub>D</sub> = 0 V, V <sub>TMR</sub> = 0 V, measure I out from TMR	9	10	11	μA
		V <sub>SNS</sub> = 0.1 V, V <sub>D</sub> = 2 V, V <sub>TMR</sub> = 0 V, measure I out from TMR	45	50	55	μA
I <sub>TMR,SNC</sub>	Timer sinking current when not in fault condition.	V <sub>SNS</sub> = 0 V, V <sub>D</sub> = 0 V, V <sub>TMR</sub> = 2 V,	1.5	2	2.5	μA
V <sub>TMR,RETRY</sub>	Voltage on timer when the timer starts going back up in retry. Retry version only.	V <sub>SNS</sub> = 0 V, V <sub>D</sub> = 0 V, TMR ↑ = 2 V, TMR ↓, measure V <sub>TMR</sub> when I into TMR change polarity	0.475	0.5	0.525	V
N <sub>RETRY</sub>	Number of retry duty cycles. Retry version only.		64			
D <sub>RETRY</sub>	Retry duty cycle. Retry version only.		0.4%			
I <sub>GATE,TIMER</sub>	Gate Sourcing Current Threshold When timer starts to run.	V <sub>G</sub> = 5 V, V <sub>D</sub> = 2 V, V <sub>SNS</sub> ↑, measure I <sub>GATE</sub> when TMR sources current	5	10	15	μA

**Electrical Characteristics (continued)**

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $1.1\text{ mA} < I_{VCC} < 10\text{ mA}$ ,  $V_{(UVEN)} = 2\text{ V}$ ,  $V_{(OV)} = V_{(SNS)} = V_{(D)} = 0\text{ V}$ ,  $V_{(SS)} = \text{GATEX} = \text{Hi-Z}$ ,  $V_{(TMR)} = 0\text{ V}$ ,  $-1\text{ V} < V_{\text{NEG48Vx}} < 150\text{ V}$ ,  $V_{\text{ref}} = V_{\text{PROG}} = \text{Hi-Z}$ ; All pin voltages are relative to VEE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{SNS,TMR1}}$	Sense Voltage when Timer starts to run.	$V_D = 2\text{ V}$ , $V_{\text{TMR}} = 0\text{ V}$ , $V_G = 5\text{ V}$ ; $V_{\text{SNS}} \uparrow$ , measure $V_{\text{SNS}}$ when TMR sources current	1.5	2.5		mV
$V_{\text{SNS,TMR2}}$	Sense Voltage when Timer starts to run.	$V_D = 0\text{ V}$ , $V_{\text{TMR}} = 0\text{ V}$ , $V_G = 5\text{ V}$ ; $V_{\text{SNS}} \uparrow$ , measure $V_{\text{SNS}}$ when TMR sources current	23.25	24.5		mV
<b>SNS – Sense Pin For Current Limit</b>						
$I_{\text{SNS,LEAK}}$	Leakage current on sense pin		-2		2	$\mu\text{A}$
$V_{\text{SNS,CL1}}$	PROG = Float	$V_{\text{TMR}} = 0\text{ V}$ , $V_{\text{GATE}} = 5\text{ V}$ , $V_D = 0\text{ V}$ , $V_{\text{SNS}} \uparrow$ , measure when $I_{\text{GATE}} = 0$ ;	24	25	26	mV
	PROG = VEE		38	40	42	mV
$V_{\text{SNS,FST}}$	PROG = FLOAT	$V_{\text{TMR}} = 0\text{ V}$ , $V_{\text{GATE}} = 5\text{ V}$ , $V_D = 0\text{ V}$ , $V_{\text{SNS}} \uparrow$ , measure when $I_{\text{GATE}} > 100\text{ mA}$	45	50	55	mV
	PROG = VEE		72	80	88	mV
	$R_{\text{PROG}} = 78.7\text{ k}\Omega$		110	120	130	mV
	$R_{\text{PROG}} = 162\text{ k}\Omega$		68	75	82	mV
$V_{\text{SNS,CL2}}$	Fold Back Current Limit	$V_{\text{TMR}} = 0\text{ V}$ , $V_{\text{GATE}} = 5\text{ V}$ , $V_D = 5\text{ V}$ , $V_{\text{SNS}} \uparrow$ , measure when $I_{\text{GATE}} = 0$ ;	2.25	3	3.75	mV
$V_{\text{SNS,FST2}}$	Fast Trip during start-up	$V_{\text{TMR}} = 0\text{ V}$ , $V_{\text{GATE}} = 5\text{ V}$ , $V_D = 5\text{ V}$ , $V_{\text{SNS}} \uparrow$ , Measure when $I_{\text{GATE}} > 100\text{ mA}$	6	9	12	mV
<b>PROG – Programming Pin to Set Current Limit (CL) and Fast Trip</b>						
$I_{\text{PROG}}$	PROG pin current		7.9	10.1	12	$\mu\text{A}$
$V_{\text{PROG,LOW}}$	Prog pin voltage	Threshold on $V_{\text{PROG}}$ , where the fast trip setting changes from 80mV to 120mV.			0.48	V
$V_{\text{PROG,MID}}$	Prog pin voltage	Threshold on $V_{\text{PROG}}$ , where the current limit setting changes from 25mV to 40mV.	0.94	1.23	1.51	V
$V_{\text{PROG,High}}$	Prog pin voltage	Threshold on $V_{\text{PROG}}$ , where the fast trip setting changes from 80mV to 120mV.	2.4			V
<b>GATE – Gate Drive for Main Hot Swap FET</b>						
$V_{(\text{VCC-GATE})}$	Output gate voltage	$V_{(\text{SNS})} = 0\text{ V}$			1	V
$I_{(\text{GATE,SRS,NORM})}$	Sourcing Current during normal operation.	$V_{(\text{TMR})} = 0\text{ V}$ , $V_{(\text{GATE})} = 8\text{ V}$ , $V_D = 0\text{ V}$ , $V_{(\text{SNS})} = 0\text{ V}$	250	400		$\mu\text{A}$
$I_{(\text{GATE,SRS,START})}$	Sourcing Current during start-up	$V_{(\text{TMR})} = 0\text{ V}$ , $V_{(\text{GATE})} = 5\text{ V}$ , $V_D = 0\text{ V}$ , $V_{(\text{SNS})} = 0\text{ V}$	15	20	25	$\mu\text{A}$
$I_{(\text{GATE,wkpd})}$	Weak pull down current	$V_{(\text{SNS})} = 0\text{ V}$ , $V_{\text{UVEN}} = 0\text{ V}$	3	5	7	mA
$I_{(\text{GATE,FST})}$	Fast Pull down current with 10mV overdrive		0.4	1	1.5	A
<b>GATE2 – Gate Drive for Auxiliary Hot Swap FET</b>						
$V_{(\text{VCC-GATE2})}$	Output gate voltage	$V_{(\text{SNS})} = 0\text{ V}$			1	V
$I_{(\text{GATE2,wkpd})}$	weak pull down	$V_{\text{GATE}} = 0\text{ V}$		5		mA
$I_{(\text{GATE2,SRC})}$	Sourcing Current			50		$\mu\text{A}$
$I_{\text{GATE2,FST}}$	Fast Pull down current with 10 mV overdrive		0.4	1	1.5	A
$V_{\text{GATE,TH}}$	Threshold on $V_{\text{GATE}}$ when GATE2 turns on	Raise $V_{\text{GATE1}}$ , measure when $V_{\text{GATE2}}$ comes up.	6.25	7.25	8	V
$V_{\text{GATE,TH,hyst}}$	Hysteresis of threshold on $V_{\text{GATE}}$ when GATE2 turns on	hysteresis		0.5		V
<b>D – Drain Sense</b>						

**Electrical Characteristics (continued)**

–40°C ≤ T<sub>J</sub> ≤ 125°C, 1.1 mA < I<sub>VCC</sub> < 10 mA, V<sub>(UVEN)</sub> = 2 V, V<sub>(OV)</sub> = V<sub>(SNS)</sub> = V<sub>(D)</sub> = 0 V, V<sub>(SS)</sub> = GATE<sub>x</sub> = Hi-Z, V<sub>(TMR)</sub> = 0 V, –1 V < V<sub>(NEG48Vx)</sub> < 150 V, V<sub>ref</sub> = V<sub>PROG</sub> = Hi-Z; All pin voltages are relative to VEE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>(D,INT)</sub>	Resistance from the drain pin to GND.		28.5	30	31.5	kΩ
V <sub>(D,CL_SW)</sub>	Voltage on drain that switches between two current limits	V <sub>(TMR)</sub> = 0 V, V <sub>(GATE)</sub> = 5 V, V <sub>(SNS)</sub> = 20 mV, D↑, measure V when I <sub>(GATE)</sub> = 0	1.46	1.5	1.54	V
V <sub>(D,TMR_SW)</sub>	Voltage on drain that switches the V <sub>TMR</sub> threshold.	V <sub>(TMR)</sub> = 1 V, V <sub>(GATE)</sub> = 5 V, V <sub>(SNS)</sub> = 20 mV, D↑, measure V when I <sub>(GATE)</sub> = 0	0.73	0.75	0.77	V
V <sub>(D,TMR_SW,hyst)</sub>	hysteresis for V <sub>(D,TMR_SW)</sub>	hysteresis		75		mV
<b>SS (Soft Start)</b>						
I <sub>(SS,PD)</sub>	Pull down current when not in inrush	V <sub>SS</sub> = 5 V	100			mA
R <sub>(SS,GATE)</sub>	Resistance between GATE and SS in the start-up phase			80		Ω
<b>Vref</b>						
V <sub>Vref</sub>	Reference output	0 < I <sub>Vref</sub> < 800 μA	4	4.9	5.5	V
I <sub>Vref</sub>	V <sub>Vref</sub> SC current	Vref ON, V <sub>Vref</sub> (shorted)		2		mA
<b>Neg48</b>						
I <sub>(Ikg,Neg48)</sub>	Leakage current	V <sub>Neg48</sub> = –50 mV, BGATE ON	–2		2	μA
		V <sub>Neg48</sub> = –100 mV, BGATE ON	–7		7	μA
		V <sub>Neg48</sub> = 150 V, BGATE off			30	μA
V <sub>(FWD)</sub>	Forward regulation voltage of the OR-ing controller. V <sub>FWD</sub> = V <sub>EE</sub> – V <sub>(NEG48Vx)</sub>		10	25	40	mV
V <sub>(FWD,FST)</sub>	Forward voltage where a fast pull up is activated.	V <sub>GATEx</sub> = 5 V. V <sub>VEE</sub> – V <sub>Neg48Vx</sub> ↑ measure when I <sub>GATEx</sub> = 100 μA	50	80	105	mV
V <sub>(RV)</sub>	Fast reverse trip voltage.		2	6	10	mV
<b>BGATE</b>						
V <sub>VCC-BGATE</sub>	Gate Output Voltage.			0.65	1.1	V
I <sub>(BGATE,SRS)</sub>	Gate sourcing current in regulation	V <sub>VEE</sub> – V <sub>Neg48Vx</sub> = 50 mV		5		μA
I <sub>(BGATE,SINK)</sub>	Gate sinking current in regulation	V <sub>VEE</sub> – V <sub>Neg48Vx</sub> = 0		5		μA
R <sub>GATE,SRC,FST</sub>	Pull up resistance in fast sourcing mode.	V <sub>VEE</sub> – V <sub>Neg48Vx</sub> = 100 mV; Measure current at V <sub>GATEx</sub> = 0 V. R = V <sub>VCC</sub> /I		10		kΩ
I <sub>(BGATE,FST)</sub>	Fast Gate pull down current	V <sub>(VEE)</sub> – V <sub>Neg48</sub> = –15 mV	0.4	1	1.5	A
<b>PGb (Power Good Bar)</b>						
V <sub>(GATE2,PGb)</sub>	Threshold on GATE2 that triggers PGb to assert.	Raise V <sub>GATE2</sub> until PGb asserts	6.5	7.25	8	V
V <sub>(PGb,PD)</sub>	Pull down strength on PGb	PGb sinking 1 mA			1.5	V
I <sub>(PGb,LEAK)</sub>	leakage current on PGb pin				1	μA
<b>OTSD (Over Temperature Shut Down)</b>						
T <sub>SD</sub>	Shutdown temperature	Temp Rising	135	155	175	°C
T <sub>SD,hyst</sub>	Shutdown temperature Hysteresis			8		°C

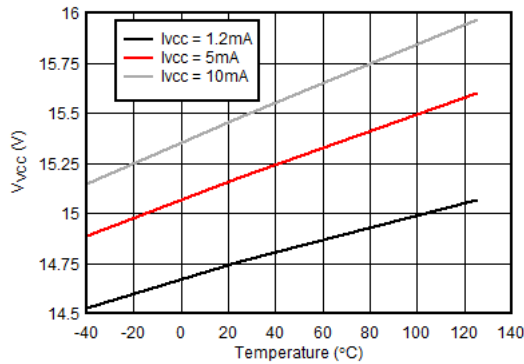
## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VCC – Clamped Supply</b>						
$t_{ID}$	Insertion Delay	$V_{VCC}$ : 0 V $\rightarrow$ 10 V, measure delay before $V_{GATE}$ $\uparrow$		32		ms
<b>UVEN</b>						
$T_{UV,degl}$	Deglintch on UVEN			4		$\mu$ s
<b>OV</b>						
$T_{OV,degl}$	Deglintch on OV			4		$\mu$ s
<b>SNS</b>						
$T_{SNS,FST,RESP}$	Response time to large over current	$V_{SNS}$ steps from 0 mV to 60 mV. Measure time for GATE and GATE2 to come down.		300		ns
<b>Neg48V</b>						
$T_{Neg48V,FST,RESP}$	Response time to large reverse current	$V_{NEG48V}$ steps from -40 mV to 15 mV. Measure time for BGATE to come down.		300		ns
<b>PGb</b>						
$t_{PGb,DEGL}$	Deglintch of PGb. (GATE2 = unloaded, raise GATE, measure delay between GATE and PGb)	Power Good $\uparrow$ ( $V_{(GATE)}$ 0 V $\rightarrow$ 10 V) Look for PGb $\downarrow$		1		ms
		Power Good $\downarrow$ ( $V_{(GATE)}$ 10 V $\rightarrow$ 0 V) Look for PGb $\uparrow$		32		ms

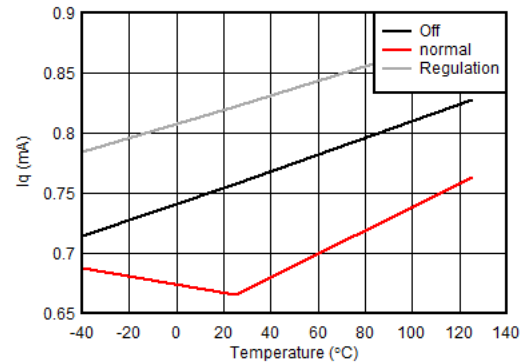
### 6.7 Typical Characteristics

Unless otherwise noted:  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $1.1\text{ mA} < I_{VCC} < 10\text{ mA}$ ,  $V_{(UVEN)} = 2\text{ V}$ ,  $V_{(OV)} = V_{(SNS)} = V_{(D)} = 0\text{ V}$ ,  $V_{(SS)} = \text{GATEX} = \text{Hi-Z}$ ,  $V_{(TMR)} = 0\text{ V}$ ,  $-1\text{ V} < V_{\text{NEG48Vx}} < 150\text{ V}$ ,  $V_{\text{Vref}} = V_{\text{PROG}} = \text{Hi-Z}$ ;



$I_{VCC}$  injected into VCC pin

Figure 1. VCC Regulation Voltage vs Current and Temperature



$V_{VCC} = 10\text{ V}$ , Regulation is current limit

Figure 2.  $I_q$  vs Temperature and Operating Condition

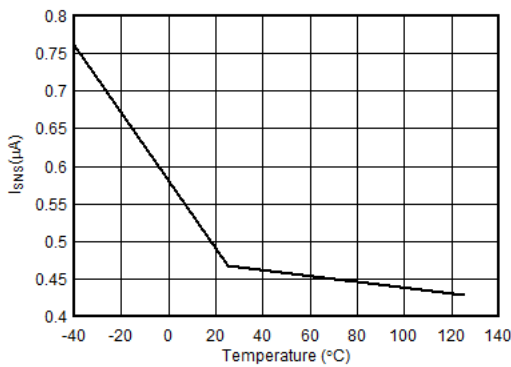


Figure 3.  $I_{SNS}$  Current Vs Temperature

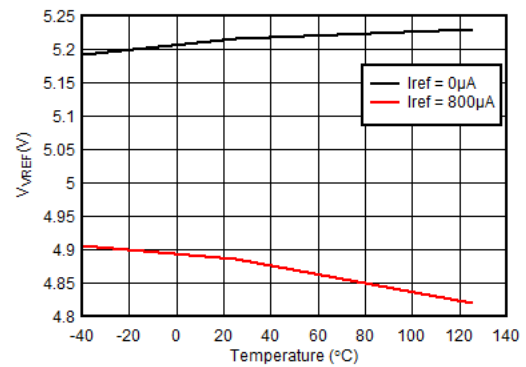
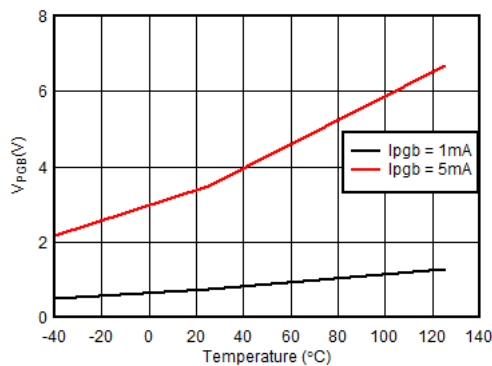


Figure 4.  $V_{Vref}$  vs Temperature and  $I_{VREF}$



In Power Good

Figure 5.  $V_{PGB}$  vs Temperature

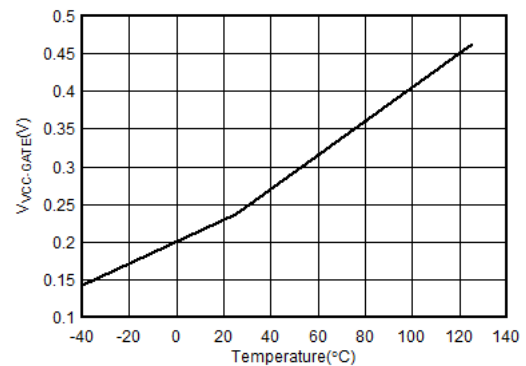


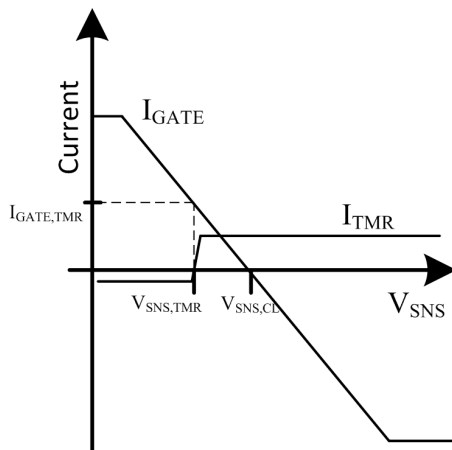
Figure 6.  $V_{VCC-GATE}$  vs Temperature

## 7 Parameter Measurement Information

### 7.1 Relationship between Sense Voltage, Gate Current, and Timer

The diagram below illustrates the relationship between the  $V_{SNS}$  (voltage across  $R_{SNS}$ ), Gate current, and the timer operation. The diagram is intended to help explain the various parameters in the electrical characteristic table and is not drawn to scale.

Note that  $I_{GATE}$  reduces as the sense voltage approaches the current limit threshold and it equals zero at the current limit regulation point. To ensure that the timer always runs when the IC is in regulation the timer starts at a slightly positive  $I_{GATE}$ .



**Figure 7. Relationship Between Timer, Gate Current, and Sense Voltage ( $V_{GATE} = 5\text{ V}$ )**

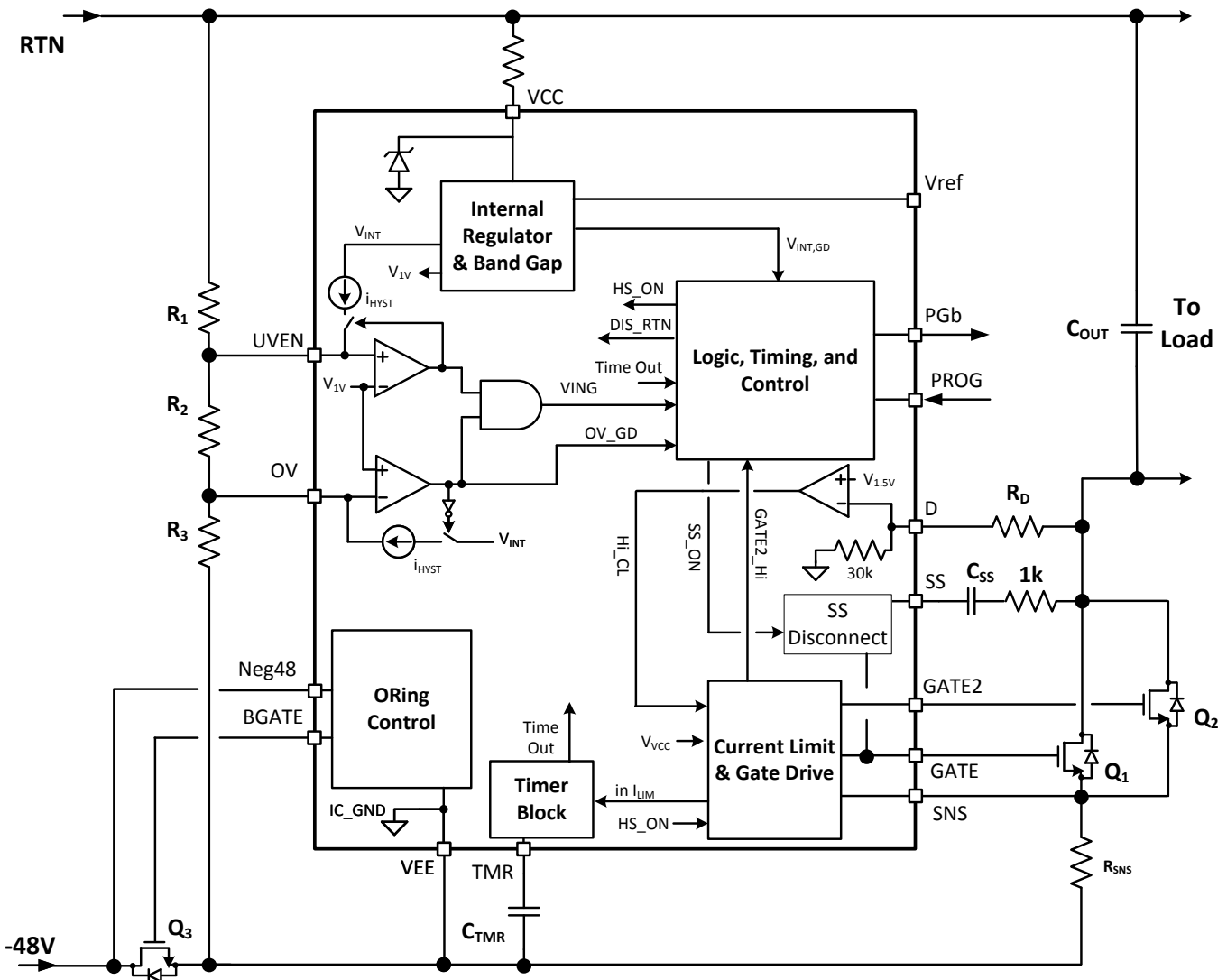
## 8 Detailed Description

### 8.1 Overview

The TPS23523 is an integrated hot swap and Single OR-ing controller that enables high power telecom systems to comply with stringent transient requirements. The soft start cap disconnect allows soft start at start-up and disconnects the soft start cap during normal operation. This allows for the use of smaller hot swap FETs without hurting the transient response. GATE2 is a second hot swap FET driver, which only turns ON when the main hot swap FET is fully on. Thus the FETs driven by GATE2 don't need to have strong SOA. This saves space and BOM cost in high power applications that require multiple hot swap FETs. The 400  $\mu\text{A}$  sourcing current allows fast recovery, which helps to avoid system resets during lightning surge tests. The dual current limit makes it easier to pass brown outs and input steps such as required by the ATIS 0600315.2013. Finally, the TPS23523 offers accurate undervoltage and overvoltage protection with programmable thresholds and hysteresis.

The TPS23523 integrates an OR-ing controller, making it ideal for  $-48\text{ V}$  systems that require reverse hook-up protection and reverse-current protection. The OR-ing controller protects the output when the input drops avoiding system resets. The OR-ing controller will turn off if any reverse current is detected.

### 8.2 Functional Block Diagram



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## 8.3 Feature Description

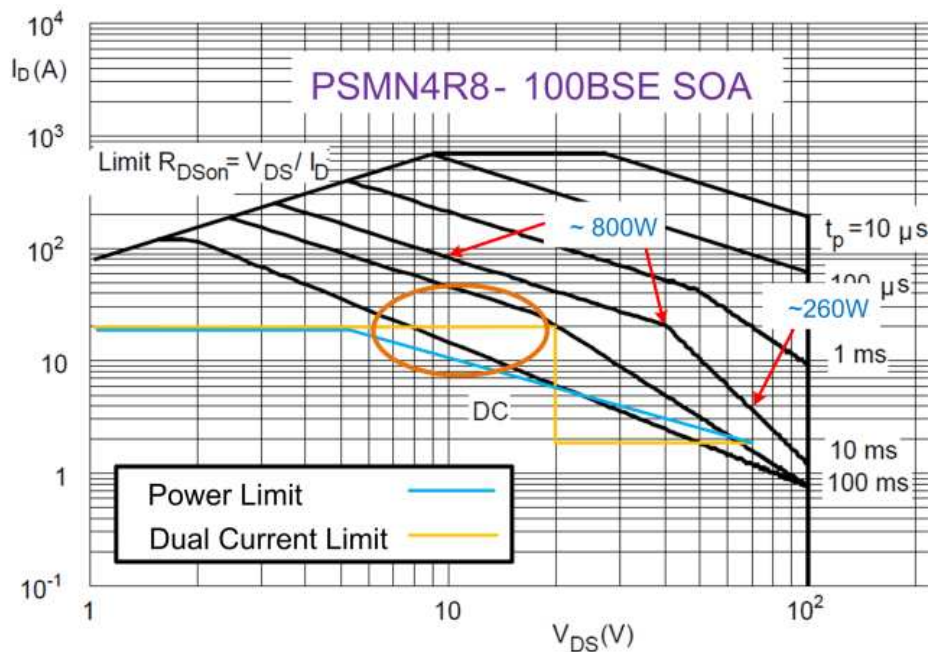
### 8.3.1 Current Limit

The TPS23523 utilizes two current limit thresholds:

- $I_{CL1}$  – also referred to as high current limit threshold, which is used when the  $V_{DS}$  of the hot swap FET is low.
- $I_{CL2}$  – lower current limit threshold, which is used when the  $V_{DS}$  of the hot swap FET is high.

This dual level protection scheme ensures that the part has a higher chance of riding out voltage steps and other transients due to the higher current limit at low  $V_{DS}$ , while protecting the MOSFET during start into short and hot-short events, by setting a lower current limit threshold for conditions with high  $V_{DS}$ . The transition threshold is programmed with a resistor that is connected from the drain of the hot swap FET to the D pin of the TPS23523. The figure below illustrates an example with a  $I_{CL1}$  set to 25 A and  $I_{CL2}$  set to 3 A. Note that compared to a traditional SOA protection scheme this approach allows better utilization of the SOA in the  $10\text{ V} < V_{DS} < 40\text{-V}$  range, which is critical in riding through transients and voltage steps.

Note that in both cases the TPS23523 regulated the gate voltage to enforce the current limit. However, this regulation is not very fast and doesn't offer the best protection against hot-shorts on the output. To protect in this scenario a fast comparator is used, which quickly pulls down the gate in case of severe over current events (2x bigger than  $V_{CL1}$ ).



**Figure 8. Dual Current Limit vs FET Power Limit**

#### 8.3.1.1 Programming the CL Switch-Over Threshold

The  $V_{DS}$  threshold when the TPS23523 switches over from  $I_{CL1}$  to  $I_{CL2}$  ( $V_{DS,SW}$ ) can be computed using Equation 1. For example, if a 15-V switch over is desired,  $R_D$  should be set to 270 k $\Omega$ .

$$V_{DS,SW} = \frac{1.5\text{ V} \times (30\text{ k}\Omega + R_D)}{30\text{ k}\Omega} \quad (1)$$

#### 8.3.1.2 Setting Up the PROG Pin

The PROG pin can be tied to VEE, left floating, or tied to VEE through a resistor to adjust  $V_{SNS,CL1}$  and the ratio of fast trip to current limit. The options are set as follows:

- PROG = NC or Float:  $V_{SNS,CL1} = 25\text{ mV}$ ,  $V_{SNS,FST}$  is  $2x V_{SNS,CL1}$
- $R_{PROG} = 196\text{ k}\Omega$  (1%):  $V_{SNS,CL1} = 25\text{ mV}$ ,  $V_{SNS,FST}$  is  $3x V_{SNS,CL1}$

## Feature Description (continued)

- $R_{\text{PROG}} = 66.5 \text{ k}\Omega$  (1%):  $V_{\text{SNS,CL1}} = 40 \text{ mV}$ ,  $V_{\text{SNS,FST}}$  is  $3 \times V_{\text{SNS,CL1}}$
- $\text{PROG} = \text{VEE}$ :  $V_{\text{SNS,CL1}} = 40 \text{ mV}$ ,  $V_{\text{SNS,FST}}$  is  $2 \times V_{\text{SNS,CL1}}$

### 8.3.1.3 Programming CL1

The current limit at low  $V_{\text{DS}}$  ( $I_{\text{CL1}}$ ) of the TPS23523 can be computed using [Equation 2](#).

$$I_{\text{CL1}} = \frac{V_{\text{SNS,CL1}}}{R_{\text{SNS}}} \quad (2)$$

To compute  $I_{\text{CL1}}$  for a 1-m $\Omega$  sense resistor use [Equation 3](#) below.

$$I_{\text{CL1}} = \frac{V_{\text{SNS,CL1}}}{R_{\text{SNS}}} = \frac{25 \text{ mV}}{1 \text{ m}\Omega} = 25 \text{ A} \quad (3)$$

### 8.3.1.4 Programming CL2

The current limit at high  $V_{\text{DS}}$  ( $I_{\text{CL2}}$ ) of the TPS23523 can be computed using [Equation 4](#).

$$I_{\text{CL2}} = \frac{V_{\text{SNS,CL2}}}{R_{\text{SNS}}} \quad (4)$$

To compute  $I_{\text{CL2}}$  for a 1-m $\Omega$  sense resistor use [Equation 5](#).

$$I_{\text{CL2}} = \frac{V_{\text{SNS,CL2}}}{R_{\text{SNS}}} = \frac{3 \text{ mV}}{1 \text{ m}\Omega} = 3 \text{ A} \quad (5)$$

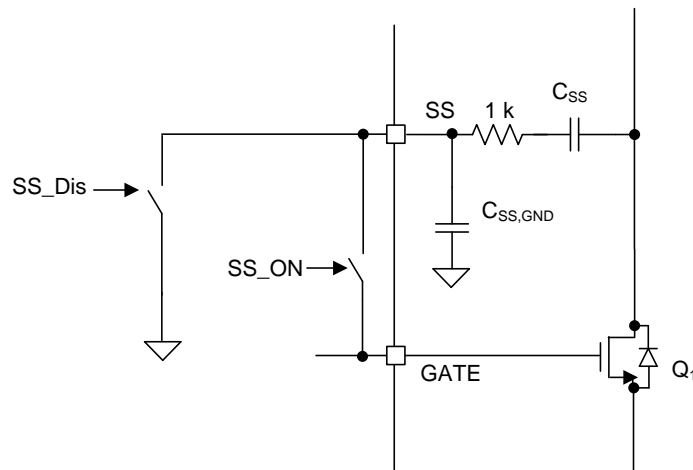
## 8.3.2 Soft Start Disconnect

The inrush current into the output capacitor ( $C_{\text{OUT}}$ ) can be limited by placing a capacitor between the SS (Soft Start) pin and the drain of the hot swap MOSFET. In that case the inrush current can be computed using [Equation 6](#).

$$I_{\text{INR}} = \frac{C_{\text{OUT}} \times I_{\text{GATE,SRS,START}}}{C_{\text{SS}}} = \frac{660 \text{ }\mu\text{F} \times 20 \text{ }\mu\text{A}}{33 \text{ nF}} = 0.4 \text{ A} \quad (6)$$

Note that with most hot swap the  $C_{\text{SS}}$  pin is tied simply to the gate pin, but this can interfere with performance during normal operation if transients or short circuits are encountered. In addition the  $C_{\text{SS}}$  capacitor tends to pull up the gate during hot plug and cause shoot through current if it is always tied to the gate. For that reason the TPS23523 has a disconnect switch between the gate pin and the SS pin as well as a discharge resistor. During the initial hot plug and during the insertion delay the switch between SS and GATE is open and SS is being discharged to GND through a resistor. Then during start-up SS and GATE are connected to limit the slew rate. Once in normal operation the SS pin is not tied to GATE and it is not shorted to GND, which prevents it from interfering with the operation during transients.

## Feature Description (continued)



**Figure 9. Implementation of SS Disconnect**

### 8.3.3 Timer

Timer is a critical feature in the hot swap, which manages the stress level in the MOSFET. The timer will source and sink current into the timer capacitor as follows:

- Not in current limit: sink 2  $\mu$ A
- If the part is in current limit and  $V_{GATE} < V_{GATE,TH}$ , the timer sources current as follows:
  - $V_D < V_{D,CL\_SW}$ : source 10  $\mu$ A
  - $V_D > V_{D,CL\_SW}$ : source 50  $\mu$ A

The TPS23523 times out and shuts down the hot swap as follows.

- If  $V_D < V_{D,TMR\_SW}$  then the hot swap times out when  $V_{TMR}$  reaches 1.5 V.
- If  $V_D > V_{D,TMR\_SW}$  then the hot swap times out when  $V_{TMR}$  reaches 0.75 V.

The above behavior maximizes the ability of the hot swap to ride out voltage steps, while ensuring that the FET remains safe even if the part can not ride out a voltage step.

A cool down period follows after the part times out. During this time the timer performs the following:

- Discharge  $C_{TMR}$  with a 2- $\mu$ A current source until 0.5 V
- Charge  $C_{TMR}$  with a 10- $\mu$ A current source until it is back to 1.5 V.
- Repeat the above 64 times
- Discharge timer to 0 V.

The part attempts to restart after finishing the above. If the UVEN signal is toggled while the 64 cycles are in progress the part restarts immediately after the 64 cycles are completed.

The timer operates as follows when recovering from POR:

- If  $V_{TMR} < 0.5$  V:
  - Proceed to regular startup
  - Do not discharge  $V_{TMR}$
- If  $V_{TMR} > 0.5$  V:
  - Go through 64 charge/discharge cycles
  - Discharge  $V_{TMR}$
  - Proceed to startup

The Time Out ( $T_{TO}$ ) can be computed using the equations below. Note that the time out depends on the  $V_{DS}$  of the MOSFET.

Feature Description (continued)

$$T_{TO} = \frac{C_{TMR} \times V_{TMR}}{I_{TMR,SRS}} \tag{7}$$

$$T_{TO}(V_D < 0.75 V) = \frac{C_{TMR} \times 1.5 V}{10 \mu A} \tag{8}$$

$$T_{TO}(0.75 V < V_D < 1.5 V) = \frac{C_{TMR} \times 0.75 V}{10 \mu A} \tag{9}$$

$$T_{TO}(V_D > 1.5 V) = \frac{C_{TMR} \times 0.75 V}{50 \mu A} \tag{10}$$

8.3.4 Gate 2

The TPS23523 features a second hot swap Gate drive, which can be used to save BOM cost and size in applications that require multiple hot swap MOSFETs. The 2nd MOSFET is only turned ON when the main FET is enhanced. As a result the 2nd MOSFET doesn't operate with large current and large voltage across it, thus reducing the SOA requirements. In many cases a 5x6 QFN FET can replace a D<sup>2</sup>PACK FET. The following figures show the operation during start-up and Hot Short event. It can be seen that the second FET is OFF during stressful operation and turns on during normal operation to improve steady state efficiency and reduce power losses.

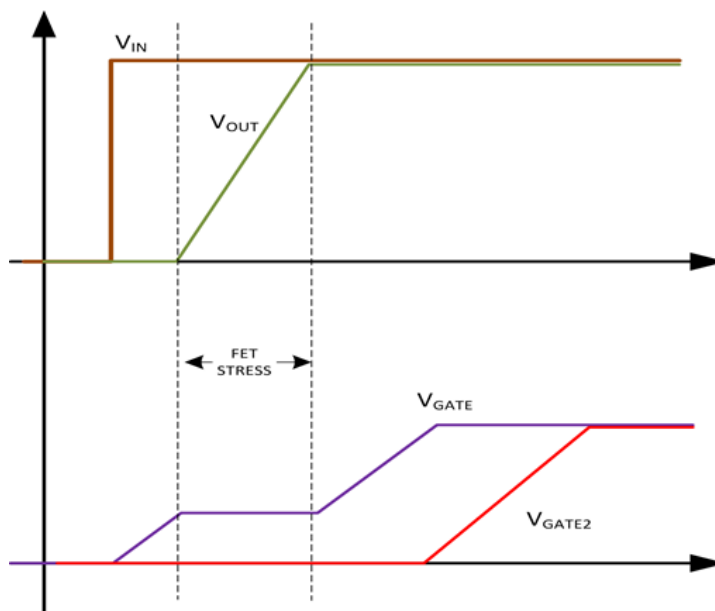


Figure 10. Gate 2 Operation During Start-Up

Feature Description (continued)

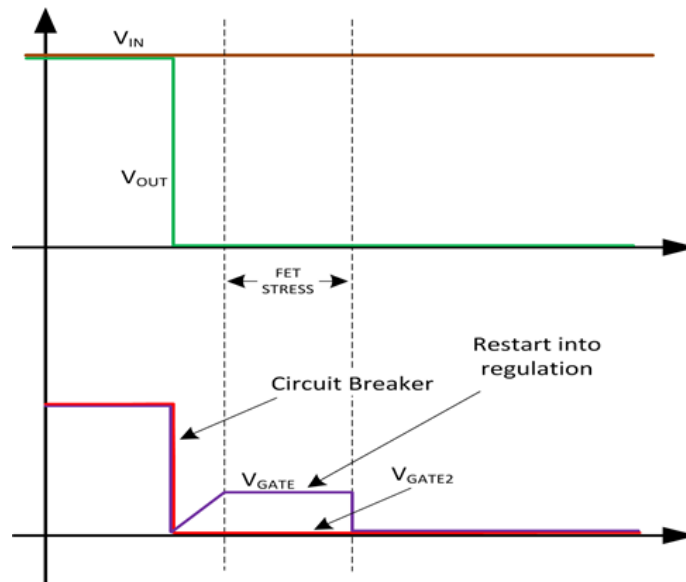


Figure 11. Gate2 Operation During Hot Short

8.3.5 OR-ing

The TPS23523 features integrated OR-ing that controls the external MOSFET in a way to emulate an ideal diode. The TPS23523 will regulate the forward drop across the OR-ing FET to 25 mV. This is accomplished by controlling the  $V_{GS}$  of the MOSFET. As the current decreases the  $V_{GS}$  is also decreased, which effectively increases the  $R_{DS(ON)}$  of the MOSFET. This process is regulated with a low gain amplifier that is gate (OR-ing FET) pole compensated. The lower gain helps ensure stability over various operating conditions. The regulating amplifier ensures that there is no DC reverse current.

However, the amplifier is not very fast and thus it is paired with a fast comparator. This comparator quickly turns off the FET if there is significant reverse current detected.

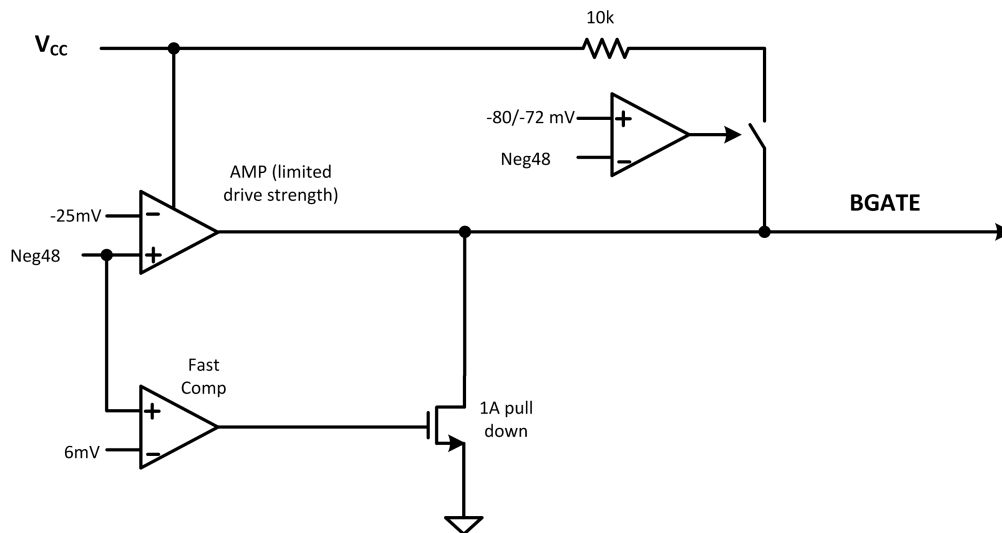
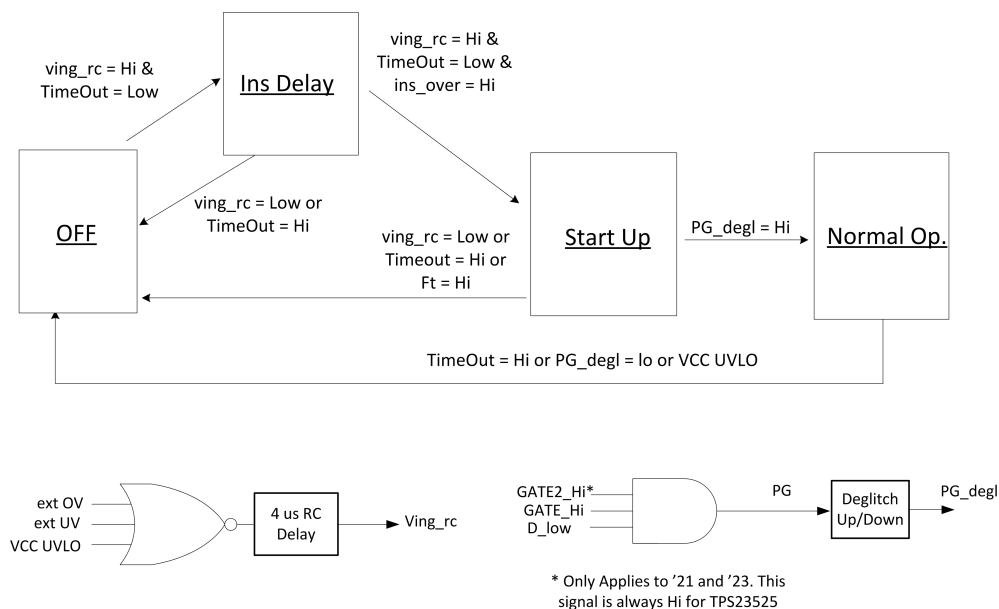


Figure 12. Simplified Diagram of OR-ing Block

## 8.4 Device Functional Modes



**Figure 13. Simplified Hot Swap State Machine**

The Figure above shows a simplified state machine of the hot swap controller. It has 4 distinct operating states and the controller switches between these states based on the following signals:

- **Ving\_rc:** This means that both the input voltage is in the right range and the IC has power with Vcc. A 4- $\mu$ s delay is added for deglitching. If the input voltage is above the OV threshold, input voltage is below the UV threshold, or VCC is below its internal UVLO, Ving\_rc will be low.
- **TimeOut:** This signal comes from the timer block and will be asserted Hi if the IC has timed out due to an over-current condition. This signal is also Hi while the timer is going through the restart cycles. Once the cycles are completed this signal will go Low.
- **ins\_over:** This signal states that the insertion delay has been completed and the hot swap is ready to start-up.
- **FT:** this is the fast trip signal coming from the fast trip comparator. It goes Hi if an extreme over current event is detected.
- **PG:** Internal Power good signal. This is high when the hot swap is fully on and the load can draw full power. For PG to be Hi, the GATE has to be Hi, GATE2 needs to be Hi, and the drain pin needs to be below 0.75 V.
- **PG\_degl:** This is a deglitched version of the PG and is the signal used to move between states and controls the external PGb pin.

### 8.4.1 OFF State

In this state the hot swap FET is turned off and the controller is waiting to start-up. The controller can be in this state due to any of these scenarios:

- Input voltage is not in the valid range.
- The hot swap is in the cool down state and the timer is going through the retry cycle after a fault condition such as output hot short or over current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

### 8.4.2 Insertion Delay State

In this state the hot swap FET is turned off and the controller is waiting for the insertion delay to finish. This allows the input supply to settle after a Hot Plug. If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

## Device Functional Modes (continued)

Once the insertion delay is finished, the controller will move to the Start-up state.

### 8.4.3 Start-up State

In this state the controller is turning on and charging the output cap. The operation is set as follows:

- The SS pin is internally connected to the GATE pin to allow for output dv/dt control.
- Lower gate sourcing current is applied to the GATE pin to allow for smaller SS caps.
- The lower current limit setting of  $V_{SNS,CL2}$  and a lower fast trip setting of  $V_{SNS,FST2}$  is used to minimize the MOSFET stress in case of a fault condition.

If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.
- Fast trip is triggered.

Once the PG\_degl signal goes Hi, the controller will move to the Normal Operation state.

### 8.4.4 Normal Operation State

In this state the hot swap is fully on and the operation is set as follows:

- The SS pin is disconnected from the GATE pin to improve transient response.
- The full gate sourcing current is used to improve transient response.
- The current limit and fast trip threshold are a function of the D pin to optimize the transient response while protecting the MOSFET.

If any of the following occur, the controller will be kicked back to the OFF state:

- PG\_degl goes low.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Note that if the input voltage is outside the valid range or the fast trip is triggered, the hot swap FET will turn off, but the controller will not exit the Normal Operation state. In this case the PG signal would go low immediately. If this condition persists, the PG\_degl will go low as well and the controller would move to the OFF state. This operation prevents the controller from re-starting the system during quick transients.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

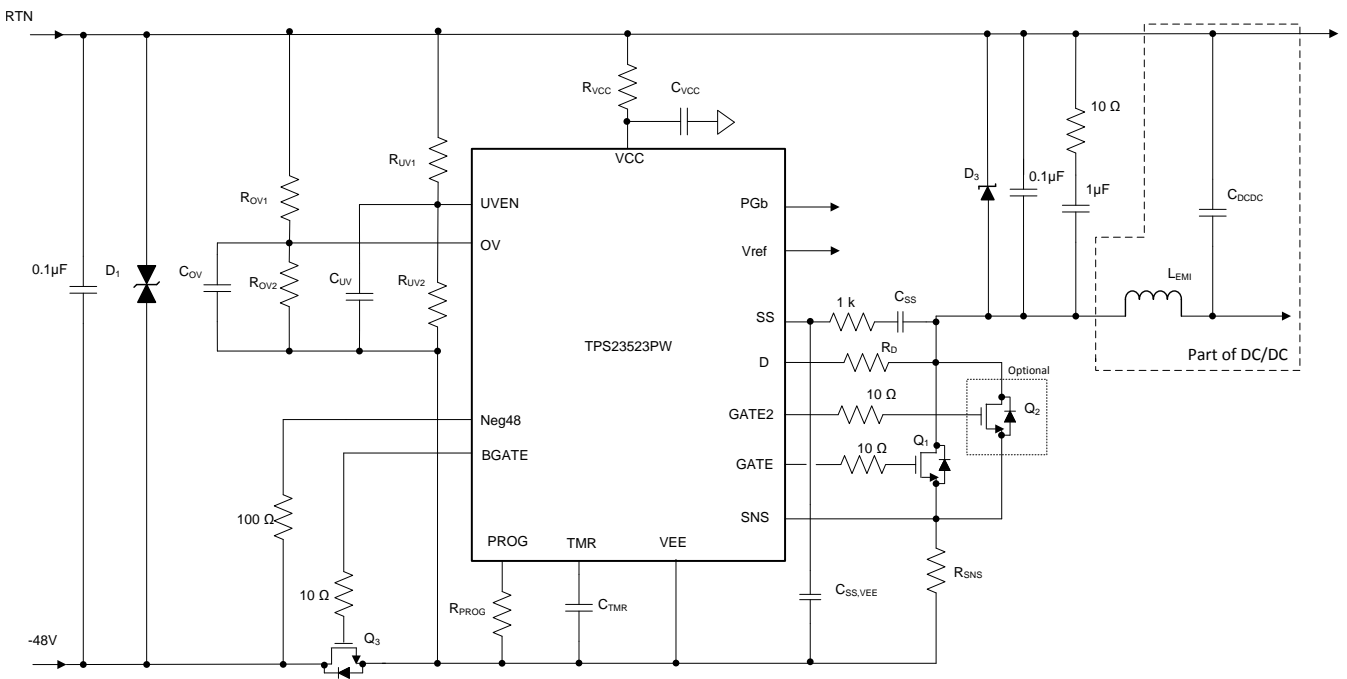
### 9.1 Application Information

The TPS23523 is a hot swap controller for  $-48\text{-V}$  applications and is used to manage inrush current and protect downstream circuitry and the upstream bus in case of fault conditions. The following key scenarios should be considered when designing a  $-48\text{-V}$  hot swap circuit:

- Start Up.
- Output of a hot swap is shorted to ground while the hot swap is on. This is often referred to as a Hot Short.
- Powering up a board when the output and ground are shorted. This is usually called a start-into-short.
- Input lightning surge. Here it is usually desired to avoid damage to downstream circuitry and to avoid system restarts.

These scenarios place a lot of stress on the hot swap MOSFET and the board designer should take special care to ensure that the MOSFET stays within its Safe Operating Area (SOA) under all of these conditions. A detailed design example is provided below and the key equations are written out. Note that solving all of these equations by hand is cumbersome and can result in errors. Instead, TI recommends using the TPS2352X Design Calculator provided on the product page.

### 9.2 Typical Application



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Figure 14. Application Diagram for Design Example

## Typical Application (continued)

### 9.2.1 Design Requirements

The table below summarizes the design parameters that must be known before designing a hot swap circuit. When charging the output capacitor through the hot swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ( $1/2CV^2$ ). Thus both the input voltage and output capacitance will determine the stress experienced by the MOSFET. The maximum load power will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ( $R_{\theta CA}$ ) will drive the selection of the MOSFET's  $R_{DS(ON)}$  and the number of MOSFETs used.  $R_{\theta CA}$  is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Air cooling will also reduce  $R_{\theta CA}$  substantially. Finally, it's important to know what transients the circuit has to pass in order to size up the input protection accordingly.

**Table 1. Design Requirements for a –38 V to –60 V, 400-W Protection Circuit**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	–38 V to –60 V
Maximum Load Power	400 W
Output Capacitance	660 $\mu$ F
Location of Output Cap	After EMI filter with ~5 $\mu$ H of inductance.
Maximum Ambient Temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	20°C/W
Pass "Hot-Short" on Output?	Yes
Pass a "Start into short"?	Yes
Is the load off until PG asserted?	Yes
Max Input Inductance	10 $\mu$ H
Level of IEC61000-4-5 to pass	2-kV Line to Line with 2- $\Omega$ series impedance
Pass Reverse Hook Up	Yes

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Selecting $R_{SNS}$

Before selecting  $R_{SNS}$ , first compute the maximum load current. For this example the worst case load current happens at the minimum input voltage of 38 V. Thus the maximum current is  $400\text{ W}/38\text{ V} = 10.5\text{ A}$ . To provide some margin, set the target current limit to 12 A and compute  $R_{SNS}$  using equation below:

$$R_{SNS,CLC} = \frac{V_{SNS,CL1}}{I_{CL1}} = \frac{25\text{ mV}}{12\text{ A}} = 2.08\text{ m}\Omega \quad (11)$$

Use next available  $R_{SNS}$  of 2 m $\Omega$ .

#### 9.2.2.2 Selecting Soft Start Setting: $C_{SS}$ and $C_{SS,VEE}$

First, compute the minimum inrush current where the timer will trip using equation below.

$$I_{INR,TMR} = \frac{V_{SNS,TMR1}}{R_{SNS}} = \frac{1.5\text{ mV}}{2\text{ m}\Omega} = 0.75\text{ A} \quad (12)$$

To avoid running the timer the inrush current needs to be sufficiently low. Target 0.4 A of inrush current to allow margin, and compute the target  $C_{SS}$  using equation below.

$$C_{SS} = \frac{C_{OUT,MAX} \times I_{GATE,SRS,START}}{I_{INR,TGT}} = \frac{792\text{ }\mu\text{F} \times 20\text{ }\mu\text{A}}{0.4\text{ A}} = 39.6\text{ nF} \quad (13)$$

Next choose, the next available  $C_{SS}$  greater than 39.6 nF. For this example 43 nF was used, which assumes a 33 nF and 10 nF cap in parallel. This results in an inrush current of 0.37 A at max  $C_{OUT}$  (792  $\mu$ F) and inrush current of 0.31 A at typical  $C_{OUT}$  (660  $\mu$ F). Also it is recommended to add a capacitor between the soft start pin and VEE ( $C_{SS,VEE}$ ) to improve immunity to input voltage noise during soft start. It's recommended to chose a capacitor that's 3x larger than  $C_{SS}$ . In this case a 150 nF capacitor was chosen.

Finally the start-up time at maximum input voltage can be computed using the equation below:

$$T_{START}(V_{IN,MAX}) = \frac{C_{SS} \times V_{IN,MAX}}{I_{GATE,SRS,START}} = \frac{43\text{nF} \times 60\text{V}}{20\mu\text{A}} = 129\text{ms} \quad (14)$$

### 9.2.2.3 Selecting $V_{DS}$ Switch Over Threshold

The  $V_{DS}$  threshold where the current limit switches from CL1 to CL2 can be programmed using  $R_D$ . In general a higher threshold improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because the larger current limit is now allowed at higher  $V_{DS}$  voltages. If there are no specific voltage step requirements, 20 V is a good starting point. Use the equation below to compute the target  $R_D$ .

$$R_D = 30\text{k}\Omega \times \left( \frac{V_{DS,SW}}{1.5\text{V}} - 1 \right) = 370\text{k}\Omega \quad (15)$$

### 9.2.2.4 Timer Selection

The timer determines how long the hot swap can be in current limit before timing out and can be programmed using  $C_{TMR}$ . In general a longer time out ( $T_{TO}$ ) improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because it takes longer for the FET to shut down during fault conditions. If there are no specific voltage step or transient requirements, 2 ms is a good starting point. Use the equation below to compute the target  $C_{TMR}$ . Choose the next available capacitor value of 15 nF, which results in a 2.25 ms time out.

$$C_{TMR} = \frac{T_{TO} \times I_{TMR,SRS}}{V_{TMR}} = \frac{2\text{ms} \times 10\mu\text{A}}{1.5\text{V}} = 13.3\text{nF} \quad (16)$$

### 9.2.2.5 MOSFET Selection and SOA Checks

When selecting MOSFETs for the –48 V application the three key parameters are:  $V_{DS}$  rating,  $R_{DS(ON)}$ , and safe operating area (SOA). For this application the CSD19535KTT was selected to provide a 100 V  $V_{DS}$  rating, low  $R_{DS(ON)}$ , and sufficient SOA. After selecting the MOSFET, it is important to double check that it has sufficient SOA to handle the key stress scenarios: start-up, output Hot Short, and Start into Short. MOSFET's SOA is usually specified at a case temperature of 25°C and should be derated based on the maximum case temperature expected in the application. Compute the maximum case temperature using the equation below. Note that the  $R_{DS(ON)}$  will vary with temperature and solving the equation below could be a repetitive process. The CSD19535KTT, has a maximum 3.4 m $\Omega$   $R_{DS(ON)}$  at room temperature and is ~1.5x higher at 100°C. N stands for the number of MOSFETs used in parallel.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times \left( \frac{I_{LOAD,MAX}}{N} \right)^2 \times R_{DS(ON)}(T_J) \quad (17)$$

$$T_{C,MAX} = 85\text{ }^\circ\text{C} + 20\text{ }^\circ\frac{\text{C}}{\text{W}} \times (10.5\text{ A})^2 \times (3.4 \times 1.5\text{ m}\Omega) = 96.3\text{ }^\circ\text{C} \quad (18)$$

Next the stress the MOSFET will experience during operation should be compared to the FETs capability. First, consider the power up. The inrush current with max  $C_{OUT}$  will be 0.37 A and the inrush will last for 129 ms. Note that the power dissipation of the FET will start at  $V_{IN,MAX} \times I_{INR}$  and reduce to zero as the  $V_{DS}$  of the MOSFET is reduced. The SOA curve of a typical MOSFET assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where  $P_{FET} = V_{IN,MAX} \times I_{INR}$  for  $t = T_{start-up} / 2$ . In this instance, the SOA can be checked by looking at a 60 V, 0.4 A, 64.5 ms pulse. Based on the SOA of the CSD19535KTT, it can handle 60 V, 1.8 A for 10 ms and it can handle 60 V, 1 A for 100 ms. The SOA at  $T_C = 25^\circ\text{C}$  for 64.5 ms can be extrapolated by approximating SOA vs time as a power function as shown in equations below:

$$I_{SOA}(t) = a \times t^m \quad (19)$$

$$m = \frac{\ln(I_{SOA}(t_1) / I_{SOA}(t_2))}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{1.8 \text{ A}}{1 \text{ A}}\right)}{\ln\left(\frac{10 \text{ ms}}{100 \text{ ms}}\right)} = -0.25 \quad (20)$$

$$a = \frac{I_{SOA}(t_2)}{t_2^m} = \frac{1 \text{ A}}{(100 \text{ ms})^{-0.25}} = 3.16 \text{ A} \times (\text{ms})^{0.25} \quad (21)$$

$$I_{SOA}(64.5 \text{ ms}, 25^\circ\text{C}) = 3.16 \text{ A} \times (\text{ms})^{0.25} \times (64.5 \text{ ms})^{-0.25} = 1.12 \text{ A} \quad (22)$$

Finally, the FET SOA needs to be derated based on the maximum case temperature as shown below. Note that the FET can handle 0.59 A, while it will have 0.37 A during start-up. Thus there is a lot of margin during this test condition.

$$I_{SOA}(64.5 \text{ ms}, T_{C,MAX}) = 1.12 \text{ A} \times \frac{175^\circ\text{C} - 96.3^\circ\text{C}}{175^\circ\text{C} - 25^\circ\text{C}} = 0.59 \text{ A} \quad (23)$$

A similar approach should be taken to compute the FETs SOA capability during a Hot Short and start into short. As shown in the following figure, during a start into short the gate is coming up very slowly due to a large capacitance tied to the gate through the SS pin. Thus it is more stressful than a Hot Short and should be used for worst case SOA calculations. To compare the FET stress during start-up into short to the SOA curves the stress needs to be approximated as a square pulse as showing in the figure below. In this example, the stress is approximated with a 1.1 ms (Teq), 1.5 A, 60 V pulse. The FET can handle 6 A, 60 V for 1 ms and 1.8 A, 60 V for 10 ms. Using approximation and temp derating as shown earlier, the FET's capability can be computed as 3 A, 60 V, for 1.1 ms at  $96^\circ\text{C}$ . 3 A is significantly larger than 1.5 A implying good margin.



Figure 15. Teq During a Start Into a Short

The final operating point to check is the operation with high current and  $V_{DS}$  just below the  $V_{DS,SW}$  threshold. In this example, the time out would be 1.1ms (one half of the time out at  $V_d = 0$  V), the current will be 12.5 A, and the voltage would be 20 V. Looking up the SOA curve, the FET can handle 30 A, 20 V for 1 ms and 10 A, 20 V for 10 ms. Repeating previously shown approximations and temp derating, the FET's capability is computed to be 16 A, 20 V, for 1.1 ms at 96°C. Again this is below the worst case operating point of 12.5 A and 20 V suggesting good margin.

#### 9.2.2.6 Input Cap, Input TVS, and OR-ing FET selection

This design example is sized for an application that needs to pass a 2 kV, 2Ω lightning strike per IEC61000-4-5. This equates to almost 1000 A of input current that needs to be clamped. In addition, the design needs to pass reverse hook up and thus the TVS needs to be bi directional. A ceramic transient voltage suppressor (2x B72540T6500S162) CT2220K50E2G was used to clamp this huge surge of current. According to it's datasheet it can clamp 500 A of current to 150 V. Note that the lightning strike can be positive or negative. The worst case voltage is dropped across the OR-ing FETs when the strike is positive (-48 V line goes above RTN). If the output of the OR-ing is -48 V and the input goes to +150 V that is a 200 V drop. Thus BSC320N20NS3 was chosen for the OR-ing FETs. This is a 200 V FET with a 32 mΩ  $R_{DS(ON)}$  at room temperature. 2 of these were used in parallel to minimize power loss and manage thermal. Finally a 0.1 μF input bypass cap is recommended.

#### 9.2.2.7 EMI Filter Consideration

In this example it is assumed that the EMI filter is right after the hot swap and the bulk cap is after the EMI filter. The EMI filter adds significant inductance and needs to be accounted for. During a Hot Short, the inductor builds up significant current that needs to go somewhere after the FET opens. For that a free wheeling diode should be used along with a snubber. For this example a 150 V, SMA diode was used: STPS1150A. The snubber consisted of a 10-Ω resistor in series with a 1-μF ceramic capacitor. In addition a 0.1-μF ceramic cap was tied directly on the output.

### 9.2.2.8 Undervoltage and Overvoltage Settings

Both the threshold and hysteresis can be programmed for undervoltage and overvoltage protection. In general the rising UV threshold should be set sufficiently below the minimum input voltage and the falling OV threshold should be set sufficiently above the maximum input voltage to account for tolerances. For this example a rising UV threshold of 37 V and a falling UV threshold of 35 V was chosen as the target. First, choose  $R_{UV1}$  based on the 2 V UV hysteresis as shown below.

$$R_{UV1} = \frac{V_{UV,hyst,tgt}}{i_{UV,hyst}} = \frac{2 \text{ V}}{10 \mu\text{A}} = 200 \text{ k}\Omega \quad (24)$$

Once  $R_{UV1}$  is known  $R_{UV2}$  can be computed based on the target rising UV threshold as shown below.

$$R_{UV2} = \frac{R_{UV1}}{V_{UV,TGT,Rising} - 1 \text{ V}} = \frac{200 \text{ k}\Omega}{37 \text{ V} - 1 \text{ V}} = 5.56 \text{ k}\Omega \quad (25)$$

The OV setting can be programmed in a similar fashion as shown in equations below.

$$R_{OV1} = \frac{V_{OV,hyst,tgt}}{i_{OV,hyst}} = \frac{3 \text{ V}}{10 \mu\text{A}} = 300 \text{ k}\Omega \quad (26)$$

$$R_{OV2} = \frac{R_{OV1}}{V_{OV,TGT,Rising} - 1 \text{ V}} = \frac{300 \text{ k}\Omega}{65 \text{ V} - 1 \text{ V}} = 4.68 \text{ k}\Omega \quad (28)$$

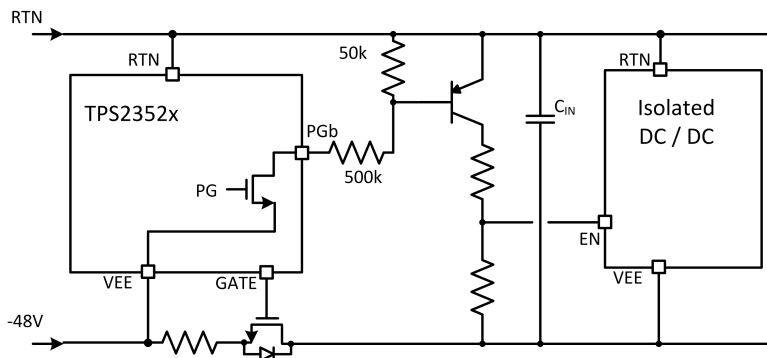
Optional filtering capacitors can be added to the UV and OV to improve immunity to noise and transients on the input bus. These should be tuned based on system requirements and input inductance. In this example place holders were added to the PCB, but the components were not populated.

### 9.2.2.9 Choosing $R_{VCC}$ and $C_{VCC}$

The VCC is used as internal supply rail and is a shunt regulator. To ensure stability of internal loop a minimum of 0.1  $\mu\text{F}$  is required for  $C_{VCC}$ . To ensure reasonable power on time it is recommended to keep  $C_{VCC}$  below 1  $\mu\text{F}$ .  $R_{VCC}$  should be sized in such a way to ensure that sufficient current is supplied to the IC at minimum operating voltage corresponding to the falling UV threshold. To allow for some margin it is recommended that the current through  $R_{VCC}$  is at least 1.2x of  $I_{Q,MAX}$  when  $RTN = \text{Falling UV threshold}$  and  $VCC = 10 \text{ V}$  (minimum recommended operating voltage on VCC). For this example  $R_{VCC}$  of 16.2 k $\Omega$  was used.

### 9.2.2.10 Power Good Interface to Downstream DC/DC

It's critical to keep the downstream DC/DC off while the hot swap is charging the bulk capacitor. This can be accomplished through the PGB pin. Note that the VEE of the hot swap and the DC/DC are different and the Power Good can not be directly tied to the EN or UV of the DC/DC. The application circuit below provides a simple way to control the downstream converter with the PGB pin of the hot swap.



**Figure 16. Interface to DC/DC**

9.2.3 Application Curves

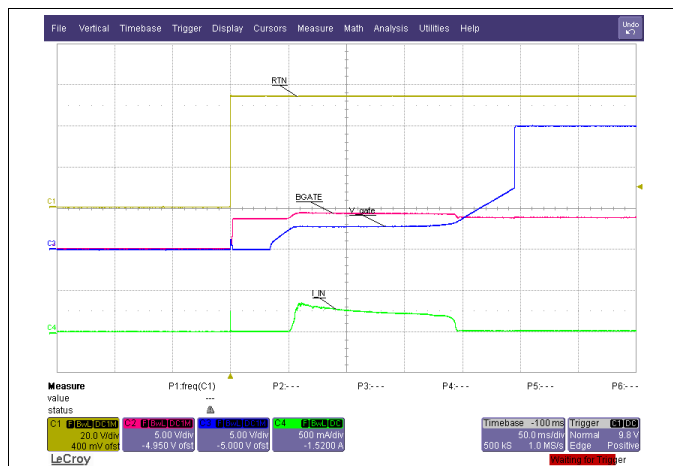


Figure 17. Start Up (Vin = 54 V)



Figure 18. Start Up (Vin = 54 V)

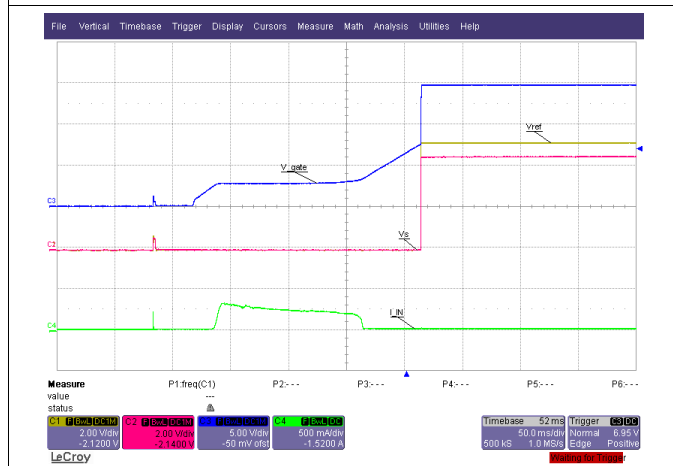


Figure 19. Start Up (Vin = 54 V)

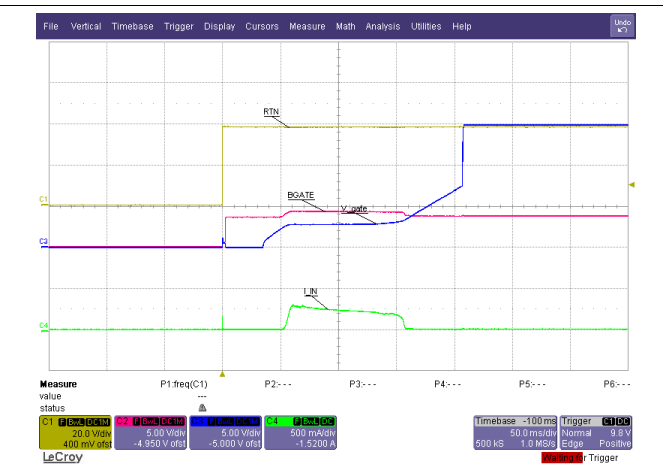


Figure 20. Start Up (Vin = 38 V)

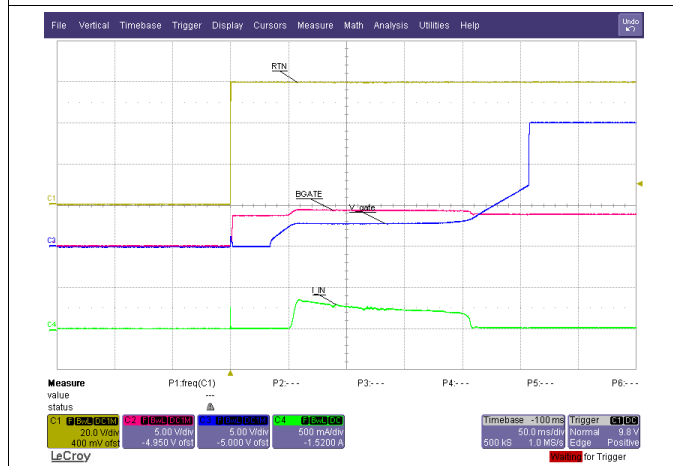


Figure 21. Start Up (Vin = 60 V)

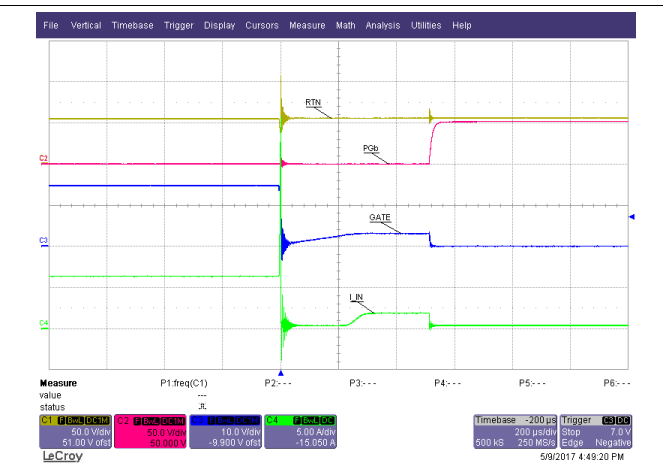
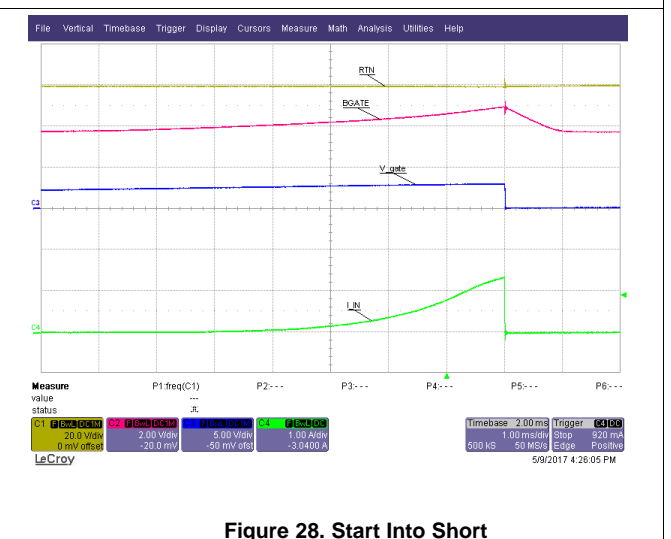
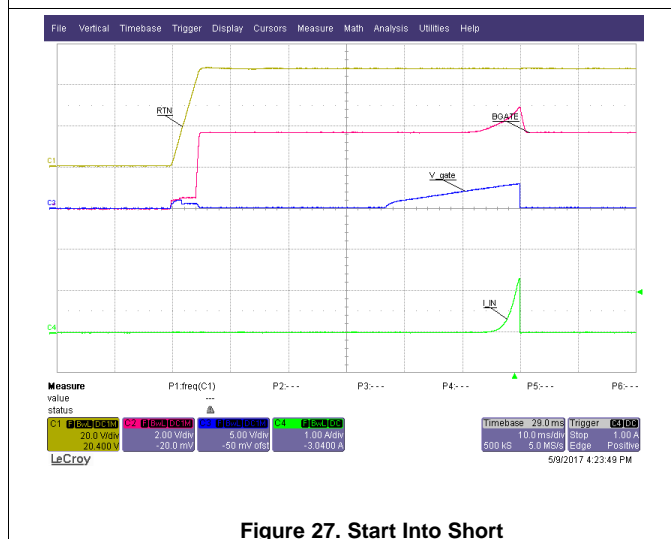
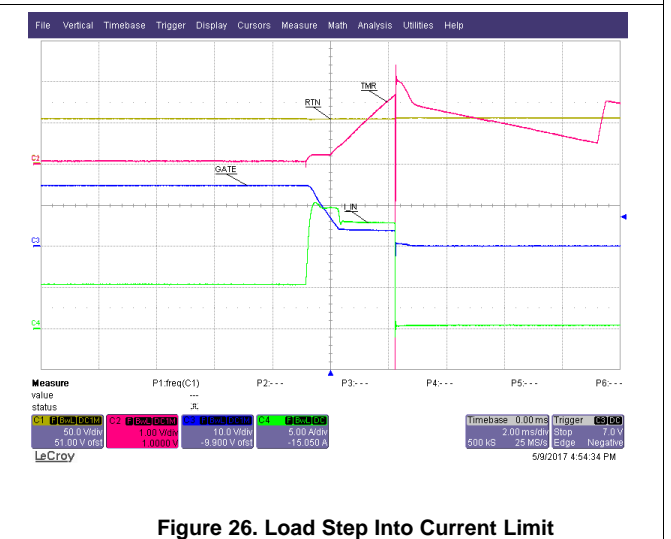
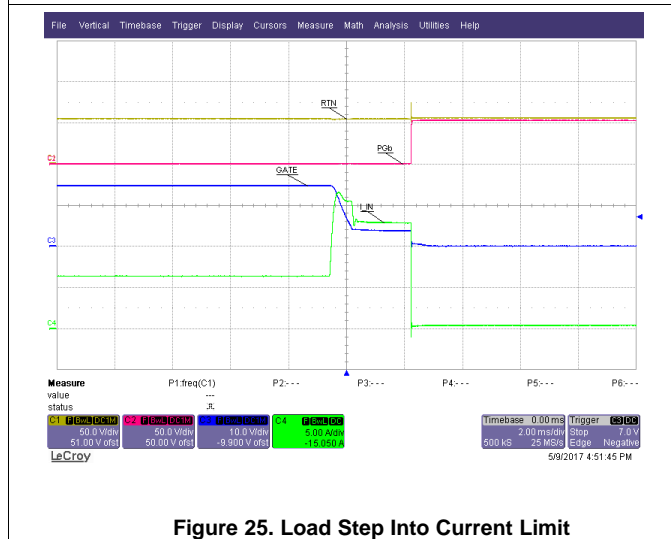
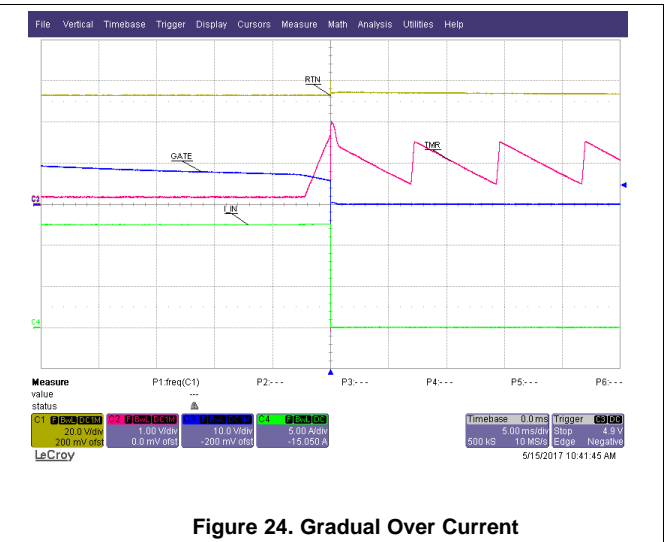
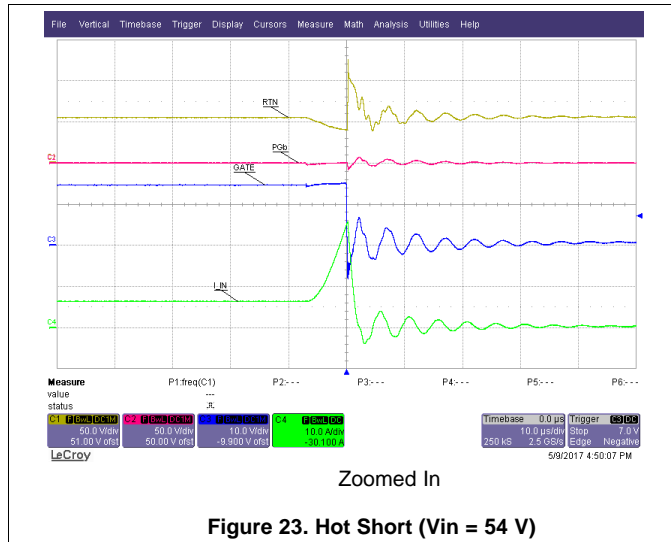


Figure 22. Hot Short (Vin = 54 V)



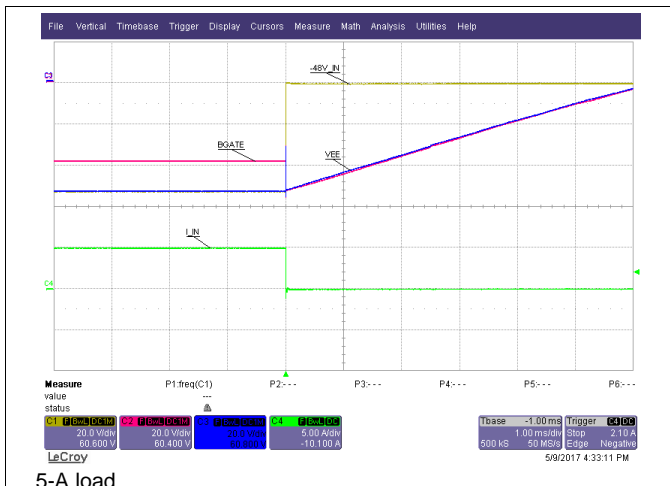


Figure 29. Short on Vin

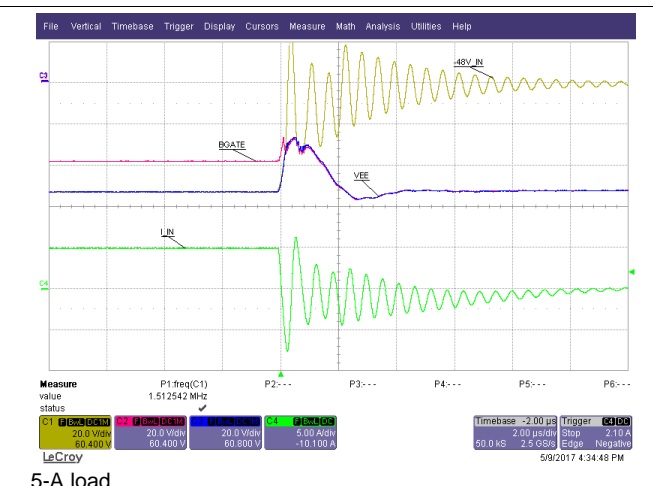


Figure 30. Short on Vin

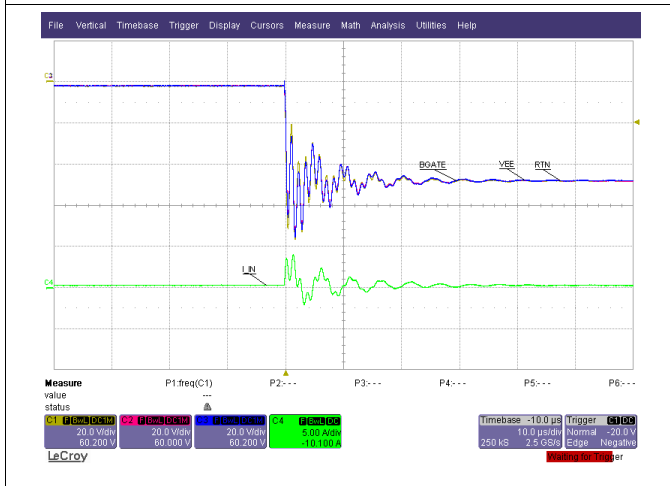


Figure 31. Reverse Hook Up

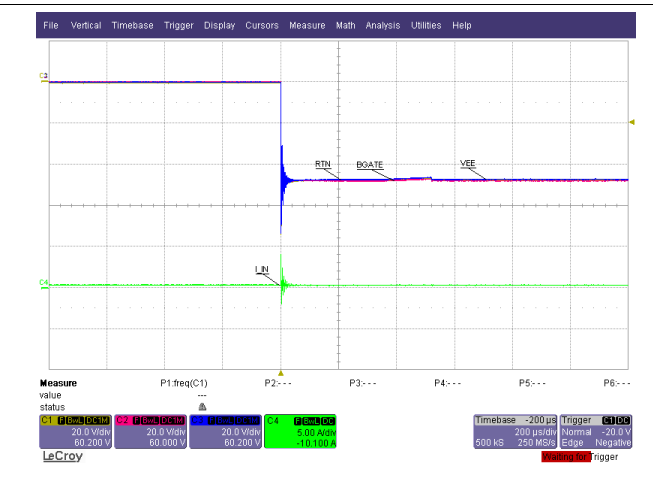


Figure 32. Reverse Hook Up

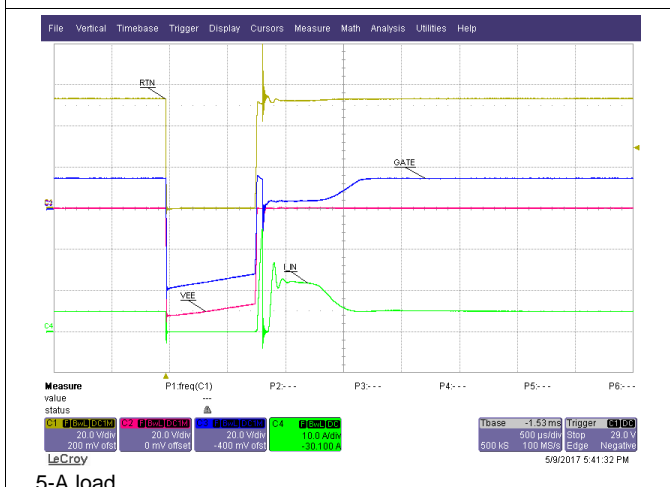


Figure 33. 1-ms Brown Out

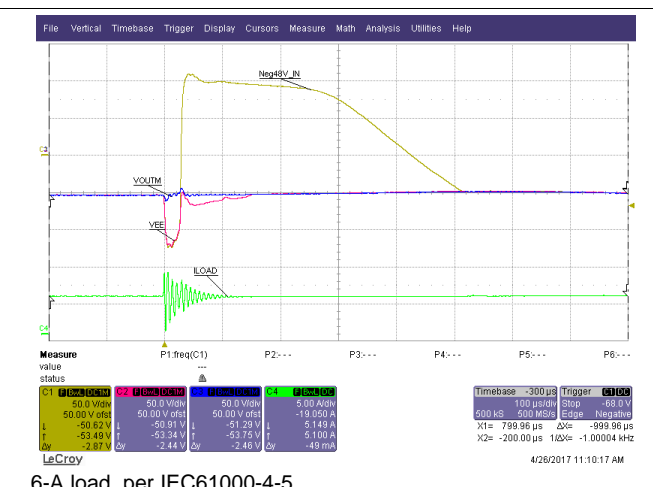
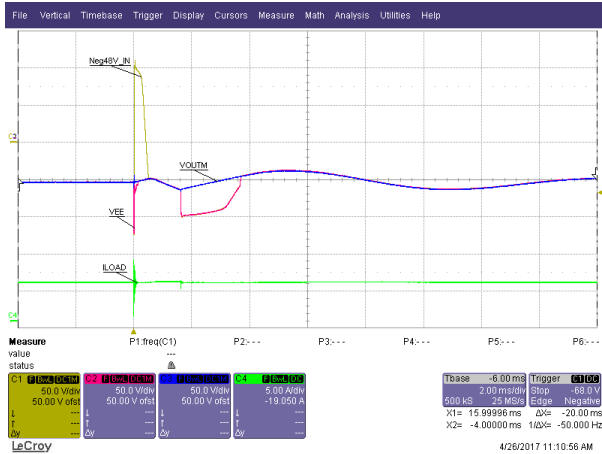
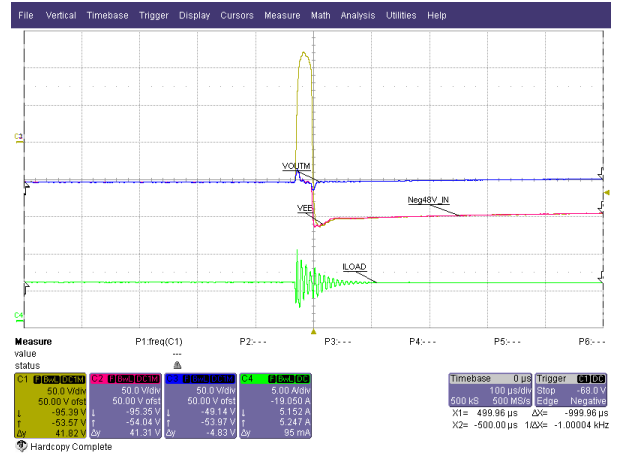


Figure 34. 2 kV (2 Ω) Lightning Surge



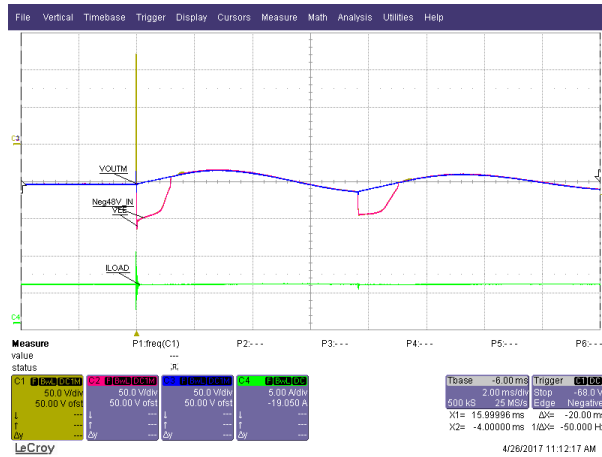
6-A load, per IEC61000-4-5

Figure 35. 2 kV (2 Ω) Lightning Surge



6-A load, per IEC61000-4-5

Figure 36. -2 kV (2 Ω) Lightning Surge



6-A load, per IEC61000-4-5

Figure 37. -2 kV (2 Ω) Lightning Surge

## 10 Power Supply Recommendations

In general, the TPS23523 is designed to have robust operation from a non-ideal  $-48\text{ V}$  bus with various transients such as the lightning surge. The IC is powered through RVCC making it more immune to supply drop outs and high voltage spikes. Regardless, TI recommends following several key precautions:

- Always test the solution with the various transients that can be encountered in the systems. This especially applies to transients that were not tested with TI's EVM.
- If large input ripple is expected during start-up, increase the ratio of  $C_{SS, VEE}$  to  $C_{SS}$  to reduce input current ripple at start-up.
- Operating from large input inductance ( $>40\ \mu\text{H}$ ) can cause instability to the current limit loop or oscillations during start-up. Add a capacitor from Gate to VEE to help stabilize the current limit loop. Add an input snubber if oscillations are observed at start-up.

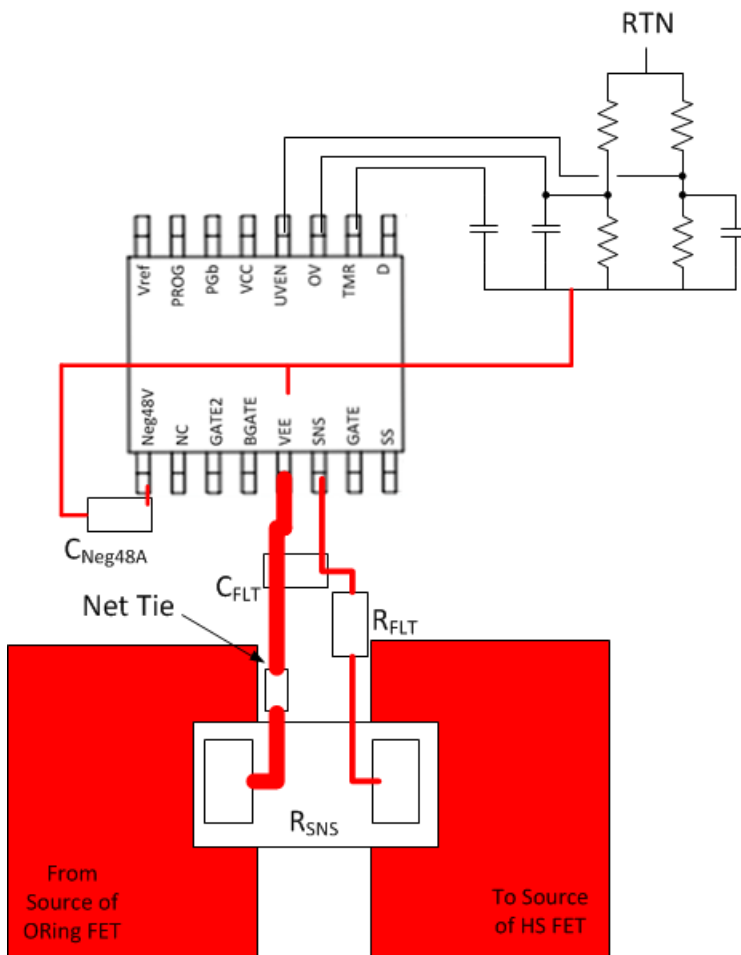
## 11 Layout

### 11.1 Layout Guidelines

There are several things to keep in mind during layout of the TPS23523 circuit:

- The VEE and SNS pin need to have a Kelvin Sense connection to the sense resistor.
- The VEE trace carries current and needs to be thick and short in order to minimize IR drop and to avoid introducing current sensing error.
- It is recommended to use a net-tie to separate the power plane coming into the  $R_{SNS}$  and the Kelvin connection to VEE.
- Connect the Neg48Vx filtering caps, UVEN resistor divider, OV resistor divider, and TMR cap to the "VEE" to insure maximum accuracy.
- The filtering caps on Neg48V and SNS should be placed as close to the IC as possible.

### 11.2 Layout Example



**Figure 38. Layout Example**

## 12 器件和文档支持

### 12.1 器件支持

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### 12.2 文档支持

#### 12.2.1 相关文档

如需相关文档，请参阅：

- 《TPS23525EVM-815 评估模块用户指南》(SLVUB36)

### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.7 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS23523PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23523	<a href="#">Samples</a>
TPS23523PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23523	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23523PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS23523PWT	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23523PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
TPS23523PWT	TSSOP	PW	16	250	210.0	185.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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