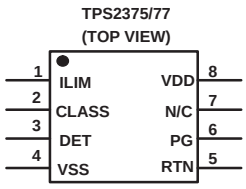
IEEE 802.3af PoE POWERED DEVICE CONTROLLERS

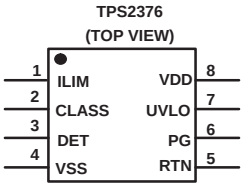
FEATURES

- Fully Supports IEEE 802.3af Specification
- Integrated 0.58-Ω, 100-V, Low-Side Switch
- 15-kV System Level ESD Capable
- Supports Use of Low-Cost Silicon Rectifiers
- Programmable Inrush Current Control
- Fixed 450-mA Current Limit
- Fixed and Adjustable UVLO Options
- Open-Drain, Power-Good Reporting
- Overtemperature Protection
- Industrial Temperature Range: -40°C to 85°C
- 8-Pin SOIC and TSSOP Packages

APPLICATIONS

- VoIP Phones
- WLAN Access Points
- Security Cameras
- Internet Appliances
- POS Terminals





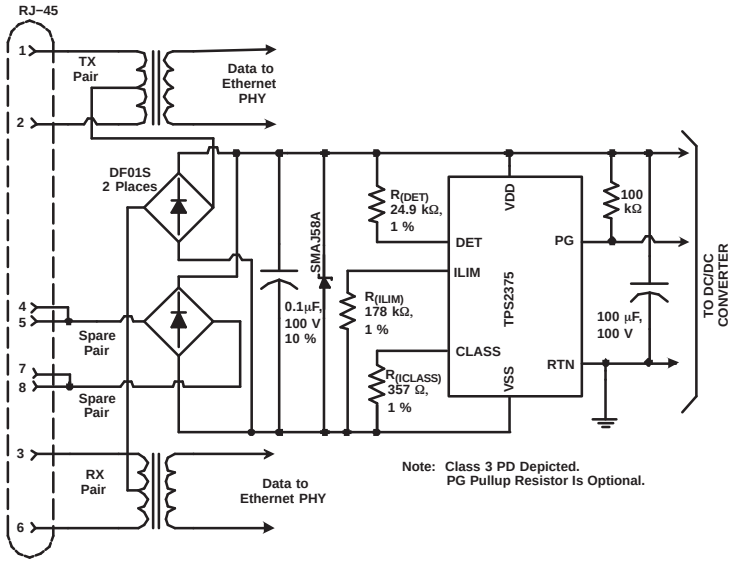
DESCRIPTION

These easy-to-use 8-pin integrated circuits contain all of the features needed to develop an IEEE 802.3af compliant powered device (PD). The TPS2375 family is a second generation PDC (PD Controller) featuring 100-V ratings and a true open-drain, power-good function.

In addition to the basic functions of detection, classification and undervoltage lockout (UVLO), these controllers include an adjustable inrush limiting feature. The TPS2375 has 802.3af compliant UVLO limits, the TPS2377 has *legacy* UVLO limits, and the TPS2376 has a programmable UVLO with a dedicated input pin.

The TPS2375 family specifications incorporate a voltage offset of 1.5 V between its limits and the IEEE 802.3af specifications to accommodate the required input diode bridges used to make the PD polarity insensitive.

Additional resources can be found on the TI Web site www.ti.com.



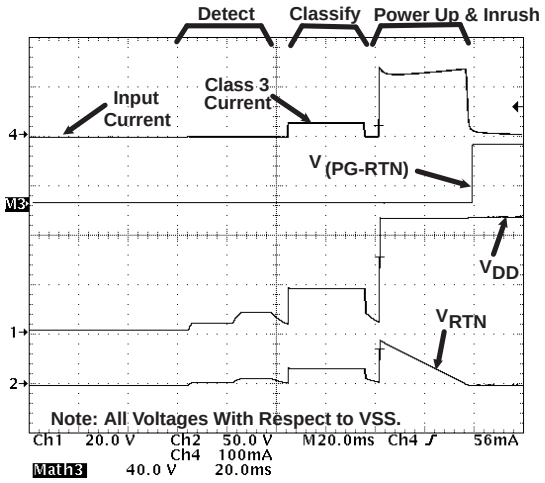


Figure 1. Typical Application Circuit and Startup Waveforms

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	UVLO THRESHOLDS (NOMINAL)			PACKAGE(1)		MARKING
	TYPE	LOW	HIGH	SO-8	TSSOP-8	
-40°C to 85°C	802.3af	30.5 V	39.3 V	TPS2375D	TPS2375PW	2375
	Adjustable	1.93 V	2.49 V	TPS2376D	TPS2376PW	2376
	Legacy	30.5 V	35.1 V	TPS2377D	TPS2377PW	2377

(1) Add an R suffix to the device type for tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1), voltages are referenced to $V_{(VSS)}$

			TPS237x
	Voltage	VDD, RTN, DET, PG(2)	-0.3 V to 100 V
		ILIM, UVLO	-0.3 V to 10 V
		CLASS	-0.3 V to 12 V
	Current, sinking	RTN(3)	0 to 515 mA
		PG	0 to 5 mA
		DET	0 to 1 mA
	Current, sourcing	CLASS	0 to 50 mA
		ILIM	0 to 1 mA
	ESD	Human body model	2 kV
		Charged device model	500 V
		System level (contact/air) at RJ-45(4)	8/15 kV
T_J	Maximum junction temperature range		Internally limited
T_{stg}	Storage temperature range		-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds - Green Packages		260°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds - Nongreen Packages		235°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) $I_{(RTN)} = 0$
(3) SOA limited to $V_{(RTN)} = 80$ V and $I_{(RTN)} = 515$ mA.
(4) Surges applied to RJ-45 of Figure 1 between pins of RJ-45, and between pins and output voltage rails per EN61000-4-2, 1999.

DISSIPATION RATING TABLE(1)

PACKAGE	θ_{JA} (LOW-K) °C/W	θ_{JA} (HIGH-K) °C/W	POWER RATING (HIGH-K) T_A = 85°C mW
D (SO-8)	238	150	266
PW (TSSOP-8)	258.5	159	251

(1) Tested per JEDEC JESD51. High-K is a (2 signal – 2 plane) test board and low-K is a double sided board with minimum pad area and natural convection.

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RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Input voltage range	VDD, PG, RTN	0	57	V
		UVLO	0	5	V
	Operating current range (sinking)	RTN	0	350	mA
	Classification resistor(1)	CLASS	255	4420	Ω
$R_{(ILIM)}$	Inrush limit program resistor (1)		62.5	500	kΩ
	Sinking current	PG	0	2	mA
T_J	Operating junction temperature		-40	125	°C
T_A	Operating free–air temperature		-40	85	°C

(1) Voltage should not be eternally applied to CLASS and ILIM.

ELECTRICAL CHARACTERISTICS

$V_{(VDD)}$ = 48 V, $R_{(DET)}$ = 24.9 kΩ, $R_{(CLASS)}$ = 255 Ω, $R_{(ILIM)}$ = 178 kΩ, and –40°C ≤ T_J ≤ 125°C, unless otherwise noted. Positive currents are into pins. $V_{(UVLO)}$ = 0 V for classification and $V_{(UVLO)}$ = 5 V otherwise for the TPS2376. Typical values are at 25°C. All voltages are with respect to VSS unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DETECTION							
	Offset current	DET open, $V_{(VDD)} = V_{(RTN)}$ = 1.9 V, measure $I_{(VDD)} + I_{(RTN)}$			0.3	3	µA
	Sleep current	DET open, $V_{(VDD)} = V_{(RTN)}$ = 10.1 V, measure $I_{(VDD)} + I_{(RTN)}$			4	12	µA
	DET leakage current	$V_{(DET)} = V_{(VDD)}$ = 57 V, measure $I_{(DET)}$			0.1	5	µA
	Detection current	$V_{(RTN)} = V_{(VDD)}$, $R_{(DET)}$ = 24.9 kΩ, measure $I_{(VDD)} + I_{(RTN)} + I_{(DET)}$	$V_{(VDD)}$ = 1.4 V	53.7	56	58.3	µA
			$V_{(VDD)}$ = 10.1 V	395	410	417	µA
CLASSIFICATION							
$I_{(CLASS)}$	Classification current(1)	$R_{(CLASS)}$ = 4420 Ω, 13 ≤ $V_{(VDD)}$ ≤ 21 V		2.2	2.4	2.8	mA
		$R_{(CLASS)}$ = 953 Ω, 13 ≤ $V_{(VDD)}$ ≤ 21 V		10.3	10.6	11.3	
		$R_{(CLASS)}$ = 549 Ω, 13 ≤ $V_{(VDD)}$ ≤ 21 V		17.7	18.3	19.5	
		$R_{(CLASS)}$ = 357 Ω, 13 ≤ $V_{(VDD)}$ ≤ 21 V		27.1	28.0	29.5	
		$R_{(CLASS)}$ = 255 Ω, 13 ≤ $V_{(VDD)}$ ≤ 21 V		38.0	39.4	41.2	
$V_{(CL_ON)}$	Classification lower threshold	Regulator turns on, $V_{(VDD)}$ rising		10.2	11.3	13.0	V
$V_{(CU_OFF)}$	Classification upper threshold	Regulator turns off, $V_{(VDD)}$ rising		21	21.9	23	V
$V_{(CU_H)}$		Hysteresis		0.5	0.78	1	V
	Leakage current	$V_{(CLASS)}$ = 0 V, $V_{(VDD)}$ = 57 V				1	µA
PASS DEVICE							
$r_{DS(on)}$	On resistance	$I_{(RTN)}$ = 300 mA			0.58	1.0	Ω
	Leakage current	$V_{(VDD)} = V_{(RTN)}$ = 30 V, $V_{(UVLO)}$ = 0 V (TPS2376)				15	µA
	Current limit	$V_{(RTN)}$ = 1 V		405	461	515	mA
$I_{(LIM)}$	Inrush limit	$V_{(RTN)}$ = 2 V, $R_{(ILIM)}$ = 178 kΩ		100	130	180	mA
	Inrush current termination (2)	$V_{(RTN)}$ falling, $R_{(ILIM)}$ = 178 kΩ, inrush state→normal operation		85%	91%	100%	
	Current rise time into inrush	$R_{(ILIM)}$ = 69.8 kΩ, $V_{(RTN-VSS)}$ = 5 V, $I_{(RTN)}$ = 30 mA→300 mA, $V_{(VDD)}$ increasing past upper UVLO		15	25		µs
	Current limit response time	Apply load ∞Ω→20 Ω, time measured to $I_{(RTN)}$ = 45 mA			2	2.5	µs
	Leakage current, ILIM	$V_{(VDD)}$ = 15 V, $V_{(UVLO)}$ = 0 V				1	µA

(1) Classification is tested with exact resistor values. A 1% tolerance classification resistor assures compliance with IEEE 802.3af limits.
(2) This parameter specifies the RTN current value, as a percentage of the steady state inrush current, below which it must fall to make PG assert (open-drain).

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ELECTRICAL CHARACTERISTICS (continued)

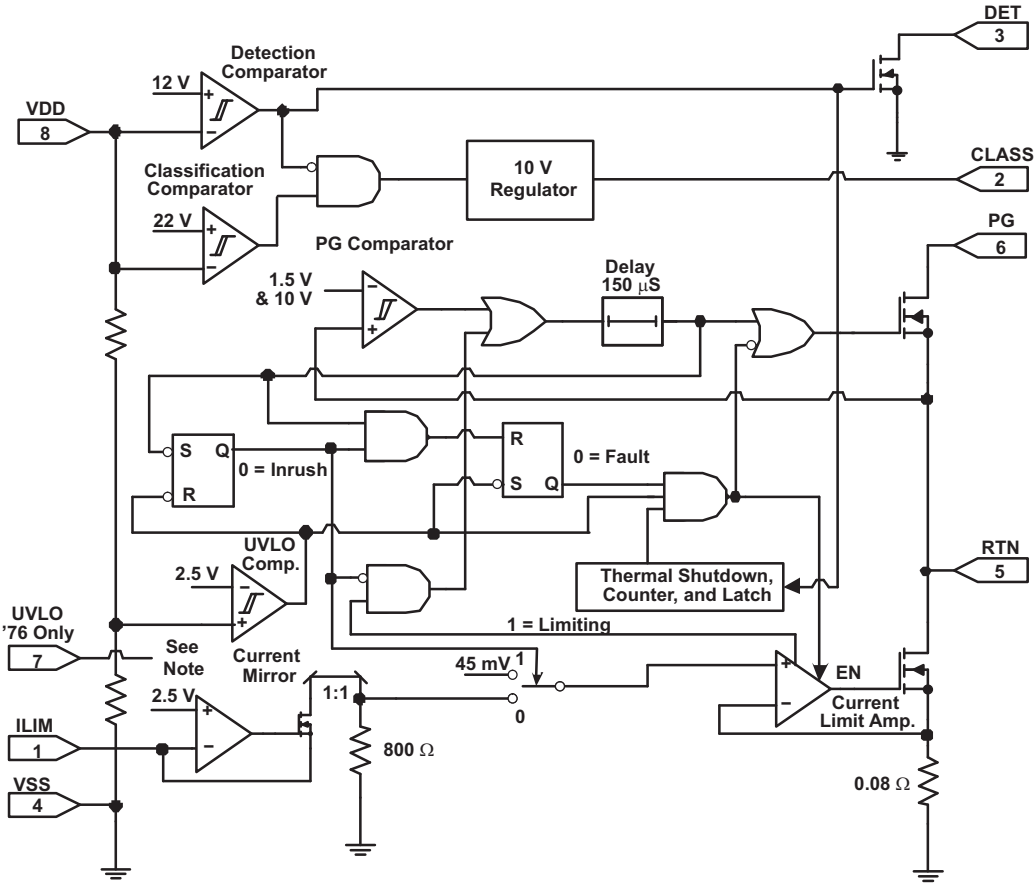
$V_{(VDD)}$ = 48 V, $R_{(DET)}$ = 24.9 kΩ, $R_{(CLASS)}$ = 255 Ω, $R_{(ILIM)}$ = 178 kΩ, and –40°C ≤ T_J ≤ 125°C, unless otherwise noted. Positive currents are into pins. $V_{(UVLO)}$ = 0 V for classification and $V_{(UVLO)}$ = 5 V otherwise for the TPS2376. Typical values are at 25°C. All voltages are with respect to VSS unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG						
	Latchoff voltage threshold rising	$V_{(RTN)}$ rising	9.5	10.0	10.5	V
	PG deglitch	Delay rising and falling PG	75	150	225	µs
	Output low voltage	$I_{(PG)}$ = 2 mA, $V_{(RTN)}$ = 34 V, $V_{(VDD)}$ = 38 V, $V_{(RTN)}$ falling		0.12	0.4	V
		$I_{(PG)}$ = 2 mA, $V_{(RTN)}$ = 0 V, $V_{(VDD)}$ = 25 V, for TPS2376 $V_{(UVLO)}$ = 0 V		0.12	0.4	V
	Leakage current	$V_{(PG)}$ = 57 V, $V_{(RTN)}$ = 0 V		0.1	1	µA
UVLO						
$V_{(UVLO_R)}$	TPS2375 Voltage at VDD	$V_{(VDD)}$ rising	38.4	39.3	40.4	V
$V_{(UVLO_F)}$		$V_{(VDD)}$ falling	29.6	30.5	31.5	
		Hysteresis	8.3	8.8	9.1	
	TPS2376 Voltage at UVLO	$V_{(VDD)}$ rising	2.43	2.49	2.57	V
		$V_{(VDD)}$ falling	1.87	1.93	1.98	
		Hysteresis	0.53	0.56	0.58	
	TPS2377 Voltage at VDD	$V_{(VDD)}$ rising	34.1	35.1	36.0	V
		$V_{(VDD)}$ falling	29.7	30.5	31.4	
		Hysteresis	4.3	4.5	4.8	
	TPS2376 Input leakage, UVLO	$V_{(UVLO)}$ = 0 V to 5 V	-1		1	µA
THERMAL SHUTDOWN						
	Shutdown temperature	Temperature rising	135			°C
	Hysteresis			20		°C
BIAS CURRENT						
	Operating current	$I_{(VDD)}$		240	450	µA

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DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



Note: For the TPS2376, the UVLO comparator connects to the UVLO pin and not to the UVLO divider.

TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER		I/O	DESCRIPTION
	TPS2375/77	TPS2376		
ILIM	1	1	O	Connect a resistor from ILIM to VSS to set the start-up inrush current limit. The equation for calculating the resistor is shown in the detailed pin description section for ILIM.
CLASS	2	2	O	Connect a resistor from CLASS to VSS to set the classification of the powered device (PD). The IEEE classification levels and corresponding resistor values are shown in Table 1.
DET	3	3	O	Connect a 24.9-kΩ detection resistor from DET to VDD for a valid PD detection.
VSS	4	4	I	Return line on the source side of the TPS2375 from the PSE.
RTN	5	5	O	Switched output side return line used as the low-side reference for the TPS2375 load.
PG	6	6	O	Open-drain, power-good output; active high.
UVLO	-	7	I	Used only on the TPS2376. Connect a resistor divider from VDD to VSS to implement the adjustable UVLO feature of the TPS2376.
NC	7	-		No connection
VDD	8	8	I	Positive line from the rectified PSE provided input.

Detailed Pin Description

The following descriptions refer to the schematic of Figure 1 and the functional block diagram.

ILIM: A resistor from this pin to VSS sets the inrush current limit per Equation 1:

$$I_{(LIM)} = \frac{25000}{R_{(ILIM)}} \quad (1)$$

where ILIM is the desired inrush current value, in amperes, and $R_{(ILIM)}$ is the value of the programming resistor from ILIM to VSS, in ohms. The practical limits on $R_{(ILIM)}$ are 62.5 kΩ to 500 kΩ. A value of 178 kΩ is recommended for compatibility with legacy PSEs.

Inrush current limiting prevents current drawn by the bulk capacitor from causing the line voltage to sag below the lower UVLO threshold. Adjustable inrush current limiting allows the use of arbitrarily large capacitors and also accommodates legacy systems that require low inrush currents.

The ILIM pin must not be left open or shorted to VSS.

CLASS: Classification is implemented by means of an external resistor, $R_{(CLASS)}$, connected between CLASS and VSS. The controller draws current from the input line through $R_{(CLASS)}$ when the input voltage lies between 13 V and 21 V. The classification currents specified in the electrical characteristics table include the bias current flowing into VDD and any RTN leakage current.

Table 1. CLASSIFICATION

CLASS	PD POWER (W)	$R_{(CLASS)}$ (Ω)	802.3af LIMITS (mA)	NOTE
0	0.44 – 12.95	4420 ±1%	0 - 4	Default class
1	0.44 – 3.84	953 ±1%	9 - 12	
2	3.84 – 6.49	549 ±1%	17 - 20	
3	6.49 – 12.95	357 ±1%	26 - 30	
4	-	255 ±1%	36 - 44	Reserved for future use

The CLASS pin must not be shorted to ground.

DET: Connect a resistor, $R_{(DET)}$, between DET and VDD. This resistor should equal 24.9 kΩ, ±1% for most applications. $R_{(DET)}$ is connected across the input line when $V_{(VDD)}$ lies between 1.4 V and 11.3 V, and is disconnected when the line voltage exceeds this range to conserve power. This voltage range has been chosen to allow detection with two silicon rectifiers between the controller and the RJ-45 connector.

VSS: This is the input supply negative rail that serves as a local ground to the TPS2375.

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RTN: This pin provides the switched negative power rail used by the downstream circuits. The operational and inrush current limit control current into the pin. The PG circuit monitors the RTN voltage and also uses it as the return for the PG pin pulldown transistor. The internal MOSFET body diode clamps VSS to RTN when voltage is present between VDD and RTN and the PoE input is not present.

PG: This pin goes to a high resistance state when the internal MOSFET that feeds the RTN pin is enabled, and the device is not in inrush current limiting. In all other states except detection, the PG output is pulled to RTN by the internal open-drain transistor. Performance is assured with at least 4 V between VDD and RTN.

PG is an open-drain output; therefore, it may require a pullup resistor or other interface.

UVLO: This pin is specific to the TPS2376; it is not internally connected on the TPS2375 and TPS2377. The UVLO pin is used with an external resistor divider between VDD and VSS to set the upper and lower UVLO thresholds. The hysteresis, as measured as a percentage of the upper UVLO, is the same as the TPS2375.

The TPS2376 enables the output when $V_{(UVLO)}$ exceeds the upper UVLO threshold. When current begins to flow, VDD sags due to cable resistance and the dynamic resistance of the input diodes. The lower UVLO threshold must be below the lowest voltage that the input reaches.

The TPS2376 implements adjustable UVLO thresholds, but is otherwise functionally equivalent to the TPS2375. The TPS2375 offers fixed UVLO thresholds designed to maximize hysteresis while maintaining compatibility with the IEEE 802.3af standard. The TPS2377 offers fixed UVLO thresholds optimized for use with legacy PoE systems.

VDD: This is the positive input supply to the TPS2375, which is also common to downstream load circuits. This pin provides operating power and allows the controller to monitor the line voltage to determine the mode of operation.

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TYPICAL CHARACTERISTICS

Graphs over temperature are interpolations between the marked data points.

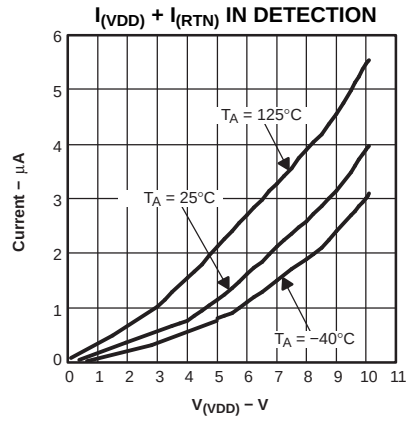


Figure 2.

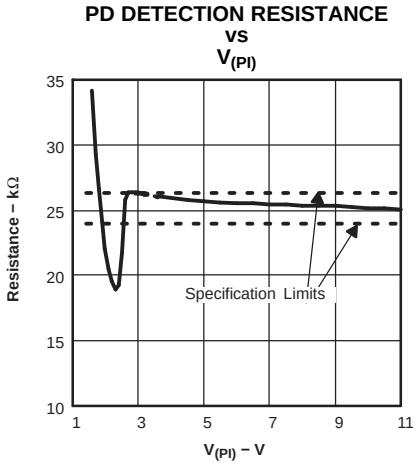


Figure 3.

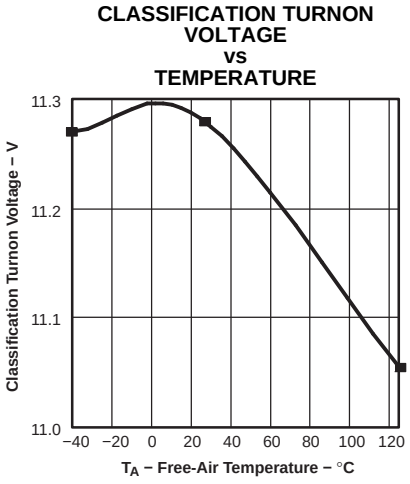


Figure 4.

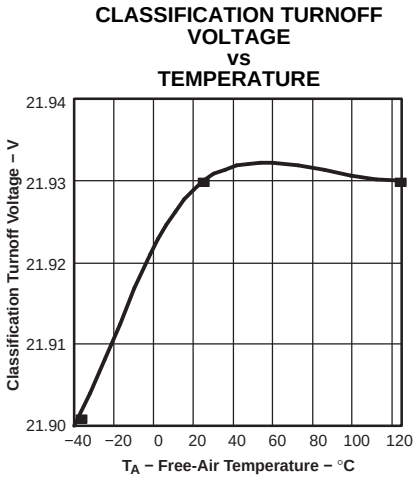


Figure 5.

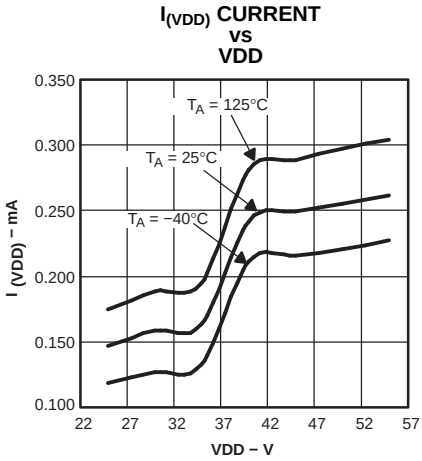


Figure 6.

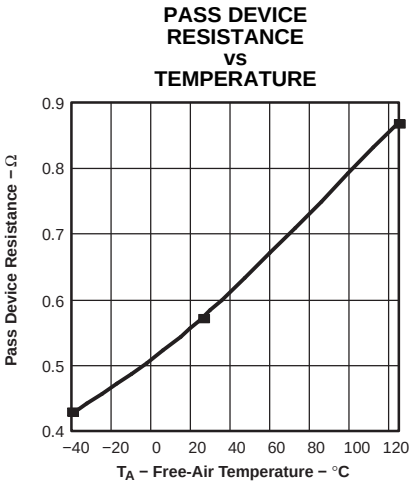


Figure 7.

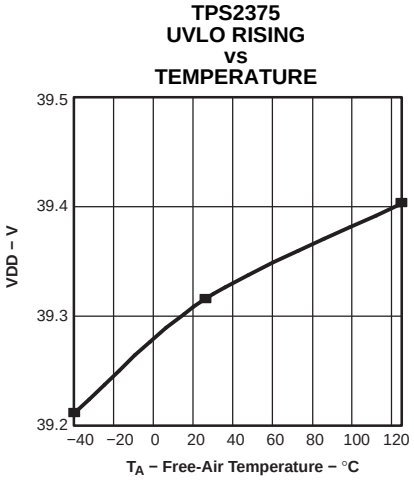


Figure 8.

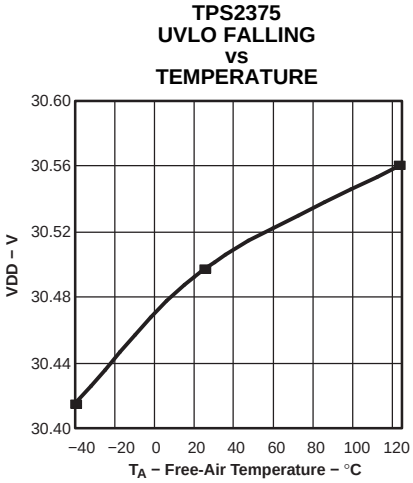


Figure 9.

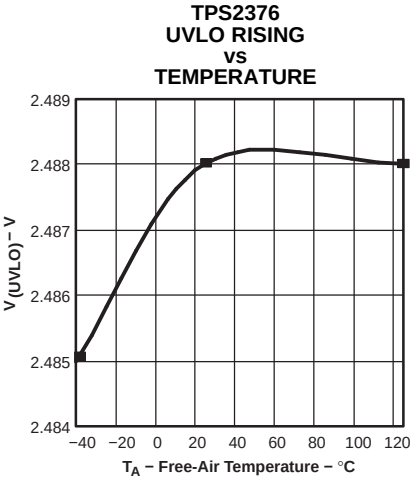


Figure 10.

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TYPICAL CHARACTERISTICS (continued)

Graphs over temperature are interpolations between the marked data points.

TPS2376
UVLO FALLING
vs
TEMPERATURE

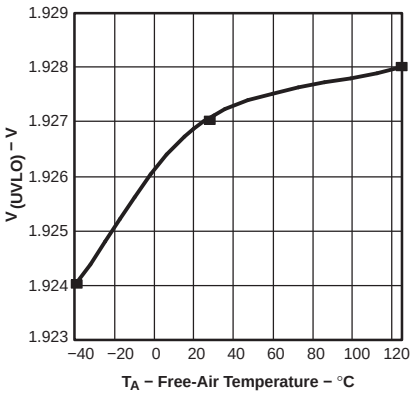


Figure 11.

TPS2377
UVLO RISING
vs
TEMPERATURE

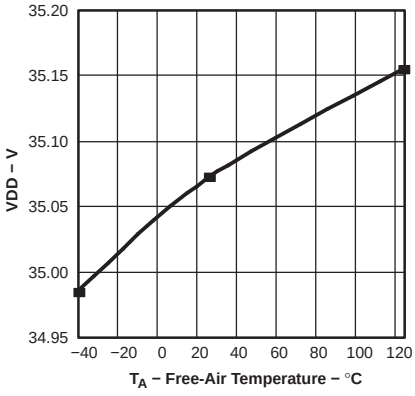


Figure 12.

TPS2377
UVLO FALLING
vs
TEMPERATURE

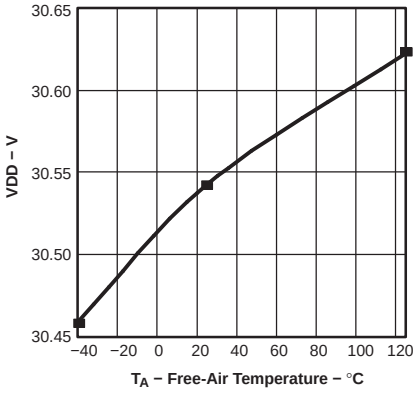


Figure 13.

INRUSH STATE TERMINATION
THRESHOLD
vs
TEMPERATURE

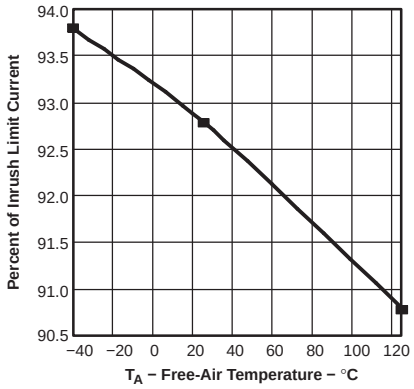


Figure 14.

INRUSH CURRENT
vs
TEMPERATURE

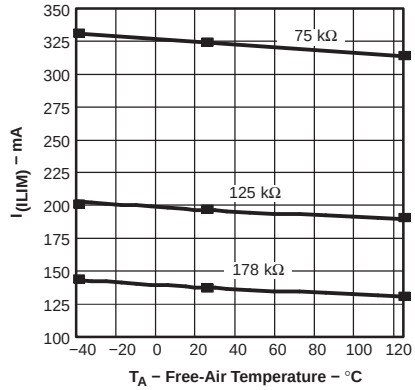


Figure 15.

CURRENT LIMIT
vs
TEMPERATURE

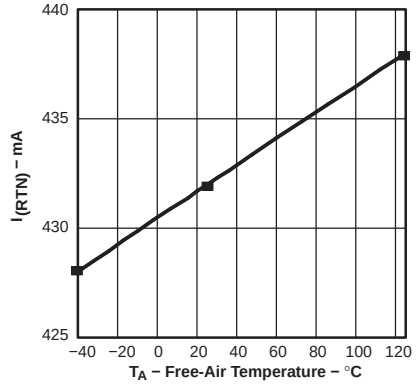


Figure 16.

PG DEGLITCH PERIOD
vs
TEMPERATURE

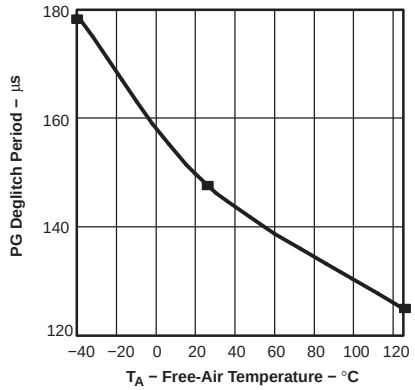


Figure 17.

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APPLICATION INFORMATION

OVERVIEW

The IEEE 802.3af specification defines a process for safely powering a PD over a cable, and then removing power if a PD is disconnected. The process proceeds through three operational states: detection, classification, and operation. The intent behind the process is to leave an unterminated cable unpowered while the PSE periodically checks for a plugged-in device; this is referred to as detection. The low power levels used during detection are unlikely to cause damage to devices not designed for PoE. If a valid PD signature is present, then the PSE may optionally inquire how much power the PD requires; this is referred to as classification. The PD may return a default full-power signature, or one of four other choices. Knowing the power demand of each PD allows the PSE to intelligently allocate power between PDs, and also to protect itself against overload. The PSE powers up a valid PD, and then monitors its output for overloads. The maintain power signature (MPS) is presented by the powered PD to assure the PSE that it is there. The PSE monitors its output for the MPS to see if the PD is removed, and turns the port off, if it loses the MPS. Loss of MPS returns the PSE to the initial state of detection. Figure 18 shows the operational states as a function of PD input voltage range.

The PD input is typically an RJ-45 (8-pin) connector, referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops in the cable and margin. The specification uses a cable resistance of 20 Ω to derive the voltage limits at the PD from the PSE output requirements. Although the standard specifies an output power of 15.4 W at the PSE output, there is only 12.95 W available at the input of the PD due to the worst case power loss in the cable.

The PSE can apply voltage either between the RX and TX pairs, or between the two spare pairs as shown in Figure 1. The applied voltage can be of either polarity. The PSE cannot apply voltage to both paths at the same time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges cause a difference between the IEEE 802.3af limits at the PI and the TPS2375 specifications.

The PSE is required to current limit between 350 mA and 400 mA during normal operation, and it must disconnect the PD if it draws this current for more than 75 ms. The PSE may set lower output current limits based on the PD advertised power requirements, as discussed below.

The following discussion is intended as an aid in understanding the operation of the TPS2375, but not as a substitute for the actual IEEE 802.3af standard. Standards change and should always be referenced when making design decisions.

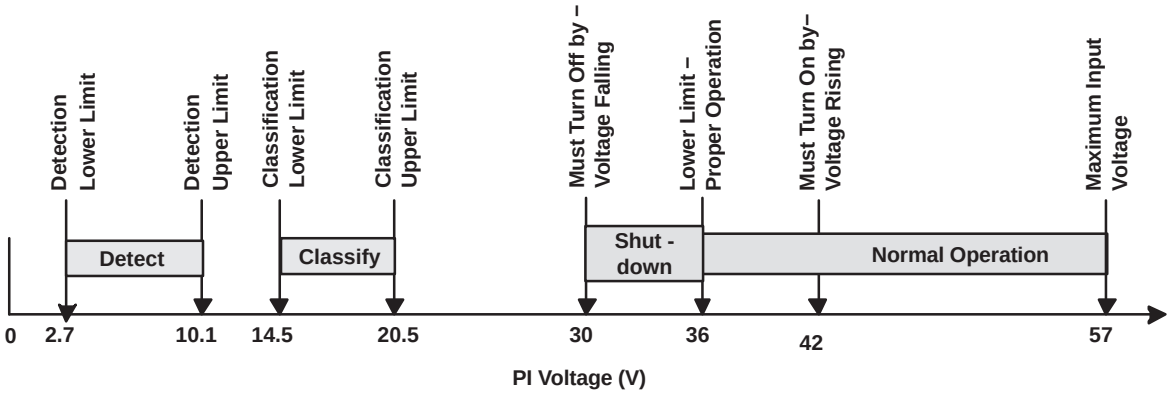


Figure 18. IEEE 802.3 PD Limits

INTERNAL THRESHOLDS

In order to implement the PoE functionality as shown in Figure 18, the TPS2375 has a number of internal comparators with hysteresis for stable switching between the various states. Figure 19 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled *idle* between classification and detection implies that the DET, CLASS, PG, and RTN pins are all high impedance.

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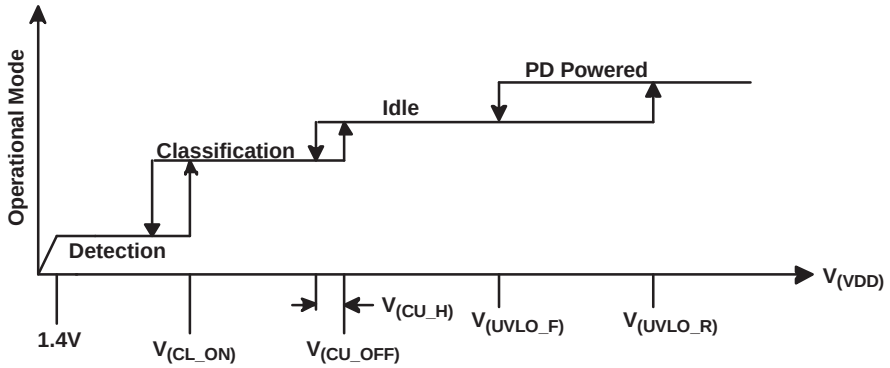


Figure 19. Threshold Voltages

DETECTION

This feature of IEEE 802.3af eliminates powering and potentially damaging Ethernet devices not intended for application of 48 V. When a voltage in the range of 2.7 V to 10.1 V is applied to the PI, an incremental resistance of 25 kΩ signals the PSE that the PD is capable of accepting power. A PD that is capable of accepting power, but is not ready, may present an incorrect signature intentionally. The incremental resistance is measured by applying two different voltages to the PI and measuring the current it draws. These two test voltages must be within the specified range and be at least 1 V apart. The incremental resistance equals the difference between the voltages divided by the difference between the currents. The allowed range of resistance is 23.75 kΩ to 26.25 kΩ.

The TPS2375 is in detection mode whenever the supply voltage is below the lower classification threshold. The TPS2375 draws a minimum of bias power in this condition, while PG and RTN are high impedance and the circuits associated with ILIM and CLASS are disabled. The DET pin is pulled to ground during detection. Current flowing through $R_{(DET)}$ to VSS (Figure 1) produces the detection signature. For most applications, a 24.9-kΩ, 1%, resistor is recommended. $R_{(DET)}$ can be a small, low-power resistor because it only sees a stress of about 5 mW. When the input voltage rises above the 11.3 V lower classification comparator threshold, the DET pin goes to an open-drain condition to conserve power.

The input diode bridge incremental resistance can be hundreds of ohms at the low currents seen at 2.7 V on the PI. The bridge resistance is in series with $R_{(DET)}$ and increases the total resistance seen by the PSE. This varys with the type of diode selected by the designer, and it is not usually specified on the diode data sheet. The value of $R_{(DET)}$ may be adjusted downwards to accommodate a particular diode type.

CLASSIFICATION

Once the PSE has detected a PD, it may optionally classify the PD. This process allows a PSE to determine the PD power requirements in order to allot only as much power as necessary from its fixed input power source. This allows the PSE to power the maximum number of PDs from a particular power budget. This step is optional because some PSEs can afford to allot the full power to every powered port.

The classification process applies a voltage between 14.5 V and 20.5 V to the input of the PD, which in turn draws a fixed current set by $R_{(CLASS)}$. The PSE measures the PD current to determine which of the five available classes (Table 1) that the PD is signalling. The total current drawn from the PSE during classification is the sum of bias currents and current through $R_{(CLASS)}$. The TPS2375 disconnects $R_{(CLASS)}$ at voltages above the classification range to avoid excessive power dissipation (Figure 18 and Figure 19).

The value of $R_{(CLASS)}$ should be chosen from the values listed in Table 1 based on the average power requirements of the PD. The power rating of this resistor should be chosen so that it is not overstressed for the required 75-ms classification period, during which 10 V is applied. The PD could be in classification for extended periods during bench test conditions, or if an auxiliary power source with voltage within the classification range is connected to the PD front end. Thermal protection may activate and turn classification off if it continues for more than 75 ms, but the design must not rely on this function to protect the resistor.

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UNDERVOLTAGE LOCKOUT (UVLO)

The TPS2375 incorporates an undervoltage lockout (UVLO) circuit that monitors line voltage to determine when to apply power to the downstream load and allow the PD to power up. The IEEE 802.3af specification dictates a maximum PD turnon voltage of 42 V and a minimum turnoff voltage of 30 V (Figure 19). The IEEE 802.3af standard assumes an 8-V drop in the cabling based on a 20-Ω feed resistance and a 400-mA maximum inrush limit. Because the minimum PSE output voltage is 44 V, the PD must continue to operate properly with input voltages as low as 36 V. The TPS2375 UVLO limits are designed to meet the turnon, turnoff, and hysteresis requirements.

Various legacy PSE systems in the field do not meet the minimum output voltage of 44 V. The TPS2377 UVLO limits are designed to support these systems with a lower turnon voltage and smaller hysteresis. Although the TPS2377 works with compliant PSEs, it could potentially exhibit startup instabilities if the PSE output voltage rises slowly. The TPS2375 is recommended for applications with compliant PSEs.

In order to provide flexibility for noncompliant designs, the TPS2376 allows the designer to program the turnon thresholds with a resistor divider. The hysteresis of the TPS2376, measured as a percentage of the turnon voltage, is similar to that of the TPS2375. To use the TPS2376, connect a resistor divider between VDD and VSS with the tap connected to the UVLO pin. The total divider resistance appears in parallel with the $R_{(DET)}$, and the combination of the two should equal 24.9 kΩ. The divider ratio should be chosen to obtain 2.5 V at the UVLO pin when $V_{(VDD)}$ is at the desired turnon voltage.

The TPS2375 uses the UVLO function to control the load through an onboard MOSFET switch. Figure 19 graphically shows the relationships of the UVLO thresholds defined in the Electrical Characteristics section to the TPS2375 operational states.

PROGRAMMABLE INRUSH CURRENT LIMIT AND FIXED OPERATIONAL CURRENT LIMIT

Inrush limiting is beneficial for a number of reasons. First, it provides a mechanism to keep the inrush current below the 400 mA, 50 ms, maximum inrush allowed by the standard. Second, by reducing the level of the current limit below the PSE operational limit, which can be as low as the classification power divided by the PSE voltage, it allows an arbitrarily large bulk capacitor to be charged. Third, some legacy PSEs may not tolerate large inrush currents while powering their outputs up.

The TPS2375 operational current limit protects the internal power switch from instantaneous output faults and current surges. The minimum operational current limit level of 405 mA is above the maximum PSE output current limit of 400 mA. This current limit allows the PD to draw the maximum available power and also allows the PSE to detect fault conditions.

The TPS2375 incorporates a state machine that controls the inrush and operational current limit states. When $V_{(VDD)}$ is below the lower UVLO threshold, the current limit state machine is reset. In this condition, the RTN pin is high impedance, and at $V_{(VDD)}$ once the output capacitor is discharged by the downstream circuits. When $V_{(VDD)}$ rises above the UVLO turnon threshold, the TPS2375 enables the internal power MOSFET with the current limit set to the programmed inrush value. The load capacitor charges and the RTN pin voltage falls from $V_{(VDD)}$ to nearly $V_{(VSS)}$. Once the inrush current falls about 10% below the programmed limit, the current limit switches to the internal 450-mA operational level after a 150-µs delay. This switchover can be seen in the operation of PG, which goes active (open drain) after inrush terminates as seen in Figure 1. The internal power MOSFET is disabled if the input voltage drops below the lower UVLO threshold.

When in the operating current-limit state, a fault on the output or a large input transient can cause the internal MOSFET to limit current. The RTN voltage rises above its normal operating level of less than 0.5 V while in current-limit state. If $V_{(RTN)}$ rises above 10 V for more than 150 µs, the MOSFET is latched off. The PD input voltage must drop below the lower UVLO threshold to clear this latch. If the RTN voltage does not exceed 10 V while in current-limit state, but the condition persists long enough to overheat the TPS2375, the thermal limit circuit activates, as described in the thermal protection section.

Practical values of $R_{(ILIM)}$ lie between 62.5 kΩ and 500 kΩ. The pin must not be left open. An inrush level of 140 mA, set by an $R_{(ILIM)}$ of 178 kΩ, should be used with TPS2377 applications for compatibility with legacy systems. This same inrush current level suffices for many TPS2375 applications.

The inrush limit, the bulk capacitor size, and the downstream dc/dc converter startup method must be chosen so that the converter input current does not exceed the inrush current limit while it is active. This can be achieved by using the PG output to enable the downstream converter after inrush finishes, by delaying the converter startup until inrush finishes, or by increasing the value of the inrush current limit.

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MAINTAIN POWER SIGNATURE

Once a valid PD has been detected and powered, the PSE uses the maintain power signature (MPS) to determine when to remove power from the PI. The PSE removes power from that output port if it detects loss of MPS for 300 ms or more. A valid MPS requires the PD to draw at least 10 mA and also have an ac impedance less than 26.25 kΩ in parallel with 0.05 µF. TI's reference designs meet the requirements necessary to maintain power.

POWER GOOD

The TPS2375 includes a power-good circuit that can be used to signal the PD circuitry that the load capacitor is fully charged. This pin is intended for use as an enable signal for downstream circuitry. If the converter tries to start up while inrush is active, and draws a current equal to the inrush limit, a latchup condition occurs in which the PD never successfully starts. Using the PG pin is the safest way to assure that there are no undesired interactions between the inrush limit, the converter startup characteristic, and the size of the bulk capacitor.

The PG pin goes to an open-drain state approximately 150 µs after the inrush current falls 10% below the regulated value. PG pulldown current is only assured when the voltage difference between VDD and RTN exceeds 4 V. This is not a limiting factor because the dc/dc converter should not be able to run from 4 V. The PG output is pulled to RTN whenever the MOSFET is disabled or is in inrush current limiting.

Referencing PG to RTN simplifies the interface to the downstream dc/dc converter or other circuit because it is referenced to RTN, not VSS. Care must be used in interfacing the PG pin to the downstream circuits. The pullup to VDD shown in Figure 1 may not be appropriate for a particular dc/dc converter interface. The PG pin connects to an internal open-drain, 100-V transistor capable of sinking 2 mA to a voltage below 0.4 V. The PG pin can be left open if it is not used.

THERMAL PROTECTION

The controller may overheat after operation in current-limit state or classification for an extended period of time, or if the ambient temperature becomes excessive. The TPS2375 protects itself by disabling the RTN and CLASS pins when the internal die temperature reaches about 140°C. It automatically restarts when the die temperature has fallen approximately 20°C. If this cycle occurs eight times, then the device latches off until the supply voltage drops below the lower classification threshold. This feature prevents the part from operating indefinitely in fault, and ensures that the PSE recognizes the fault condition when using dc MPS. Thermal protection is active whenever the TPS2375 is not in detection.

Figure 20 shows how the TPS2375 responds when it is enabled into a short. The TPS2375 starts in the inrush current-limit state when the input voltage exceeds the upper UVLO limit. A power dissipation of over 5 W heats the die from 25°C to 140°C in approximately 400 ms. The TPS2375 then shuts down until the die temperature drops to about 120°C, which occurs in about 20 ms. This process repeats eight times before the TPS2375 latches off. The PG pin is high because RTN is tied to VDD.

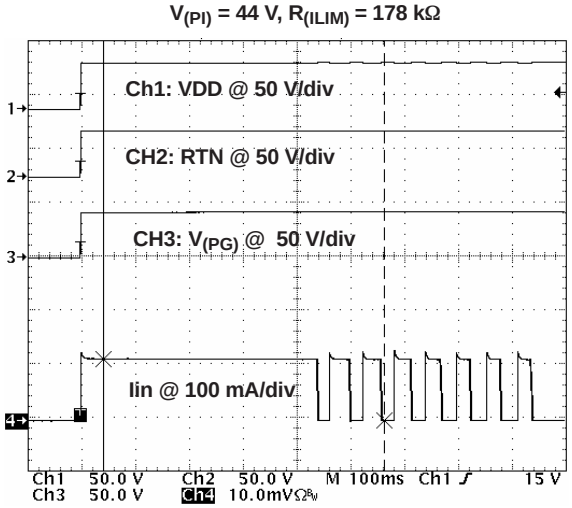


Figure 20. TPS2375 Started Into Short

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POWER SYSTEM DESIGN

The PSE is a power and current limited source, which imposes certain constraints on the PD power supply design. DC/DC converters have both a constant input power characteristic that causes them to draw high currents at low voltage, and they tend to go to a full input power mode during start-up that is often 25% or more above their rated power. Improper design of the power system can cause the PD to not start up with all combinations of Ethernet lines and PSE sources.

The following guidelines should be used:

1. Set the TPS2375 inrush to a moderate value as previously discussed.
2. Hold the dc/dc converter off during inrush as previously discussed.
3. The converter should have a softstart that keeps the peak input start-up current below 400 mA, and preferably only a modest amount over the operating current, with a 44-V PSE source and a 20-Ω loop.
4. If step 3 cannot be met, the bulk input capacitor should not discharge more than 8 V during converter start up from a 400-mA limited, 44-V source with a 20-Ω line. Start-up must be completed in less than 50 mS

Step 4 requires a balance between the converter output capacitance, load, and input bulk capacitance. While there are some cases which may not require all these measures, such as a 1-W PD with minimal converter output capacitance, it is always a good practice to follow them.

AUXILIARY POWER SOURCE ORING

Many PoE capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used regardless of PoE availability. Attempting to create solutions where the two power sources coexist in a specific controlled manner results in additional complexity, and is not generally recommended. Figure 21 demonstrates three methods of diode ORing external power into a PD. Option 1 inserts power on the output side of the PoE power conversion. Option 2 inserts power on the TPS2375 output. Option 3 applies power to the TPS2375 input. Each of these options has advantages and disadvantages. The wall adapter must meet a minimum 1500-Vac dielectric withstand test voltage to the ac input power and to ground for options 2 and 3.

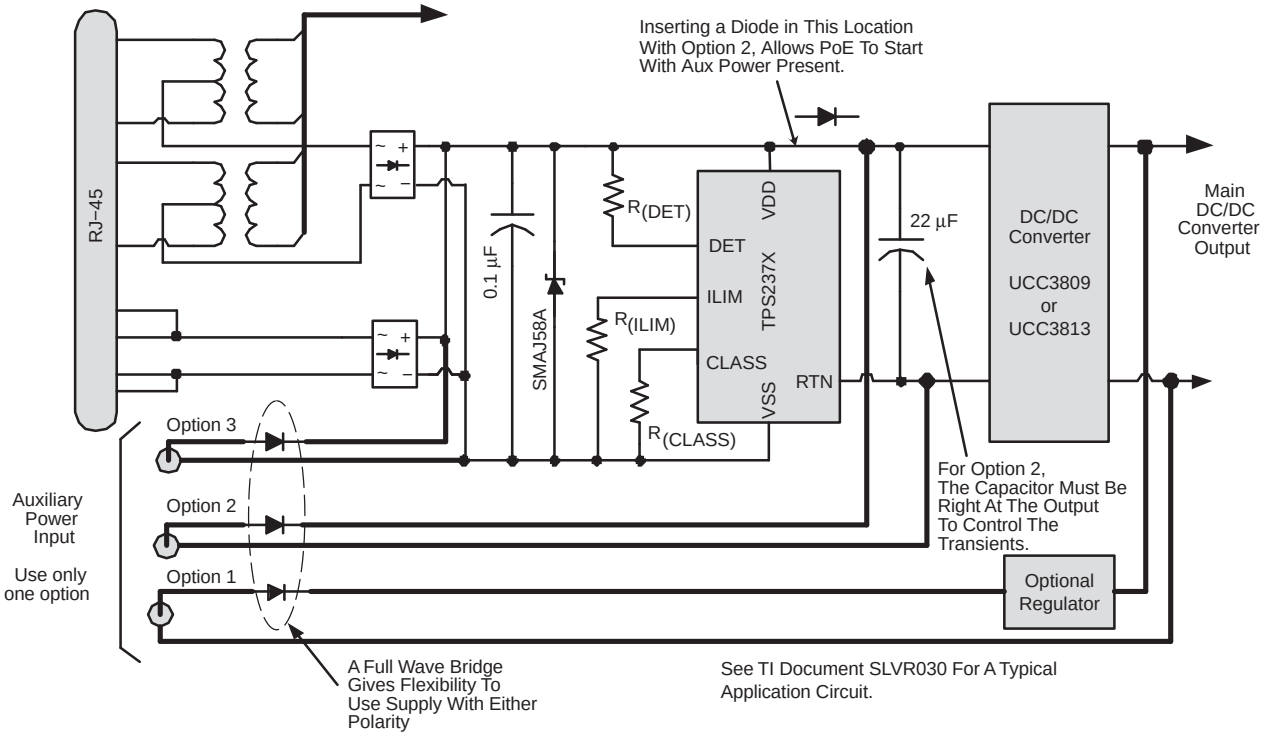


Figure 21. Auxiliary Power ORing

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Option 1 consists of ORing power to the output of the PoE dc/dc converter. This option is preferred in cases where PoE is added to an existing design that uses a low-voltage wall adapter. The relatively large PD capacitance reduces the potential for harmful transients when the adapter is plugged in. The wall adapter output may be grounded if the PD incorporates an isolated converter. This solution requires two separate regulators, but low-voltage adapters are readily available. The PoE power can be given priority by setting its output voltage above that from the auxiliary source.

Option 2 has the benefits that the adapter voltage may be lower than the TPS2375 UVLO, and that the bulk capacitor shown can control voltage transients caused by plugging an adapter in. The capacitor size and location are chosen to control the amount of ringing that can occur on this node, which can be affected by additional filtering components specific to a dc/dc converter design. The optional diode blocks the adapter voltage from reverse biasing the input, and allows a PoE source to apply power provided that the PSE output voltage is greater than the adapter voltage. The penalty of the diode is an additional power loss when running from PSE power. The PSE may not be able to detect and start powering without the diode. This means that the adapter may continue to power the PD until removed. Auxiliary voltage sources can be selected to be above or below the PoE operational voltage range. If automatic PoE precedence is desired when using the low-voltage auxiliary source option, make sure that the TPS2375 inrush program limit is set higher than the maximum converter input current at its lowest operating voltage. It is difficult to use PG with the low-voltage auxiliary source because the converter must operate during a condition when the TPS2375 would normally disable it. Circuits may be designed to force operation from one source or the other depending on the desired operation and the auxiliary source voltage chosen. However, they are not recommended because they increase complexity and thus cost.

Option 3 inserts the power before the TPS2375. It is necessary for the adapter to meet the TPS2375 UVLO turnon requirement and to limit the maximum voltage to 57 V. This option provides a valid power-good signal and simplifies power priority issues. The disadvantage of this method is that it is the most likely to cause transient voltage problems. Plugging a powered adapter in applies a step input voltage to a node that has little capacitance to control the dv/dt and voltage ringing. If the wall mount supply applies power to the PD before the PSE, it prevents the PSE from detecting the PD. If the PSE is already powering the PD when the auxiliary source is plugged in, priority is given to the higher supply voltage.

ESD

The TPS2375 has been tested using the surge of EN61000-4-2 in an evaluation module (EVM) using the circuit in Figure 1. The levels used were 8-kV contact discharge and 15-kV air discharge. Surges were applied between the RJ-45 and the dc EVM outputs, and between an auxiliary power input jack and the dc outputs. No failures were observed.

ESD requirements for a unit that incorporates the TPS2375 have much broader scope and operational implications than those used in TI's testing. Unit level requirements should not be confused with EVM testing that only validated the TPS2375.

EXTERNAL COMPONENTS

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer per IEEE 802.3 requirements, see Figure 1. For powered devices, the isolation transformer must include a center tap on the media (cable) side. Proper termination is required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. Transformers must be specifically rated to work with the Ethernet chipset, and the IEEE 802.3af standard.

Input Diodes or Diode Bridges

The IEEE 802.3af requires the PD to accept power on either set of input pairs in either polarity. This requirement is satisfied by using two full-wave input bridge rectifiers as shown in Figure 1. Silicon p-n diodes with a 1-A or 1.5-A rating and a minimum breakdown of 100 V are recommended. Diodes exhibit large dynamic resistance under low-current operating conditions such as in detection. The diodes should be tested for their behavior under this condition. The diode forward drops must be less than 1.5 V at 500 µA and at the lowest operating temperature.

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Input Capacitor

The IEEE 802.3af requires a PD input capacitance between 0.05 µF and 0.12 µF during detection. This capacitor should be located directly adjacent to the TPS2375 as shown in Figure 1. A 100-V, 10%, X7R ceramic capacitor meets the specification over a wide temperature range.

Load Capacitor

The IEEE 802.3af specification requires that the PD maintain a minimum load capacitance of 5 µF. It is permissible to have a much larger load capacitor, and the TPS2375 can charge in excess of 470 µF before thermal issues become a problem. However, if the load capacitor is too large, the PD design may violate IEEE 802.3af requirements.

If the load capacitor is too large, there can be a problem with inadvertent power shutdown by the PSE caused by failure to meet the MPS. This is caused by having a long input current dropout due to a drop in input voltage with a large capacitance-to-load ratio. The standard gives Equation 2:

$$C \leq \frac{I_{(PD)} \times 180}{10\ mA} \quad (2)$$

where C is the bulk capacitance in µF and $I_{(PD)}$ is the PD load current in mA.

A particular design may have a tendency to cause ringing at the RTN pin during startup, inadvertent hot-plugs of the PoE input, or plugging in a wall adapter. It is recommended that a minimum value of 1 µF be used at the output of the TPS2375 if downstream filtering prevents placing the larger bulk capacitor right on the output. When using ORing option 2, it is recommended that a large capacitor such as a 22 µF be placed across the TPS2375 output.

Transient Suppressor

Voltage transients on the TPS2375 can be caused by connecting or disconnecting the PD, or by other environmental conditions like ESD. The TPS2375 is specified to operate with absolute maximum voltages $V_{(VDD-VSS)}$ and $V_{(RTN-VSS)}$ of 100 V. A transient voltage suppressor, such as the SMAJ58A, should be installed after the bridge and across the TPS2375 input as shown in Figure 1. Various configurations of output filters and the insertion of local power sources across either the TPS2375 input or output have the potential to cause stresses outside the absolute maximum ratings of the device. Designers should be aware of this possibility and account for it in their circuit designs. For example, use adequate capacitance across the output to limit the magnitude of voltage ringing caused by downstream filters. Plugging an external power source across the output may cause ESD-like events. Some form of protection should be considered based on a study of the specific waveforms seen in an application circuit.

Layout

The layout of the PoE front end must use good practices for power and EMI/ESD. A basic set of recommendations include:

1. The parts placement must be driven by the power flow in a point-to-point manner such as RJ-45 → Ethernet transformer → diode bridges → TVS and 0.1-µF capacitor → TPS2375 → output capacitor.
2. There should not be any crossovers of signals from one part of the flow to another.
3. All leads should be as short as possible with wide power traces and paired signal and return.
4. Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
5. The TPS2375 should be over a local ground plane or fill area referenced to VSS to aid high-speed operation.
6. Large SMT component pads should be used on power dissipating devices such as the diodes and the TPS2375.

Use of added copper on local power and ground to help the PCB spread and dissipate the heat is recommended. Pin 4 of the TPS2375 has the lowest thermal resistance to the die.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2375D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2375DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2375DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2375DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2375PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2375PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2375PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2375	Samples
TPS2376D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2376DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2376DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2376PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2376PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2376PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2376PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376	Samples
TPS2377D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2377	Samples
TPS2377DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2377	Samples
TPS2377DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2377	Samples
TPS2377PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2377	Samples
TPS2377PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2377	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

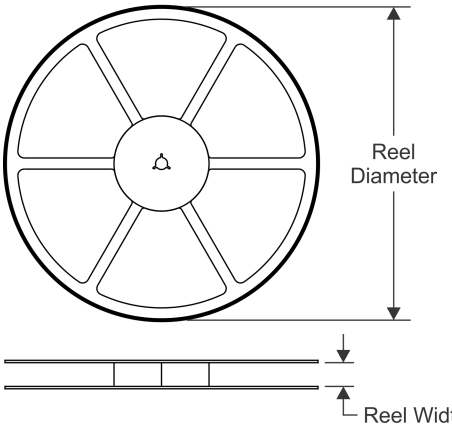
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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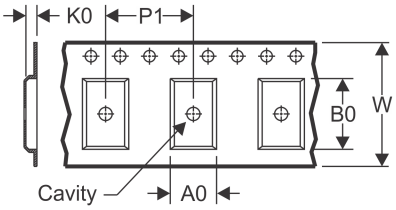
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

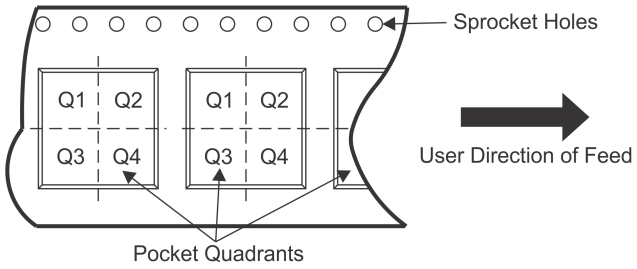


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

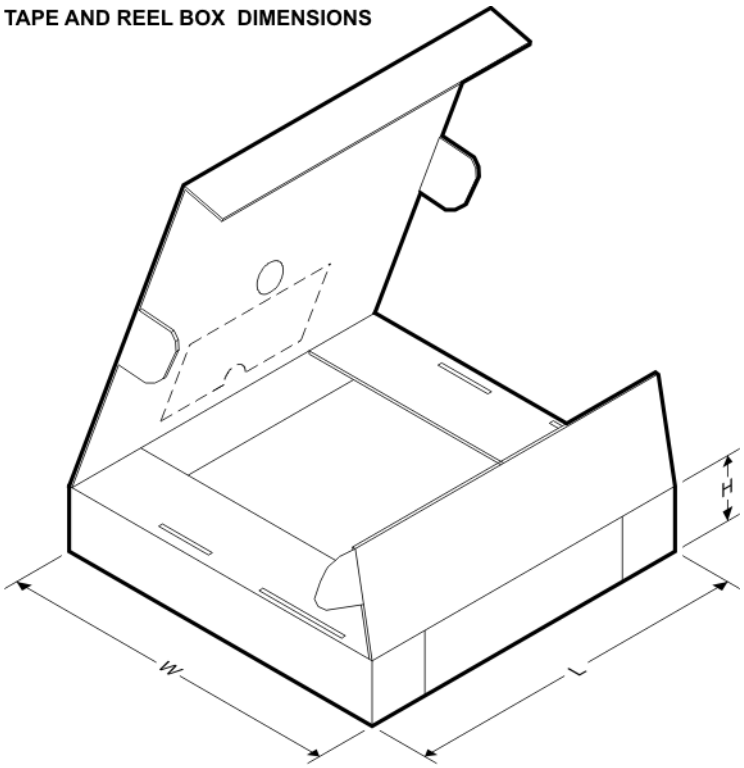
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2375DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2375PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2376DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2376PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2377DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2377PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

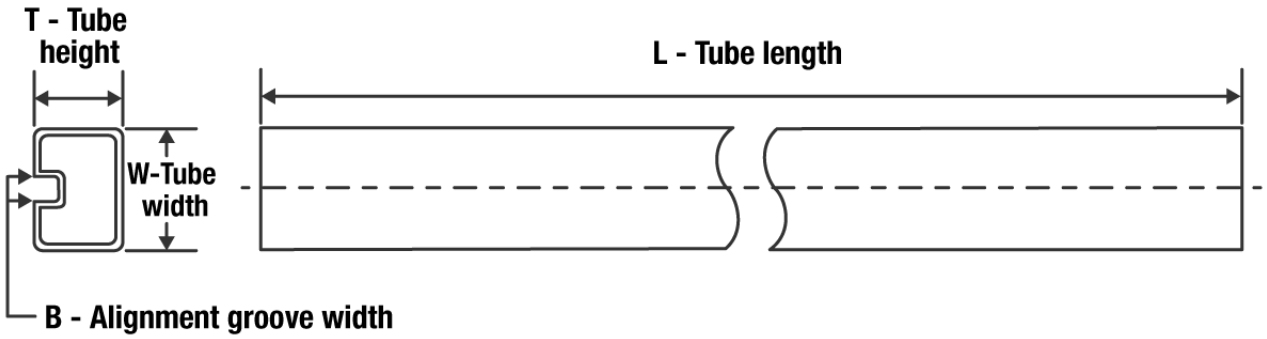
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

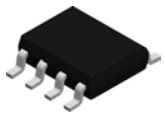
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2375DR	SOIC	D	8	2500	340.5	336.1	25.0
TPS2375PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TPS2376DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS2376PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TPS2377DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS2377PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2375D	D	SOIC	8	75	507	8	3940	4.32
TPS2375DG4	D	SOIC	8	75	507	8	3940	4.32
TPS2375PW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2376D	D	SOIC	8	75	505.46	6.76	3810	4
TPS2376DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS2376PW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2376PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2377D	D	SOIC	8	75	505.46	6.76	3810	4
TPS2377PW	PW	TSSOP	8	150	530	10.2	3600	3.5

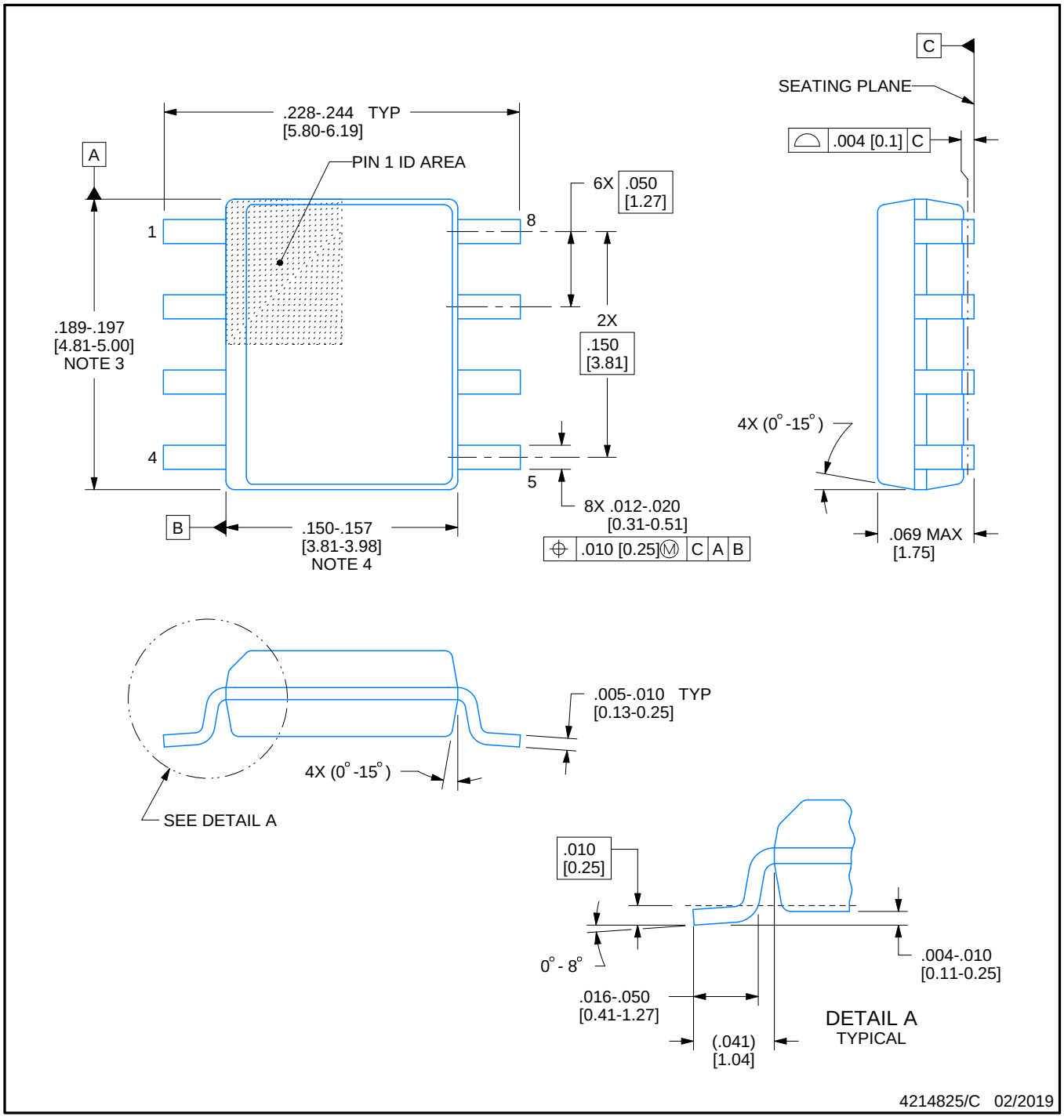


PACKAGE OUTLINE

D0008A

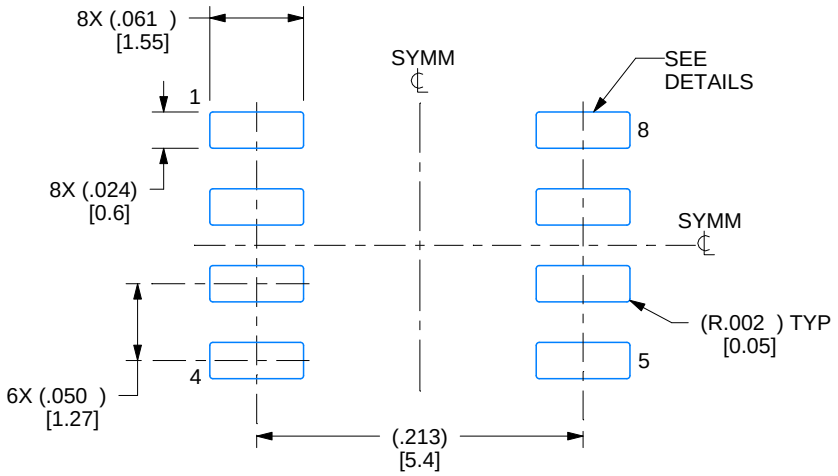
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

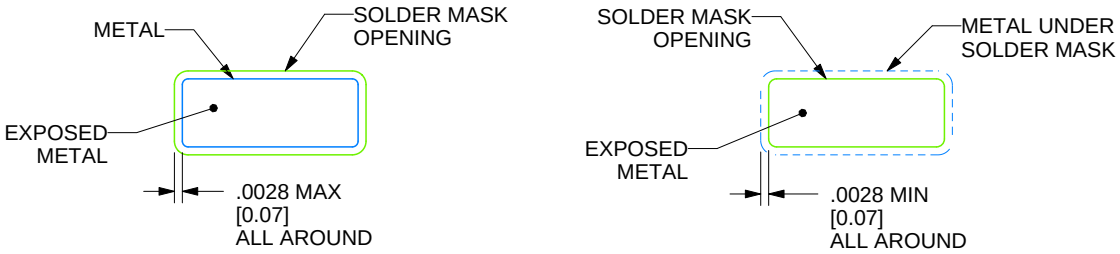


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

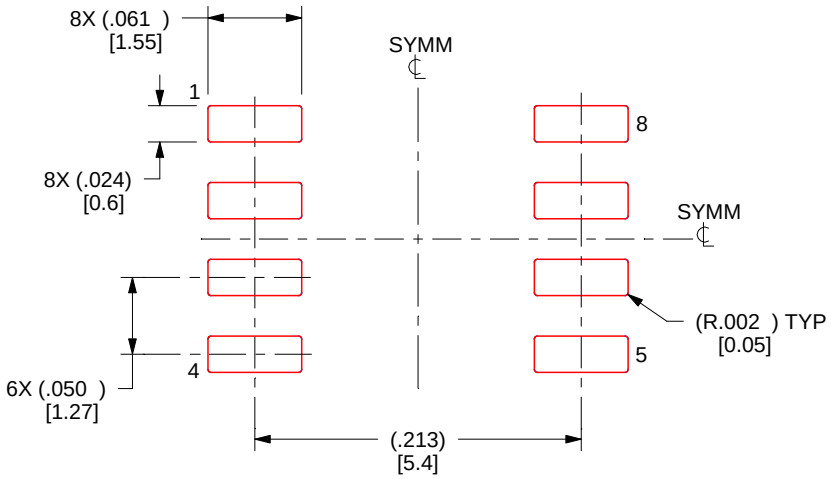
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

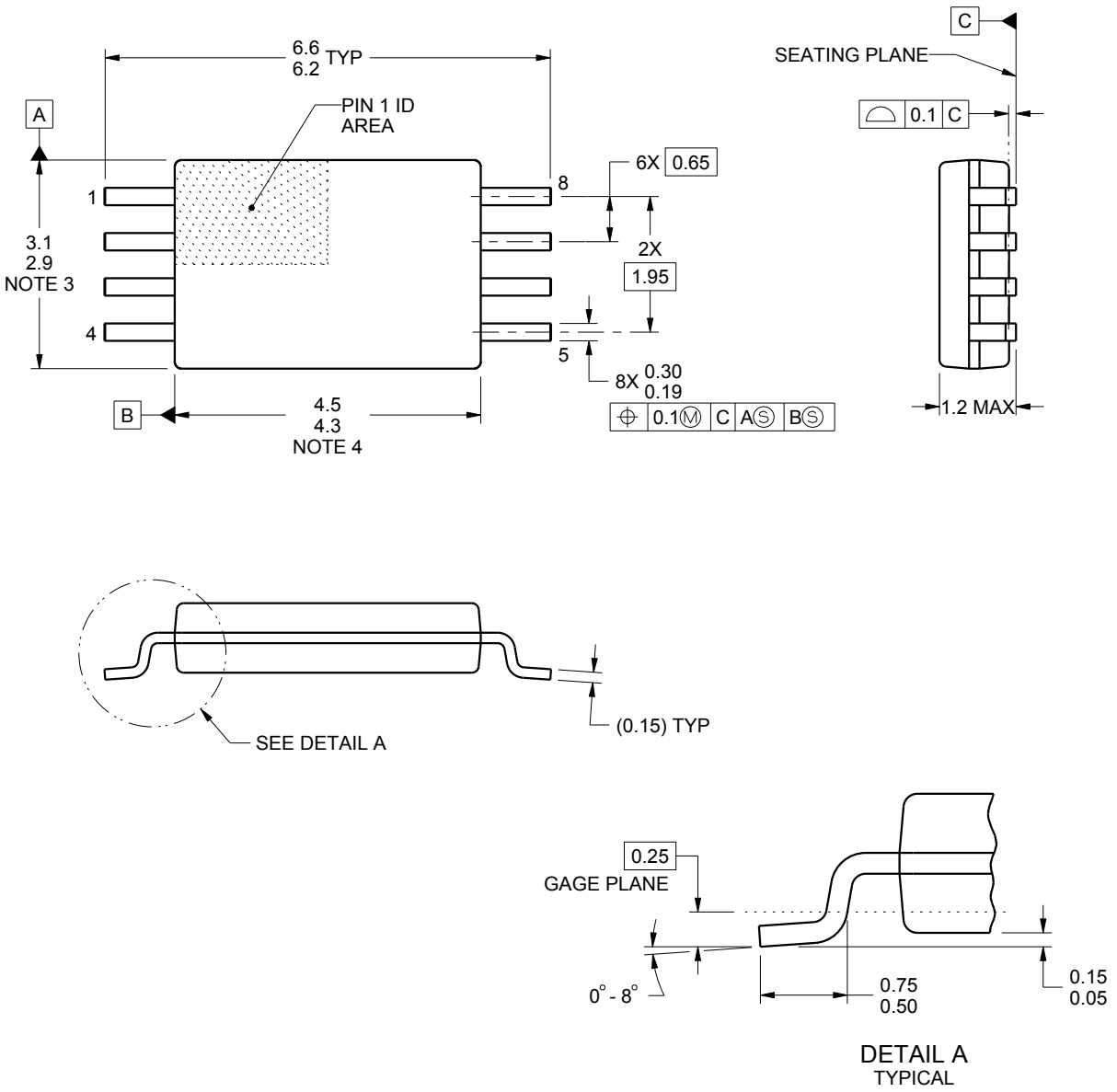
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

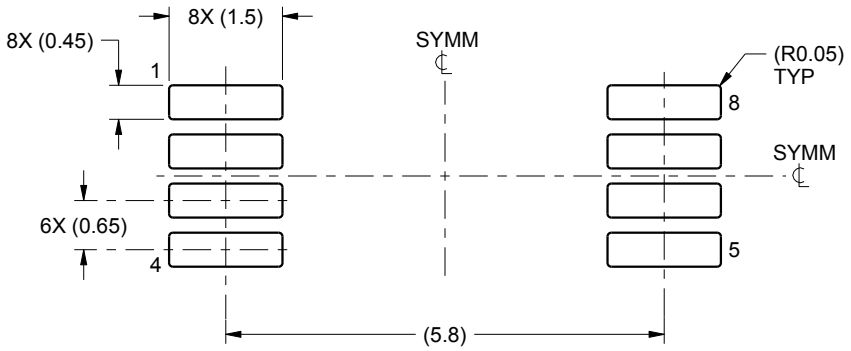
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

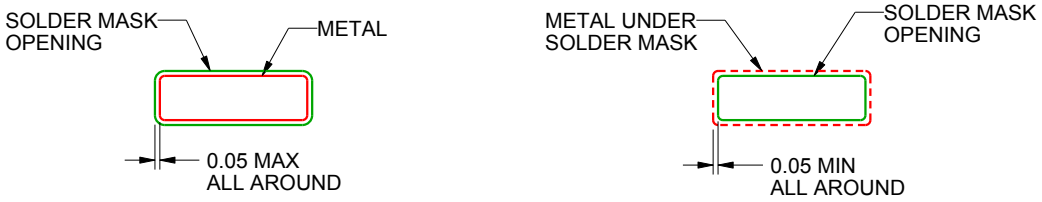


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

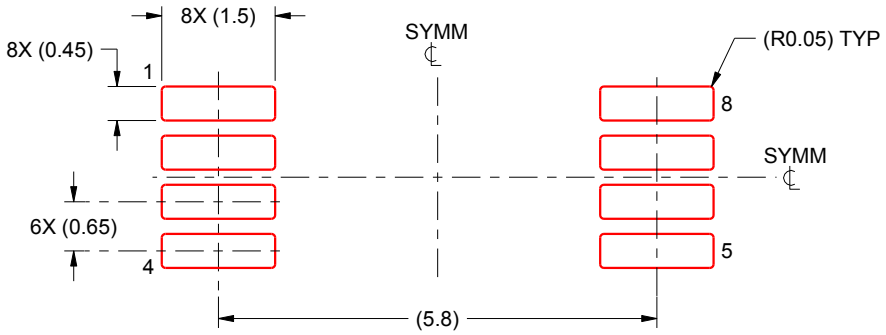


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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