

TPS2663x 60V 6A 功率限制浪涌保护工业电子保险丝

1 特性

- 工作电压为 4.5V 至 60V，绝对最大值为 67V
- 集成式 60V、31mΩ R_{ON} 热插拔 FET
- 通过外部 N 沟道 FET 提供反极性保护和反向电流阻断支持
- 可调电流限制为 0.6A 至 6A ($\pm 7\%$)
- 浪涌期间具有电气快速瞬变 (IEC61000-4-4) 抗扰性和负载保护 (IEC 61000-4-5) 并提供 A 类系统性能
- 快速反向电流阻断 (0.17μs)
- 具有可调节输出功率限制功能 ($\pm 6\%$) 的型号
- 可调节 UVLO、OVP 切断、输出压摆率控制，用于浪涌电流限制
- 通过在器件加电期间进行热调节，为大型及未知容性负载充电
- 具有最大 35V 和 39V 过压钳位的型号
- 电源正常输出 (PGOOD)
- 可选过流故障响应选项 (自动重试和闭锁模式)
- 具有 2x 脉冲过流支持的型号
- 模拟电流监控器 (IMON) 输出 ($\pm 6\%$)
- UL 2367 认证正在申请中

2 应用

- 工厂自动化和控制 – PLC、DCS、HMI、I/O 模块、传感器集线器
- 电机驱动器 – CNC、编码器电源
- 电子断路器

3 说明

TPS2663x 器件是易于使用的正极 60V 和 6A 电子保险丝，其中包含一个 31mΩ 的集成式 FET。该器件具有一个 B-FET 驱动器，用于在需要输入反极性故障和反向电流阻断保护的系统中控制外部 N 沟道 FET。该器件具有强大的保护功能，可简化在 IEC61000-4-5 工业浪涌测试等系统测试期间需要保护的系统设计。此器件具有可调节输出功率限制 (PLIM) 功能，从而简化需要符合 IEC61010-1 和 UL1310 等标准的系统设计。其他保护功能包括可调节过流保护、快速短路保护、输出压摆率控制、过压保护和欠压锁定。

为实现系统状态监视和下游负载控制，该器件提供了故障和精确的电流监视器输出。可以使用 PGOOD 来启用和禁用下游直流/直流转换器控制。MODE 引脚可用于在两种限流故障响应（闭锁和自动重试）之间灵活地对器件进行配置。

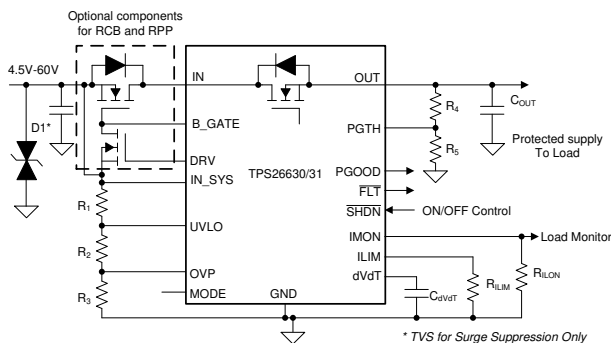
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS26630 TPS26631 TPS26632 TPS26633 TPS26635	VQFN (24)	4.00mm x 4.00mm
TPS26631 TPS26633 TPS26636	HTSSOP (20)*	6.50mm x 4.40mm

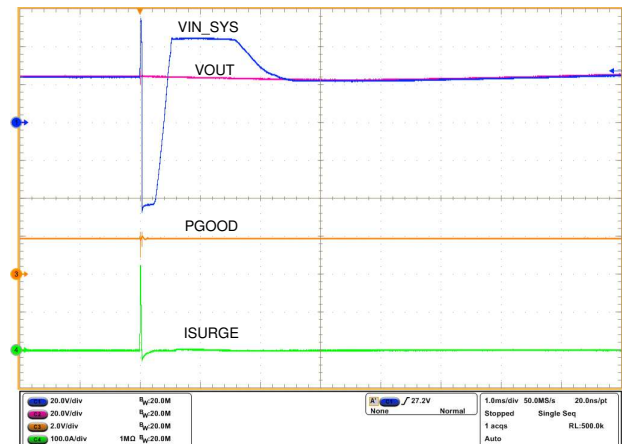
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) * 预览

简化原理图



24V 电源下的 IEC61000-4-5 浪涌性能



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4 修订历史记录

Changes from Revision C (March 2019) to Revision D	Page
• 将器件信息 表中的 TPS26632 器件替换为 TPS26636 器件	1
• Added the TPS26636 device to the Pin Configuration and Functions table	3
• Added the TPS26636 device to the Pin Functions table	4
• Updated the Input Voltage in the Specifications Absolute Maximum Ratings table	6
• Updated the PLIM Input and Output Ramp Control in the Specifications Electrical Characteristics table	6

Changes from Revision B (January 2019) to Revision C	Page
• 已更改 将“预告信息”更改为“生产数据”	1

Changes from Revision A (December 2018) to Revision B	Page
• Updated the Pin Configuration and Functions section	3
• Updated Layout Example	41

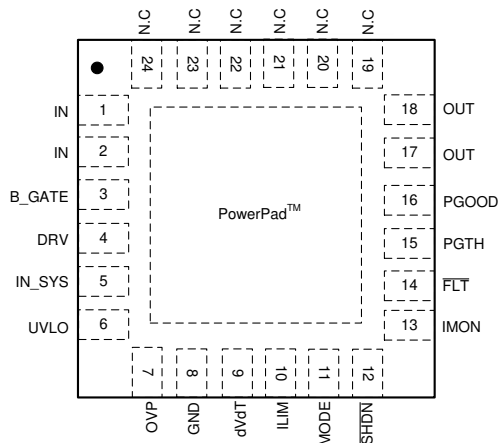
Changes from Original (September 2018) to Revision A	Page
• Updated the Pin Configuration and Functions section	3
• Updated Functional Block Diagram	17
• Updated Layout Example	41

5 Device Comparison Table

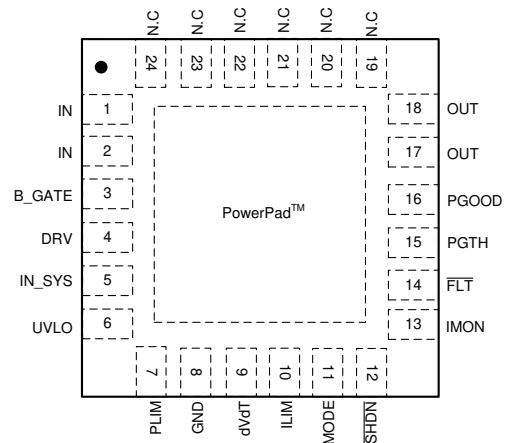
PART NUMBER	OVERVOLTAGE PROTECTION	OVERLOAD FAULT RESPONSE	ADJUSTABLE OUTPUT POWER LIMITING
TPS26630	Overvoltage cut-off, adjustable	Active Current Limiting (1x)	No
TPS26631	Overvoltage cut-off, adjustable	Active Current Limiting with Pulse current support (2x)	No
TPS26632	Overvoltage clamp, fixed (35 V max)	Active Current Limiting (1x)	Yes
TPS26633	Overvoltage clamp, fixed (35 V max)	Active Current Limiting with Pulse current support (2x)	Yes
TPS26635	Overvoltage clamp, fixed (39 V max)	Active Current Limiting with Pulse current support (2x)	Yes
TPS26636	Overvoltage clamp, fixed (35 V max)	Active Current Limiting with Pulse current support (2x)	Yes

6 Pin Configuration and Functions

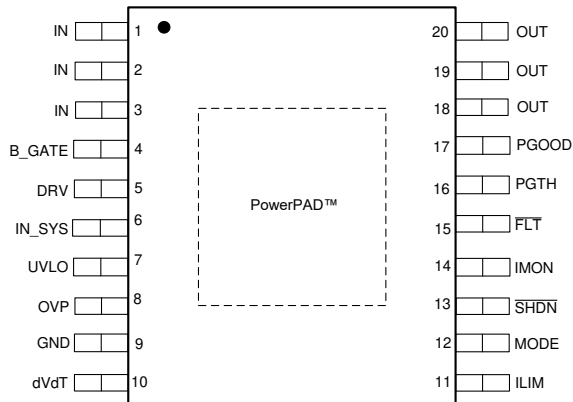
**TPS26630, TPS26631 RGE Package
24-Pin VQFN
Top View**



**TPS26632, TPS26633, TPS26635 RGE Package
24-Pin VQFN
Top View**



**TPS26631 PWP Package
20-Pin HTSSOP
Top View**



**TPS26633, TPS26636 PWP Package
20-Pin HTSSOP
Top View**

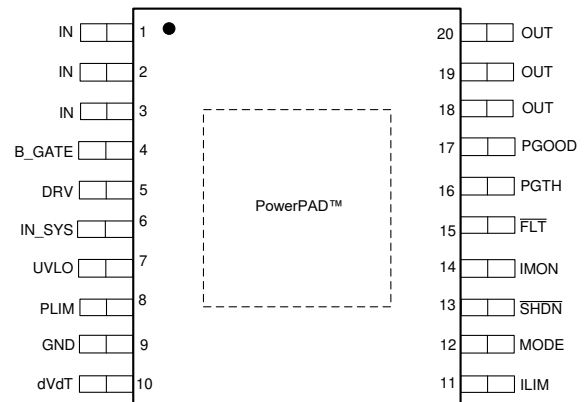


Table 1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS26630, TPS26631, TPS26632, TPS26633, TPS26635, TPS26636			
	VQFN	HTSSOP		
IN	1	1	P	Power input. Connects to the DRAIN of the internal FET
	2	2		
	—	3		
B_GATE	3	4	O	Blocking FET gate driver output. Connect B_GATE to GATE of the external NFET. If external FET is not used then leave B_GATE pin floating. See the Input Reverse Polarity Protection (B_GATE, DRV) section
DRV	4	5	O	Blocking FET fast pull down switch drive. Connect DRV to the GATE of external pull down switch. Leave this pin floating if external N-FET is not used.
IN_SYS	5	6	P	Power input and supply voltage of the device. When an external Blocking FET is used then connect IN_SYS to source of the FET. Short IN_SYS to IN in case blocking FET is not used
UVLO	6	7	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns off the internal FET and asserts FLT to indicate the power-failure. Connect UVLO pin to GND pin to select the internal default threshold
OVP	7	8	I	Input for setting the programmable overvoltage protection threshold (For TPS26630 and TPS26631 Only). An overvoltage event turns off the internal FET and asserts FLT to indicate the overvoltage fault. Connect OVP pin to GND pin externally to select the internal default threshold.
PLIM	7	8	I	Input for setting the programmable output power limiting threshold (For TPS26632, TPS26633, TPS26635 and TPS26636 Only). Connect a resistor across PLIM to GND to set the output power limit. Connect PLIM to GND if PLIM feature is not used. See the Output Power Limiting, PLIM (TPS26632, TPS26633, TPS26635 and TPS26636 Only) section
GND	8	9	—	Connect GND to system ground
dVdT	9	10	I/O	A capacitor from this pin to GND sets output voltage slew rate. See the Hot Plug-In and In-Rush Current Control section
ILIM	10	11	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit. See the Overload and Short Circuit Protection section
MODE	11	12	I	Mode selection pin for overload fault response. See the Device Functional Modes section
$\overline{\text{SHDN}}$	12	13	I	Shutdown pin. Pulling $\overline{\text{SHDN}}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{\text{SHDN}}$ pin voltage resets the device that has latched off due to a fault condition
IMON	13	14	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage. If unused, leave it floating
$\overline{\text{FLT}}$	14	15	O	Fault event indicator. It is an open drain output. If unused, leave floating or connect to GND
PGTH	15	16	I	PGOOD comparator input.
PGOOD	16	17	O	Active High. A high indicates PGTH has crossed the $V_{(\text{PGTHR})}$ threshold and the internal FET is enhanced. PGOOD goes low when $V_{(\text{PGTH})}$ hits $V_{(\text{PGTHF})}$ threshold. If PGOOD is unused then connect to GND or leave it floating
OUT	17	18	P	Power output of the device
	18	19		
	—	20		
N. C	19	—	—	No Connect
	20			
	21			
	22			
	23			
	24			

Table 1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS26630, TPS26631, TPS26632, TPS26633, TPS26635, TPS26636			
	VQFN	HTSSOP		
PowerPad™	—	—	—	Connect PowerPad to GND plane for heat sinking. Do not use PowerPad as the only electrical connection to GND

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
IN_SYS	Input Voltage	–60	67	V
IN_SYS (10ms transient), T _A = 25 °C		–60	75	V
IN, OUT, UVLO, $\overline{\text{FLT}}$, PGOOD, PGTH		–0.3	67	V
IN_SYS – OUT (10ms transient), with a Blocking FET		–85		V
IN (10ms transient), T _A = 25 °C		–0.3	75	V
BGATE		–60	81	V
BGATE – IN_SYS		–0.3	14	V
DRV		–60	72	V
DRV – IN_SYS		–0.3	20	V
OVP, dVdT, IMON, MODE, $\overline{\text{SHDN}}$, ILIM, PLIM		–0.3	5.5	V
$\overline{\text{FLT}}$, I _{dVdT} , I _{PGOOD}	Sink current		10	mA
I _{dVdT} , I _{ILIM} , I _{PLIM} , I _{MODE} , I $\overline{\text{SHDN}}$	Source current	Internally limited		
T _J	Operating Junction temperature	–40	150	°C
	Transient junction temperature	–65	T _(TSD)	
T _{stg}	Storage temperature	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN_SYS, IN	Input Voltage	4.5		60	V
OUT, UVLO, PGTH, PGOOD, $\overline{\text{FLT}}$		0		60	
OVP, dVdT, IMON, MODE		0		4	
$\overline{\text{SHDN}}$		0		5	
ILIM	Resistance	3		30	kΩ
IMON	Resistance	1			
PLIM	Resistance	60.4		150	
IN, IN_SYS, OUT	External Capacitance	0.1			μF
dVdT		10			nF
T _J	Operating Junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS2663		UNIT
		RGE (VSON)	PWP (HTSSOP)	
		24 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	31.4	32.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	23.2	23.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	10.2	10	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	10.2	9.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.8	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < V_(IN_SYS) = V_(IN) < 60 V, V_(SHDN) = 2 V, R_(ILIM) = 30 kΩ, IMON = PGOOD = FLT = OPEN, C_(OUT) = 1 μF, C_(dVdT) = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _(IN_SYS)	Operating input voltage		4.5		60	V
I _{Q(ON)}	Supply current	Enabled: V _(SHDN) = 2 V		1.38	1.7	mA
I _{Q(OFF)}		V _(SHDN) = 0 V		21	60	μA
I _(GND)	Ground current during reverse polarity	V _(IN_SYS) = −24V, V _(IN) = Floating, V _(OUT) = 0 V		144	200	μA
V _(OVC)	Over voltage clamp	TPS26632, TPS26633, TPS26636 Only, V _(IN_SYS) > 35 V, I _(OUT) = 1 mA	32	32.8	35	V
		TPS26635 Only, V _(IN_SYS) > 40 V, I _(OUT) = 1 mA	35.7	36.6	39	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
V _(INSYS_UVLO)	Factory set V _(IN_SYS) undervoltage trip level trip level	V _(IN_SYS) rising, V _(UVLO) = 0 V	15.1	15.46	15.9	V
		V _(IN_SYS) falling, V _(UVLO) = 0 V	14	14.47	15.1	V
V _(SEL_UVLO)	Internal UVLO select threshold		180	210	240	mV
V _(UVLOR)	UVLO threshold voltage, rising		1.176	1.2	1.224	V
V _(UVLOF)	UVLO threshold voltage, falling		1.09	1.122	1.15	V
I _(UVLO)	UVLO Input leakage current	0 V ≤ V _(UVLO) ≤ 60 V	−150	8	150	nA
OVERVOLTAGE PROTECTION (OVP) INPUT						
V _(IN_SYS_OVP)	Factory set V _(IN_SYS) overvoltage trip level trip level	V _(IN_SYS) rising, V _(OVP) = 0 V	33.2	34.33	35.4	V
		V _(IN_SYS) falling, V _(OVP) = 0 V	32.7	33.89	35	V
V _(SEL_OVP)	Internal OVP select threshold		180	210	240	mV
V _(OVPR)	over-voltage threshold voltage, rising		1.176	1.2	1.224	V
V _(OVPF)	over-voltage threshold voltage, falling		1.09	1.122	1.15	V
I _(OVP)	OVP Input leakage current	0 V ≤ V _(OVP) ≤ 4 V	−150	0	150	nA
CURRENT LIMIT PROGRAMMING (ILIM)						
I _(OL)	Over Load current limit	R _(ILIM) = 30 kΩ, V _(IN) − V _(OUT) = 1 V	0.54	0.6	0.66	A
		R _(ILIM) = 9 kΩ, V _(IN) − V _(OUT) = 1 V	1.84	2	2.16	A
		R _(ILIM) = 4.02 kΩ, V _(IN) − V _(OUT) = 1 V	4.185	4.5	4.815	A
		R _(ILIM) = 3 kΩ, V _(IN) − V _(OUT) = 1 V	5.58	6	6.42	A
I _(OL_Pulse)	Transient Pulse Over current limit	3 kΩ < R _(ILIM) < 30 kΩ, TPS26631, TPS26633, TPS26635 and TPS26636 Only	2xI _(OL)			A
I _(FASTRIP)	Fast-trip comparator threshold	TPS26630 and TPS26632 Only	2xI _(OL)			A
I _(FASTRIP)	Fast-trip comparator threshold	TPS26631, TPS26633, TPS26635 and TPS26636 Only	3xI _(OL)			A

Electrical Characteristics (continued)

$-40^{\circ}\text{C} \leq T_A = T_J \leq +125^{\circ}\text{C}$, $4.5\text{ V} < V_{(\text{IN_SYS})} = V_{(\text{IN})} < 60\text{ V}$, $V_{(\text{SHDN})} = 2\text{ V}$, $R_{(\text{ILIM})} = 30\text{ k}\Omega$, $\text{IMON} = \text{PGOOD} = \overline{\text{FLT}} = \text{OPEN}$, $C_{(\text{OUT})} = 1\text{ }\mu\text{F}$, $C_{(\text{dVdT})} = \text{OPEN}$. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(SCP)	Short Circuit Protect current			45		A
OUTPUT POWER LIMITING CONTROL (PLIM) INPUT – TPS26632, TPS26633, TPS26635 and TPS26636 ONLY						
V(SEL_PLIM)	Power Limit Feature select threshold		160	217	240	mV
I(PLIM)	PLIM sourcing current	V(PLIM) = 0 V	4.4	5.02	5.6	μA
P(PLIM)	Max Output power	R(PLIM) = 100 kΩ	94	100	106	W
		R(PLIM) = 150 kΩ ⁽¹⁾	141.9	151	160.1	W
B_GATE (BLOCKING FET GATE DRIVER)						
V(B_GATE)	B_GATE clamp voltage	V(B_GATE) – V(IN_SYS)	8.3	10.23	14	V
I(B_GATE)	Blocking FET Gate drive current	V(B_GATE) – V(IN_SYS) = 1 V	16	19.4	23	μA
Rpd_BGATE	B_GATE Pull down resistance		800	1010	1200	kΩ
V(DRV_OH)	DRV logic high level	V(DRV) – V(IN_SYS), C(DRV) ≤ 50 pF	3	4.25	5.2	V
PASS FET OUTPUT (OUT)						
R_ON	IN to OUT total ON resistance	0.6 A ≤ I(OUT) ≤ 6 A, T_J = 25°C	26	30.44	34.5	mΩ
R_ON	IN to OUT total ON resistance	0.6 A ≤ I(OUT) ≤ 6 A, T_J = 85°C	33		45	mΩ
R_ON	IN to OUT total ON resistance	0.6 A ≤ I(OUT) ≤ 6 A, –40°C ≤ T_J ≤ +125°C	19	30.44	53	mΩ
I_lkg(OUT)	OUT leakage during input supply brownout	V(IN_SYS) = 0 V, V(OUT) = 24 V, V(IN) = Floating, V(SHDN) = 2V, Sinking	–100			μA
V(REVTH)	V(IN_SYS) – V(OUT) threshold for reverse protection comparator, rising		–20	–15	–9	mV
V(FWDTH)	V(IN_SYS) – V(OUT) threshold for reverse protection comparator, falling		45	57	67	mV
OUTPUT RAMP CONTROL (dVdT)						
I(dVdT)	dVdT charging current	V(dVdT) = 0 V	1.775	2	2.225	μA
GAIN(dVdT)	dVdT to OUT gain	V(OUT) / V(dVdT)	23.5	25	26	V/V
V(dVdTmax)	dVdT maximum capacitor voltage		3.8	4.17	4.75	V
R(dVdT)	dVdT discharging resistance		10	16.6	26.6	Ω
LOW IQ SHUTDOWN (SHDN) INPUT						
V(SHDN)	Open circuit voltage	I(SHDN) = 0.1 μA	2.48	2.7	3.3	V
V(SHUTF)	SHDN threshold voltage for low IQ shutdown, falling		0.8			V
V(SHUTR)	SHDN threshold rising				2	V
I(SHDN)	Leakage current	V(SHDN) = 0 V	–10			μA
CURRENT MONITOR OUTPUT (IMON)						
GAIN(IMON)	Gain factor I(IMON):I(OUT)	0.6 A ≤ I(OUT) ≤ 2 A	25.66	27.9	30.14	μA/A
		2 A ≤ I(OUT) ≤ 6 A	26.22	27.9	29.58	μA/A
FAULT FLAG (FLT): ACTIVE LOW						
R(FLT)	FLT Pull-down resistance		36	70	130	Ω
I(FLT)	FLT Input leakage current	0 V ≤ V(FLT) ≤ 60 V	–150	6	150	nA
POWER GOOD (PGOOD)						
R(PGOOD)	PGOOD Pull-down resistance		36	70	130	Ω
I(PGOOD)	PGOOD Input leakage current	0 V ≤ V(PGOOD) ≤ 60 V	–150		150	nA
POSITIVE INPUT FOR POWER GOOD COMPARATOR (PGTH)						
V(PGTHR)	PGTH threshold voltage, rising		1.176	1.2	1.224	V
V(PGTHF)	PGTH threshold voltage, falling		1.09	1.123	1.15	V
I(PGOOD)	PGTH input leakage current	0 V ≤ V(PGTH) ≤ 60 V	–150		150	nA

(1) Parameter guaranteed by design and characterization, not tested in production

Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < V_(IN_SYS) = V_(IN) < 60 V, V_(SHDN) = 2 V, R_(ILIM) = 30 kΩ, IMON = PGOOD = $\overline{\text{FLT}}$ = OPEN, C_(OUT) = 1 μF, C_(dVdT) = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL PROTECTION						
T _(J_REG)	Thermal regulation set point		136	145	154	°C
T _(TSD)	Thermal shutdown (TSD) threshold, rising			165		°C
T _(TSDhyst)	TSD hysteresis			11		°C
MODE						
MODE_SEL	Mode selection	MODE = Open		Latch		
		MODE = Short to GND		Auto – Retry		

7.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < V_(IN_SYS) = V_(IN) < 60 V, V_(SHDN) = 2 V, R_(ILIM) = 30 kΩ, IMON = PGOOD = $\overline{\text{FLT}}$ = OPEN, C_(OUT) = 1 μF, C_(dVdT) = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT (UVLO)						
UVLO_t _{on(dly)}	UVLO switch turnon delay	UVLO↑ (100 mV above V _(UVLOR)) to V _(OUT) = 100 mV with V _(PGTH) < V _(PGTHF) , C _(dVdT) ≥ 10 nF, [C _(dVdT) in nF]		742 + 49.5 x C _(dVdT)		μs
UVLO_t _{on(fast_dly)}	UVLO switch turnon delay (fast)	UVLO↑ (100 mV above V _(UVLOR)) to FET ON with V _(PGTH) > V _(PGTHF)	70	150	251	μs
UVLO_t _{off(dly)}	UVLO switch turnoff delay	UVLO↓ (20 mV below V _(UVLOF)) to $\overline{\text{FLT}}$ ↓	9	11	16	μs
t _{UVLO_FLT(dly)}	UVLO to fault de-assertion delay	UVLO↑ to $\overline{\text{FLT}}$ ↑ delay	500	617	700	μs
OVER VOLTAGE PROTECTION INPUT (OVP)						
OVP_t _{off(dly)}	OVP switch turnoff delay	OVP↑ (20 mV above V _(OVPR)) to $\overline{\text{FLT}}$ ↓	8.5	11	14	μs
OVP_t _{on(fast_dly)}	OVP switch turnon delay (fast)	OVP↓ (100 mV below V _(OVPR)) to FET ON with V _(PGTH) > V _(PGTHF)	58	129	225	μs
OVP_t _{on(dly)}	OVP switch disable delay	OVP↓ (100 mV below V _(OVPR)) to FET ON with V _(PGTH) < V _(PGTHF) , C _(dVdT) ≥ 10 nF, [C _(dVdT) in nF]		150 + 49.5 x C _(dVdT)		μs
t _{OVC(dly)}	Maximum duration in over voltage clamp operation	TPS26632, TPS26633, TPS26635 and TPS26636 Only		162		ms
OVC_t _{FLT(dly)}	$\overline{\text{FLT}}$ assertion delay in over voltage clamp operation	TPS26632, TPS26633, TPS26635 and TPS26636 Only		617		μs
SHUTDOWN CONTROL INPUT (SHDN)						
t _{SD(dly)}	SHUTDOWN entry delay	SHDN↓ (below V _(SHUTF)) to FET OFF	0.8	1	1.5	μs
CURRENT LIMIT						
t _{FASTTRIP(dly)}	Hot-short response time	I _(OUT) > I _(SCP)		1		μs
	Soft short response	I _(FASTTRIP) < I _(OUT) < I _(SCP)	2.2	3.2	4.5	μs
t _{CL_PLIM(dly)}	Maximum duration in current & (power limiting: TPS26632, TPS26633, TPS26635 and TPS26636 Only)		129	162	202	ms
t _{CB(dly)}	Maximum duration in 2x current limiting	I _(OL) < I _(OUT) ≤ I _(2xOL)	20	25.5	31	ms
t _{CBRetry(dly)}	Retry delay in Pulse over current limiting	MODE = GND, TPS26631, TPS26633, TPS26635 and TPS26636 Only	550	670	800	ms
t _{CL_PLIM_FLT(dly)}	$\overline{\text{FLT}}$ delay in current & (power limiting: TPS26632, TPS26633, TPS26635 and TPS26636 Only)		1.09	1.3	1.6	ms
REVERSE CURRENT BLOCKING (RCB) COMPARATOR						

Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < V_(IN_SYS) = V_(IN) < 60 V, V_(SHDN) = 2 V, R_(ILIM) = 30 kΩ, IMON = PGOOD = $\overline{\text{FLT}}$ = OPEN, C_(OUT) = 1 μF, C_(dVdT) = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t _{RCB(fast_dly)}	Reverse protection comparator detection delay (reverse)	(V _(IN_SYS) – V _(OUT))↓ (1 V overdrive below V _(REVTH)) to V _(DRV) – V _(IN_SYS) = V _(DRV_OH)		0.17	0.37	μs
t _{RCB(dly)}		(V _(IN_SYS) – V _(OUT))↓ (10 mV overdrive below V _(REVTH)) to V _(DRV) – V _(IN_SYS) = V _(DRV_OH)		0.48	3	μs
t _{RCB(flt_dly)}	Fault assertion Delay	(V _(IN_SYS) – V _(OUT))↓ (10 mV overdrive below V _(REVTH)) to $\overline{\text{FLT}}$ ↓	500	617	800	μs
t _{FWD_FLT(dly)}	Reverse protection comparator detection delay (forward)	(V _(IN_SYS) – V _(OUT))↑ (10 mV overdrive above V _(FWDTH)) to V _(BGATE) – V _(IN_SYS) = 5 V, C _(BFET-IN_SYS) = 4.7 nF		0.87		ms
	Fault de-assertion Delay	(V _(IN_SYS) – V _(OUT))↑ (10 mV overdrive above V _(FWDTH)) to $\overline{\text{FLT}}$ ↑	434	605	800	μs
OUTPUT RAMP CONTROL (dVdT)						
t _(FASTCHARGE)	Output ramp time in fast charging	C _(dVdT) = Open, 10% to 90% V _(OUT) , C _(OUT) = 1 μF; V _(IN) = 24V	350	495	700	μs
t _(dVdT)	Output ramp time	C _(dVdT) = 22 nF, 10% to 90% V _(OUT) , V _(IN) = 24V		8.35		ms
POWER GOOD (PGOOD)						
t _{PGOODR}	PGOOD delay (deglitch) time	Rising edge	1.07	1.3	1.6	ms
t _{PGOODF}	PGOOD delay (deglitch) time	Falling edge, PGTH↓ (10mV below V _(PGTHF))	1.3	2.12	4	μs
FAULT FLAG ($\overline{\text{FLT}}$)						
t _{CB_FLT(dly)}	$\overline{\text{FLT}}$ assertion delay in Pulse over current limiting	Delay from I _(OUT) > I _(OL) to $\overline{\text{FLT}}$ ↓. TPS26631, TPS26633, TPS26635 and TPS26636 Only	22	25.5	30	ms
THERMAL PROTECTION						
t _(TSD_retry)	Retry delay in TSD	MODE = GND	500	648	800	ms
t _(Treg_timeout)	Thermal Regulation Timeout		2.3	2.54	2.9	s

7.7 Typical Characteristics

$-40^{\circ}\text{C} \leq T_A = T_J \leq +125^{\circ}\text{C}$, $V_{(\text{IN_SYS})} = V_{(\text{IN})} = 24\text{ V}$, $V_{(\text{SHDN})} = 2\text{ V}$, $R_{(\text{ILIM})} = 30\text{ k}\Omega$, $\text{IMON} = \text{PGOOD} = \overline{\text{FLT}} = \text{OPEN}$, $C_{(\text{OUT})} = 1\text{ }\mu\text{F}$, $C_{(\text{dVdT})} = \text{OPEN}$. (Unless stated otherwise)

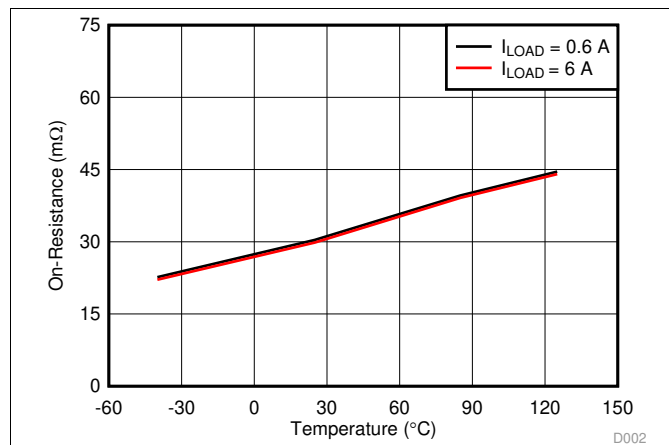


图 1. On-Resistance vs Temperature Across Load Current

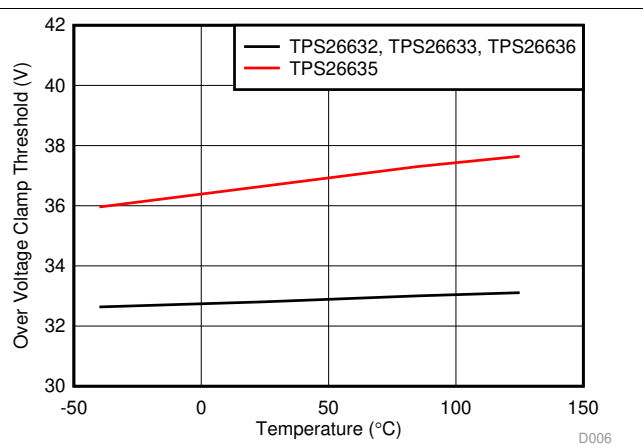


图 2. Overvoltage Clamp Threshold vs Temperature

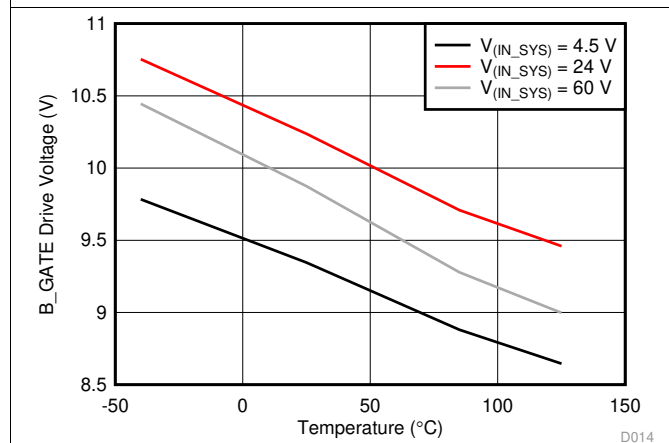


图 3. B_GATE Drive Voltage vs Temperature

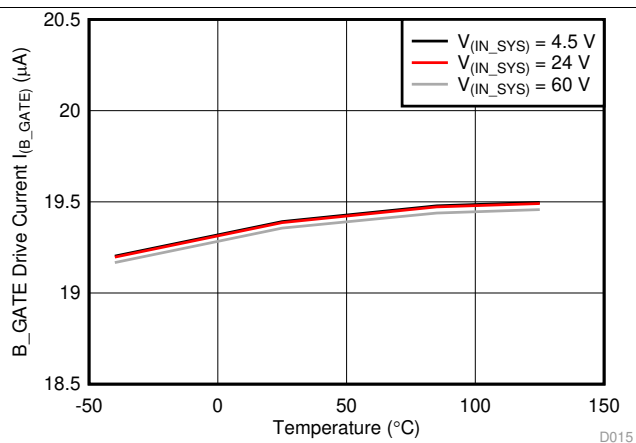


图 4. B_GATE Drive Current vs Temperature

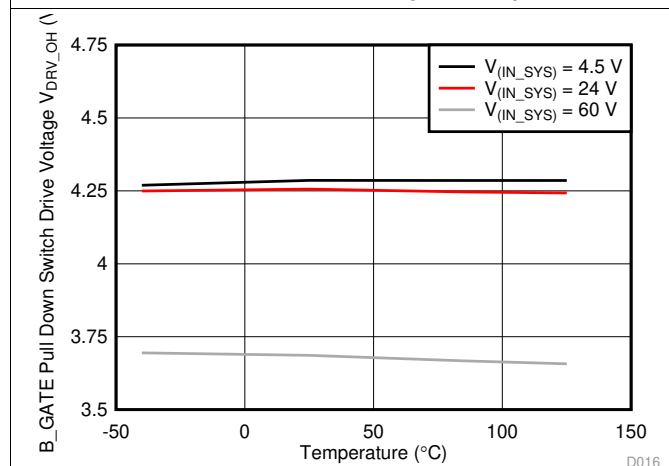


图 5. B_GATE Pull Down Drive Voltage vs Temperature

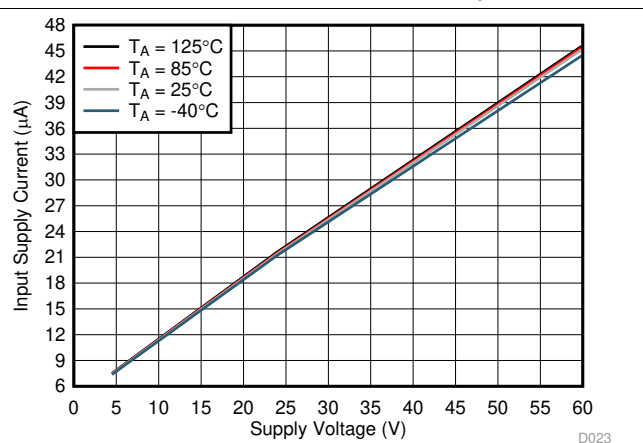


图 6. Input Supply Current vs Supply Voltage in Shutdown

Typical Characteristics (接下页)

$-40^{\circ}\text{C} \leq T_A = T_J \leq +125^{\circ}\text{C}$, $V_{(\text{IN_SYS})} = V_{(\text{IN})} = 24\text{ V}$, $V_{(\text{SHDN})} = 2\text{ V}$, $R_{(\text{ILIM})} = 30\text{ k}\Omega$, $\text{IMON} = \text{PGOOD} = \overline{\text{FLT}} = \text{OPEN}$, $C_{(\text{OUT})} = 1\text{ }\mu\text{F}$, $C_{(\text{dVdT})} = \text{OPEN}$. (Unless stated otherwise)

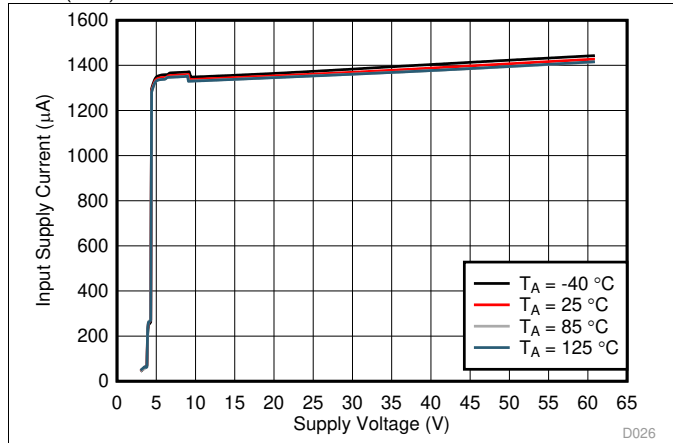
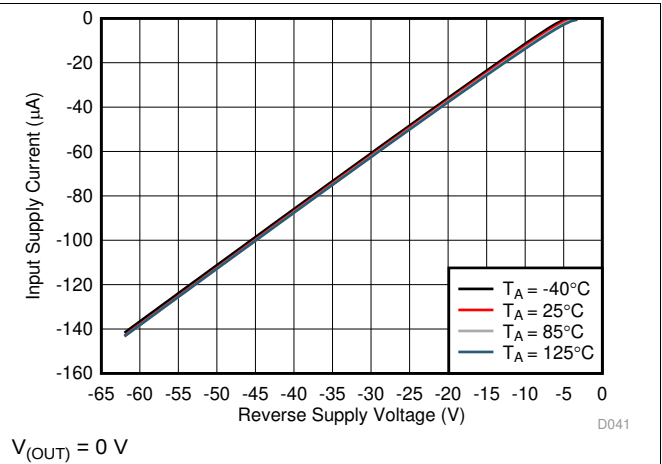


图 7. Input Supply Current vs Supply Voltage During Normal Operation



$V_{(\text{OUT})} = 0\text{ V}$

图 8. Input Supply Current vs Reverse Supply Voltage, $-V_{(\text{IN_SYS})}$

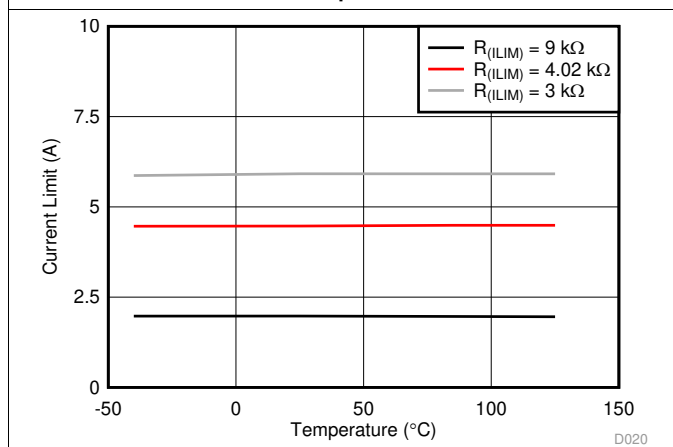


图 9. Overload Current Limit vs Temperature

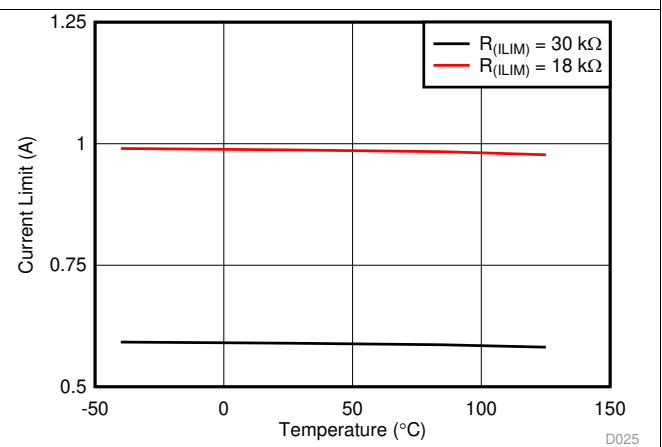


图 10. Overload Current Limit vs Temperature

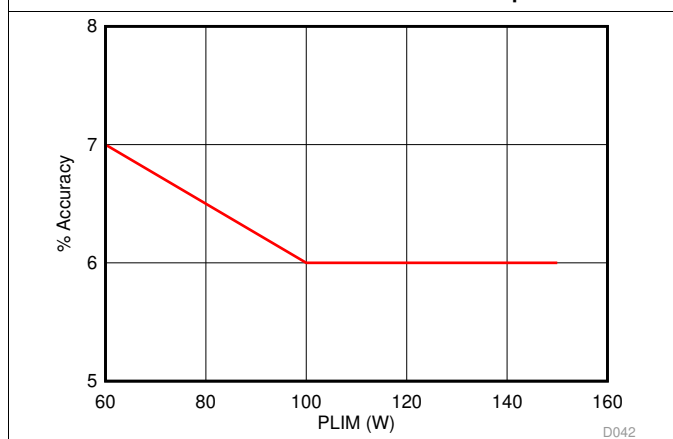


图 11. Output Power Limiting Accuracy vs PLIM

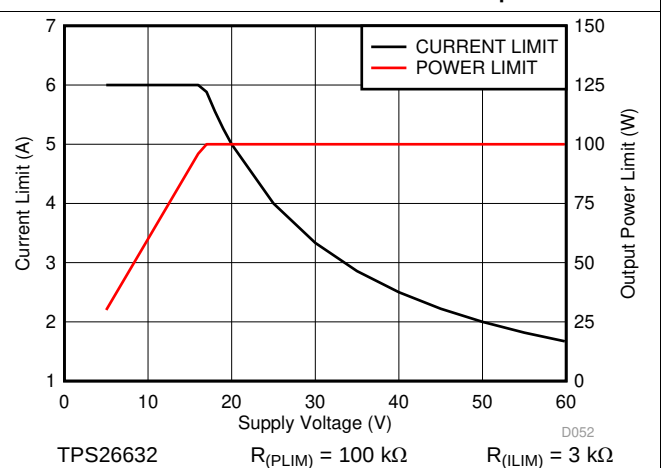


图 12. Power Limit, Current limit vs Supply Voltage

Typical Characteristics (接下页)

$-40^{\circ}\text{C} \leq T_A = T_J \leq +125^{\circ}\text{C}$, $V_{(\text{IN_SYS})} = V_{(\text{IN})} = 24\text{ V}$, $V_{(\text{SHDN})} = 2\text{ V}$, $R_{(\text{ILIM})} = 30\text{ k}\Omega$, $\text{IMON} = \text{PGOOD} = \overline{\text{FLT}} = \text{OPEN}$, $C_{(\text{OUT})} = 1\text{ }\mu\text{F}$, $C_{(\text{dVdT})} = \text{OPEN}$. (Unless stated otherwise)

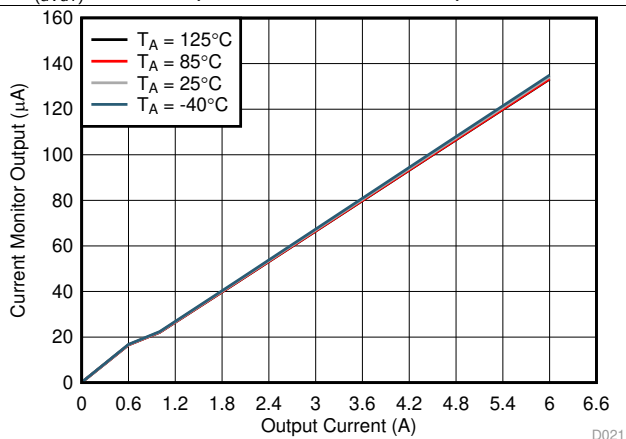


图 13. Current Monitor Output vs Output Current

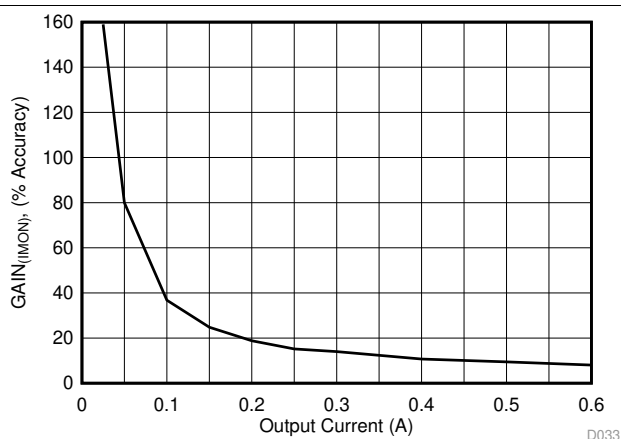


图 14. IMON Gain Accuracy at < 0.6-A Output Current

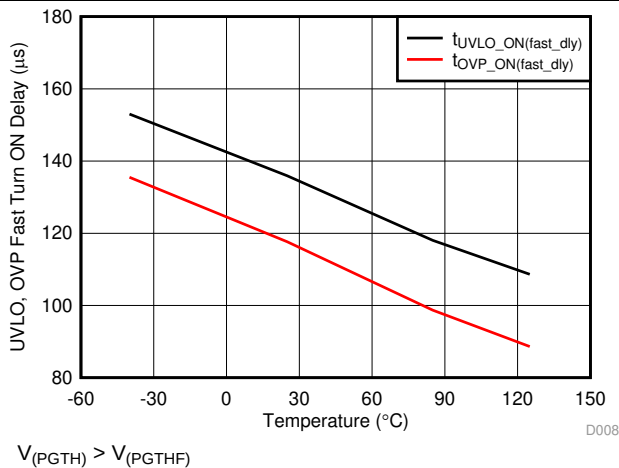


图 15. UVLO, OVP Fast Turn ON Delay vs Temperature

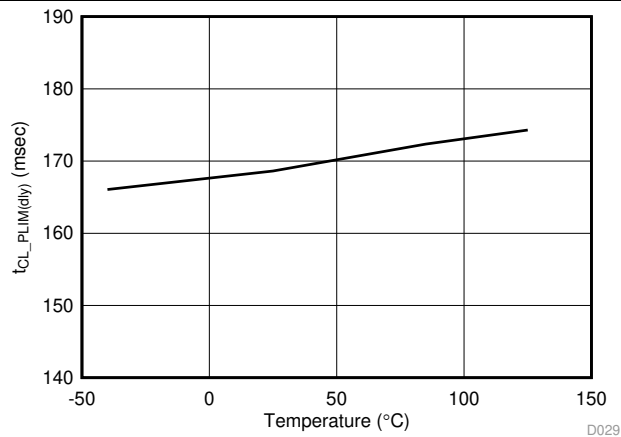


图 16. Maximum Duration in Current and Power Limiting vs Temperature

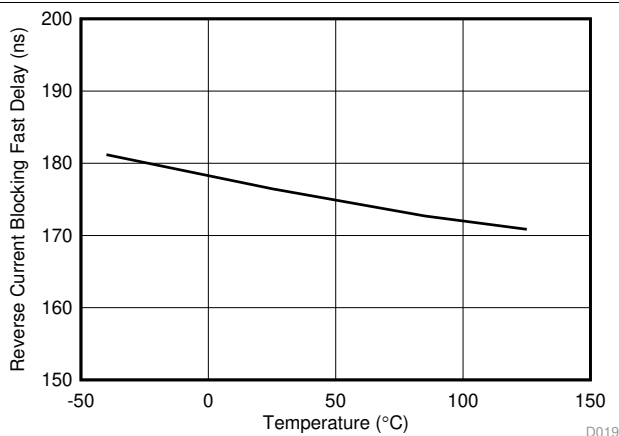


图 17. Reverse Current Blocking Response vs Temperature

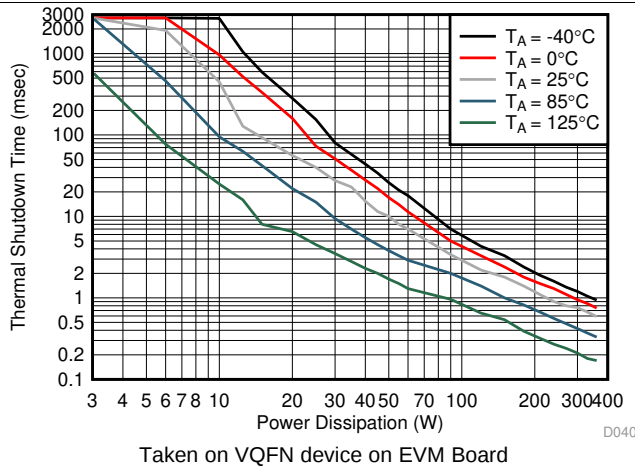


图 18. Thermal Shutdown Time vs Power Dissipation

8 Parameter Measurement Information

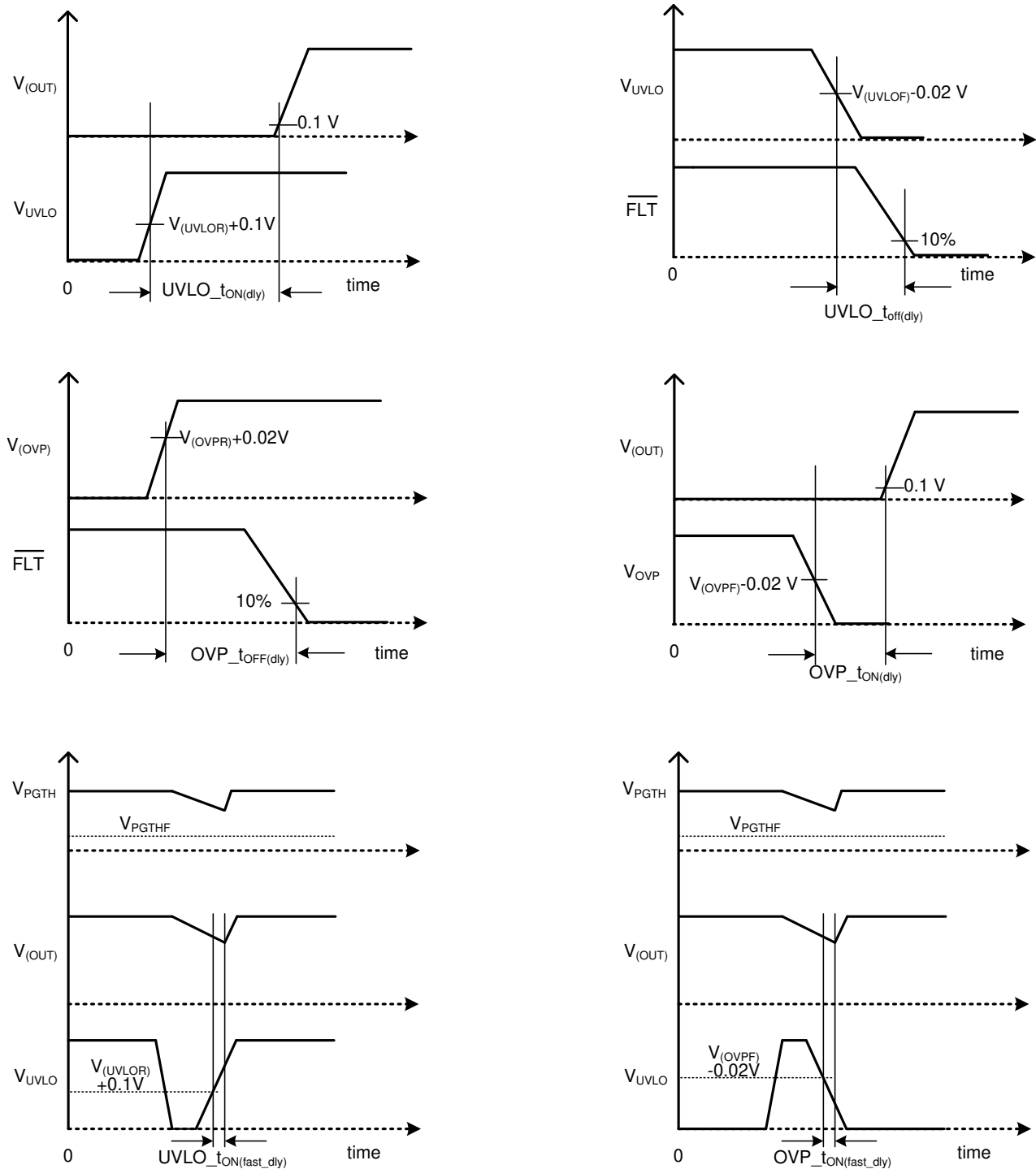


图 19. Timing Waveforms

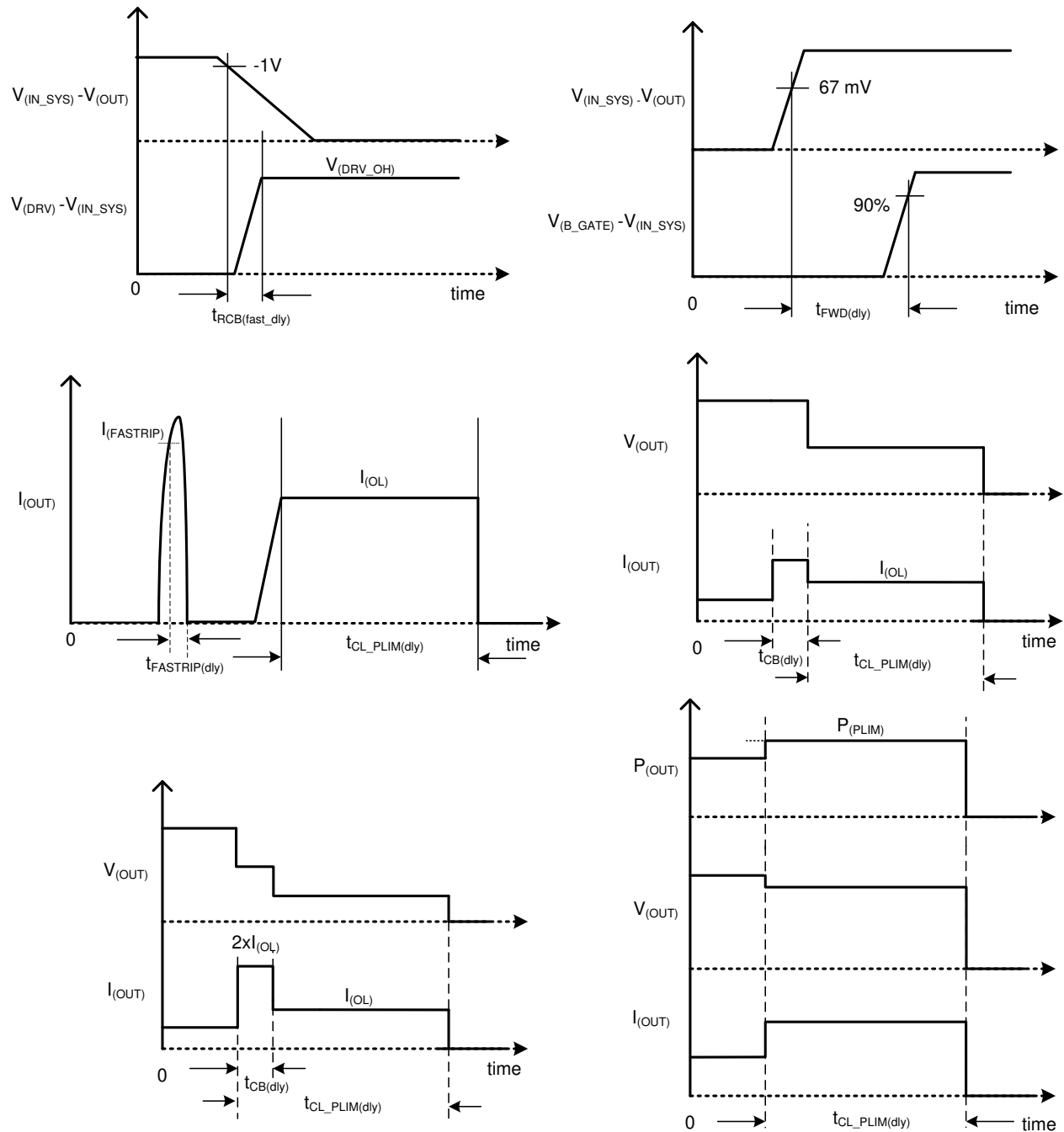


图 20. Timing Waveforms

9 Detailed Description

9.1 Overview

The TPS2663x devices are a family of 60-V industrial eFuses. The devices provides robust protection for all systems and applications powered from 4.5 V to 60 V. With an external N-channel FET the devices can be used to protect the loads from negative supply voltages down to –60 V. For hot-pluggable boards, the devices provides hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage and undervoltage. The precision overcurrent limit ($\pm 7\%$ at 6 A) helps to minimize over design of the input power supply, while the fast response short circuit protection 1- μ s (typical) immediately isolates the faulty load from the input supply when a short circuit is detected. The device features fast reverse current blocking response (0.17 μ s). The internal robust protection control blocks of the TPS2663x along with its ± 60 -V rating, helps to simplify the system designs for the industrial surge compliance ensuring complete protection of the load and the device. The 60-V maximum DC operating and 70-V absolute maximum voltage rating enables system protection from 60-V DC input supply faults and from industrial SELV power supplies.

By monitoring the output (Load) voltage through the PGTH pin, the device distinguishes between real system faults and system transients and the turn ON delay during a fault recovery is controlled accordingly. The valid load voltage detection threshold can be adjusted using a resistor ladder network from OUT, PGTH and GND. This scheme ensures fast recovery during system tests like voltage interruption and brown-out tests, EMC testing like Electrical Fast Transients (IEC61000-4-4) and Surge (IEC61000-4-5).

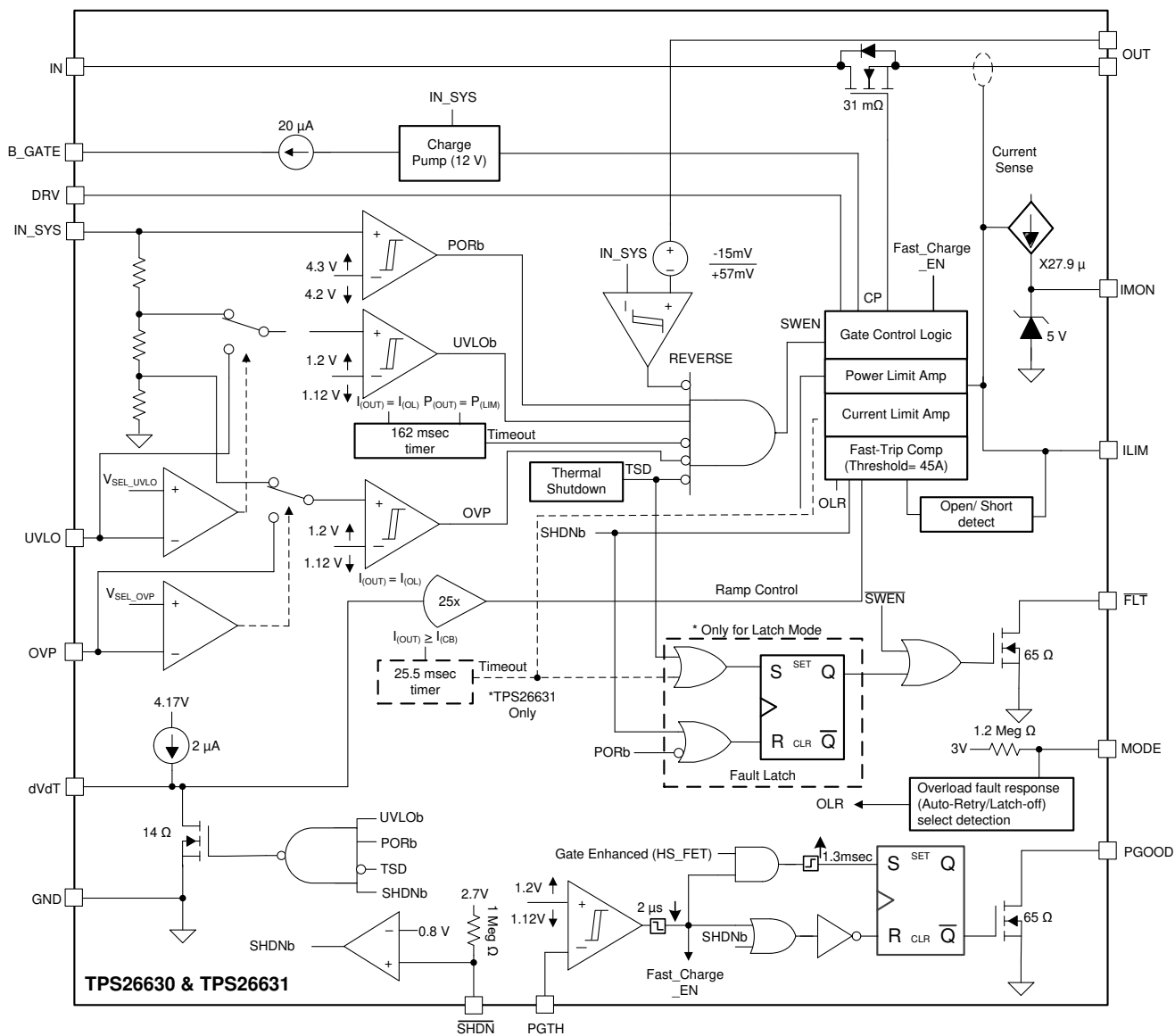
The TPS26632, TPS26633, TPS26635 and TPS26636 devices integrate adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to standards like IEC61010-1 and UL1310.

The devices provides precise monitoring of voltage bus for brown-out, overvoltage conditions and asserts fault signal for the downstream system. Its overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip. The devices monitors $V_{(IN_SYS)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

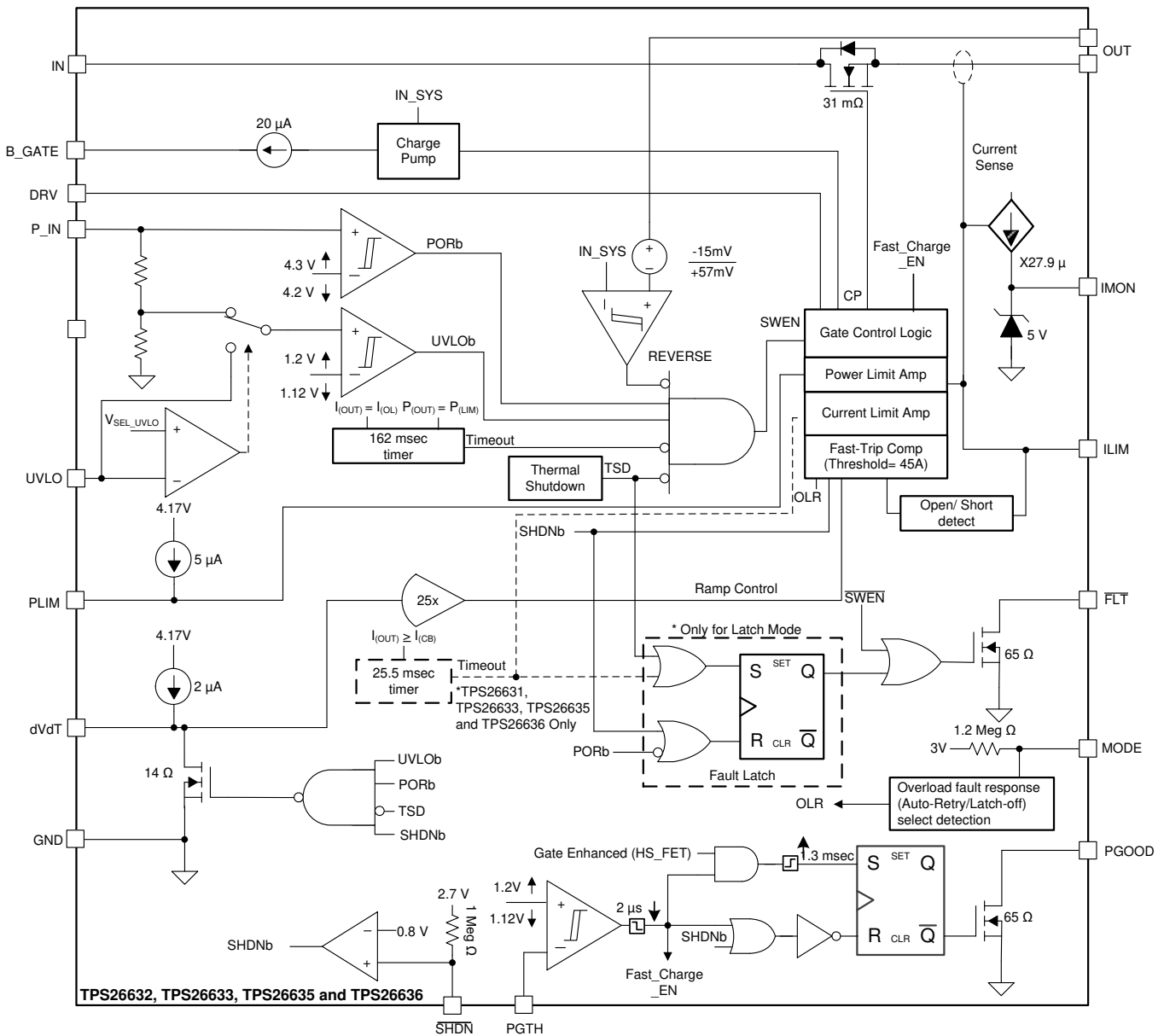
Additional features of the TPS2663x devices include:

- $\pm 6\%$ Current monitor output (IMON) for health monitoring of the system
- A choice of latch off or automatic restart mode response during current limit, power Limit and thermal fault using MODE pin
- PGOOD indicator output with $\pm 2\%$ accurate adjustable valid load voltage detection threshold (PGTH)
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for supply brown-out and overvoltage faults
- Enable and disable control from an MCU using $\overline{\text{SHDN}}$ pin

9.2 Functional Block Diagram



Functional Block Diagram (接下页)



9.3 Feature Description

9.3.1 Hot Plug-In and In-Rush Current Control

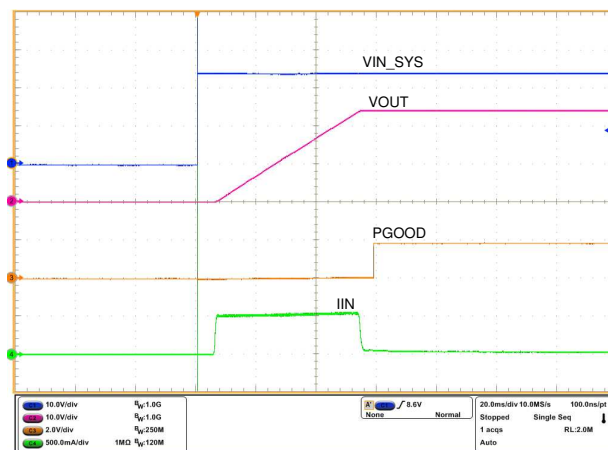
The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24V/500 μs can be achieved by leaving dVdT pin floating. The inrush current can be calculated using 公式 1.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (1)$$

where

$$t_{dVdT} = 20.8 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

图 21 illustrates in-rush current control performance of the device during Hot Plug-In.



$$C_{dVdT} = 100 \text{ nF} \quad C_{OUT} = 1000 \text{ }\mu\text{F} \quad R_{IIM} = 4.02 \text{ k}\Omega$$

21. Hot Plug In and Inrush Current Control at 24-V Input

9.3.1.1 Thermal Regulation Loop

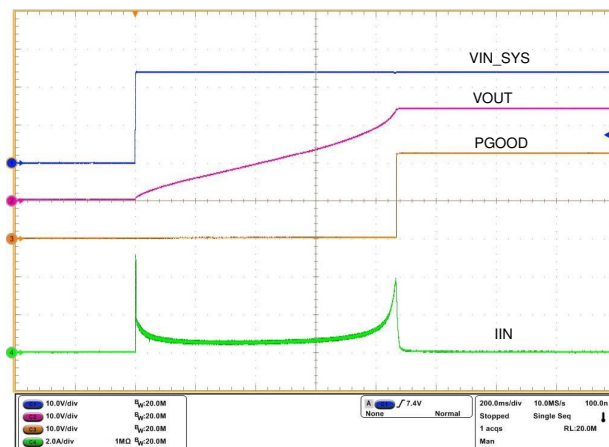
The average power dissipation within the eFuse during power up with a capacitive load can be calculated using [公式 3](#).

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (3)$$

System designs requiring to charge large output capacitors rapidly may result in an operating point that exceeds the power dissipation versus time boundary limits of the device defined by [图 18](#) characteristic curve. This may result in increase in junction temperature beyond the device's maximum allowed junction temperature. To keep the junction temperature within the operating range, the thermal regulation control loop regulates the junction temperature at $T_{(J_REG)}$, 145°C (typical) by controlling the inrush current profile and thereby limiting the power dissipation within the device automatically. An internal 2.5 seconds (typical) timer starts from the instance the thermal regulation operation kicks in. If the output does not power up within this time then the internal FET is turned OFF. Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as shown in [表 2](#). The maximum time-out of 1.25 seconds (typical) in thermal regulation loop operation ensures that the device and the system board does not heat up during steady fault conditions such as wake up with output short-circuit. This scheme ensures reliable power up operation.

Thermal regulation control loop is internally enabled during power up by $V_{(IN)}$, UVLO cycling and turn ON using SHDN control. [Figure 22](#) illustrates performance of the device operating in thermal regulation loop during power up by $V_{(IN)}$ with a large output capacitor. The Thermal regulation loop gets disabled internally after the power up sequence when the internal FET's gate gets fully enhanced or when the $t_{(Treg_timeout)}$ of 2.5 seconds (typical) time is elapsed.

Feature Description (接下页)



$$C_{dVdT} = \text{Open} \quad C_{OUT} = 30 \text{ mF} \quad R_{ILIM} = 4.02 \text{ k}\Omega$$

图 22. Thermal Regulation Loop Response During Power up with Large Capacitive Load

9.3.2 PGOOD and PGTH

The devices feature an open drain Power good (PGOOD) indicator output. PGOOD can be used for enable and disable of the downstream loads like DC-DC converters. Connect a resistor ladder network from VOUT, PGTH and GND to set the PGOOD threshold level. PGOOD goes high when the internal FET's gate is enhanced and $V_{(PGTH)}$ is above $V_{(PGTHR)}$. PGOOD goes low when $V_{(PGTH)}$ goes below $V_{(PGTHF)}$. There is a deglitch of t_{PGOODR} , 1.2 msec (typical) at the rising edge and t_{PGOODR} , 2.1 μ s (typical) deglitch on the falling edge of PGOOD indication. PGOOD is a rated for 60 V and can be pulled to IN_SYS or OUT through a resistor. PGTH can be used for setting downstream's supply UVLO levels and PGOOD as enable and disable control.

9.3.2.1 PGTH as VOUT Sensing Input

The devices use PGTH as the output (Load) voltage monitor input and to set the down stream loads UVLO threshold. To set the input PGTH threshold, connect a resistor divider network from VOUT to PGTH terminal to GND as shown in the [简化原理图](#). During a system fault recovery (example: OVP high to low or UVLO low to high) when the internal FET gate control is enabled, the device samples the PGTH information and decides whether to turn ON the FET with fast slew rate or dVdT mode based on the sampled $V_{(PGTH)}$ information.

[图 19](#) shows the turn ON behavior based on $V_{(PGTH)}$ information. During the fault recovery instance if the $V_{(PGTH)}$ level is above $V_{(PGTHF)}$ then the internal FET turns ON within a delay of $t_{OVP(dly_fast)}$ with fast slew rate (ignores the capacitance connected at dVdT pin) with thermal regulation loop enabled for a duration of $t_{CL_PLIM(dly)}$. Maximum current through the device during this operation is limited at $I_{(OL)}$ in TPS26630 and TPS26632 devices and at $2 \times I_{(OL)}$ in TPS26631, TPS26633, TPS26635 and TPS26636 devices for a maximum duration of $t_{CB(dly)}$. During the fault recovery instance if the $V_{(PGTH)}$ level is below $V_{(PGTHF)}$ then the device turns ON the internal FET in dVdT mode and the slew rate will depend on the dVdT capacitor value and maximum current through the devices is limited at $I_{(OL)}$. This way the device distinguishes between real system faults and system transients and the turn ON delay is controlled accordingly. This scheme ensures fast recovery during system tests like voltage interruption and brown-out tests, EMC testing like Electrical Fast Transients (IEC61000-4-4) and Surge (IEC61000-4-5). The fast turn ON during transient recovery feature can be disabled by connecting PGTH to GND. In this case, PGOOD will be pulled low.

Feature Description (接下页)

9.3.3 Undervoltage Lockout (UVLO)

The TPS2663x devices feature an accurate $\pm 2\%$ adjustable undervoltage lockout functionality. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input undervoltage fault, the internal FET quickly turns off and FLT is asserted. The UVLO comparator has a hysteresis of 78 mV (typical). To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to GND as shown in the [简化原理图](#). The TPS2663x devices also features a factory set 15 V input supply undervoltage lockout $V_{(IN_SYS_UVLO)}$ threshold with 1-V hysteresis. This feature can be enabled by connecting the UVLO terminal directly to the GND terminal. If the Undervoltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN_SYS terminal. UVLO terminal must not be left floating. In the applications where reverse polarity protection is required connect a minimum of 300-k Ω resistor between UVLO and IN_SYS.

[图 19](#) shows the turn ON behavior when UVLO pin voltage exceeds $V_{(UVLOR)}$ threshold.

9.3.4 Overvoltage Protection (OVP)

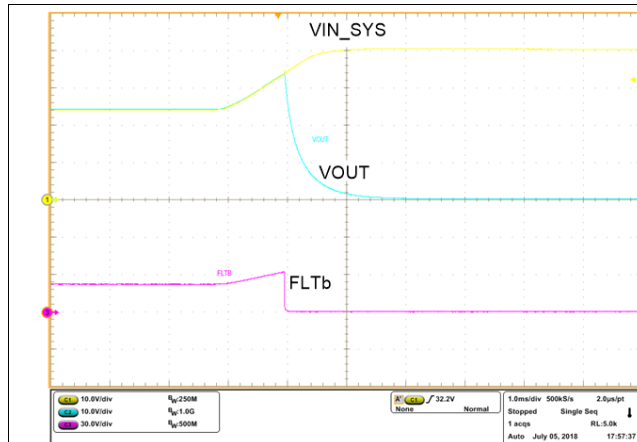
The TPS2663x devices incorporate circuitry to protect the system during overvoltage conditions. The TPS26630 and TPS26631 feature an accurate $\pm 2\%$ adjustable overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN_SYS supply to OVP terminal to GND as shown in the [简化原理图](#).

The TPS26630 and TPS26631 also feature a factory set 34.3-V input overvoltage cut off $V_{(IN_SYS_OVP)}$ threshold with a 440 mV hysteresis. This feature can be enabled by connecting the OVP terminal directly to the GND terminal. The TPS26632, TPS26633 and TPS26636 feature an internally fixed 35-V maximum overvoltage clamp $V_{(OVC)}$ functionality. The TPS26632 and TPS26633 clamps the output voltage to $V_{(OVC)}$, when the input voltage exceeds 35 V. TPS26635 features a fixed 39-V maximum overvoltage clamp level. During the output voltage clamp operation, the power dissipation in the internal MOSFET is $PD = (V_{(IN_SYS)} - V_{(OVC)}) \times I_{(OUT)}$. Excess power dissipation for a prolonged period can increase the device temperature. To avoid this, the internal FET is operated in overvoltage clamp for a maximum duration of $t_{OVC(dly)}$, 162 msec (typical). After this duration, the internal FET is turned OFF and the subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as shown in [表 2](#).

[图 19](#) shows the turn ON behavior when OVP pin voltage falls below $V_{(OVPF)}$ threshold.

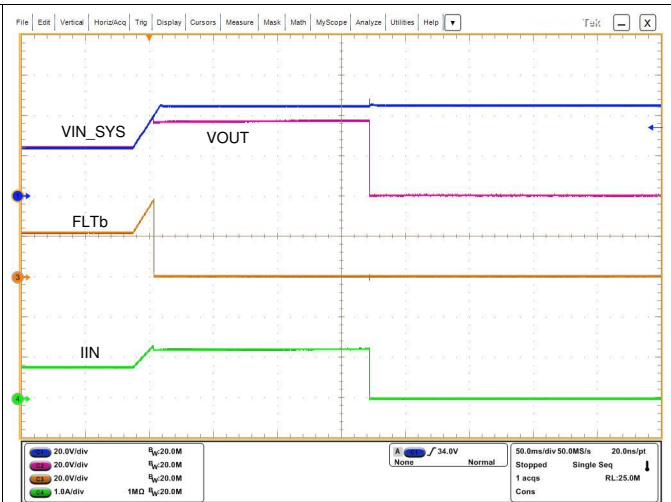
[图 23](#) illustrates the overvoltage cut-off functionality and [图 24](#) illustrates the overvoltage clamp functionality. FLT is asserted after a delay of 617 μ s (typical) after entering in overvoltage clamp mode and remains asserted until the overvoltage fault is removed.

Feature Description (接下页)



TPS26630 and TPS26631

图 23. Overvoltage Cut-off Response at 33-V Level



TPS26635

$R_{LOAD} = 30\Omega$, FLT connected to VOUT

图 24. Overvoltage Clamp Response with TPS26635

9.3.5 Input Reverse Polarity Protection (B_GATE, DRV)

The TPS2663x devices support the reverse input polarity protection feature. Connect an N-channel power FET (Q1) with the source to IN_SYS, drain to IN and GATE to B-GATE as shown in 图 25. This forms a back to back FET topology in power path that is required to protect the load from input reverse polarity faults. Connect an external signal FET (Q2) across BGATE, DRV and IN_SYS. Q2 acts as a pull down gate switch for Q1. In the applications where reverse polarity protection and reverse current blocking is not required then connect IN_SYS and IN together. Leave BGATE and DRV open as shown in 图 26. 图 27 illustrates the reverse input polarity protection functionality.

The TPS2663x devices support a maximum differential voltage across $V_{(IN_SYS)} - V_{(OUT)}$ upto -85 V . This high voltage transients generally appear during the IEC61000-4-5 surge testing at the $V_{(IN_SYS)}$. This voltage stress appears across the external N-channel FET. The TPS2663x provides a gate drive (B_GATE) of 10.2 V (typical). The fast pull down gate switch Q2 pulls down the GATE of the Q1 during reverse current and reverse polarity fault events. Q2 should be atleast 15-V , V_{DS} rated FET with a maximum V_{GS} rating of 20-V , $C_{iss} \leq 50\text{ pF}$ and $VGTH(\min) \leq 3\text{ V}$.

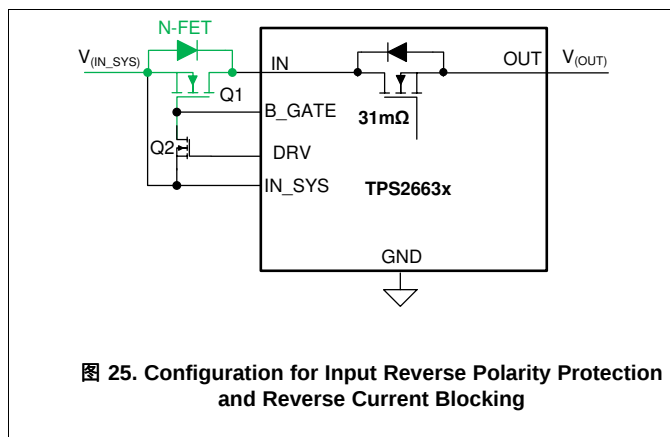


图 25. Configuration for Input Reverse Polarity Protection and Reverse Current Blocking

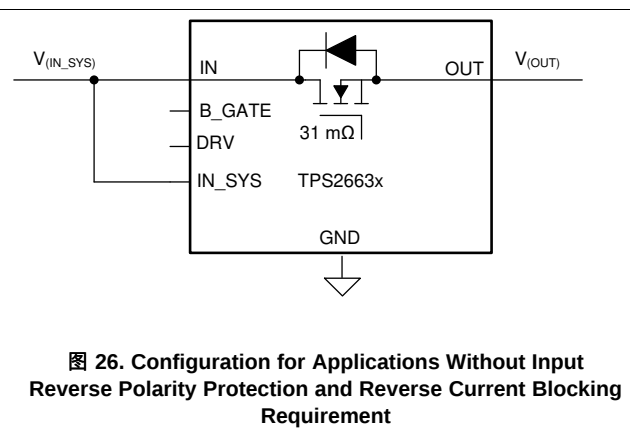


图 26. Configuration for Applications Without Input Reverse Polarity Protection and Reverse Current Blocking Requirement

Feature Description (接下页)

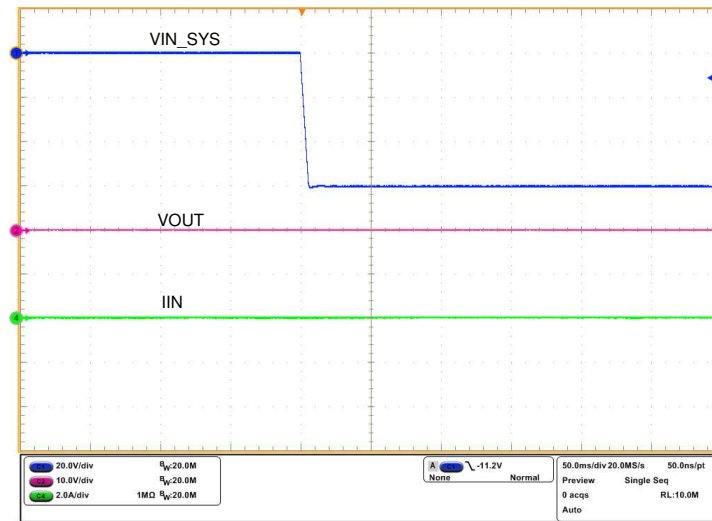


图 27. Input Reverse Polarity Response at -60-V Input

9.3.6 Reverse Current Protection

The device monitors $V_{(IN_SYS)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected. The reverse comparator turns OFF the external blocking FET Q1 quickly as soon as $V_{(IN_SYS)} - V_{(OUT)}$ falls below -1 V. The total time taken to turn OFF the FET Q1 in this condition is $t_{RCB(fast_dly)} + t_{(Driver)}$. The delay due to the driver stage $t_{(Driver)}$ can be calculated using 公式 4.

$$t_{(Driver)} = -RDSON_{(Q2)} \times Ciss_{(Q1)} \times \ln\left(\frac{VGTH_{(Q1)}}{V_{BGATE}}\right)$$

where

- $RDSON_{(Q2)}$ is the on resistance of the fast pull down switch Q2
- $Ciss_{(Q1)}$ is the input capacitance of the blocking FET Q1
- $VGTH_{(Q1)}$ is the GATE threshold voltage of the blocking FET Q1
- $V_{BGATE} = 10.2$ V (typical)

(4)

In a typical system design, $t_{(Driver)}$ is generally 10% to 20% of $t_{RCB(fast_dly)}$ of 120 nsec (typical).

图 28 and 图 29 illustrates the behavior of the system during input hot short circuit condition. The blocking FET Q1 is turned ON within 1.6 ms (typical) once the differential forward voltage $V_{(IN_SYS)} - V_{(OUT)}$ exceeds 67 mV (typical).

Feature Description (接下页)

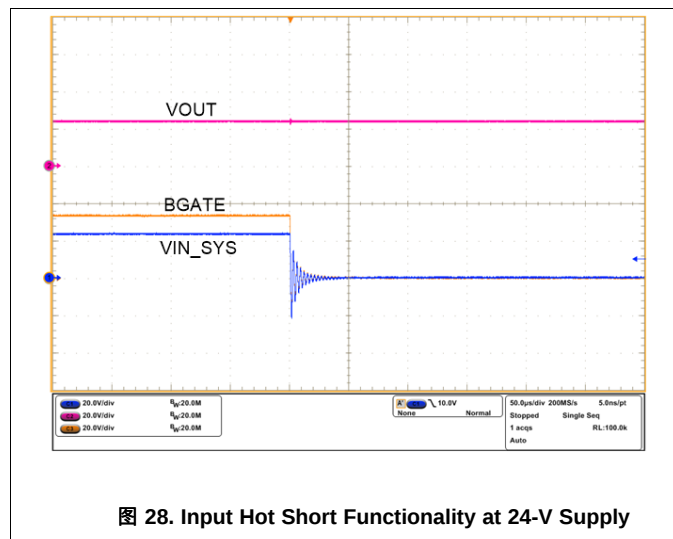


图 28. Input Hot Short Functionality at 24-V Supply

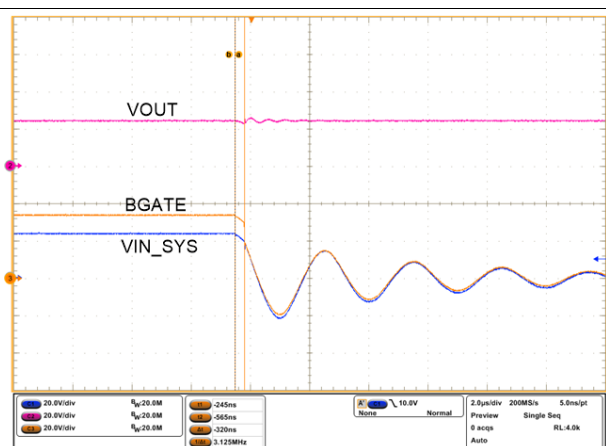


图 29. Input Hot-Short: Fast Trip Response (Zoomed)

The reverse comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over-drive differential voltage $V_{(IN_SYS)} - V_{(OUT)}$ over $V_{(REVTH)}$. Higher the over-drive, faster the turn OFF time, $t_{RCB(dly)}$.

9.3.7 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

9.3.7.1 Overload Protection

Set the current limit using 公式 5

$$I_{OL} = \frac{18}{R_{(ILIM)}}$$

where

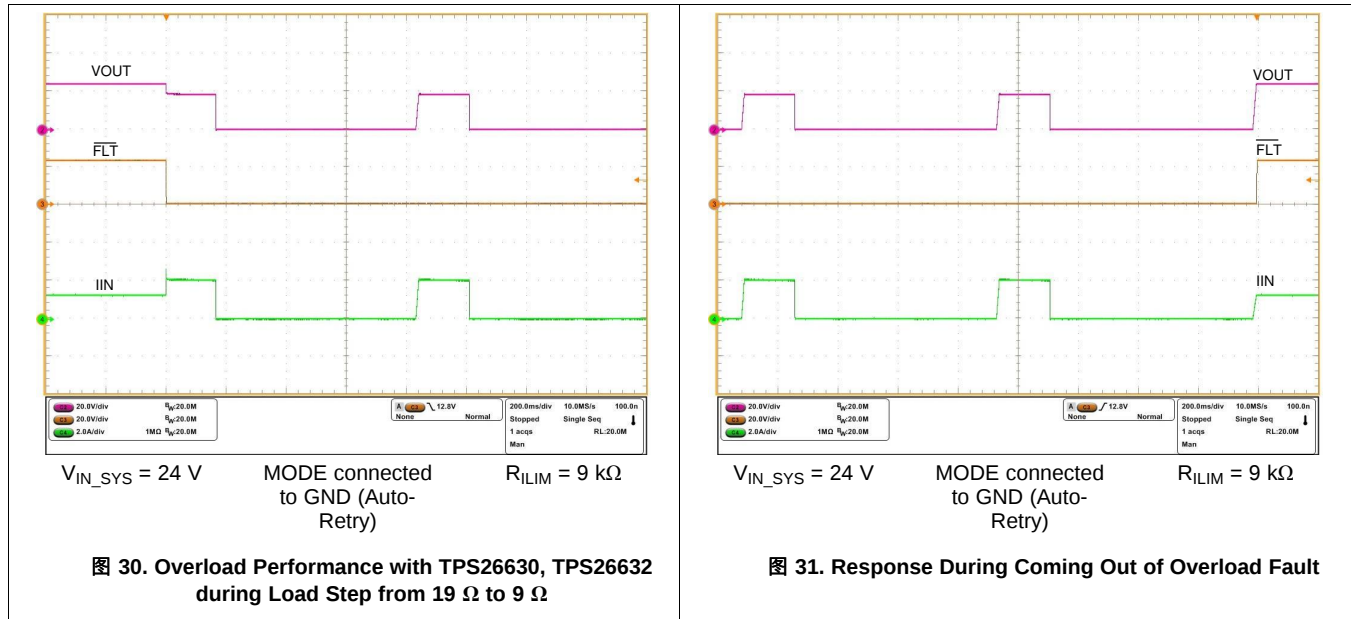
- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in $k\Omega$

(5)

9.3.7.1.1 Active Current Limiting at $1 \times I_{OL}$, (TPS26630 and TPS26632 Only)

The TPS2663x devices feature accurate overload current limiting and fast short circuit protection feature. With TPS26630 and TPS26632 if the load current exceeds the programmed current limit I_{OL} , the device regulates the current through it at I_{OL} eventually reducing the output voltage. The power dissipation across the device during this operation will be $(V_{IN} - V_{OUT}) \times I_{OL}$ and this could heat up the device and eventually enter into thermal shutdown. The maximum duration for the overcurrent through the FET $t_{CL_PLIM(dly)}$, 162 msec (typical). If the thermal shutdown occurs before this time the internal FET turns OFF and the subsequent operation (auto-retry or latch OFF) will depend on the MODE pin configuration in 表 2. 图 30, and 图 31 illustrate overload current limiting performance.

Feature Description (接下页)



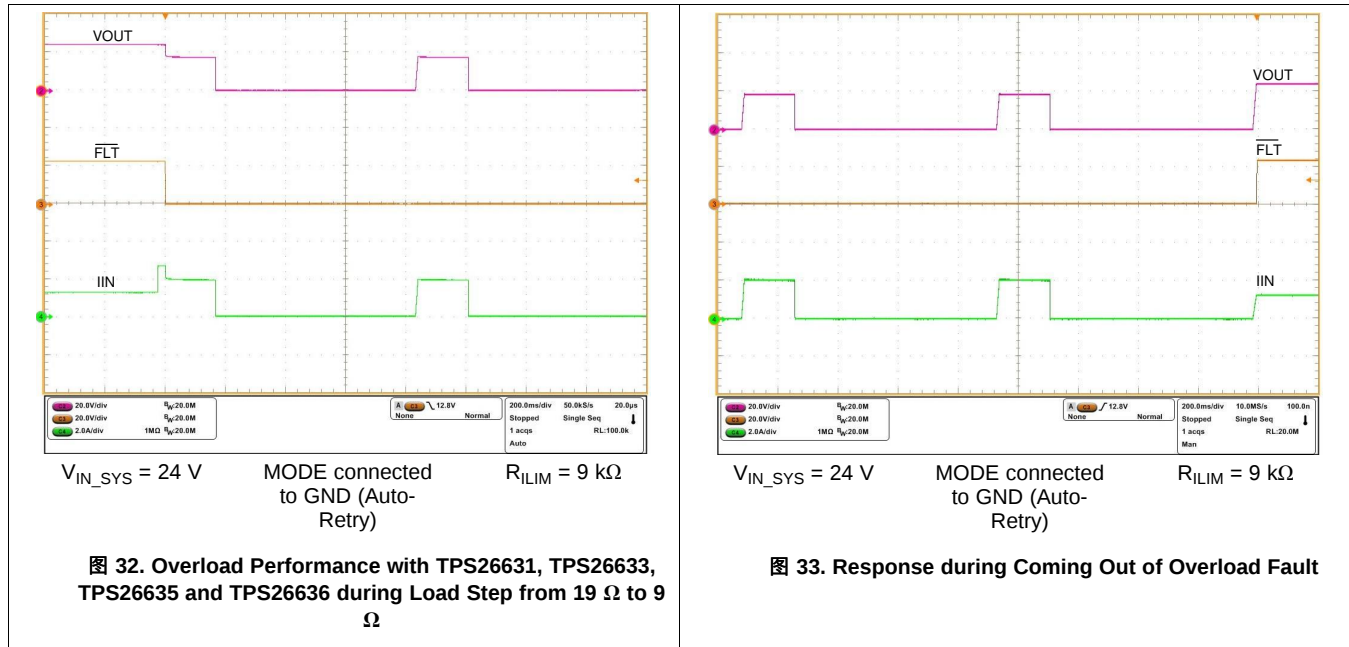
9.3.7.1.2 Active Current Limiting with 2x I_{OL} Pulse Current Support , (TPS26631, TPS26633, TPS26635 and TPS26636 Only)

TPS26631, TPS26633, TPS26635 and TPS26636 after the start-up and with PGOOD high, if the load current exceeds I_{OL}, then an internal fixed t_{CB(dly)}, 25.5 msec (typical) timer starts. During this time the device will pass through the over current demanded by the load not more than 2 x I_{OL} above which the device will regulate at 2 x I_{OL}. After t_{CB(dly)} time, the device regulates the current at I_{OL}. The power dissipation across the device during this operation will be (V_{IN} - V_{OUT}) x I_{OL} and this could heat up the device and eventually enter into thermal shutdown. The maximum duration for the internal FET in current regulation is t_{CL_PLIM(dly)}. The subsequent operation will be based on the MODE setting (either auto-retry or latch OFF) in 表 2.

The 2 x I_{OL} pulse current support is activated only after PGOOD goes high. If PGOOD is in low state such as during start-up operation or during auto-retry cycles, the 2 x I_{OL} pulse current support is not activated and the device limits the current at I_{OL} level.

图 32, and 图 33 illustrate overload current limiting performance.

Feature Description (接下页)

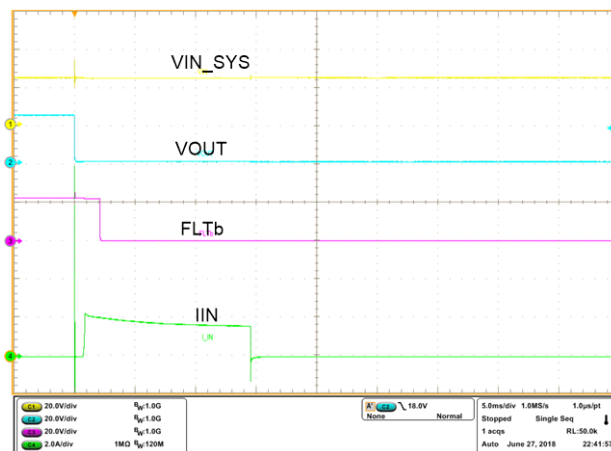


The TPS2663x devices feature ILIM pin short and open fault detection and protection. The internal FET is turned OFF when ILIM pin is detected short or open to GND and it remains OFF till the ILIM pin fault is removed.

Refer to 图 20 for more information on $t_{CB(dly)}$ and $t_{CL_PLIM(dly)}$ parameter measurement information.

9.3.7.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)} = 1\text{ }\mu\text{s}$ (typical) with $I_{(SCP)} = 45\text{ A}$ of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTTRIP)}$. The fasttrip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. 图 34 illustrates output hot-short performance of the device.



$V_{IN_SYS} = 24\text{ V}$

$R_{ILIM} = 9.09\text{ k}\Omega$

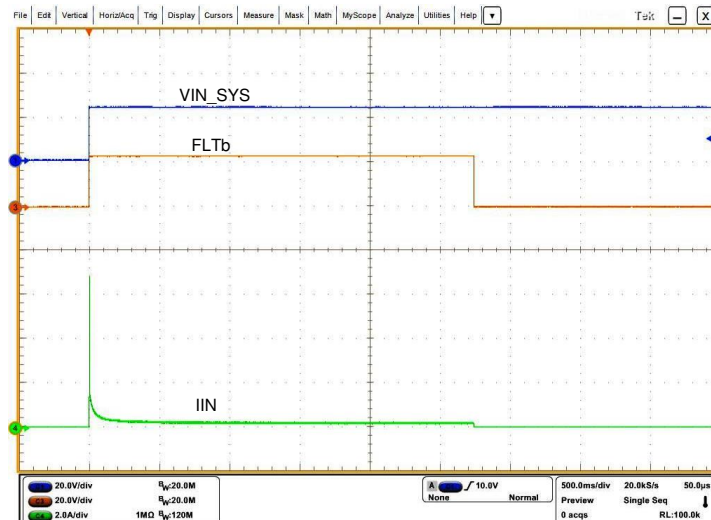
图 34. Output Hot-Short Response

Feature Description (接下页)

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the overcurrent level, $I_{(FASTTRIP)}$ through the device. Higher the overcurrent, faster the turn OFF time, $t_{(FASTTRIP(dly))}$. At overload current level in the range of $I_{FASTTRIP} < I_{OUT} < I_{SCP}$ the fast-trip comparator response is 3.2 μs (typical).

9.3.7.2.1 Start-Up With Short-Circuit On Output

When the device is started with short-circuit on the output, the current begins to limit at $I_{(OL)}$. Due to high power dissipation of $V_{IN} \times I_{(OL)}$ within the device the junction temperature increases. Subsequently, the thermal regulation control loop limits the load current to regulate the junction temperature at $T_{(J_REG)}$, 145°C (typical) for a duration of $t_{(Treg_timeout)}$, 2.5 sec (typical). Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as per the 表 2. FLT gets asserted after $t_{(Treg_timeout)}$ and remains asserted till the output short-circuit is removed. 图 35 illustrates the behavior of the device in this condition.



(1)

$$V_{IN} = 24V$$

$$R_{LIM} = 3\text{ k}\Omega$$

图 35. Start-Up With Short on Output

9.3.8 Output Power Limiting, PLIM (TPS26632, TPS26633, TPS26635 and TPS26636 Only)

The TPS26630 and TPS26631 devices with a fixed overcurrent limit threshold the maximum output power limit increases linearly with supply input. Electrical industrial process control equipment such as PLC CPU needs to comply with standards like IEC61010-1 and UL1310 for fire safety, which require limited energy and power circuits. Limiting the output power becomes a challenge in such high power applications where the operating supply voltage range is wide. The TPS26632, TPS26633, TPS26635 and TPS26636 devices integrate adjustable output power limiting functionality that simplifies the system design requiring compliance in accordance to this standard.

Connect a resistor from PLIM to GND as shown in 图 36 to set the output power limiting value. If output power limiting is not required then connect PLIM to GND directly. This disables the PLIM functionality.

During an over power load event the TPS26632 limits the output power at the programmed value set by PLIM resistor. This indirectly results in the device operation in current limiting mode with steady state output voltage and current set by the load characteristics and $P_{LIM} = V_{OUT} \times I_{OUT}$. 图 12 shows the output power limit and current limit characteristics of TPS26632 with 100 W power limit setting. The maximum duration for the device in power limiting mode is 162 msec (typical), $t_{CL_PLIM(dly)}$. After this time, the device operates either in auto-retry or latch off mode based on MODE pin configuration in 表 2.

Feature Description (接下页)

During an over power load event the TPS26633, TPS26635 and TPS26636 allows the extra power for a maximum duration of $t_{CB(dly)}$, 25.5 msec (typical). The maximum power during this time is limited to $V_{OUT} \times 2 \times I_{OL}$ where I_{OL} is the overload current limit set by the $R_{(ILIM)}$ resistor. After the $t_{CB(dly)}$ time, the output power gets limited to the value programmed by the PLIM resistor. Set the power limit using 公式 6.

$$P_{(PLIM)} = 1 \times R_{(PLIM)} \quad (6)$$

Here $P_{(PLIM)}$ is output power limit in watts, $R_{(PLIM)}$ is the power limit setting resistor in k Ω . 图 37 and 图 38 illustrate output power limiting performance of TPS26632 and TPS26633 devices respectively.

Refer to 图 20 for more information on $t_{CB(dly)}$ and $t_{CL_PLIM(dly)}$ parameter measurement information.

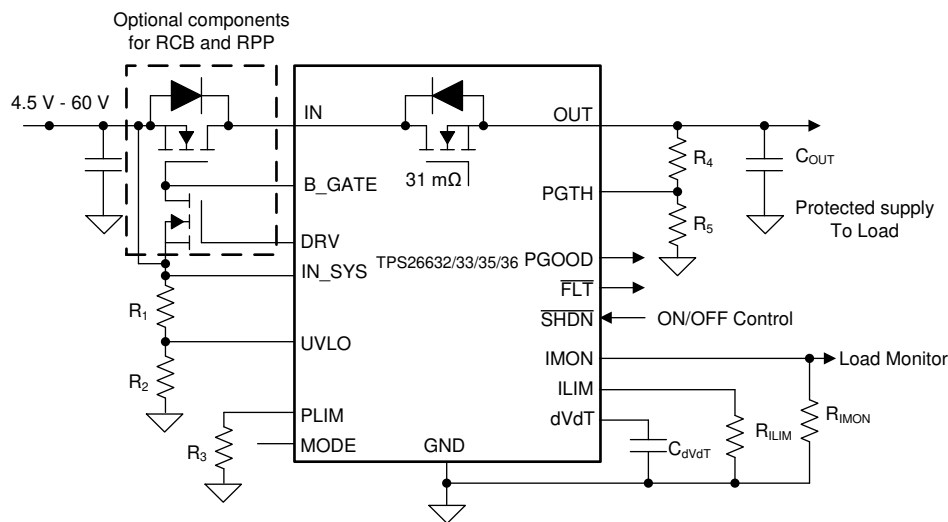
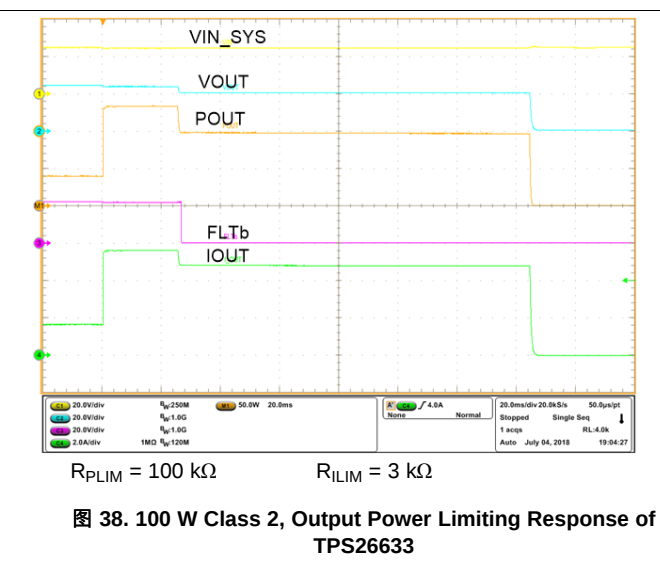
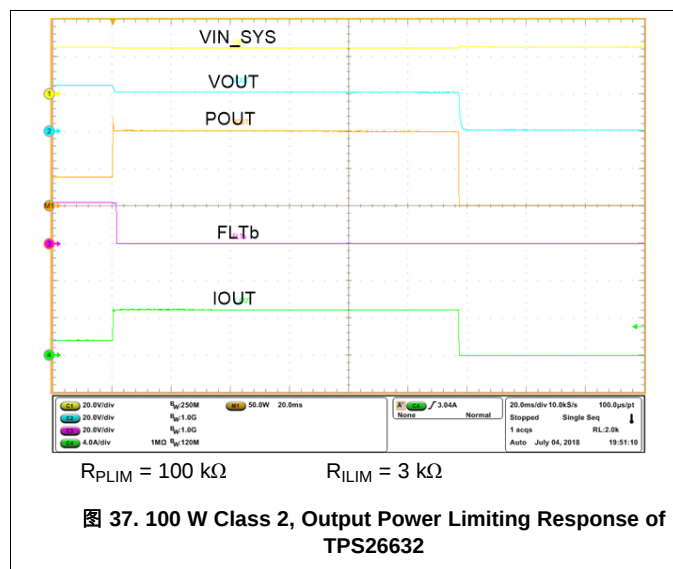


图 36. TPS26632, TPS26633, TPS26635 和 TPS26636 Typical Application Schematic



9.3.9 Current Monitoring Output (IMON)

The TPS2663x devices feature an accurate analog current monitoring output. A current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage ($V_{(IMONmax)}$) for monitoring the current is limited to 4 V. This puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by 公式 7.

Feature Description (接下页)

$$V_{(IMON)} = [I_{(OUT)} \times GAIN_{(IMON)}] \times R_{(IMON)}$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)} \cdot I_{(OUT)} = 27.9 \mu A/A$ (Typical)
- $I_{(OUT)}$ is the load current

(7)

Refer to 图 13 for IMON output versus load current plot. 图 39 illustrates IMON performance.

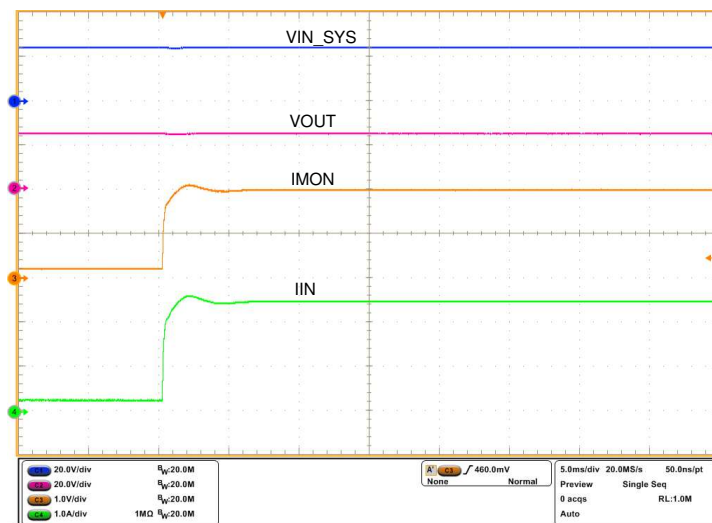


图 39. IMON Response During a Load Step

The IMON pin must not have a bypass capacitor to avoid delay in the current monitoring information.

9.3.10 FAULT Response ($\overline{FLT}$)

The $\overline{FLT}$ open-drain output asserts (active low) under the faults events such as undervoltage, overvoltage, overload, power limiting, reverse current, ILIM pin short and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry. $\overline{FLT}$ can be left open or connected to GND when not used.

9.3.11 IN_SYS, IN, OUT and GND Pins

Connect a minimum of 0.1uF capacitor across IN_SYS and GND. For systems and applications where reverse polarity protection and/or reverse current blocking feature is required

- Connect a N-channel FET between IN_SYS and IN with source of the FET connected to IN_SYS, Drain at IN and GATE to B_GATE.
- Connect a N-channel signal FET with GATE to DRV, Drain to B_GATE, Source to IN_SYS

If the external N-channel FET is not used then connect IN_SYS and IN together and leave B_GATE and DRV pins floating as shown in 图 27. Do not leave any of the IN and OUT pins un-connected.

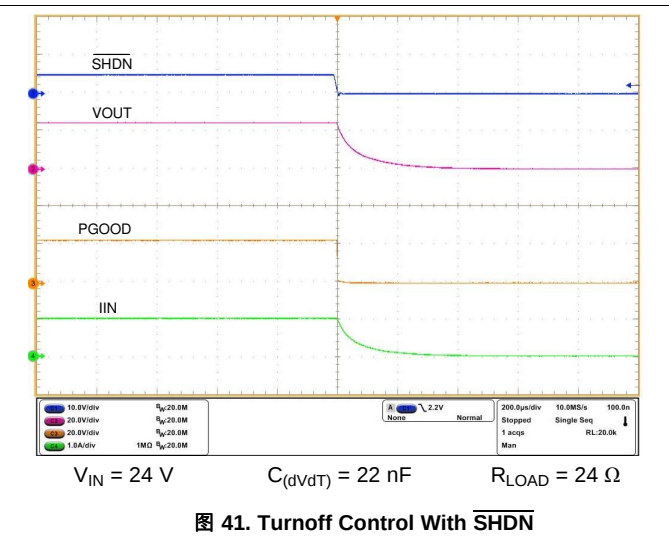
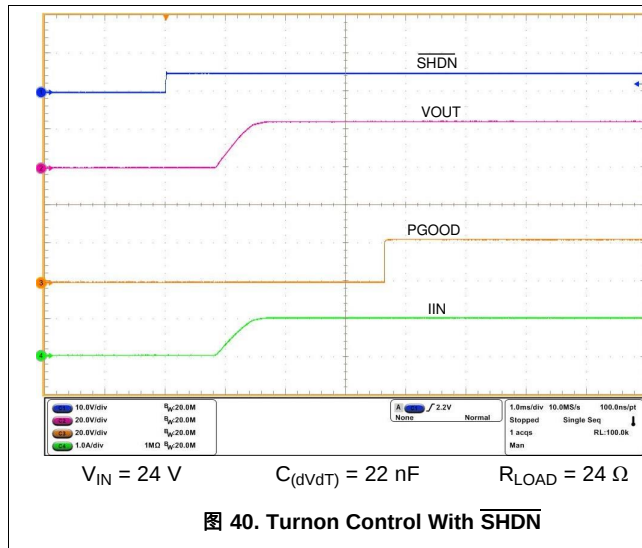
9.3.12 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET, if the junction temperature exceeds $T_{(TSD)}$, 165°C (typical). After the thermal shutdown event, depending upon the mode of fault response configured as per the 表 2, the device either latches off or commences an auto-retry cycle of 648 msec (typical), $t_{(TSD_retry)}$ after $T_J < [T_{(TSD)} - 11^\circ C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

Feature Description (接下页)

9.3.13 Low Current Shutdown Control ($\overline{\text{SHDN}}$)

The internal, external FET and hence the load current can be switched off by pulling the $\overline{\text{SHDN}}$ pin below 0.8-V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device quiescent current reduces to 21 μA (typical) in shutdown state. To assert SHDN low, the pull down must have sinking capability of at least 10 μA . To enable the device, SHDN must be pulled up to atleast 2 V. Once the device is enabled, the internal FET turns on with dVdT mode. 图 40 和 图 33 illustrate the performance of SHDN control.



9.4 Device Functional Modes

The TPS2663x devices respond differently to overload with MODE pin configurations. The operational differences are explained in 表 2.

表 2. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	Overload Protection Operation	Device
Open	Active Current limiting at 1x for a maximum duration of $t_{\text{CL_PLIM(dly)}}$. There after Latches OFF. Latch reset by toggling SHDN low to high or UVLO low to high or power cycling IN_SYS	TPS26630, TPS26632
	Active Current limiting at 2x for $t_{\text{CB(dly)}}$ duration followed with 1x current limiting for a maximum duration of $t_{\text{CL_PLIM(dly)}}$. There after Latches OFF. Latch reset by toggling SHDN low to high or UVLO low to high or power cycling IN_SYS	TPS26631, TPS26633, TPS26635, TPS26636
Shorted to GND	Active Current limiting at 1x for a maximum duration of $t_{\text{CL_PLIM(dly)}}$. There after auto-retries after a delay of $t_{\text{(TSD_retry)}}$.	TPS26630, TPS26632
	Active Current limiting at 2x for $t_{\text{CB(dly)}}$ duration followed with 1x current limiting for a maximum duration of $t_{\text{CL_PLIM(dly)}}$. There after auto-retries after a delay of $t_{\text{(TSD_retry)}}$.	TPS26631, TPS26633, TPS26635

Refer to 图 20 for more information on $t_{\text{CB(dly)}}$ and $t_{\text{CL_PLIM(dly)}}$ parameter measurement information.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2663x is an industrial eFuse, typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 60 V with adjustable current limit, output power limit, overvoltage, undervoltage and reverse polarity protections. The device aids in controlling in-rush current and provides robust protection against reverse current and filed miss-wiring conditions for systems such as PLCs, Industrial PCs, Control and Automation and Sensors. The device also provides robust protection for multiple faults on the system rail

The [Detailed Design Procedure](#) section can be used to select component values for the device. Additionally, a spreadsheet design tool [TPS2663 Design Calculator](#) is available in the web product folder.

10.2 Typical Application: Power Path Protection in a PLC System

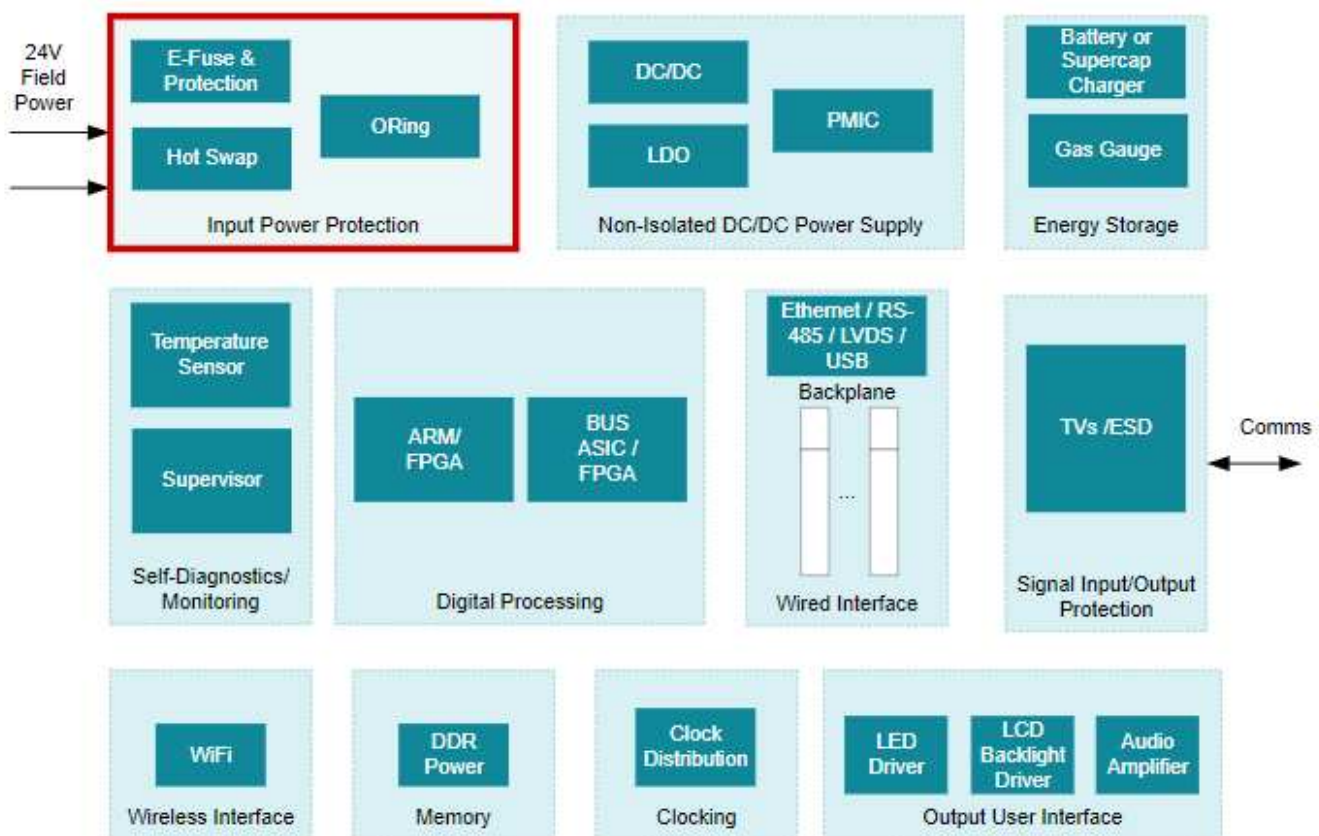


图 42. A Typical CPU (PLC Controller) System Block Diagram

The PLC system is usually connected to an external 24-V DC power supply to provide power to the controller unit, backplane, and I/O modules. Input protection circuits are required to protect the PLC from faults such as overvoltage, undervoltage, and overload. Because input supply connectors are screw type, there can always be a possibility of reverse supply connections. Protection circuits should block the reverse polarity to protect the PLC from possible negative voltages. At the same time, every PLC is tested for electrostatic discharge (ESD)

10.2.2.2 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1 , R_2 and R_3 connected between IN_SYS, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 公式 9 and 公式 10.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \quad (9)$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \quad (10)$$

For minimizing the input current drawn from the power supply $\{I_{(R123)} = V_{(IN)} / (R_1 + R_2 + R_3)\}$, it is recommended to use higher value resistance for R_1 , R_2 and R_3 .

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I_{(R123)}$ must be chosen to be 20x greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)} = 1.2$ V and $V_{(UVLOR)} = 1.2$ V. From the design requirements, $V_{(OV)}$ is 33 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of $R_3 = 34$ k Ω and use 公式 9 to solve for $(R_1 + R_2) = 916$ k Ω . Use 公式 10 and value of $(R_1 + R_2)$ to solve for $R_2 = 29.4$ k Ω and finally $R_1 = 887$ k Ω .

Choose the closest standard 1% resistor values: $R_1 = 887$ k Ω , $R_2 = 29.4$ k Ω , and $R_3 = 34$ k Ω .

The UVLO and the OVP pins can also be connected to the GND pin to enable the internal default $V_{(OV)} = 34.2$ V and $V_{(UV)} = 15.6$ V.

10.2.2.3 Output Buffer Capacitor – C_{OUT}

During the power interruption time T_{FAIL_TR} the output capacitor C_{OUT} of the TPS26630 provides energy to the 15 W DC-DC converter load. Use 公式 11 to compute the required buffer capacitor C_{OUT}

$$C_{OUT} = \frac{2 \times P_{(DC-DC)} \times T_{FAIL_TR}}{V_{(IN_SYS)}^2 - V_{(UV_DC-DC)}^2}$$

where

- $P_{(DC-DC)} = 15$ W/ η . Assuming efficiency of 95%, $P_{(DC-DC)} = 15.8$ W
 - $T_{FAIL_TR} = 10$ msec
 - $V_{(IN_SYS)} = 24$ V
 - $V_{(UV_DC-DC)} = 15$ V
- (11)

$C_{OUT} = 0.9$ mF. Choose a capacitor with $\pm 10\%$ tolerance, $C_{OUT} = 1$ mF/35 V electrolytic capacitor. 图 45 and 图 46 illustrate the performance during the power interruption tests on TPS26630. 图 48 illustrate the performance on TPS26631.

10.2.2.4 PGTH Set Point

Set the V_{PGTHF} threshold at the down-stream DC-DC converter UVLO falling threshold. VIN minimum operating voltage of the DC-DC converter is at 15 V. Assuming UVLO to be at 20% lower level, $V_{UVLO_DC-DC} = 12$ V. Use 公式 12 to calculate R_4 and R_5 .

$$V_{(PGTHF)} = \frac{R_5}{R_4 + R_5} \times V_{UVLO_DC-DC} \quad (12)$$

$V_{(PGTHF)} = 1.14$ V. Assuming $R_5 = 56$ k Ω , R_4 comes out to be approximately 499 k Ω .

10.2.2.5 Setting Output Voltage Ramp Time—(t_{dVdT})

Use 公式 1 and 公式 2 to calculate required $C_{(dVdT)}$ for achieving an inrush current of 500 mA. $C_{(dVdT)} = 0.1$ μ F. 图 44 illustrates the inrush current limiting performance during 24-V hot-plug in condition.

10.2.2.5.1 Support Component Selections— R_{PGOOD} and $C_{(IN)}$

The R_{PGOOD} serves as pull-up for the open-drain output. The current sink by this pin must not exceed 10 mA (see the [Absolute Maximum Ratings](#) table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for R_{PGOOD}. Connect PGOOD directly to the EN pin of the DC-DC converter. [Figure 47](#) and [Figure 49](#) illustrate the power up and power down performance of the system respectively. The C_{IN} is a local bypass capacitor to suppress noise at the input. A minimum of 1 μF is recommended for C_(IN) for limit the slew rates during the surge test.

10.2.2.6 Selecting Q1, Q2 and TVS Clamp for Surge Protection

For $\pm 500\text{-V}$, $2\text{-}\Omega$ surge, typically a SMC sized TVS like SMCJ36CA clamps the voltage around $\pm 55\text{ V}$. During the negative surge strike, the input voltage $V_{\text{IN_SYS}}$ spikes to -55 V . This results in a voltage stress of $-(55\text{ V} + 24\text{ V}) = -79\text{ V}$ across the external blocking FET Q1. Choose at least a 80-V rated N-channel FET. B_GATE drive is in the range of 10 V to 14 V . Select a suitable FET with the target $R_{\text{DS(on)}}$ specified at this gate drive voltage. The fast pull down gate switch Q2 pulls down the GATE of the Q1 during the reverse current event appearing during the surge test. Q2 should be at least 15-V VDS rated FET with a maximum VGS rating of 20-V , $C_{\text{iss}} \leq 50\text{ pF}$ and $V_{\text{GTH(min)}} \leq 3\text{ V}$. CSD19537Q3 and BSS138 are selected for Q1 and Q2 respectively. 图 50 and 图 51 illustrate the performance of the system during the surge testing.

10.2.3 Application Curves

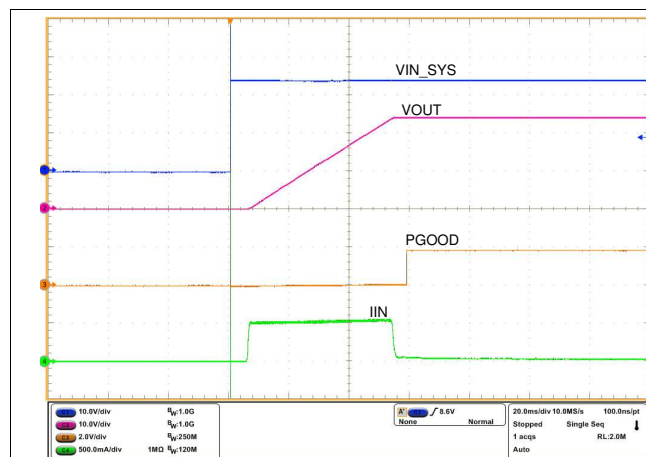


图 44. Hot-Plug In at 24-V Supply

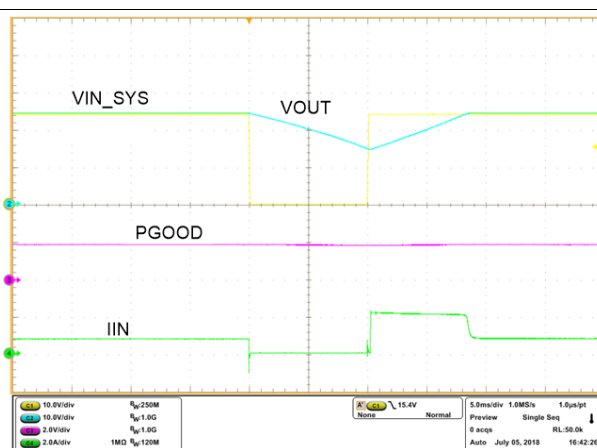


图 45. Voltage Interruption Response With TPS26630

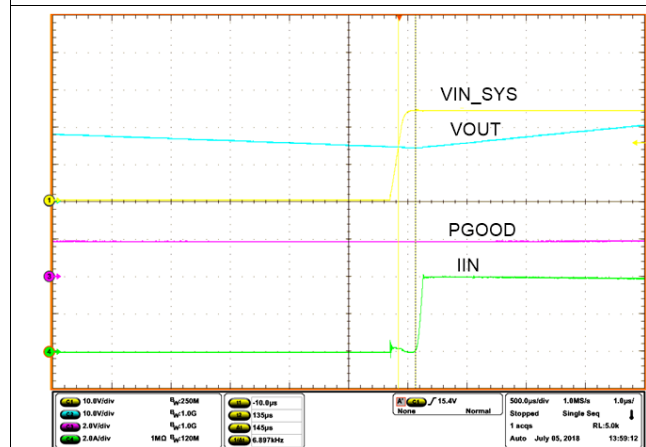


图 46. Voltage Interruption Response With TPS26630 (Zoomed)

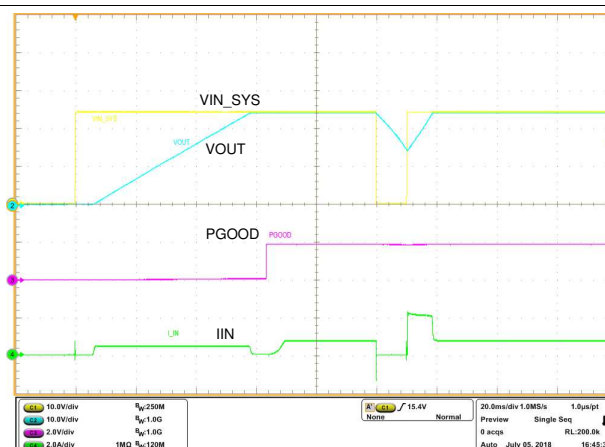


图 47. Power Up Followed With Voltage Interruption With TPS26630

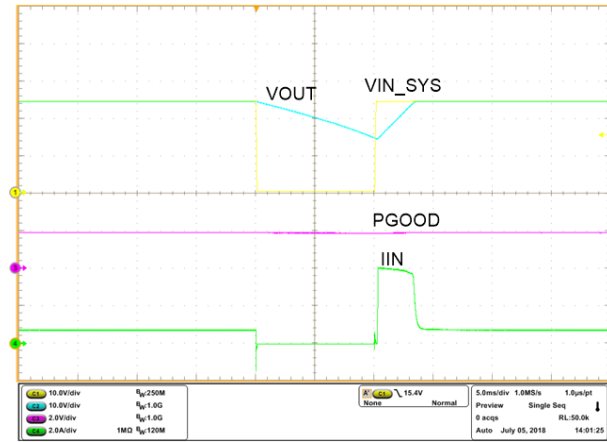


图 48. Voltage Interruption Performance With TPS26631

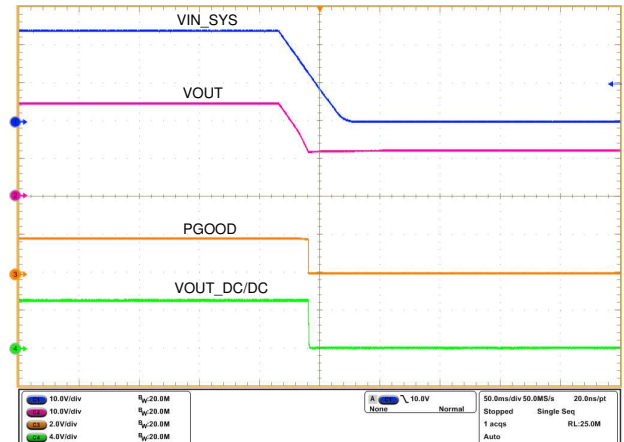


图 49. Power Down Response

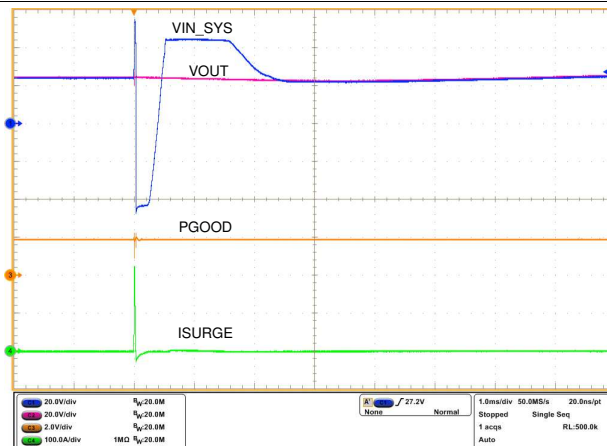


图 50. 500-V, 2-Ω Surge Response

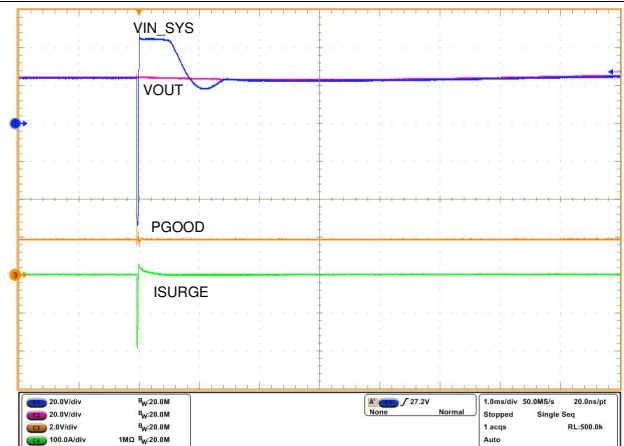


图 51. -500-V, 2-Ω Surge Response

10.3 System Examples

10.3.1 Simple 24-V Power Supply Path Protection

With the TPS2663x devices, a simple 24-V power supply path protection can be realized using a minimum of five external components as shown in the schematic diagram in 图 52. The external components required are: a N-Channel Power FET Q_1 , a N-Channel signal FET Q_2 and a $R_{(ILIM)}$ resistor to program the current limit, $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

System Examples (接下页)

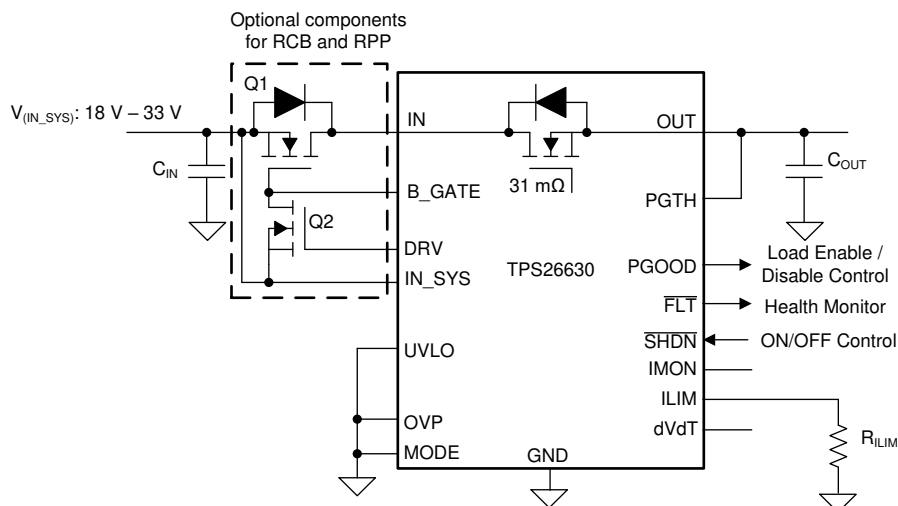


图 52. TPS26630 Configured for a Simple 24-V Supply Path Protection

Protection features with this configuration include:

- Load and device protection from reverse input polarity fault down to –60 V (with a 60-V rated Q₁)
- Overvoltage Protection at 34 V
- Inrush current control with 24 V/240 μs output voltage slew rate
- Reverse Current Blocking
- Accurate current limiting with Auto-Retry

10.3.2 Priority Power MUX Operation

Applications having two energy sources such as Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adaptor) has the priority over the internal back-up power or auxiliary power. These applications demand for switch over from mains power to backup power only when main input voltage falls below a user defined threshold. The TPS2663x devices provide a simple solution for priority power multiplexing needs.

图 53 shows a typical priority power multiplexing implementation using devices. When the MAIN power is present, the device in VIN_MAIN path powers the OUT bus irrespective of whether auxiliary power VIN_AUX is greater than or less than VIN_MAIN. Once the voltage on the VIN_MAIN rail falls below the user-defined threshold, the device VIN_MAIN issues a signal to switch over to auxiliary power VIN_AUX. The transition happens seamlessly in $t_{OVP(dly_fast)}$, with minimal voltage droop on the output. The voltage droop during transition is a function of load current and output capacitance. See 公式 13.

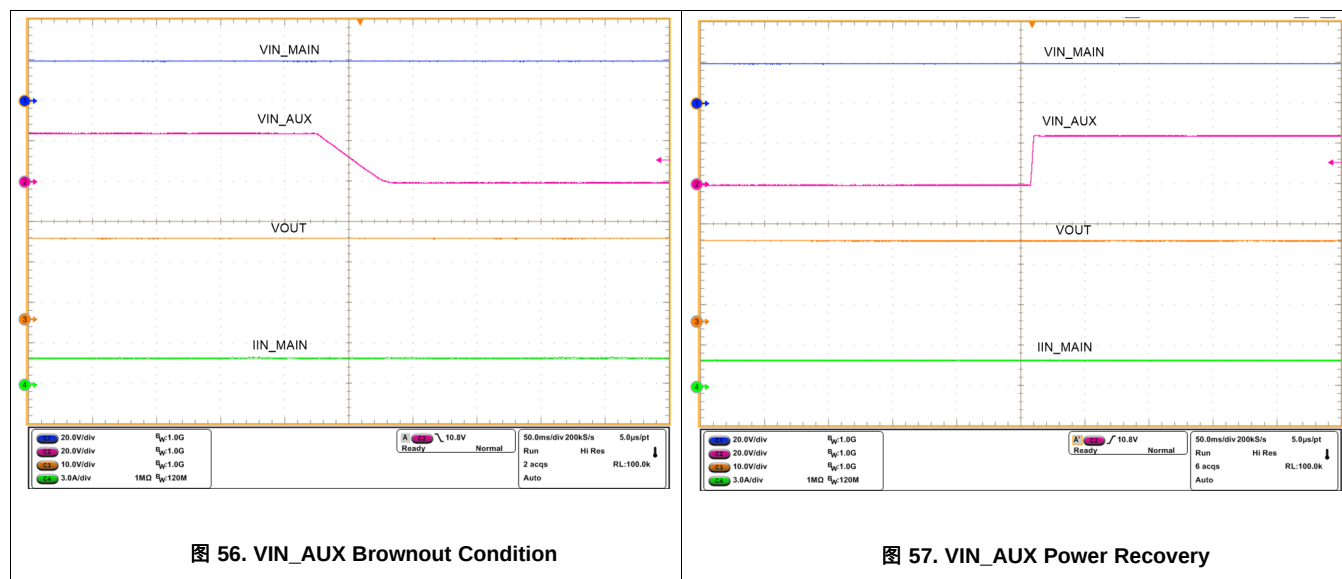
$$V_{(DROOP)} = \frac{I_{(LOAD)} \times t_{OVP(fast_dly)}}{C_{(OUT)}}$$

where

- $V_{(DROOP)}$ is in volts, $I_{(LOAD)}$ is load current in Ampere, $C_{(OUT)}$ is output capacitance in μF, $t_{OVP(fast_dly)} = 140 \mu s$ (typical) (13)

图 54, 图 55, 图 56 和 图 57 show typical switch-over waveforms of Priority Muxing implementation using the TPS26630 or TPS26631 for 20-V Primary and 24-V Auxiliary Bus.

System Examples (接下页)



10.3.3 Input Protection for a Compact 24-V Auxiliary Power Supply for Servo Drives

TPS2663x eFuse protects the system from common faults such as reverse polarity, reverse power flow, overvoltage, undervoltage and overcurrents along with a robust EMC immunity performance. Refer to, [Compact, efficient, 24-V input auxiliary power supply reference design for servo drives](#) TI Design Guide for further information.

10.4 Do's and Don'ts

- In the applications where reverse polarity protection is required use external FETs Q1 and Q2.
- Connect at least a 300 kΩ resistor across UVLO and IN_SYS in the applications where reverse polarity protection is required.

11 Power Supply Recommendations

The TPS2663x eFuse is designed for the supply voltage range of $4.5\text{ V} \leq V_{\text{IN}} \leq 60\text{ V}$. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 μF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

11.1 Transient Protection

In case of short circuit and overload current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the [Absolute Maximum Ratings](#) of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor (C_{IN}) to approximately 0.1 μF to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with [公式 14](#).

Transient Protection (接下页)

$$V_{\text{spike(Absolute)}} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}}$$

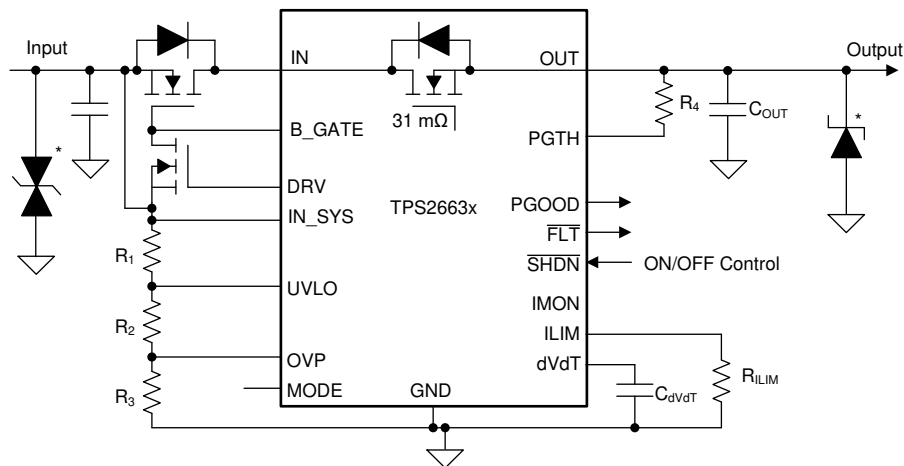
where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

(14)

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place at least 1 μF of input capacitor.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in 图 58



* Optional components needed for suppression of transients

图 58. Circuit Implementation With Optional Protection Components for TPS2663x

12 Layout

12.1 Layout Guidelines

- For all the applications, a 0.1 μF or higher value ceramic decoupling capacitor is recommended between IN_SYS terminal and GND.
- The external FET Q1 should be placed with DRAIN close to the V_{IN} pins of the IC and connected through a plane. The fast pull down switch Q2 DRAIN and SOURCE should be placed very close to the GATE and SOURCE terminals of Q1 with very short loop. See 图 59 and 图 60 for a typical PCB layout example.
- The optimum placement of decoupling capacitor is closest to the IN_SYS and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN_SYS terminal, and the GND terminal of the IC.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- Locate all the TPS2663x family support components $R_{(\text{ILIM})}$, $C_{(\text{dVdT})}$, $R_{(\text{IMON})}$, UVLO, OVP and PGTH resistors close to their connection pin. Connect the other end of the component to the GND with shortest trace length.
- The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

-  Top Layer
-  Bottom layer GND plane
-  Top Layer GND Plane
-  Via to Bottom Layer

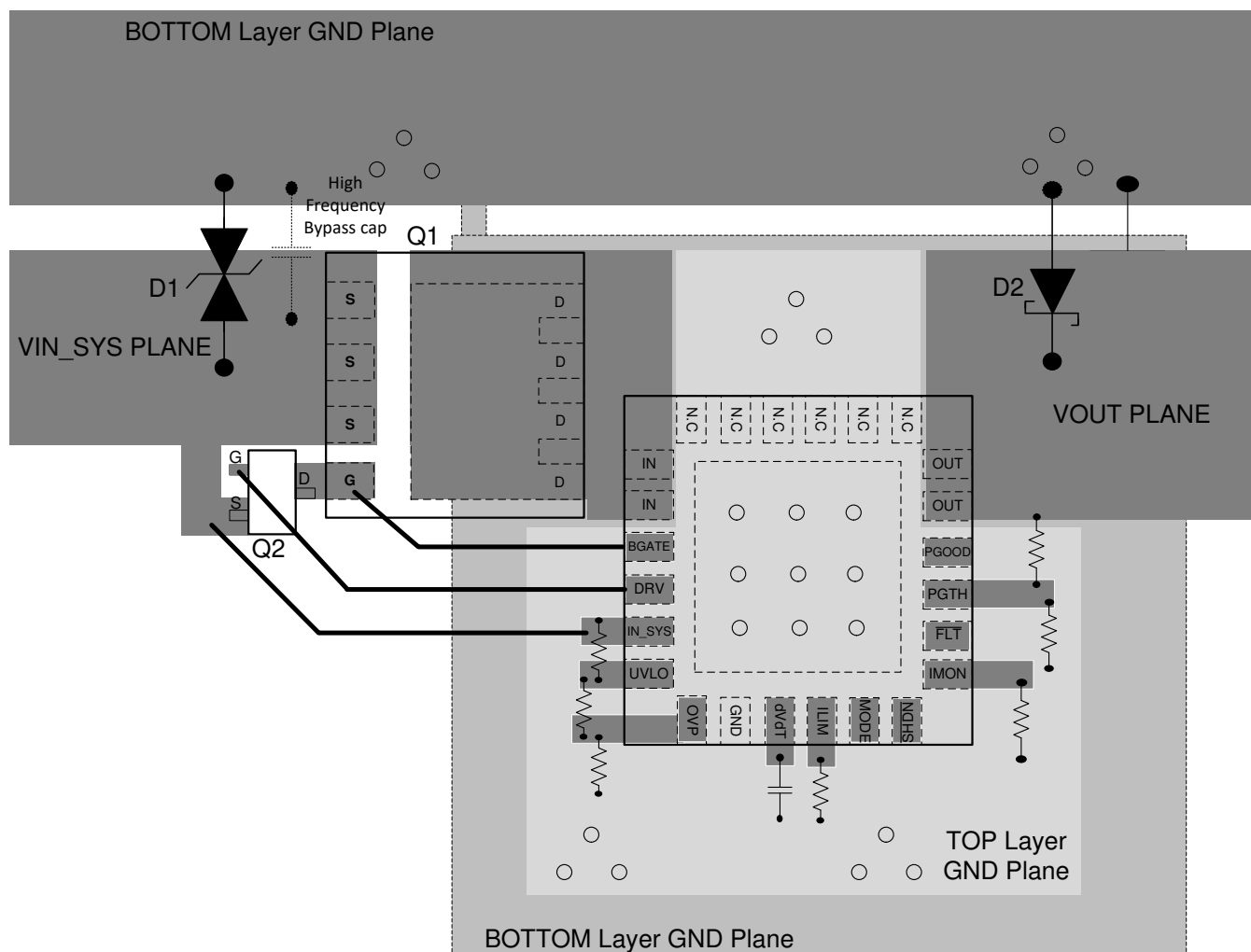


图 59. Typical PCB Layout Example With QFN Package With a 2 Layer PCB

Layout Example (接下页)

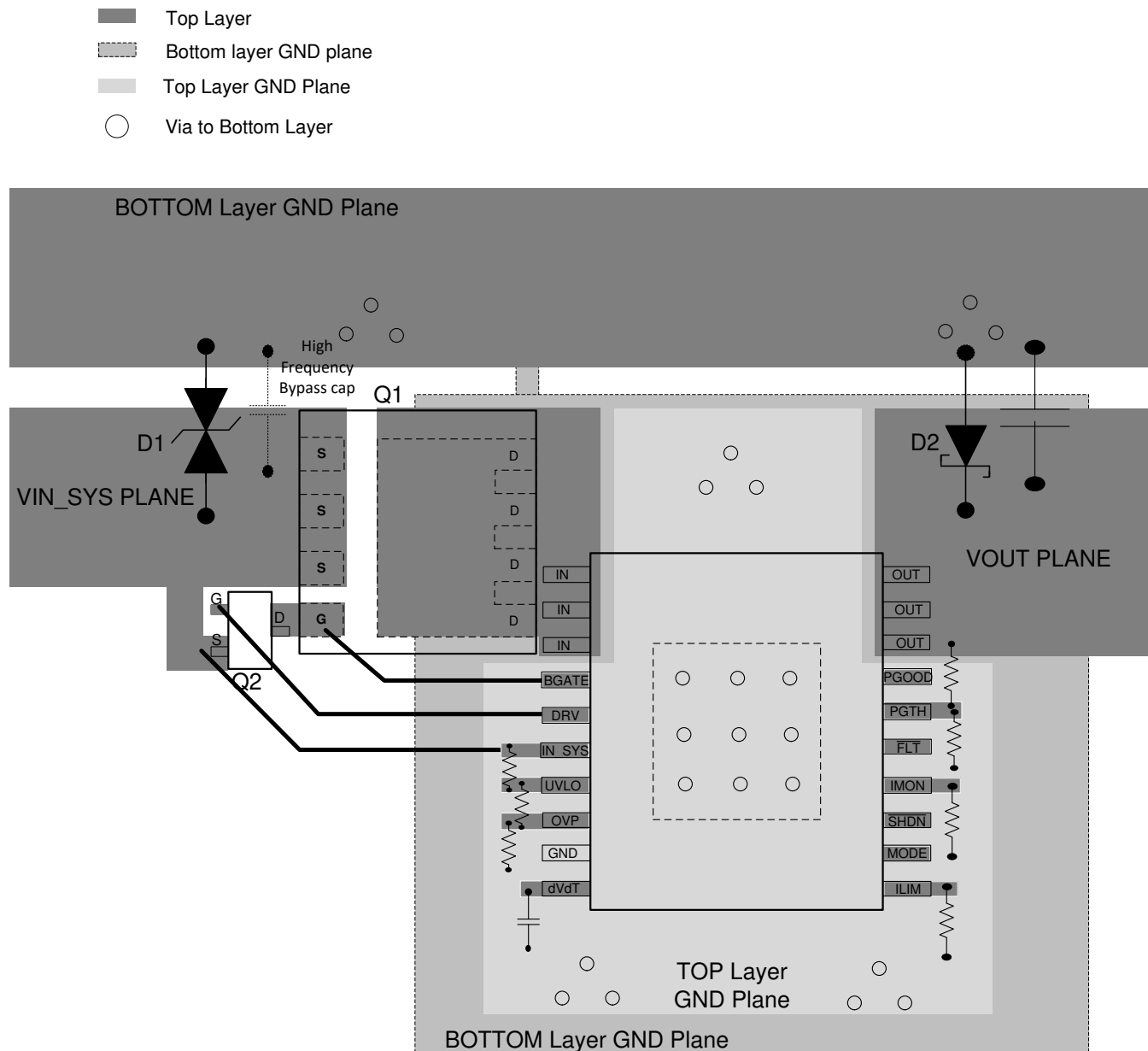


图 60. Typical PCB Layout Example With HTSSOP Package With a 2 Layer PCB

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

- [TPS2663 设计计算器](#)
- [CPU \(PLC 控制器\)](#)
- [适用于伺服驱动器的紧凑型、高效、24V 输入辅助电源参考设计](#)

13.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.4 商标

E2E is a trademark of Texas Instruments.

13.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

14.1 Package Option Addendum

14.1.1 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾⁽⁶⁾
PTPS26631PWPR	ACTIVE	HTSSOP	PWP	20	2000	TBD	Call TI	Call TI	–40 to 125	
TPS26630RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS 26630
TPS26630RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS 26630

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

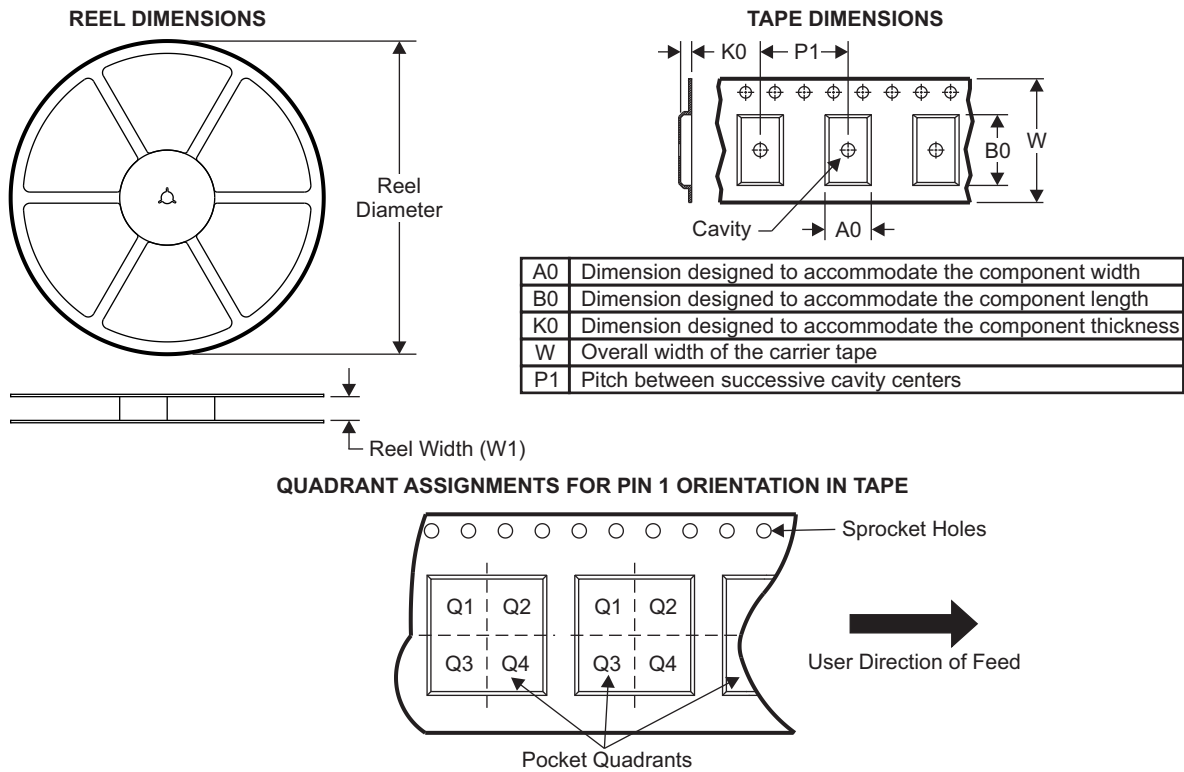
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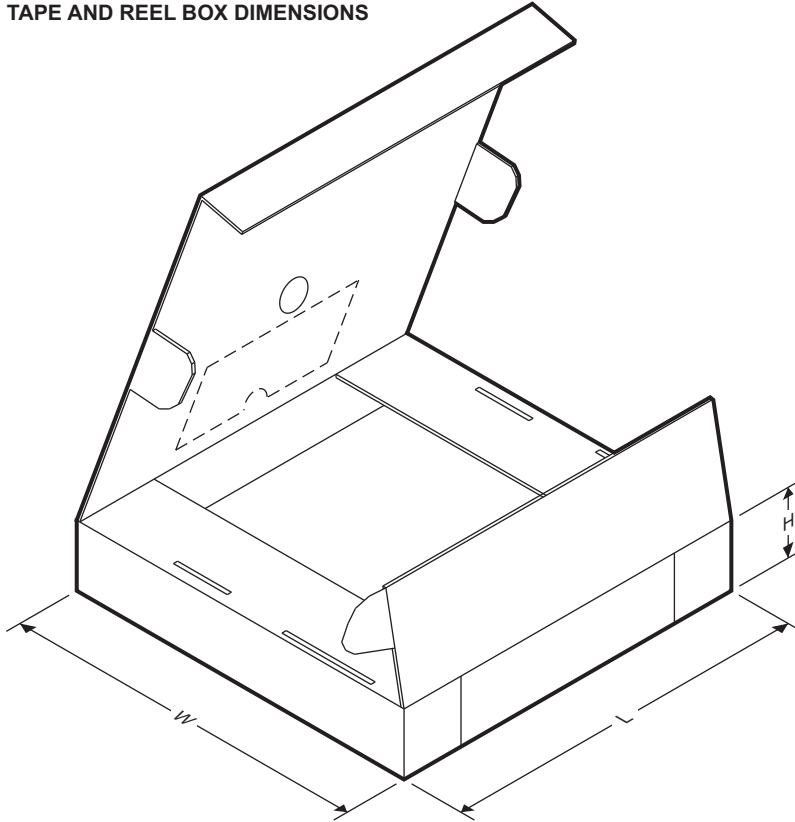
Package Option Addendum (接下页)

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾⁽⁶⁾
TPS26631PWPT	PREVIEW	HTSSOP	PWP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26631
TPS26631RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26631
TPS26631RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26631
TPS26632RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26632
TPS26632RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26632
TPS26633PWPR	PREVIEW	HTSSOP	PWP	20	2000	TBD	Call TI	Call TI	–40 to 125	
TPS26633PWPT	PREVIEW	HTSSOP	PWP	20	250	TBD	Call TI	Call TI	–40 to 125	
TPS26633RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26633
TPS26633RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26633
TPS26635RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26635
TPS26635RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26635
TPS26636PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS26636
TPS26636PWPT	ACTIVE	HTSSOP	PWP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	–40 to 125	TPS26636

14.1.2 Tape and Reel Information



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS26630RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26630RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26631RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26631RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26632RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26632RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26633RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26633RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26635RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26635RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS26630RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26630RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26631RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26631RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26632RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26632RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26633RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26633RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26635RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26635RGET	VQFN	RGE	24	250	210.0	185.0	35.0

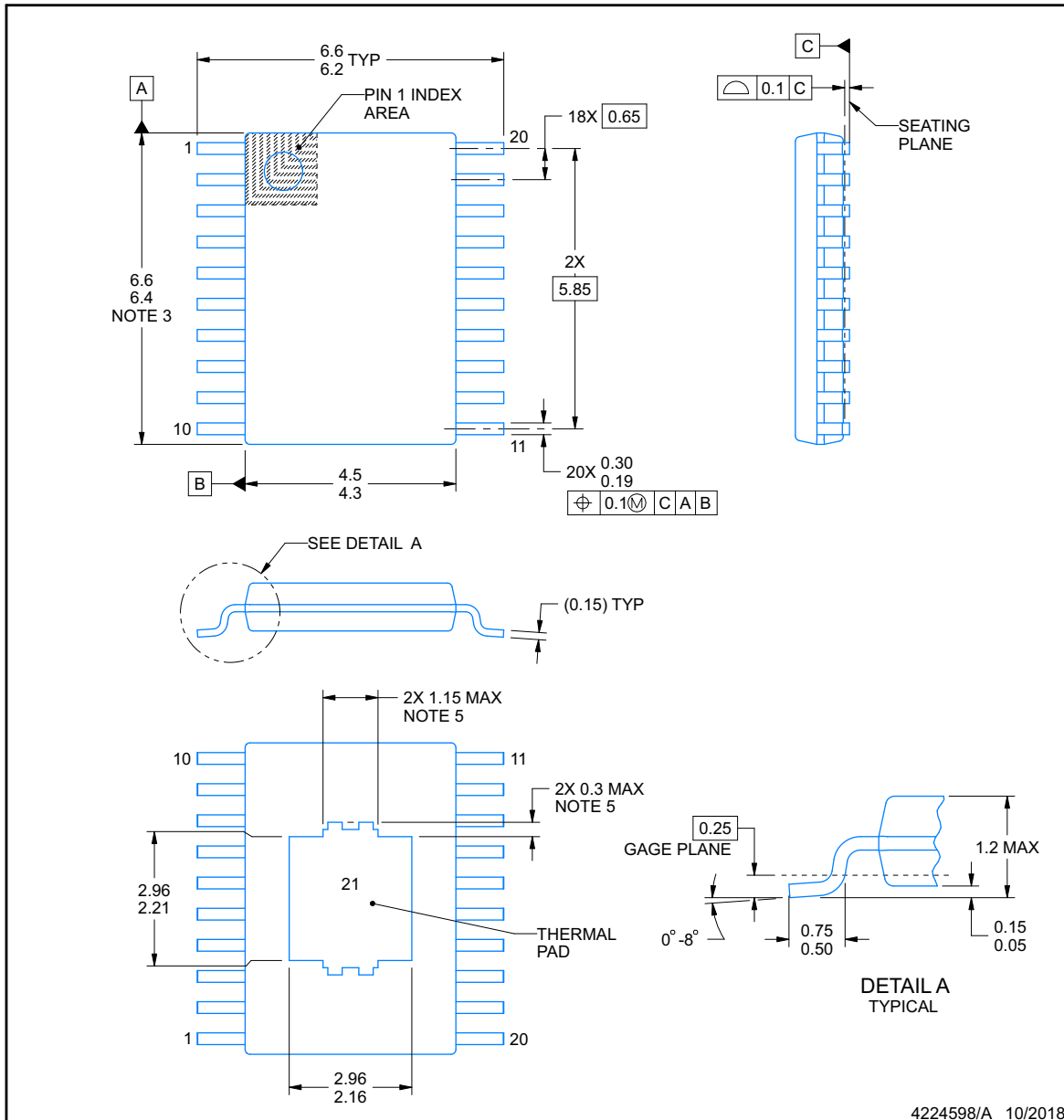


PACKAGE OUTLINE

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4224598/A 10/2018

NOTES:

PowerPAD is a trademark of Texas Instruments.

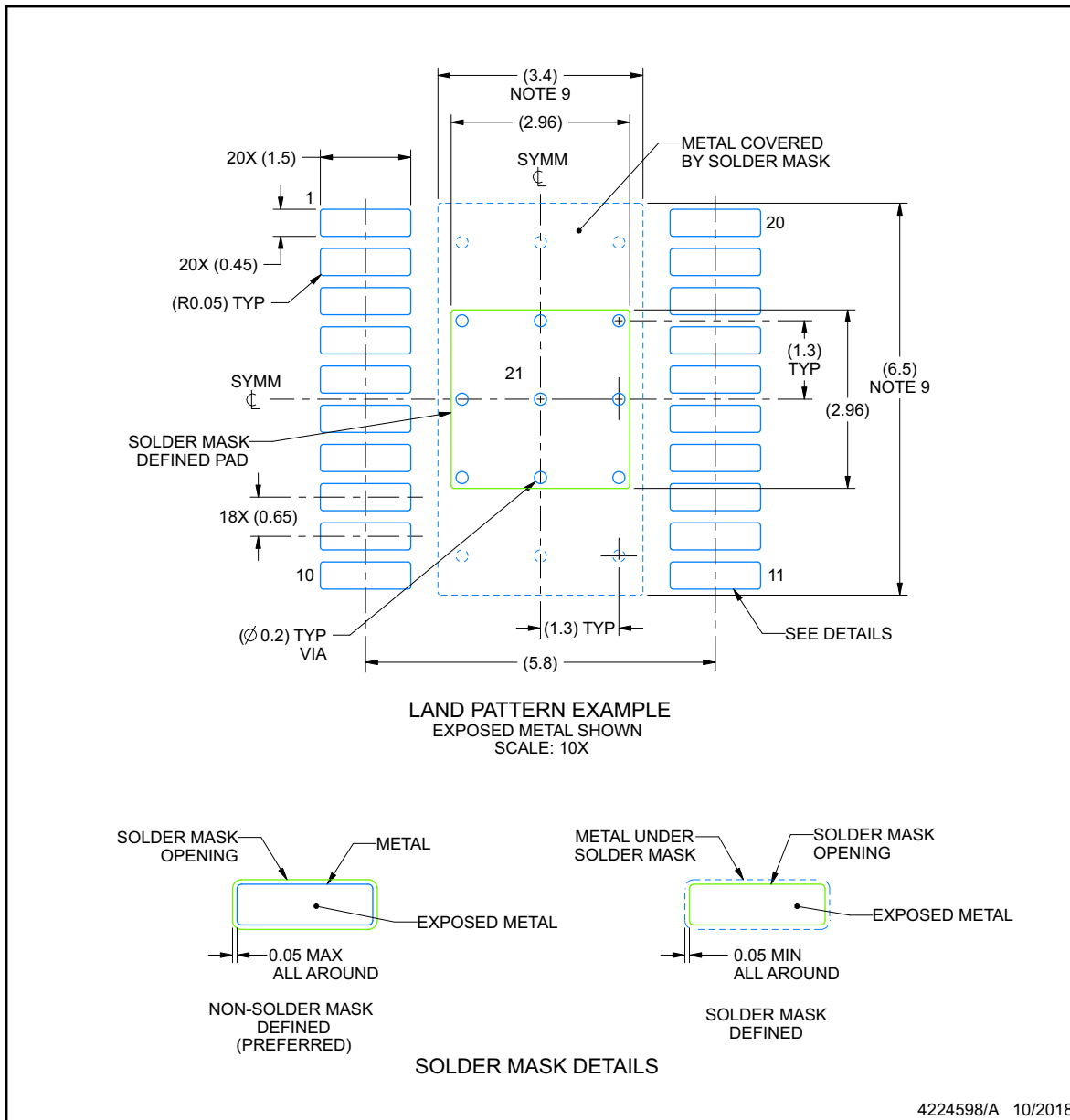
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

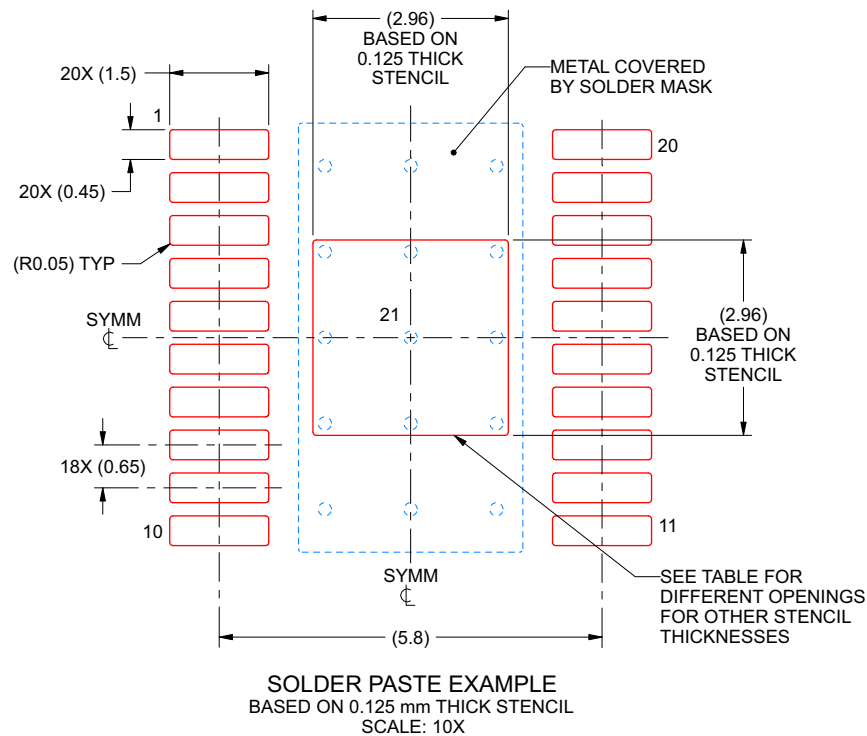
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 3.31
0.125	2.96 X 2.96 (SHOWN)
0.15	2.70 X 2.70
0.175	2.50 X 2.50

4224598/A 10/2018

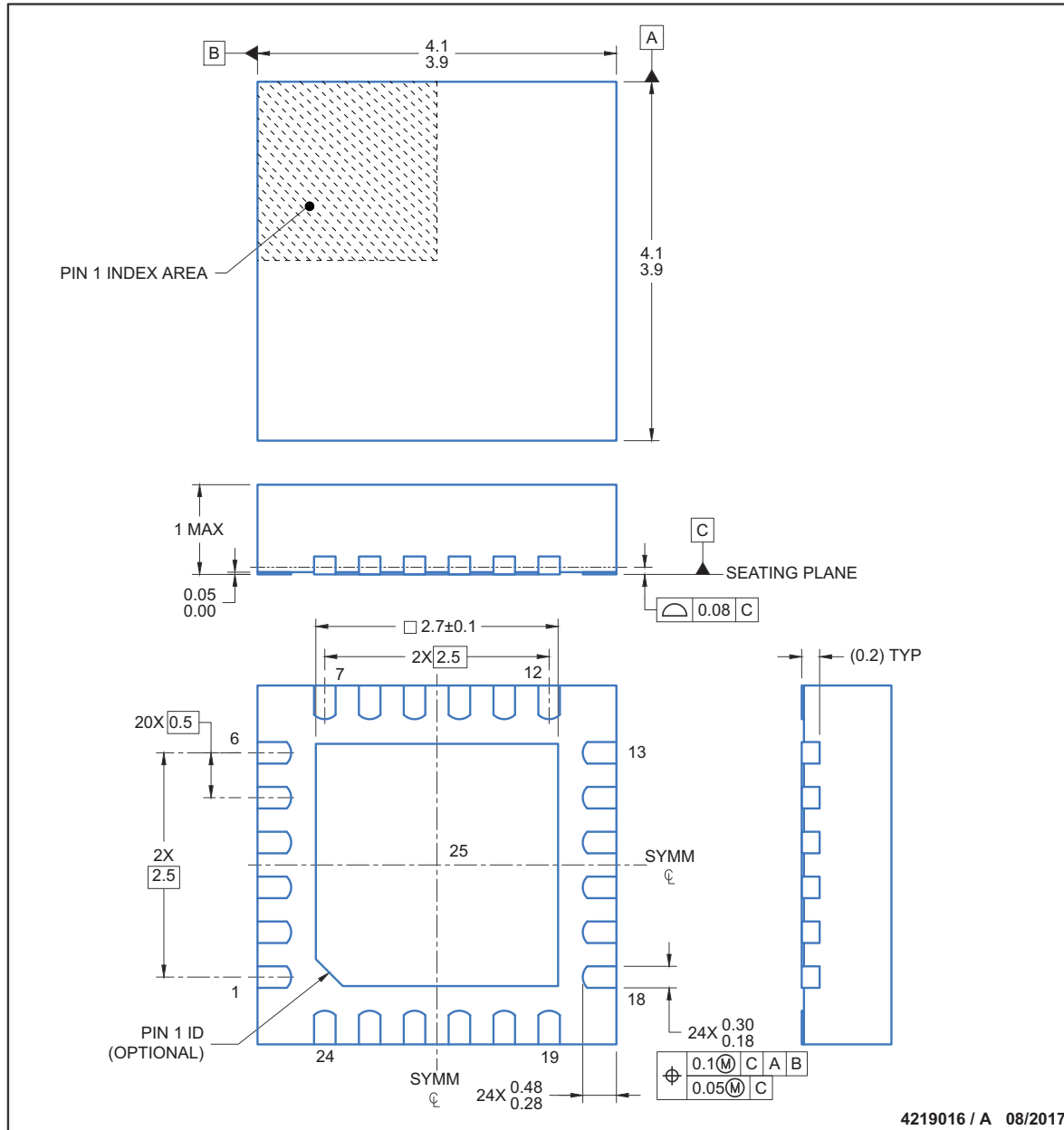
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RGE0024H

PACKAGE OUTLINE VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

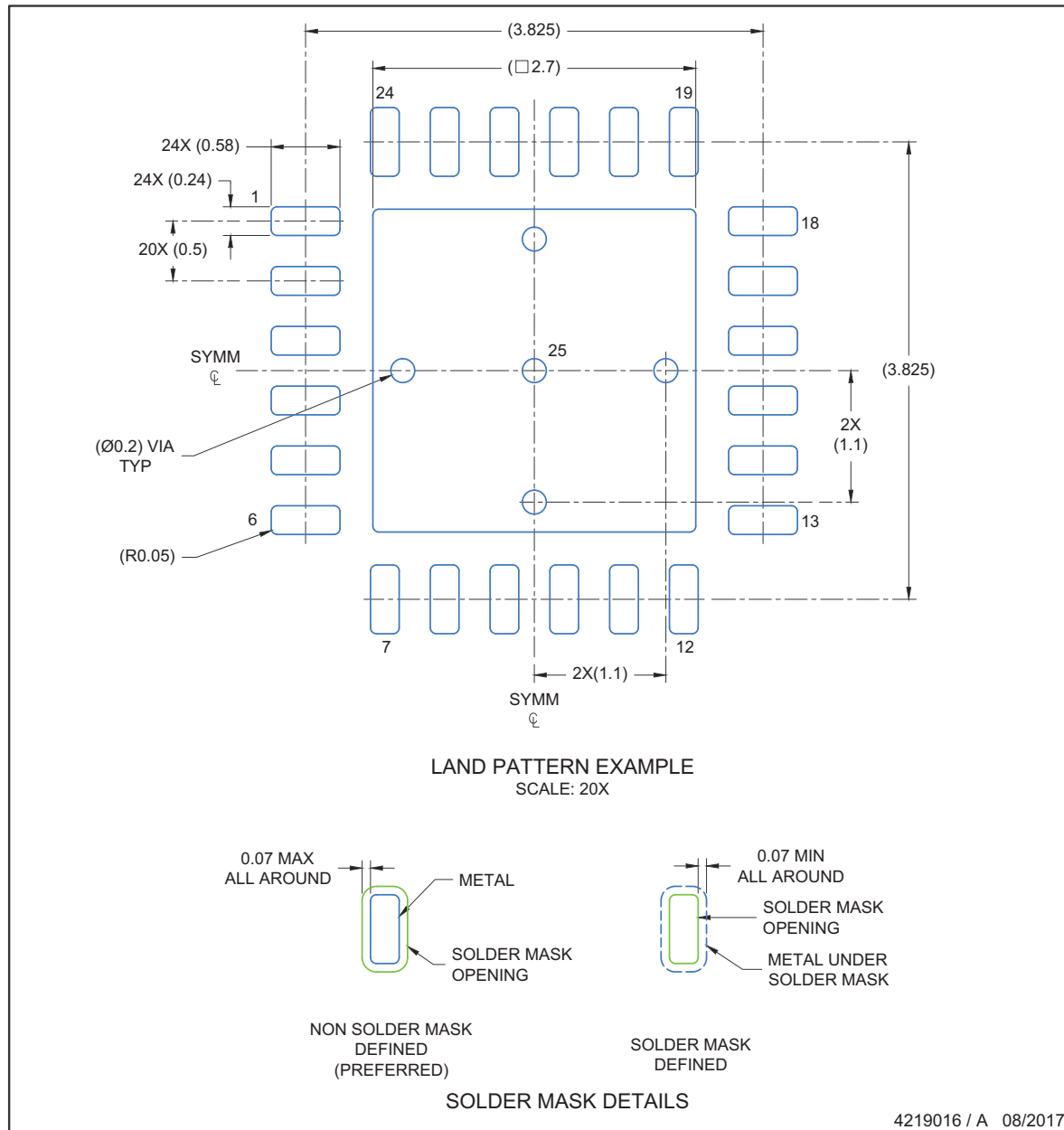
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

RGE0024H

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

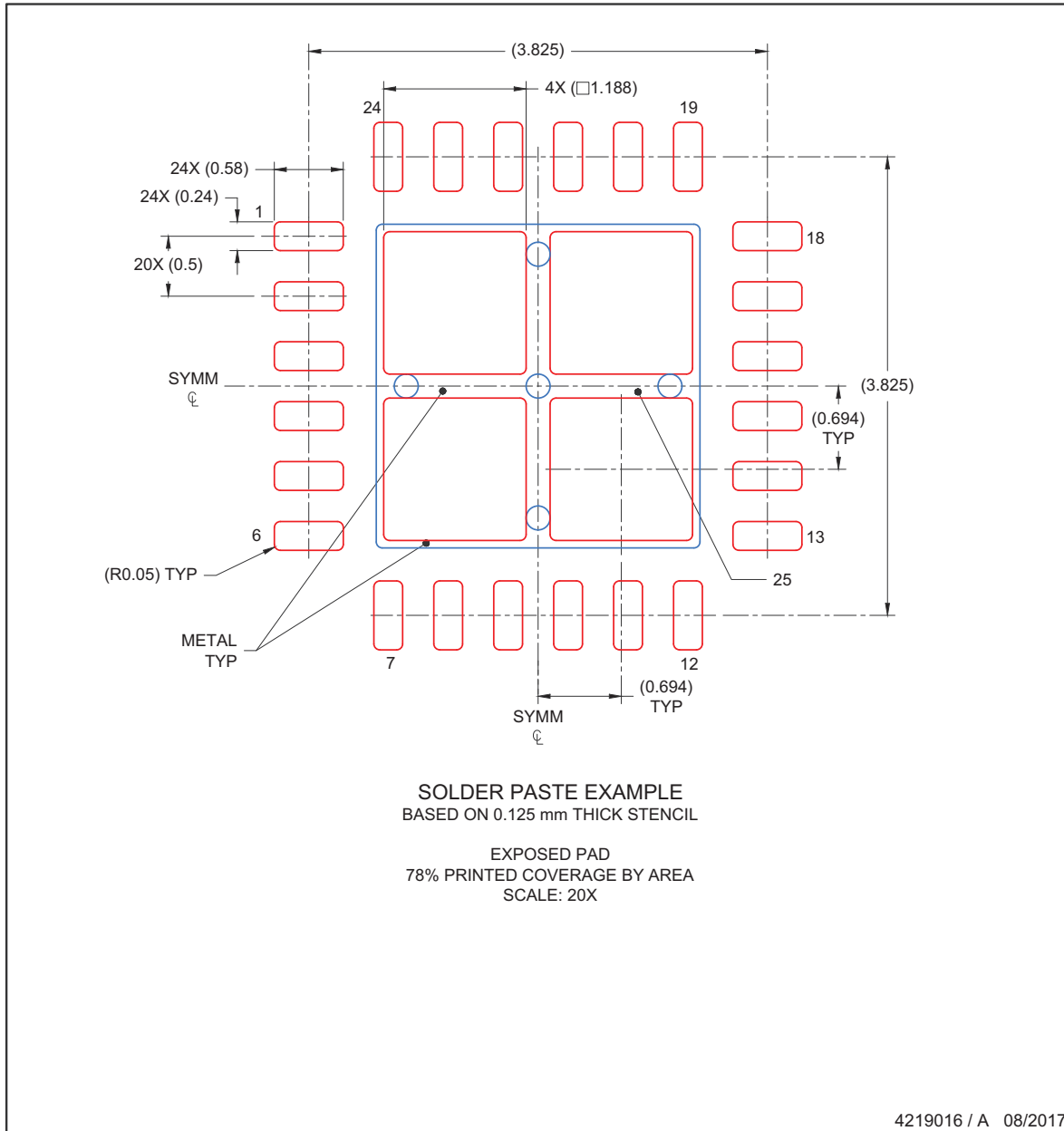
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGE0024H

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS26630RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26630	Samples
TPS26630RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26630	Samples
TPS26631PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS26631	Samples
TPS26631PWPT	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS26631	Samples
TPS26631RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26631	Samples
TPS26631RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26631	Samples
TPS26632RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26632	Samples
TPS26632RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26632	Samples
TPS26633PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS26633	Samples
TPS26633PWPT	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS26633	Samples
TPS26633RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26633	Samples
TPS26633RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26633	Samples
TPS26635RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26635	Samples
TPS26635RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 26635	Samples
TPS26636PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS26636	Samples
TPS26636PWPT	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-2-250C-1 YEAR	-40 to 125	TPS26636	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

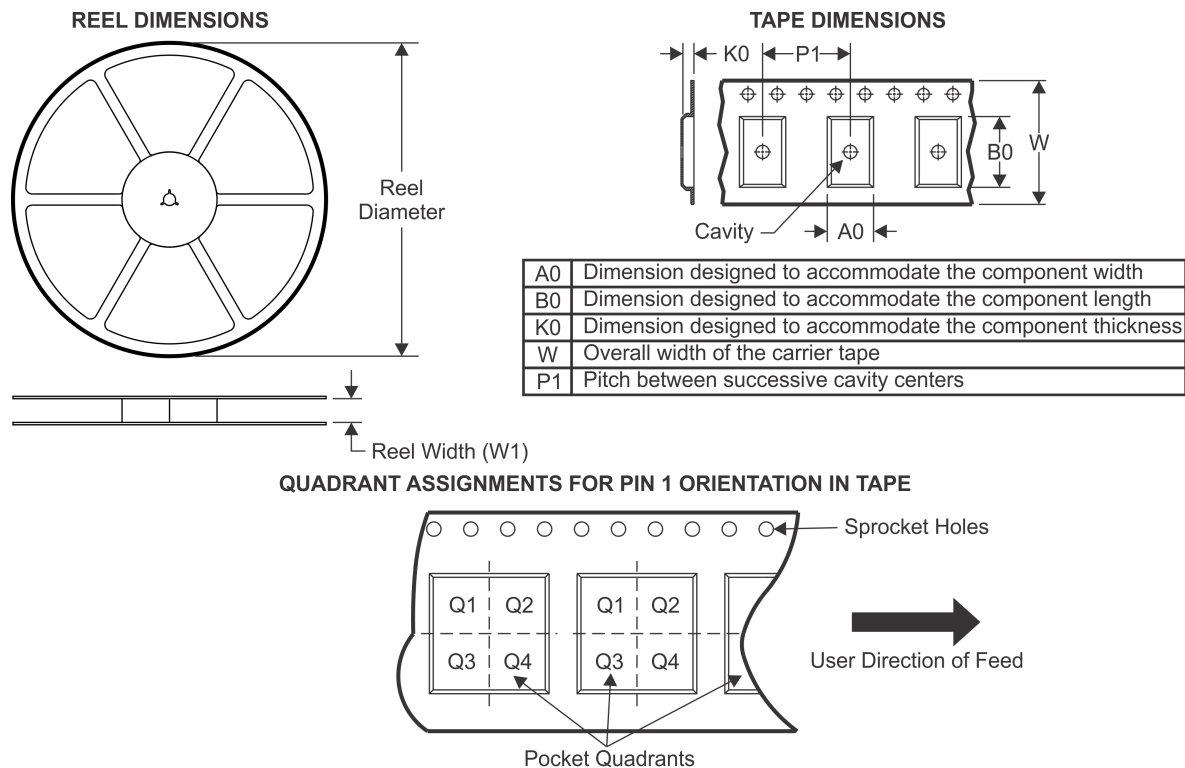
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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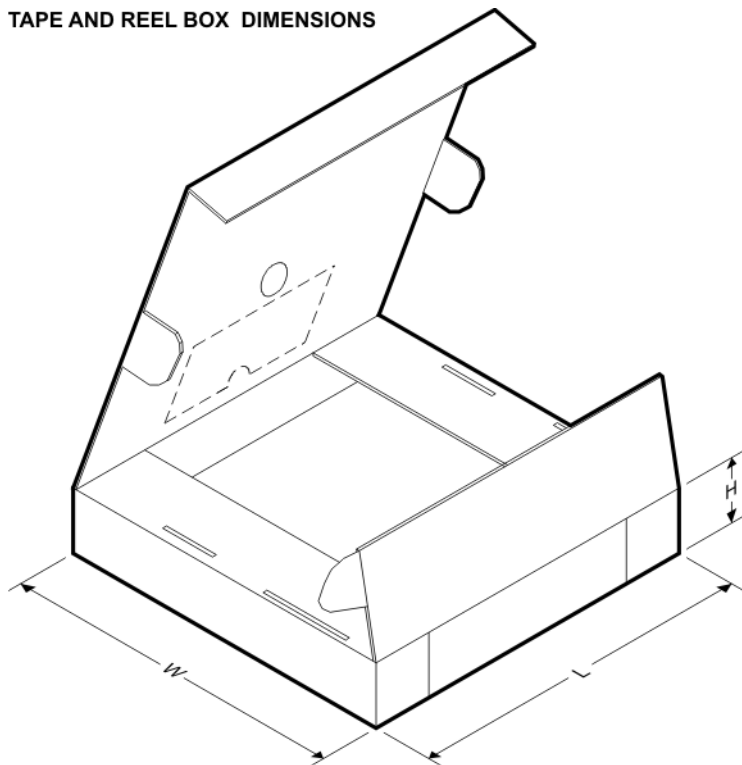
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS26630RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26630RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26631PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS26631PWPT	HTSSOP	PWP	20	250	180.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS26631RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26631RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26632RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26632RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26633PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS26633PWPT	HTSSOP	PWP	20	250	180.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS26633RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26633RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26635RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26635RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS26636PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS26636PWPT	HTSSOP	PWP	20	250	180.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

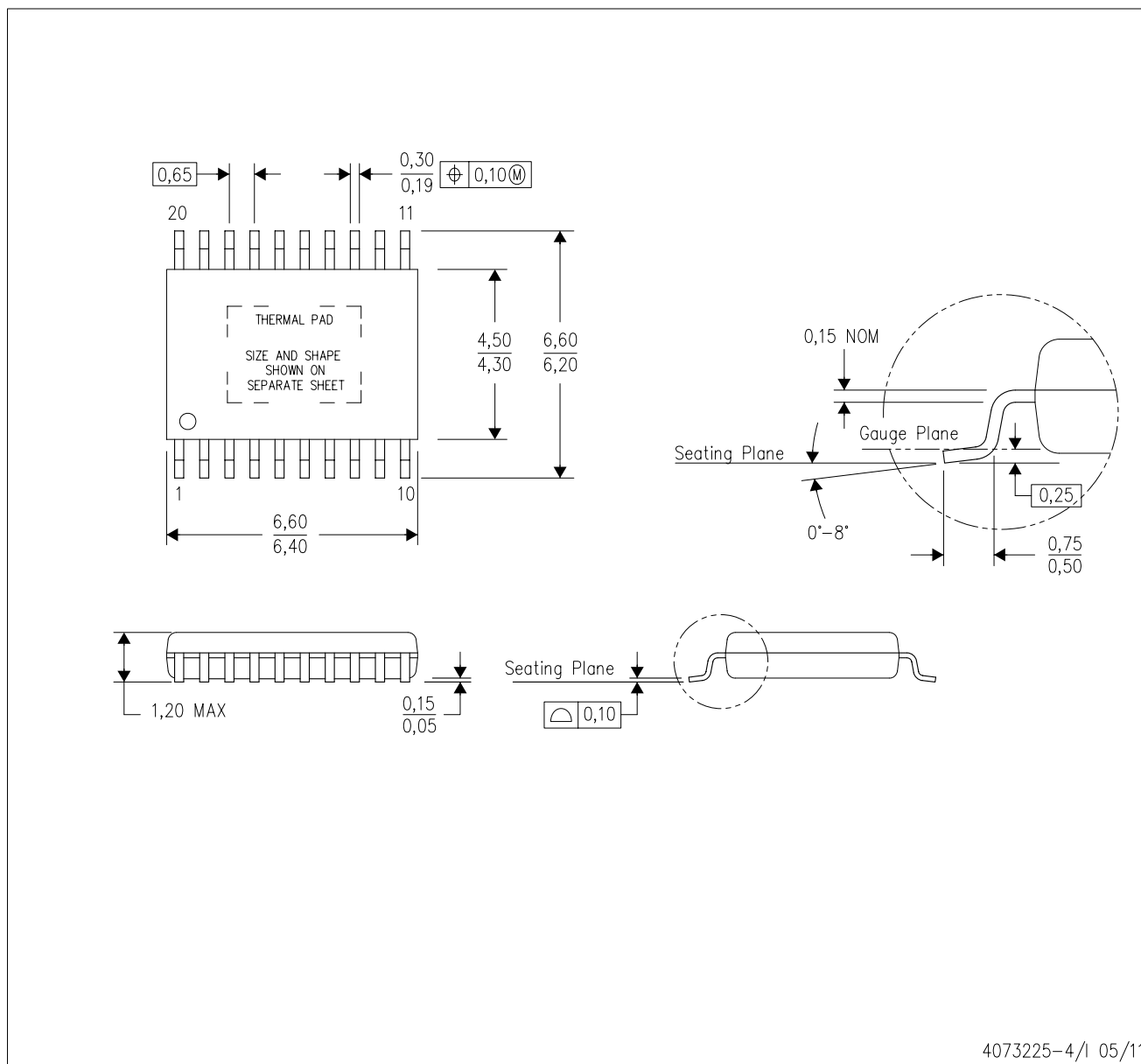


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS26630RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26630RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26631PWPR	HTSSOP	PWP	20	2000	853.0	449.0	35.0
TPS26631PWPT	HTSSOP	PWP	20	250	210.0	185.0	35.0
TPS26631RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26631RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26632RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26632RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26633PWPR	HTSSOP	PWP	20	2000	853.0	449.0	35.0
TPS26633PWPT	HTSSOP	PWP	20	250	210.0	185.0	35.0
TPS26633RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26633RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26635RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS26635RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS26636PWPR	HTSSOP	PWP	20	2000	853.0	449.0	35.0
TPS26636PWPT	HTSSOP	PWP	20	250	210.0	185.0	35.0

PWP (R-PDSO-G20)

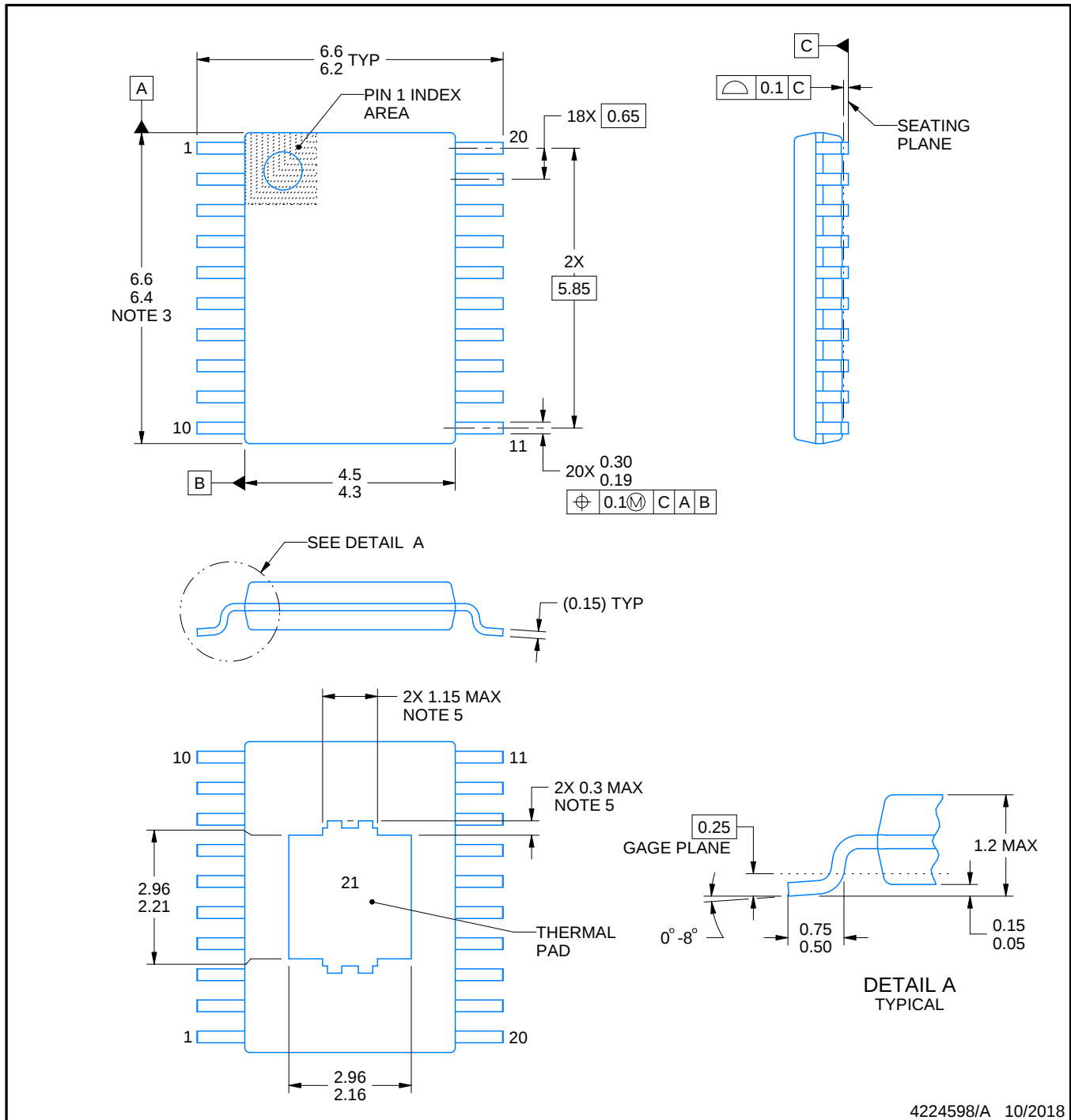
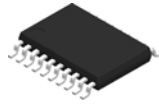
PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



4224598/A 10/2018

PowerPAD is a trademark of Texas Instruments.

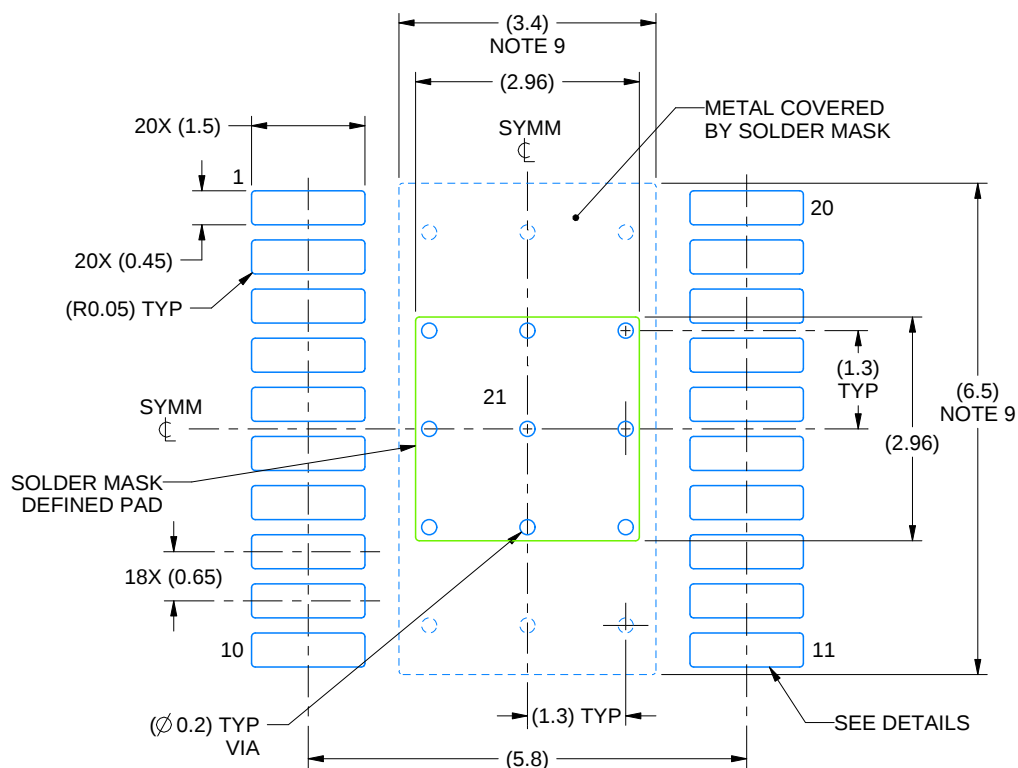
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

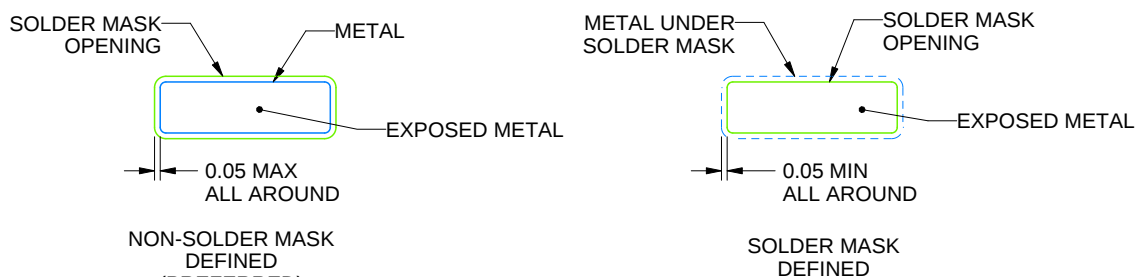
PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4224598/A 10/2018

NOTES: (continued)

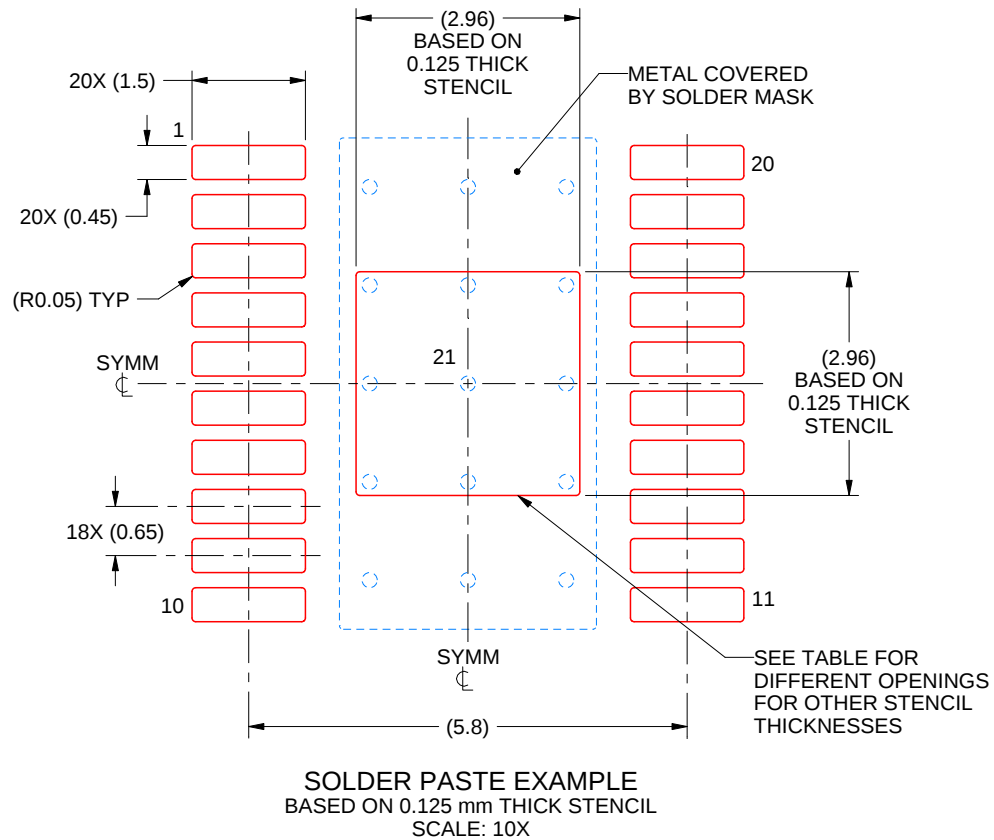
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 3.31
0.125	2.96 X 2.96 (SHOWN)
0.15	2.70 X 2.70
0.175	2.50 X 2.50

4224598/A 10/2018

NOTES: (continued)

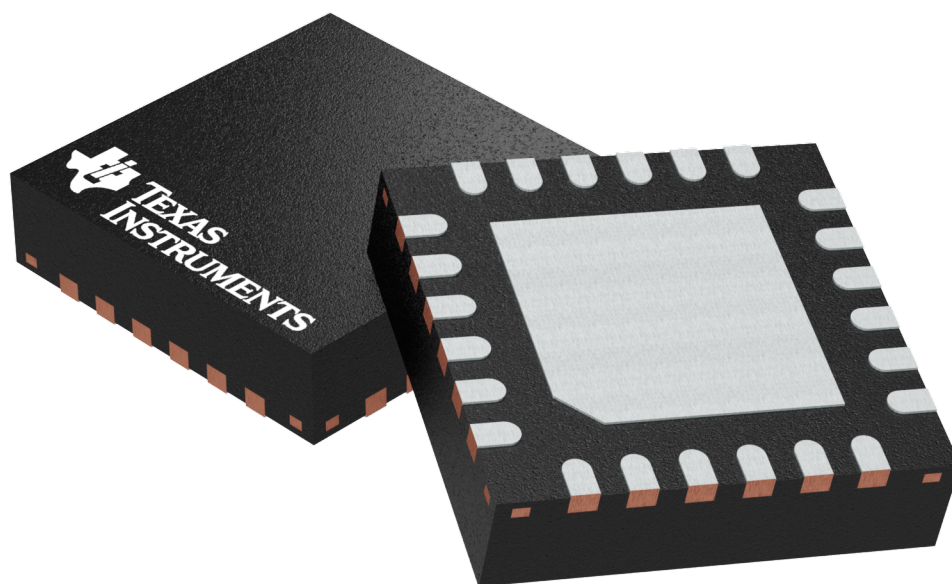
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RGE 24

GENERIC PACKAGE VIEW

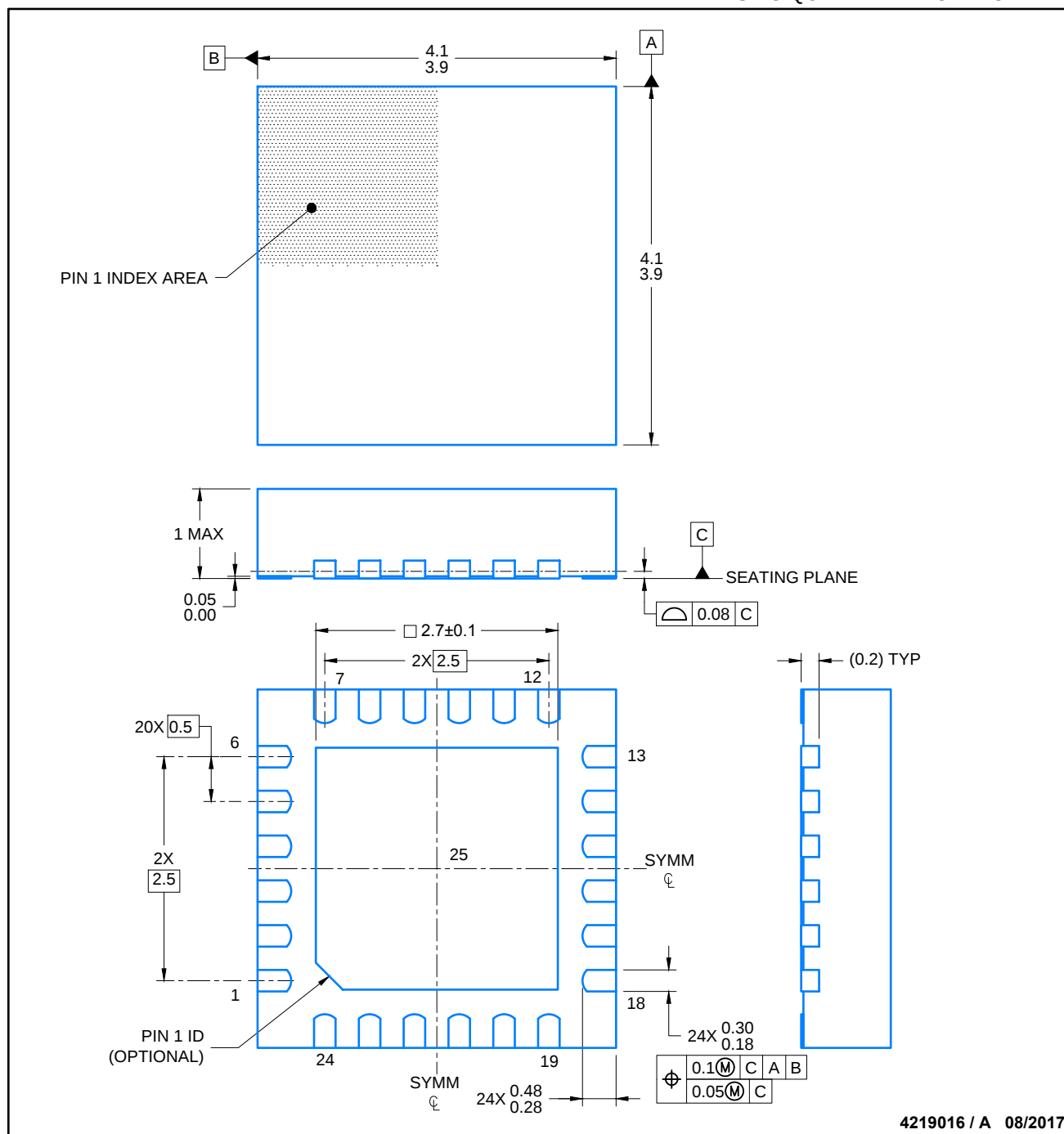
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

VQFN - 1 mm max height

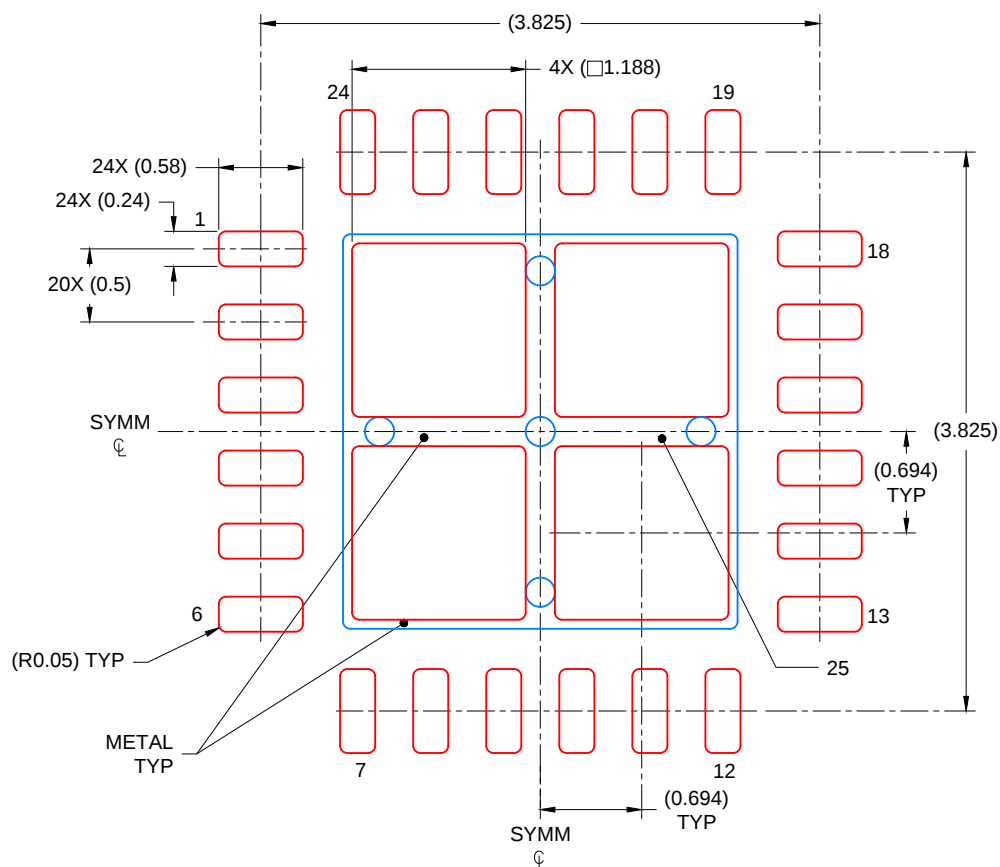
This mechanical drawing shows a 19-pin connector layout. The overall width is 3.825 inches. The pin pitch is 0.2 inches, with a total width of 24X (0.58) inches for the pins. The pin numbers 1 through 19 are indicated. The drawing includes dimensions for the pin spacing (24X (0.58), 24X (0.24), 20X (0.5)), the pin diameter (Ø0.2) VIA TYP, and the pin thickness (R0.05). The drawing also shows the pin positions relative to the centerline (SYMM) and the overall height (3.825 inches). The pin positions are defined by 2X (1.1) inches from the centerline.

The diagram illustrates two types of solder mask openings on a metal pad:

- NON SOLDER MASK DEFINED (PREFERRED):** This type shows a metal pad with a solder mask opening. The dimensions are specified as 0.07 MAX ALL AROUND. The labels indicate the METAL and the SOLDER MASK OPENING.
- SOLDER MASK DEFINED:** This type shows a metal pad with a solder mask opening. The dimensions are specified as 0.07 MIN ALL AROUND. The labels indicate the SOLDER MASK OPENING and the METAL UNDER SOLDER MASK.

SOLDER MASK DETAILS

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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